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History of the Crystalline Silicon Photovoltaic Cell Research Program at Sandia National Laboratories

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Abstract

The Sandia Photovoltaic Program conducted research in crystalline-silicon solar cells between 1986 and 2000 for the U.S. Department of Energy. This period saw rapid improvements in the fundamental understanding of c-Si materials and devices, improvements in c-Si PV manufacturing and control, and a rapid expansion of c-Si PV manufacturing capacity. Crystalline-silicon technology has provided the basis for PV to emerge as a serious option for global energy needs. The c-Si cell research at Sandia examined c-Si materials, devices, processing, and process integration. This report summarizes research conducted in this program over the past 15 years.

Acknowledgements

A large number of people have contributed to the success of the Sandia Crystalline-Silicon Photovoltaic Project over the past 15 years, so it will be difficult to acknowledge everyone. Many researchers from industry and academia have contributed to the project through interactions and collaborations. These include: Kim Mitchell, Richard R. King, Teresa Jester, Richard Swanson, Pierre Verlinden, Ronald Sinton, William Bottenberg, Ishaq Shayryar, Bhushan Sopori, John Benner, Wihu Tang, Simon Tsuo, Ted Ciszek, Juris Kalejs, Mark Rosenblum, Mike Kardauskas, Fritz Wald, Roger Little, Keith Matthei, Chandra Khattak, John Wohlgemuth, Mohan Narayanan, James Rand, Robert Hall, Jack Hanoka, Daniel Meier, Ajeet Rohatgi, Deiter Ast, Deiter Schroder, Arnost Neugroschel, Karl Boer, Eicke Weber, George Rozgonyi, Teh Tan, and Saleem Zaidi. A large number of dedicated and creative graduate students have also contributed to the project.

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We are particularly indebted to Dan Arvizu and Paul Basore for their leadership and vision.

Successful R&D projects require a committed, patient sponsor. We are thankful for the opportunity from the U.S. Department of Energy to perform this research in such an important topic.

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Executive Summary

The Sandia Photovoltaic Program conducted research in crystalline-silicon solar cells between 1986 and 2000 for the U.S. Department of Energy. This period saw rapid improvements in the fundamental understanding of c-Si materials and devices, improvements in c-Si PV manufacturing and control, and a rapid expansion of c-Si PV manufacturing capacity. *Crystalline-silicon technology has provided the basis for PV to emerge as a serious option for global energy needs.*

The rapid technological progress required sustained public and private R&D support and the coordinated efforts of many researchers from industry, academia, and the national laboratories. The technical issues challenging the community also evolved over this time period – moving from fundamental understanding of materials and devices in the early years, to developing processes that could take advantage of our fundamental material and device understanding, and finally towards implementing advanced device and processing concepts into production.

The c-Si cell research at Sandia examined critical challenges in all these issues (c-Si materials, devices, processing, and process integration) while coordinating with the various elements in the c-Si PV community to help advance the technology.

This report summarizes research conducted in this program over the past 15 years. Some of the highlights from this research include the following:

- Provided early research support for dendritic web (Westinghouse) and silicon sheet (AstroPower) that are now beginning to enter production.
- Helped found University Center of Excellence in Photovoltaics (UCEP) program, and supported UCEP at Georgia Institute of Technology (GIT). GIT has been very productive in c-Si device and process research that includes a variety of world-record efficiencies (RTP cells), novel processes (RTP, SiN/SiO passivation, etc.), and fundamental understanding of commercial processes (e.g., Al alloy and screen-printed metallizations).
- Developed standard program (PC1D) for performing numerical simulations of photovoltaic devices. This program was the first numerical semiconductor device-modeling program that could run on a desktop computer, and revolutionized solar cell device research.
- Demonstrated world's first, and still world-record, 15.3%-efficient multicrystalline-silicon module. Demonstration required transfer of many features from high-efficiency float-zone silicon solar cells (e.g., light trapping, surface passivation, Al-alloyed BSF, etc.) fabrication to the fabrication of large-area mc-Si solar cells.
- Developed first industry/laboratory/university research team (Crystalline-Silicon Research Cooperative) within the DOE PV Program. The CSRC has helped guide the laboratory and university research for the past 10 years, and facilitated improved communications among researchers within the community.

- Championed use of plasma processing for c-Si solar cell fabrication in the U.S. Plasma-enhanced CVD of silicon nitride is already in use as an antireflection coating that also provides surface and bulk passivation of defects. More importantly, we extensively investigated reactive ion etching for texturing c-Si substrates – texturing would significantly improve the performance of mc-Si solar cells.
- Developed a low-cost back-contact cell design (Emitter Wrap-Through) that has the potential for both high efficiency *and* lower cost. The cost advantage is due to the module assembly advantages of using back-contact cells.
- Supported development of ultra-high-efficiency one-sun silicon solar cells at Stanford University as a means to understand fundamental performance limits. At the time, the large-area one-sun cell performance (22%) was a world record. Some of this work is now in use at SunPower Corporation. The work also determined many of the fundamental parameters (e.g., recombination at surfaces and in highly doped regions, intrinsic-carrier concentration, bandgap narrowing, etc.) in c-Si devices.
- Examined the optics of c-Si solar cells and modules. Supported research at University of New South Wales that thoroughly examined geometrical structures for light trapping in c-Si solar cells. We extended research to examine optimization of textured surfaces within modules.
- Developed new device characterization techniques that have become standards in the PV community. In particular, we developed a method for analyzing the near-infrared internal quantum efficiency that could determine both recombination parameters (bulk excess-carrier lifetime and back-surface recombination velocity) and parameters associated with the optical structure (effective number of passes, back-surface reflectance, etc.).
- Championed the use of sophisticated statistical methods, such as design-of-experiments using response surface methodology and statistical process control, for process optimization and process control. These methods efficiently use resources to systematically investigate and control complex processes involving many variables. Such statistical methods are now in widespread use throughout the PV manufacturing industry.

Table of Acronyms

APCVD	Atmospheric-pressure chemical-vapor deposition
ARC	Antireflection coating
BSF	Back surface field
BC-EWT	Buried contact emitter wrap-through
BLP	Belt line processing
CFO	Conventional furnace oxides
CFP	Conventional furnace processing
c-Si	Crystalline silicon
CSRC	Crystalline Silicon Research Cooperative
CVD	Chemical vapor deposition
DC or dc	direct current
DLARC	Double-layer antireflection coating
DOE	Department of Energy
DRE	Damage removal etch
EBIC	Electron-beam induced current
EFG	Edge-defined film-fed growth
EMC	Electromagnetically cast
EPRI	Electric Power Research Institute
EVA	Ethylene vinyl acetate
EWT	Emitter wrap-through
FF	Fill factor
FZ	Float Zone
GIT	Georgia Institute of Technology
HEM	Heat-exchanger method
IBC	Interdigitated back contact
IQE	Internal quantum efficiency
J_{oe}	Emitter saturation-current density
JPL	Jet Propulsion Laboratory
J_{sc}	Short-circuit current density
LPE	Liquid phase epitaxy
mc-Si	Multicrystalline silicon
NREL	National Renewable Energy Laboratory
PCD	Photo conductance decay
PECVD	Plasma-enhanced chemical vapor deposition
PERC	Passivated emitter rear-cell
PERL	Passivated emitter rear locally diffused
PERT	Passivated emitter rear totally diffused
PESC	Passivated emitter solar cell
PV	photovoltaic
RIE	Reactive ion etching
RTP	Rapid thermal processing
SASE	Self-aligned selective emitter
sc-Si	Single-crystal silicon

SEM	Scanning electron microscopy
SERI	Solar Energy Research Institute
SEWT	Screen-printed emitter wrap-through
SLAR	Single-layer antireflective
SOD	Spin-on dopants
SPV	Surface photovoltaic
TDC	Textured dielectric coating
TEM	Transmission electron microscopy
UCEP	University Center of Excellence in Photovoltaics
UNSW	University of New South Wales
UV	Ultraviolet
V_{oc}	Open-circuit voltage
η	Efficiency

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Chapter 1. INTRODUCTION

Solar-electric power using photovoltaic modules is a very attractive energy technology. It is one of the most environmentally clean and low-impact energy technologies available; it is modular and easily sited, and it provides energy security since it uses a domestic (i.e, the sun) energy source. Solar-electric power has historically been primarily used in applications remote from an electric grid where it has very favorable economics. However, governments and consumers are increasingly recognizing the advantages of solar-electric power across the world, which has led to rapid growth of grid-tied solar-electric power and photovoltaic (PV) module and system shipments. As an example, the Energy Information Agency of the Department of Energy (DOE) projects that solar photovoltaic energy will be this nation's fastest growing energy source over the next 20 years.[1]

Crystalline-silicon (c-Si) photovoltaics was the first PV technology to reach the commercial market in the late 1970s, and still commanded a market share of over 90% of PV power modules in 1999. Crystalline-silicon technology has a number of advantages that have helped it reach this point:

- Silicon is plentiful and non-toxic.
- There is an enormous technology base and industrial infrastructure in silicon and silicon processing.
- Silicon PV modules are reliable and durable.
- Silicon PV modules have had the highest PV conversion efficiencies to date for commercial one-sun PV modules.

Despite these advantages, silicon PV has required considerable development over the years to maintain its market position and its cost and performance advantage over alternative photovoltaic technologies. DOE has supported R&D programs in c-Si PV since the inception of the National Photovoltaics Program in 1975, which has been instrumental in helping c-Si PV reach its present commercial success. In 1986, DOE asked Sandia National Laboratories to lead the c-Si PV R&D program for one-sun applications. Sandia had a program in concentrator cells with a thorough knowledge of device physics and processing that provided an ideal background for leading this project. The overall goal of the Sandia c-Si PV Project was *to promote the more rapid expansion of c-Si PV technology through improvements in c-Si cell performance and cost.* Module technology, where much of the cost of a c-Si PV module is incurred and where most of the durability issues are associated, is covered in other elements of the DOE PV Program. The Sandia c-Si PV Project used a dynamic project management structure that accommodated the rapid improvements in commercial c-Si PV technology. In particular, the research needs of the PV community evolved as the technology and industry evolved. The Sandia c-Si PV Project completed its research in 2000. This report provides a summary of research conducted within the Sandia c-Si PV Project. The report is roughly organized chronologically to reflect the evolution and progress of c-Si technology.

Table 1.1 provides a timeline of events from the project that helps illustrate the technical progression of the project.

Table 1.1 Timeline of events in the Sandia c-Si PV Project

YEAR	EVENTS
1986	Crystalline-Silicon Research Project initiated at Sandia
1987	c-Si Industry Materials research begun with AstroPower and Westinghouse
1988	University c-Si Research Program begun jointly with SERI 22.3% one-sun sc-Si cell (Stanford)
1989	PDFL dedicated
1990	23.3% sc-Si and 17.1% mc-Si (UNSW)
1991	>22% large-area sc-Si (Stanford) Fundamental c-Si device parameters (bandgap narrowing, minority-carrier mobility, intrinsic-carrier concentration, etc.) elucidated (UNSW, Stanford, and GIT). PC-1D/Ver. 3 released.
1992	Crystalline-Silicon Research Cooperative (national lab/industry research team) begun. University Center of Excellence at Georgia Institute of Technology dedicated.
1993	Extended IQE analysis technique demonstrated. Low-cost back-contact c-Si cell research begun. Tutorial on c-Si processing presented at IEEE conference.
1994	World's First 15%-efficient mc-Si module demonstrated (Sandia and Crystal Systems). Published *Crystalline-Silicon Photovoltaics: Necessary and Sufficient*
1995	Low-temperature PECVD nitride optimization completed
1996	PC-1D for Windows released. 18.6%-efficient mc-Si cell demonstrated (GIT and Crystal Systems) Fabrication of world-record efficiency c-Si module (22.7%, an area of 778cm^2. This module record still stands today.
1997	Cost and performance advantages of back-contact cells and modules documented.
1998	Improved performance with self-aligned selective-emitter cell demonstrated.
1999	Improved RIE texturing technique for mc-Si cells demonstrated.
2000	Program termination.

Chapter 2 provides a description of the concentrator and high-efficiency cell development that formed the basis for the project. Chapter 3 describes some of the early research on silicon materials and characterization. The fundamentals of c-Si material growth and

properties were not very clear at this stage, and many process and device characterization tools still needed to be developed. As the industry matured with more established baselines, the research needs evolved into understanding the particulars of processing and process integration. Chapter 4 describes the establishment of a process research laboratory to address this need, along with the development of a laboratory/industry research cooperative that would help guide the project. Chapter 5 is devoted to the University Center of Excellence in Photovoltaic Research and Education at the Georgia Institute of Technology (GIT) where the project continues research in c-Si devices. Chapter 6 covers some early research on processing. As industry and the market matured further, research needs evolved into process integration and understanding how to incorporate high-efficiency features into manufacturable processes. Chapters 7 and 8 cover research on process integration and advanced, manufacturable cells and modules. Finally, Conclusions (Chapter 9), provides some personal views of the authors on the future prospects for c-Si PV technology.

A comprehensive bibliography for the project is included as an Appendix for further information.

[1] "Solar PV Shows Major Generation Jump," press release, Energy Information Agency, US Department of Energy, December 18, 2000.

Chapter 2. CONCENTRATOR CELLS

Very early in Sandia's involvement with PV cell research, concentrator cells were seen as a means of reducing PV module cost by replacing expensive semiconductor area with inexpensive optical collector area. In this way, more intricate and expensive cell processing could be afforded because smaller cells were required. Indeed, extremely high-efficiency cells are needed in this approach to increase the amount of electricity generated, and hence drive down the cost.

University of New South Wales (UNSW) Research

This vision was implemented initially by funding several competitively bid concentrator and high-efficiency cell development contracts with universities and aerospace companies. Some of our initial funding went to UNSW, since they were one of the world leaders in high-efficiency Si solar cell research. In fact, our initial funding of UNSW was instrumental in the growth and progress of their extremely successful PV research center.

UNSW based their original concentrator cell design on their successful high-efficiency passivated-emitter solar cell (PESC) structure. This resulted in a marked improvement in low-resistivity concentrator cell efficiency from the previous best of 20%, achieved at Sandia's IC lab, to values in the 23-25% range at 50-150 suns. Values above 20% were obtained up to 1000 suns. One-sun open-circuit voltages up to 640 mV were demonstrated on both p- and n-type high-resistivity substrates. Light trapping based on both randomizing and geometrical schemes was examined. It was concluded that light trapping might allow 30% module efficiency to be reached using thin Si cells. (SAND87-7007)

Their next foray into concentrator cell research led UNSW to develop cells designed for use with prism covers that redirect incident light away from the top metal gridlines. This approach was capable of producing 25% cells of relatively large areas in the range of 100-500 suns. They reported the first demonstration of 19% lens/cell efficiency using c-Si, and the feasibility of applying the laser-grooved cell approach to large-area, low-cost concentrator cells. They developed a theory of sublinear effects in high-resistivity cells and devised a new light-trapping scheme based on tilted pyramids and slats that was shown to perform better than any other scheme to date. (SAND88-7032)

The UNSW project continued with the goal of achieving a 24% efficient "module-ready" cell. This target was comfortably achieved with efficiencies as high as 25.2% at 125 suns. In outdoor testing at Sandia, cells of this type resulted in lens/cell efficiency above 20% for the first time. Results were obtained with a new passivated emitter and rear cell (PERC) structure, which demonstrated an efficiency of 21.8% for a non-concentrating cell, the highest demonstrated efficiency at the time for a bifacially contacted cell. Progress was also reported for cells fabricated on n-type substrates and for plasma-grooved, buried-contact solar cells. (SAND89-7041)

A project to develop and supply 550 concentrator cells for use in prototype point-focus concentrator modules ensued. The target efficiency of 24% was exceeded, with efficiencies as high as 25.2% reached in the design concentration range of 200 suns. A combined lens/cell efficiency of 20.4% was measured at Sandia using a point-focus Fresnel lens. Subsequently, a peak module efficiency of 20.3% was achieved at Sandia using 12 cells and lenses. This was the first PV module to surpass the 20% efficiency milestone. (SAND89-7043)

The UNSW project continued with the goal of achieving a cell efficiency in the 26-27% range at a concentration level of 150 suns or greater. The target efficiency was achieved with the new Passivated Emitter, Rear Locally diffused (PERL) cell structure, but only at low concentration levels around 20 suns. The PERL structure, shown in Figure 2.1, combines oxide-passivation of both top and rear surfaces of the cells with small-area contact to heavily doped regions on the top and rear surfaces. Efficiency in the 22-23% range was also demonstrated for large-area concentrator cells fabricated with the buried-contact solar cell processing sequence, either when combined with prism covers, or with other innovative approaches to reduce top contact shadowing. (SAND91-7016)

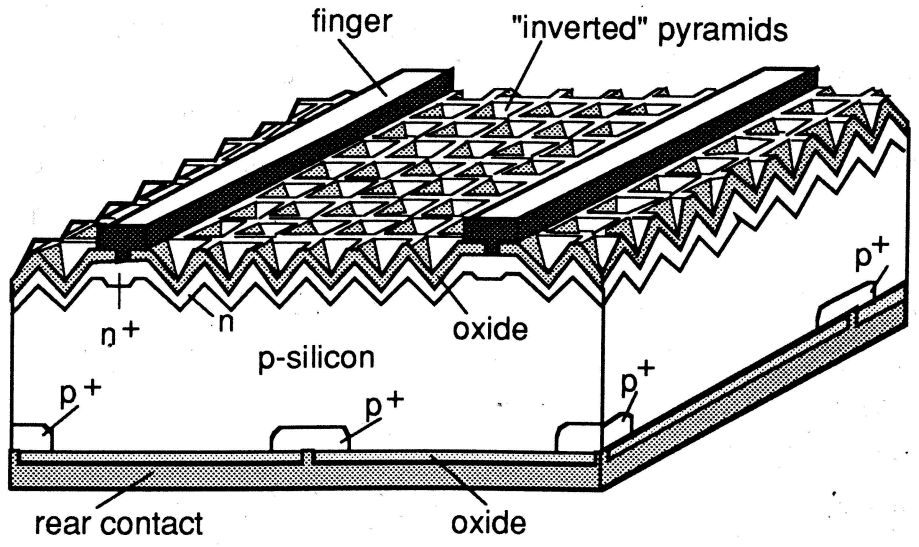

Figure 2.l. The PERL Cell Developed at UNSW

A change in calibration standards at Sandia implemented in January 1991 reduced all previous measured efficiency values by a relative amount of 4.8%. Thus, previous efficiency targets of 25% were actually only 23.8%, and the 20% cells and modules were really only 19%.

UNSW continued progress on one-sun cells by improving open-circuit voltage up to 703.8 mV with calibrated efficiencies up to 23% demonstrated. Improvements in light trapping were demonstrated with a path length enhancement factor up to 32 measured, with more benefits expected to arise from the use of “off-axis” schemes. (SAND92-7013)

An important result of the project was the proof that UV-degradation was not an immediate issue for these cells. Excellent progress was made in development of both PERL and PERT (rear totally diffused) cells on n-type substrates. This resulted in development of front-surface field, rear-junction cells. These cells showed excellent one-sun response, but performance under concentration suffered due to marked sublinearity with illumination level. One conclusion from this work was that the best PERL concentrator cells would incorporate low-resistivity p-type substrates. A major achievement of this project was the successful transfer of PESC cell technology to US industry at both Applied Solar Energy Corporation and Solarex Corporation. (SAND93-7049)

Cells of this type have been used to fabricate s-Si modules with a world-record efficiency of 22.7%, an area of 778 cm^2 measured at Sandia in September of 1996. This module record still stands today.

Stanford University / SunPower Corporation

While high-efficiency concentrator cell research was being funded overseas at UNSW, a parallel effort with a different approach was also being supported in the US at Stanford University under the direction of Professor Richard Swanson. Instead of using low-resistivity substrates, the Stanford approach was to use hyperpure high-resistivity substrates with all dopant diffusions and metal contacts on the back of the cell, a structure named the Point-Contact Solar Cell. This avoided the problems of gridline obscuration and competing tradeoffs between front emitter optical and electrical properties, but relied instead on high diffusion lengths in the cell bulk and significantly reduced cell thickness. It also mandated extremely well-passivated front and rear surfaces.

Early work evolved from EPRI-supported research into thermophotovoltaic cells. Much theoretical work was done showing the need for and developing more complex models of carrier mobility. Modeling and experimental study of recombination under high-level injection conditions led to an understanding of how this limits cell performance. Trade-offs between light-trapping and surface recombination for a variety of textures were studied, and an optimization of oxidation parameters to minimize surface recombination was performed. The theoretical studies done at Stanford were perhaps the most comprehensive in the field of Si photovoltaics, improving the modeling, predictive, and cell design capabilities in the field. The experimental techniques were carefully described so as to be extremely useful in the process optimization of Si solar cell fabrication. (SAND88-7026)

Stanford detailed the principal issues involved in the design and fabrication of both backside-contact cells and cells with front-side grids. Several simplified designs were considered. A simple one-photomask alignment process resulted in 23% two-sided cells at 140 suns, with room for improvement up to 25% with further development. With an additional alignment, 27% cells were thought to be feasible without the use of prism covers. A new backside contact cell design was developed that requires only one mask

and no alignments. Cells of this type were 15.4% efficient at 40 suns without AR coating or texturization. Fundamental studies of this design predicted 25% cells when fully developed. A new light-trapping scheme was proposed which could increase attainable efficiencies to 33%. (SAND88-7037)

Stanford continued to perform extensive process development for high-efficiency Si concentrator cells. An advanced design for a 1.56-cm^2 cell with front grids achieved 26% efficiency at 90 suns without the use of a prism cover. New designs for simplified backside-contact solar cells demonstrated 21-22% for one-sun cells in sizes up to 37.5 cm^2. An efficiency of 26% was achieved for similar 0.64-cm^2 concentrator cells at 150 suns. A diagram of such a back point contact cell is shown in Figure 2.2. More fundamental work on dopant-diffused regions was also conducted. The recombination vs. process parameters was studied in detail for boron and phosphorus diffusions.

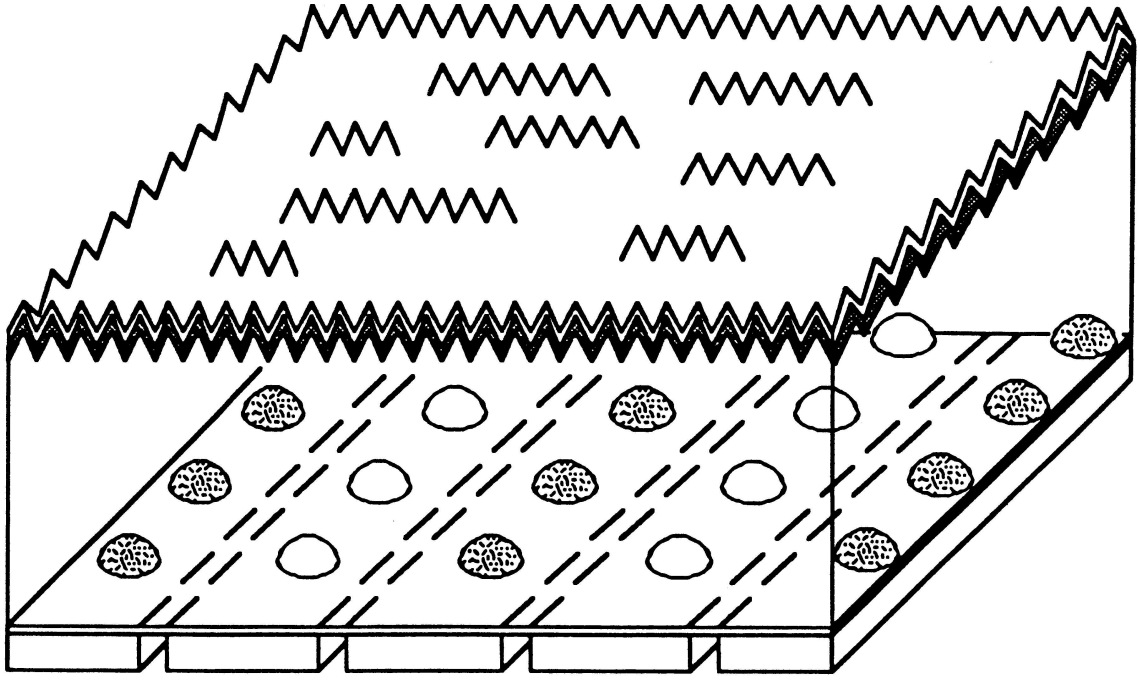

Figure 2.2. Back-point-contact Cell Developed at Stanford University
The shaded dots represent p-type diffused regions, while the clear dots show the n-type diffusions. Each type is contacted by alternating polarity interdigitated metal gridlines on the backside of the cell.

Emitter-design studies based solidly upon these new data indicate the performance vs. design parameters for a variety of the cases of most interest to solar cell designers. Extractions of p-type bandgap narrowing and the surface recombination for p- and n-type regions from these studies have a generality that extends beyond solar cells into basic device modeling. (SAND90-7033)

Beginning in 1990, Professor Swanson left Stanford and established SunPower Corporation, to begin the process of commercializing the concentrator cells his team had developed. Further Sandia contracts were issued in a joint program with EPRI to develop a commercial manufacturing facility. During just the first year of the program, SunPower established a solar cell fabrication pilot line, developed a baseline concentrator cell process, and completed a cell testing facility. Initial cell efficiencies were 23% for the baseline process, with a long-range goal to improve this to 27%. (SAND93-7055)

The Concentrator Initiative

Early in the 1990s, Sandia began a program to encourage and accelerate commercialization of the advancements in concentrator cell technology that had been cultivated at universities like Stanford and UNSW. The early SunPower contract mentioned above was issued under this program, which had been named the Concentrator Initiative. Along with module manufacturers, additional concentrator cell suppliers such as Applied Solar Energy Corporation, Spectrolab Corporation, and Solarex Corporation were also issued contracts under a competitive bid process to get concentrator cells into production.

Applied Solar Energy Corporation (ASEC)

ASEC licensed the PESC cell concept from UNSW and hired a key UNSW graduate student to get the process into the manufacturing line. The microgrooved PESC approach combines a 0.2μm phosphorus-diffused emitter layer with a thin 10-nm silicon dioxide surface passivation layer. The front gridlines sit on top of a heavily diffused region to reduce contact resistance between front gridlines and the emitter. Hyperpure float-zone silicon with a low resistivity of 0.2 ohm-cm was used. To achieve lower system cost, the cell area was reduced to 1 cm^2 from the 1.58-cm^2 used at UNSW. The cell was designed to be used under an available prism cover.

The baseline process required four photolithographic masking steps. A lift-off, metal-evaporation gridline process was used to provide thick gridlines without the use of hazardous plating solutions. Space-qualified, vacuum-deposited metal layers were used for front and back contacts. A double-layer antireflection coating (DLARC) designed to match the oxide passivation layer was used to minimize reflection. Different gridline widths were tested and evaluated for best performance at high solar intensities. A three-mask process was evaluated for reduced costs and a five-mask process was evaluated for increased yield. Efficiencies up to 21.5% at 50 suns were obtained. (SAND92-7006)

A limited pilot production run of PESC cells for use at concentrations of 200 to 400 suns was conducted. The front contact design of the cells was modified for operation without prism covers. The original objective was to implement all process improvements in the production run to provide the basis for estimating cells costs at high production levels. Because of funding limitations, the Concentrator Initiative was put on hold, and ASEC's contract was operated at a low level of effort for most of 1993. The results obtained from

the reduced scope pilot run showed the effects of discontinuous process optimization.

However, cells over 22% were produced and the run provided valuable insight into the technical areas that needed further optimization to achieve the original goals. (SAND94-2068)

Spectrolab Corporation

From 1991-1993, Spectrolab embarked on a program to develop a commercial, high-efficiency, low-cost concentrator solar cell compatible with their existing manufacturing infrastructure for space solar cells. They used a simplified PESC process and achieved an efficiency of over 19% between 200 to 300 suns. The cells were designed to be compatible with DOE cost goals of 12¢/kW-hr. A production lot of 1000 cells was delivered with efficiencies as high as 20% at 100 suns. (SAND94-2453)

Solarex Corporation

Solarex also participated in the Concentrator Initiative, and one of its tasks was to provide cells for the Entech linear-focus concentrator module. These were relatively large-area, 38-cm^2 cells designed for use at 22-suns. They were PESC-type, using 0.8 ohm-cm p-type substrates, randomly textured front surfaces, DLARCs, passivated emitters, restricted metal contact areas and wide silver gridlines. Prism covers were used to eliminate shading losses from the gridlines. Cell efficiencies as high as 20.3% were demonstrated on prism-covered cells at 20 suns. The production-environment process sequence used a single diffusion step, a thin thermal oxide growth, and two mechanically aligned photolithography steps. (SAND90-7026)

Solarex also developed PESC cells for higher solar concentrations. These cells were 1.6-cm^2 with relatively large gridlines to minimize series resistance losses and used prism covers to minimize shadowing loss. The front surface was textured and oxide-passivated. Two separate diffusion steps were used, a light emitter diffusion for good current collection, and a heavy patterned diffusion under the gridlines to reduce recombination. Six photomask steps were needed. Cell efficiencies as high as 22.3% were demonstrated at 75 suns and over 21.5% at 150 suns. (SAND90-7030)

Solarex also licensed the buried-contact solar cell design from UNSW, and used it to develop a low-cost concentrator cell for use in the Entech 22-sun, linear focus, Fresnel lens module. The concentrator cell was designed, a baseline process developed, and preliminary cells fabricated. Mechanical grooving was substituted for the previously utilized laser scribing. The best cell was 11.5% efficient at one-sun and increased to over 13% at 12 suns. This project was terminated when the Concentrator Initiative ended before its final goals could be reached. (SAND92-7007)

Chapter 3. FUNDAMENTALS OF C-SI PV: 1987-1989

Sandia National Laboratories received guidance from DOE to initiate a c-Si PV research program in 1986. While very considerable technical progress had been achieved within the JPL (Jet Propulsion Laboratory) c-Si research project, the c-Si PV industry and technology was still in an early stage of development. There were still many options to be considered for crystal growth, processing, and device design. In addition, many fundamental issues associated with c-Si materials (effect of impurities, crystalline defects, mechanical properties at high temperatures, etc.) still needed to be investigated and process and device characterization tools were not widely available.

The project in these early years emphasized long-range research on fundamentals of c-Si PV. The intent was to provide a solid foundation for a stronger c-Si PV industry.

Crystalline-Silicon Crystal Growth

Crystalline-silicon PV was based on growth of large ingots of crystalline silicon followed with slicing into c-Si wafers. This approach is expensive and wasteful in that much of the silicon is lost during the slow slicing operation due to the thickness of the cutting blade and slurry ("KERF" loss).

Alternative crystal-growth techniques could avoid the costly slicing step by growing the silicon directly into thin sheets. Such techniques could include, for example, growth of c-Si in sheets, ribbons, or films on a substrate. Alternative c-Si growth techniques were an active research topic in the JPL program.

Dendritic web is a very attractive c-Si growth technique in that it yields a potentially high-quality single-crystal ribbon. It was developed at Westinghouse with support from the JPL c-Si research program. The technique grows single-crystal silicon by slowly removing two silicon dendrites from a molten Si bath.

Westinghouse investigated methods to improved dendritic cell performance and growth technology. Dendritic web is easier to grow very thin (<150 μm), but cell performance is degraded due to insufficient light absorption. Westinghouse developed a method to texture the surface using isotropic acidic etchants and a photoresist mask, but this method is expensive and the texture was not sufficient optically to enhance the absorption. The need to inexpensively enhance the optical absorption of thin c-Si substrates is still an issue for the industry.

Westinghouse also examined the effect of different dopants on material quality. Boron, phosphorus, and antimony were compared. Antimony yielded the best results with hole diffusion lengths of 272 μm demonstrated on lightly doped ($5*10^{14}$ cm^{-3}) n-type material. These diffusion lengths greatly exceed the dendritic web thickness (117 μm), so that very high efficiency cells could potentially be made from this material with good surface passivation and optical enhancement. An efficiency of 16.7% (J_{sc} of 36.7 mA/cm^2, V_{oc} of

0.586 V, FF of 0.774, and area of 1 cm^2) was demonstrated, which was probably about the highest demonstration at the time on a potentially low-cost one-sun c-Si material. This demonstrated the advantage of the single-crystal ribbon growth for high quality. The largest issue for dendritic web was improving the yield and throughput of the dendritic web growth. Hence, the bulk of the research was spent on understanding the thermal characteristics of the crystal growth. A detailed thermal model of the crystal growth was combined with a model of crystal defect generation in the growing crystal (Figure 3.1). The model results were compared with experimental observations, and good agreement was found. The origin of dislocations in the silicon web was discrete sources on the dendrites, which was thought to be related to freezing droplets. Localized heating of the dendrite using a laser significantly reduced the generation of dislocations. Thermal stresses farther from the growth front can be controlled with a thermal modifier that reduces buckling of the web crystal and concomitant generation of dislocations. The crystalline defects were correlated with cell performance – material with higher stress had lower efficiencies and yields.

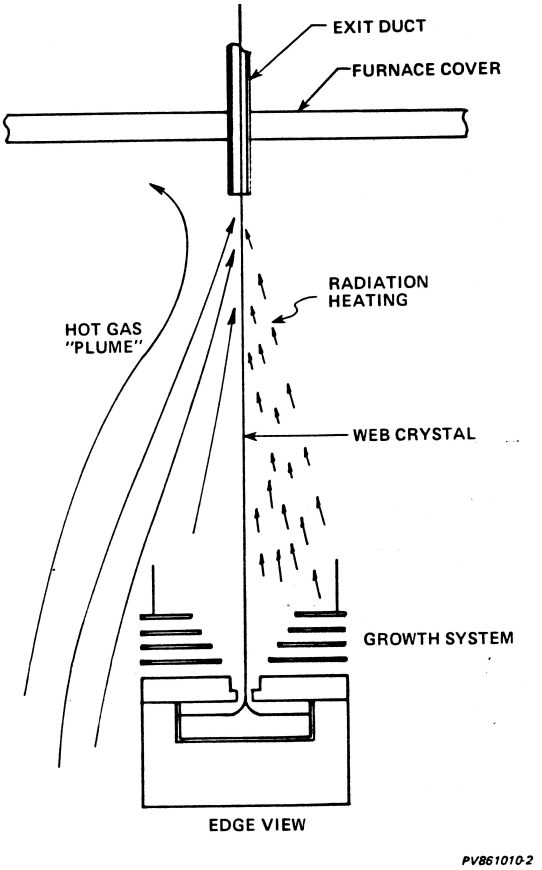

Figure 3.1. Illustration of Factors Affecting the Thermal Profile in Dendritic Web Growth

A second approach to reducing the c-Si wafer cost was to use c-Si films on a supporting substrate. AstroPower Corporation championed this approach. Their vision included a series of products based on the thick-film silicon that would evolve into larger solar cells, thinner silicon with optical enhancement, and monolithic integration (Figure 3.2). AstroPower developed a proprietary c-Si deposition technique (Silicon-Film™) and conductive ceramic substrates using processes that could easily be scaled to support their product vision (Figure 3.3).

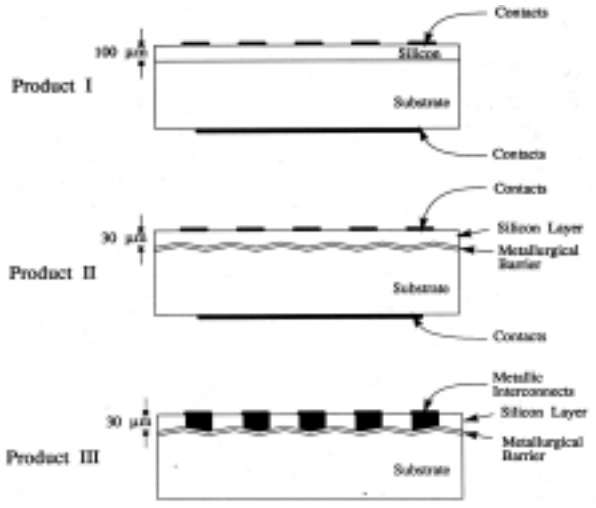

Figure 3.2. Illustration of Evolution of Products based on AstroPower's Silicon-Film™ Process

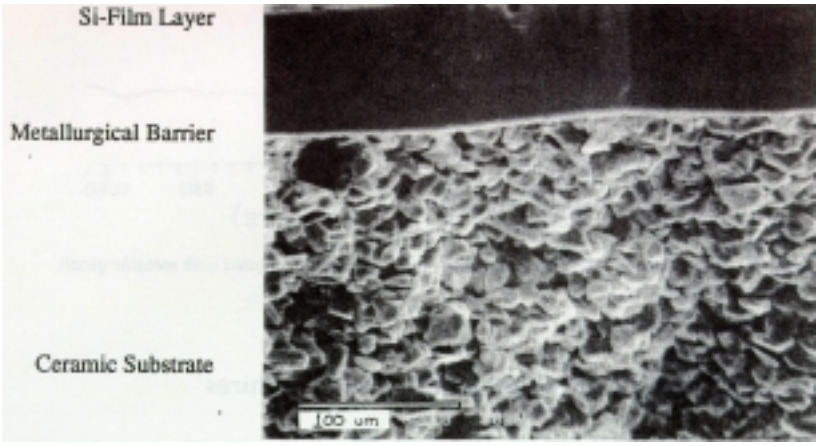

Figure 3.3. Cross-sectional Photomicrograph of Silicon-Film™ Material Deposited on Ceramic Substrate with Metallurgical Barrier Layer

AstroPower made very rapid progress in these early years. The small-area efficiencies of 10.2%, 14.7%, and 15.7% were reported for cells fabricated using Silicon-Film™ material between 1987 and 1989. T he Silicon-Film™ process was also improved and scaled to larger dimensions. Large-area efficiencies of 8.7% (78 cm^2) and 10.9% (100 cm^2) were reported in 1989 and 1990, respectively.

AstroPower guided their development with device and optical modeling, and developed a set of "design guidelines" for the material and processes. An example design guideline is that the grain size should be several times greater than the film thickness. AstroPower and Sandia had also begun identification of impurities in the Silicon-Film™ material and the source of the impurities in the process towards the end of this program.

University c-Si Materials Research

The lower cost c-Si materials that were under development generally involved faster growth rates that produce higher concentration of crystalline defects, and lower quality feedstocks and processes that yield higher levels of contamination. The contamination might involve metallic impurities and, depending upon the specific growth technique and equipment, carbon, oxygen, and/or nitrogen at solid solubility.

Research was conducted with universities to help understand these issues. Cornell University (Dieter Ast, Principal Investigator) examined the high-temperature deformation of silicon. The intent was to understand the stress-strain relationship nearer the growth temperature, which is important for modeling crystal growth and defect generation. In addition, a fundamental study of stress and dislocations in c-Si was warranted due to the strong correlation between cell efficiency and stress.

Cornell used a four-point bending apparatus to measure the stress-strain relationship. Solarex provided Cornell with both high-quality and low-quality material for analysis. Cornell found that the low-quality material resisted plastic deformation at 1100°C and was harder than the high-quality materials (Figure 3.4). High contrast EBIC also found regions with extended dislocation networks in the low-quality material. It was hypothesized that the extensive dislocation networks dominated both the mechanical and recombination properties of the low-quality samples, and were related to the stresses during the crystal growth.

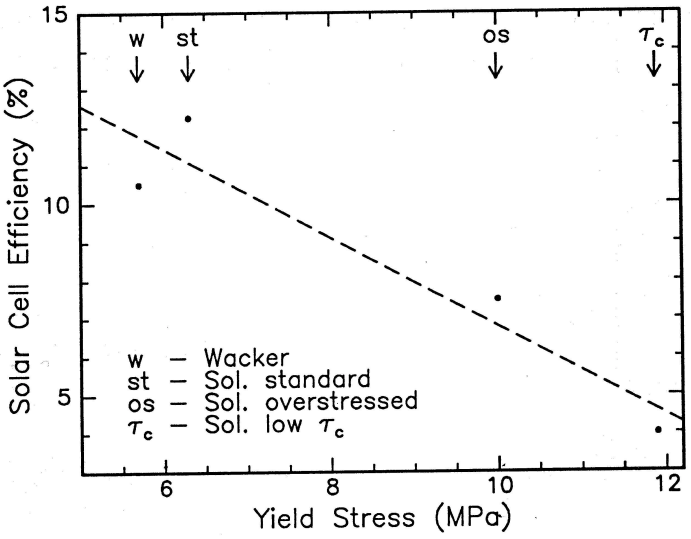

Figure 3.4. Correlation of Solar Cell Performance with Yield Stress in mc-Si Substrates

Cornell next examined the electrical activity of defects using a variety of microscopy techniques. A particularly useful result was a comparison of low- and high-accelerating voltages (20- and 200-keV, respectively) for EBIC. A much better correlation was found between J_{sc} and high-accelerating voltage EBIC than with the low-accelerating voltage EBIC, which is due the greater penetration depth of the electrons with the high acceleration voltage.

A comprehensive examination of the electrical activity of defects in mc-Si was found to be difficult due to the very complex environment. Cornell fabricated well-controlled crystalline defects that were free of impurities by wafer bonding sc-Si FZ substrates to form twist boundaries. These studies found the electrical activity correlated well with the crystalline structure; i.e., the jogs and kinks were responsible for the electrical activity in the screw dislocation.

Arizona State University (ASU) (Dieter Schroder, Principal Investigator) used a wide variety of techniques to examine the electrical activity of impurities and defects in edge-defined film-fed growth (EFG) silicon from Mobil Solar Energy Corporation. EFG is a promising mc-Si silicon ribbon growth technique that features long crystal grains oriented in the growth direction, high concentration of carbon, and low concentration of oxygen.

Mobil provided ASU with samples that were intentionally contaminated with high levels of chromium. Chromium is a common contaminant due to its use in stainless steel. A wide variety of characterization techniques (current-voltage, DLTS, EBIC, TEM, SPV, etc.) were used to examine the materials. ASU found that chromium ions reversibly bond with boron ions in the silicon lattice similar to the iron-boron reaction; i.e., Cr^+ bonds with B^- to form Cr-B pairs. The Cr-B pairs can be dissociated into ions with a short

210°C anneal, and these ions will subsequently bond again into Cr-B pairs with a 230-hour time constant (Figure 3.5). ASU also found $CrSi_2$ precipitates in the Cr-contaminated EFG mc-Si with denuded zones around the precipitate.

ASU also examined ingot mc-Si material provided by Solarex. The material included wafers from both standard and highly stressed mc-Si ingots. The highly stressed mc-Si ingot was due to insufficient release between the ingot mold and the silicon ingot during solidification. ASU found large SiC precipitates with a "morningstar" structure in the low-efficiency highly stressed material (Figure 3.6).

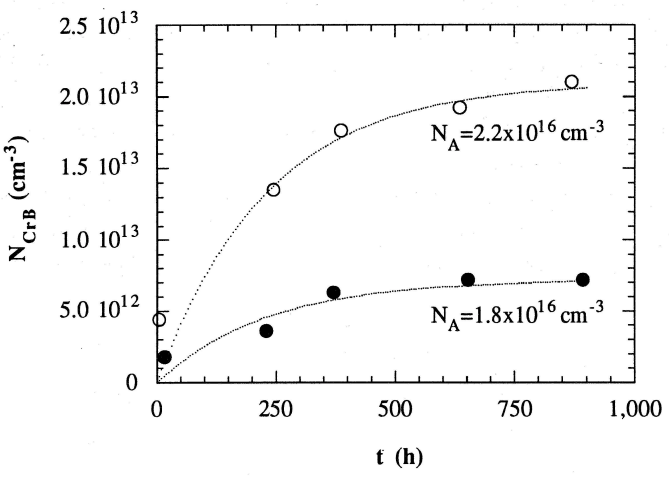

Figure 3.5. The Number of Cr-B Pairs as a Function of Time in EFG mc-Si at Room Temperature

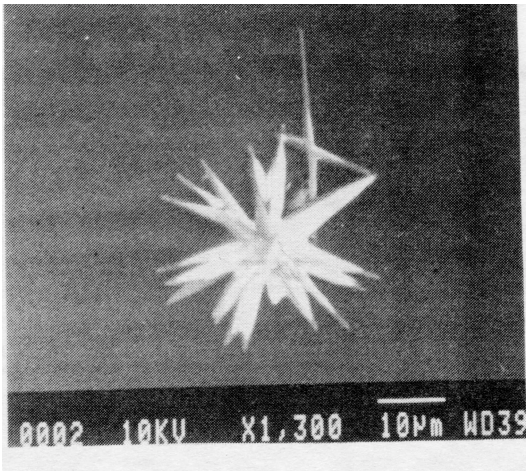

Figure 3.6. SEM Photomicrograph of a SiC Precipitate with a "morningstar" Crystallographic Structure in a mc-Si Substrate

High-Efficiency One-Sun PV Research

The research in c-Si concentrator cells provided a solid base to understand issues required for high efficiencies. As described in the previous chapter, the concentrator cell research at UNSW and Stanford was used to demonstrate the features required for a high-efficiency one-sun c-Si solar cell. This research also advanced the understanding of c-Si parameters for device modeling, such as improved values for the intrinsic-carrier concentration (n_i), bandgap narrowing, and minority-carrier diffusivity.

To complement this work, university research was conducted to develop tools for high-efficiency one-sun c-Si cell research. The University of Florida (Arnost Neugroschel, Principal Investigator) investigated a new technique for extracting the recombination parameters from a c-Si solar cell. The technique analyzed the transient response of a solar cell in the frequency domain, and was able to independently determine the bulk diffusion length, back-surface recombination velocity, and minority-carrier diffusivity. It is very difficult to measure the minority-carrier diffusivity at these low concentrations. The University of Florida found evidence that the widely used presumption of assuming that the minority-carrier density is equal to the majority-carrier concentration may be erroneous.

The University of Delaware (Karl Boer, Principal Investigator) compared different approaches for numerically modeling the device physics of solar cells. Most numerical models use the finite element method to solve the semiconductor equations. Both Purdue University (which performed considerable numerical device modeling under the concentrator program) and PC-1D (a Sandia model that will be described in the next chapter) use the finite-element method. While the finite-element method is computationally efficient, it is more difficult to set up and to modify. Runge-Kutta approach involves fewer approximations and is more physically rigorous, but is less computationally efficient.

The University of Delaware found that the finite element approach worked very well in comparison with the Runge-Kutta technique. Discrepancies were found for subtle effects in space-charge recombination when the recombination center has a large difference in the cross-section for electron and hole capture.

Conclusions

The project was reaccessed based on progress on high-efficiency devices and on one-sun c-Si materials. The high-efficiency work had established most of the fundamental c-Si material and device parameters, provided tools for device and optical design and characterization, and established the requirements for high-efficiency one-sun c-Si solar cells. The latter included:

- Optics – maximize J_{sc} through maximum optical absorption, including minimizing extrinsic reflectance losses and maximizing internal optical path length ("light trapping")
- Device Structure – maximize V_{oc} through minimizing recombination losses, including long bulk diffusion lengths, optimally doped contacts, and well passivated surfaces
- Processing – low-cost high-throughput processes for low-obscuration, low-resistance contacts and grids, optimally doped contacts, passivated surfaces, etc.
- Material – low-cost c-Si material with bulk diffusion lengths greater than device thickness.

The fundamental requirements were now well understood for high efficiencies – the issue became how to translate these requirements into manufacturable processes. The c-Si materials project was transferred to SERI, while the Sandia c-Si project emphasized research on processes that could translate the high-efficiency features into manufacturing.

Chapter 4. THE PDFL COMES ON LINE: 1989-1993

New Process Development Laboratory for c-Si PV Research

The rapid progress in high-efficiency c-Si solar cells provided a thorough understanding of the features necessary for high conversion efficiencies. The issue then becomes how to incorporate these features into manufacturable processes. This type of research is not properly performed in one-of-a-kind laboratory environments. Rather, a laboratory with a tightly controlled, manufacturing-like environment is needed in order that true process characterization (repeatability, tolerance limits, etc.) can be performed. In essence, a laboratory that spanned the region between university-like experiments (high efficiency and fundamental understanding) and industrial needs (process refinement and low cost) was needed (Figure 4.1).

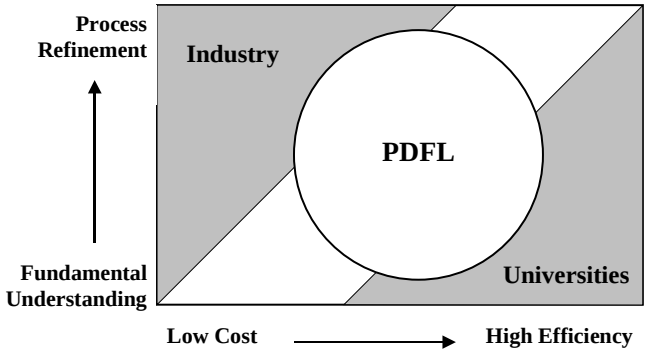

Figure 4.1. Philosophy of Process Development Laboratory

The Photovoltaic Device Fabrication Laboratory (PDFL) was inaugurated at Sandia in June of 1989 in order to meet this need. The laboratory featured exceptionally clean processing environment and sophisticated semiconductor process equipment compared to typical laboratories used for photovoltaic research at the time. The PDFL was fortunate in that a 100-mm integrated-circuit production line at Sandia was decommissioned at about the same time so that many materials, some process equipment, and some facilities were obtained at no charge to the program. All laboratory operations (experiments, equipment process controls, equipment maintenance, material control, etc.) were handled through an internally developed database that essentially functioned as a manufacturing execution system. The laboratory featured very tight internal process controls and baselines to ensure process repeatability.

The objective of the process laboratory was to assist in the transfer of laboratory-scale advances in cell design and processing, which are typically first developed at universities, to large-scale processing in industry. The PDFL pursed this goal through maintenance of high-quality and tightly controlled batch (25 wafers per batch) processing that is capable of state-of-the-art cell performance, and through strong collaborative research programs with PV industrial and university partners.

This chapter reviews the process development and control strategies of the project, the initial development of new modeling and characterization tools, and the institution of an industry/National Laboratory research team to guide the research.

Process Development Strategies

The PDFL and the Sandia c-Si PV Project adopted modern strategies for process control and process development to help demonstrate advantages of these strategies to the PV industry. For process development, the project made extensive use of statistically based, experimental designs. These experimental designs obtain the required information with the minimum number of experiments, and are therefore particularly useful for characterizing complex processes with a large number of variables.

The PDFL primarily used experimental designs based on response surface methodology. This experimental strategy maps out the response surface of the observable to a range of experimental conditions. A typical experimental sequence might first screen a large number of variables to determine the most significant factors, and then perform a more detailed experiment to map the response over these factors. This experimental strategy was used for optimizing many of the processes in the laboratory, such as wafer cleaning, texture etching, laser scribing, and phosphorus diffusions – and then was used in much of the device and process research that will be described in subsequent chapters. Some particularly useful examples of this work follow.

Wafer Cleaning Optimization. A critical step in high-efficiency c-Si solar cell fabrication is the wafer clean prior to high-temperature processes (e.g., oxidation or diffusion of dopants). The issue is to clean the surface and maintain long injected-carrier lifetimes in the silicon while using less chemical and generating less chemical waste. The semiconductor industry's standard clean uses several chemical processing steps and hydrogen peroxide ("RCA" clean) that is optimized to sequentially remove organic residues and metal ions. The PV industry generally only uses a alkaline silicon etch (typically NaOH) followed with an HCl dip to remove any alkali metal ions.

There are a large number of chemical processing steps that might be considered for a wafer clean. We examined 22 possible factors associated with wafer cleaning, and monitored the wafer cleanliness with a PCD lifetime measurement after a high-temperature oxidation. A "main effects" experimental design was used to determine the most significant factors (Figure 4.2).

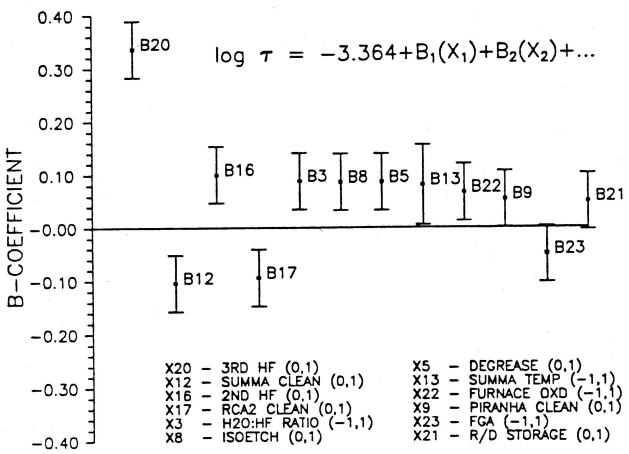

Figure 4.2. Regression coefficients of the 12 largest factors for the PCD lifetime. The other factors were statistically insignificant. Positive values indicate that the factor improved the lifetime of the oxidized wafer.

The final step (dilute HF acid dip) had the largest positive influence on the wafer lifetime. The most important result of the experiment, however, was that the expensive semiconductor-industry cleans based on solutions with hydrogen peroxide were not necessary and, in the case of the ammonium hydroxide:hydrogen peroxide step, even detrimental to the lifetime.

Texture Etch Optimization. A second example of the use of experimental design strategies to optimize processing is texture etch. Anisotropic silicon etches based on isopropyl alcohol:potassium hydroxide:water solutions is widely used in c-Si PV manufacturing to texture the silicon surface. Textured silicon surfaces are advantageous for reducing surface reflectance and increasing the solar cell's current. Texture etches have also been difficult to control and optimize.

This experiment used a "quadratic" design that allows for finding maxima in the response surface. Such designs are useful for optimization in that it identifies areas where the response is optimized. Five factors associated with the etch were investigated (Figure 4.3). The quality of the textured surface was monitored with the hemispherical reflectance at 1000 nm.

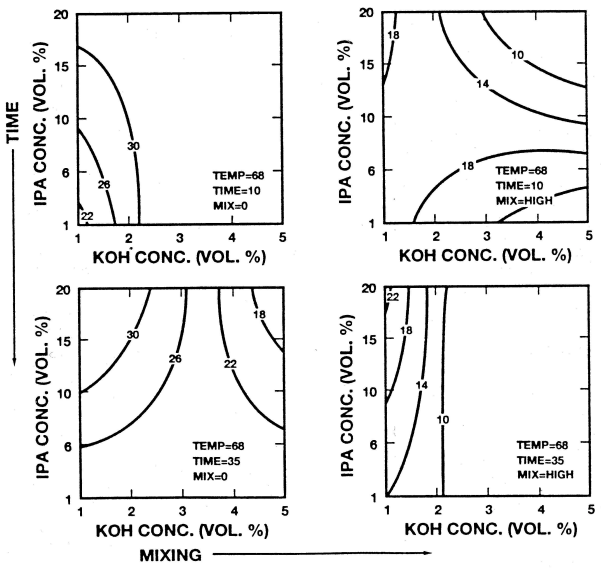

Figure 4.3. A plane from the 5-dimensional response surface of hemispherical reflectance at 1000 nm and solution temperature of 68°C.

The response surface exhibited a high degree of interactions, with no single variable having a dominant effect. This is consistent with the difficulty in identifying a repeatable texturing process. The experiment was able to identify a texture-etch process that yields excellently textured surfaces with wide process latitude.

Process Control Strategies

A second element of the process control and development strategy is use of rudimentary statistical process control. In particular, control charts were maintained on a number of critical processes. A "baseline" experiment was performed approximately every two weeks that monitored critical processes – e.g., phosphorus diffusion, oxidation, PCD lifetime, etc. The inclusion of the PCD lifetime measurement meant that this baseline monitored both the state of processes and the cleanliness of the laboratory.

PCD Lifetime Control Charts. The most important and useful control chart concerned the PCD lifetime. The PCD lifetime measures the effective recombination lifetime of injected carriers in the c-Si substrate, which is the most fundamental parameter affecting the PV conversion efficiency. Figure 4.4 presents an example of the baseline in early laboratory operations. Early operations used a conservative schedule where acid solutions were replaced every week and the acid baths were given an acid clean. The baseline was able to identify a simpler and less expensive procedure where only the chemical in the final step (HF dip) was replaced with each experiment.

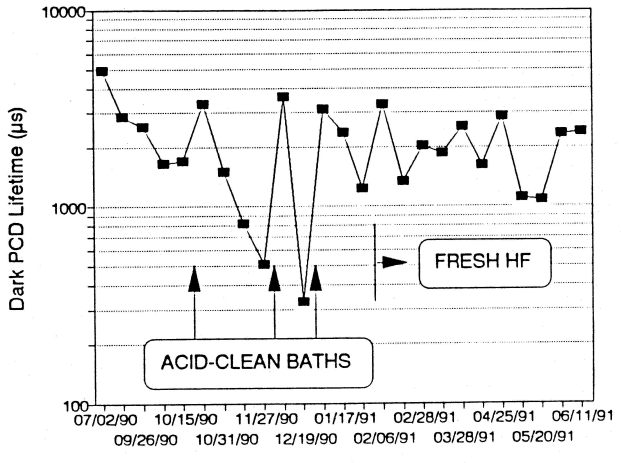

Figure 4.4. Control chart of PCD lifetimes of oxidized FZ wafers from biweekly baseline experiments illustrating effect of different cleaning procedures.

Statistical process controls were also able to identify other subtle sources of contamination. For example, we discovered that the silicon carbide paddle that holds the quartz boat with the silicon wafers inside the furnace tube can be a source of contamination – the edges of the wafers nearest the paddle exhibited low PCD lifetimes. This problem could be avoided by oxidizing the silicon carbide paddle at high temperatures. Similarly, cleaning and/or replacement of the furnace tubes was scheduled based on the control charts. Cleaning of the furnace tubes only as needed helped reduced chemical consumption and waste generation.

Chemical Waste Reduction. Chemical wastes involve substantial costs for disposal and environmental risks. By use of statistical process controls, we were able to systematically reduce chemical consumption by increasing the period of use of chemical solutions and through equipment modifications (Table 4.1). The reduction of 5000 liters of waste between 1993 and 1995 corresponded to a reduction of $160,000 in waste disposal costs.

Table 4.1. Chemical waste reduction in PDFL

Year	Liters of Waste	Processing Steps	Intensity (liters/step)
1990	3157	2800	1.13
1991	4082	3797	1.08
1992	4068	6802	0.60
1993	2872	6898	0.42
1994	2191	6293	0.35
1995	2080	6600	0.32

Our experience in process optimization and control was highlighted in a short course on c-Si solar cells and processing that was presented at the 22nd IEEE Photovoltaic Specialists Conference (Louisville, KY, 1991).

Photoconductance Decay Lifetime Measurement

PCD lifetime measurements were found to be very useful and important process diagnostic. We improved the data acquisition and added a dc light bias to a commercial instrument. The addition of the light bias was particularly important for avoiding measurement anomalies due to traps that are common in many low-cost c-Si materials. We also used the modification to develop a new technique for measuring the emitter saturation current density (J_{oe}), which is a parameter associated with the recombination current in a heavily doped region on the surface of a c-Si solar cell ("emitter").

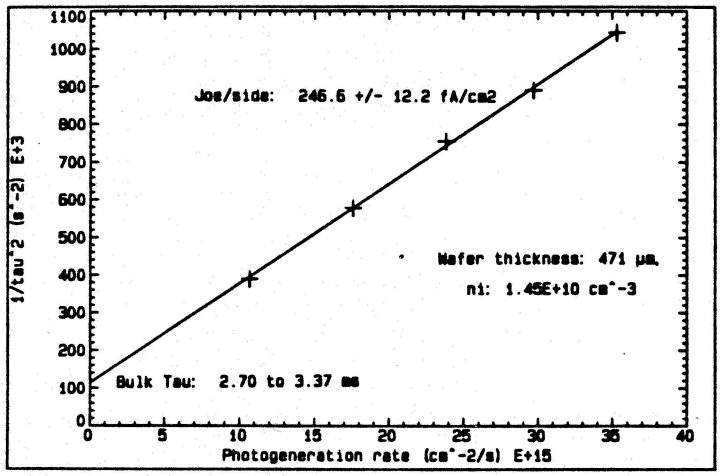

Figure 4.5. Extraction of J_{oe} using PCD measurements.

The technique measured the PCD lifetime as a function of dc light bias in high-resistivity silicon wafers (Fig. 5). The technique was transferred to several universities.

Numerical Modeling of Silicon Solar Cells

Device models are critical elements in device design and optimization. Fully numerical modeling is the most rigorous since fewer simplifications are necessary compared to analytical models.

We developed a numerical semiconductor device model that was optimized for analysis of solar cells. The notable feature of this program (PC-1D) is that it runs on personal computers while most previous models could only run on more expensive machines. In keeping with making the

program more useful to a wide part of the community, the program also featured a simple user interface, automatic mesh generation, integrated parameters for common semiconductor materials (e.g., silicon, GaAs, etc.), ability to input user defined parameters, detailed photogeneration model including some thin-film and thick-film optics, both transient and steady-state simulations, batch processing for running series of simulations, and many other features for solar cell simulation. A series of releases over the life of the Sandia c-Si PV Project has implemented various significant improvements, such as improved speed and convergence, ability to simulate textured cells and other improvements in the optical models, and operation under Windows™ environment.

This program has been extremely useful in all our c-Si research. For example, it was instrumental in developing new characterization techniques and understanding transient measurement anomalies in high-resistivity c-Si solar cells. It has also become a standard in the PV community for device modeling and is one of the most cited programs in the PV technical literature.

Industry/National Laboratory c-Si Research Team

The project early recognized the need for coordination of research among different organizations in c-Si research. In addition, it wished to directly incorporate c-Si industry needs into the project planning. This procedure would facilitate technology transfer, help direct the project towards critical needs, and provide coordination of c-Si PV research. The original request to form such a research team came from industry.

A research team was formed in 1992. The team was originally formed to examine multicrystalline-silicon materials and processing, and was therefore called the *Multicrystalline-Silicon Research Cooperative.* The cooperative was expanded to include sc-Si manufacturers in 1995, and was renamed the *Crystalline-Silicon Research Cooperative.*

These research teams were among the first industry/laboratory research teams to be formally instituted within the DOE PV Program. The research team consisted of senior researchers from US c-Si PV manufacturers, and researchers from the National Renewable Energy Laboratory (NREL) and Sandia National Laboratories. The team met once or twice a year to review the project. Sandia managed the project, which included establishing a Statement of Work and providing quarterly reports to the research team members. The industry members provided input on tasks for the Statement of Work, review of the work progress, and material and processing as needed for the experiments. It was at the urging of some of the industry members that some of the most productive research in the Sandia c-Si PV Project were initiated. These new tasks included texturing of mc-Si and plasma processing for surface and bulk passivation and texture etching.

Chapter 5. CENTER OF EXCELLENCE AT GEORGIA TECH: 1992-2000

The University Center of Excellence for Photovoltaics Research and Education in Crystalline Silicon Solar Cells at the Georgia Institute of Technology (GIT) has been a critical partner in achieving DOE's goal of advancing solar photovoltaic energy to become a significant electrical energy source for the US.

The objectives of the Center are to advance the state of technology in crystalline silicon solar cells through research and development; to educate and train undergraduate and graduate students through courses and laboratory experience; and to collaborate with US crystalline cell manufacturers to improve manufacturing processes, product performance, and cost.

Historically, a gap has existed between laboratory cell performance (24.5%) and commercially produced crystalline silicon cells (13-15%). One activity of the Center is to research processes and designs that have the potential for increasing performance, reducing production costs, and ultimately reducing this performance gap. Over the course of this collaboration, Center researchers have investigated device designs that can lower manufacturing costs and collaborate with manufacturers to improve performance, reduce costs, and increase reliability. Georgia Tech also provides educational opportunities for college and university students in cell fabrication, characterization, modeling, and analysis.

Research and development has included the investigation of potentially lower-cost or higher-throughput processes, and higher-performance, yet inexpensive, device designs. Process and design are based on a fundamental understanding of device behavior and performance-limiting mechanisms. Low-cost processes are directed to remove or avoid these performance limitations. Computer simulation tools are employed to test and predict the performance of new designs and processes.

The Mission

The University Center of Excellence in Photovoltaics Research and Education was awarded to the Georgia Institute of Technology by DOE in 1992 for sustained contributions to the science and technology of photovoltaics. Georgia Tech's mission includes:

- Improving the fundamental understanding of advanced photovoltaic devices
- Fabricating high efficiency solar cells with promising low-cost materials
- Developing low-cost rapid thermal technologies that can reduce manufacturing costs and increase throughput — without sacrificing cell efficiency
- Providing classroom education and hands-on training to enrich the educational experience of students in this field
- Giving the US photovoltaic industry a competitive edge through high quality research and education.

Research at GIT's PV center complemented the research activities at both Sandia and NREL. While NREL concentrated on the growth and characterization of photovoltaic materials, Sandia focused on devices with an emphasis on improvements to industrial design and processes. Research activities at Georgia Tech range from fundamental understanding of photovoltaic materials to modeling and design of high efficiency cells; development of rapid thermal technologies; fabrication of low-cost, high-efficiency cells; and design and performance of photovoltaic systems.

The Approach: High Performance at Low Cost

The first step in GIT's approach toward achieving high performance while keeping costs low involves the fundamental understanding and characterization of performance limiting defects and mechanisms in low-cost photovoltaic materials (see Figure 5.1). The Georgia Institute of Technology has extensive material characterization facilities, DLTS, FTIR, PL, SEM, TEM, PCD Lifetime, EBIC, LBIC, etc., for accomplishing this task.

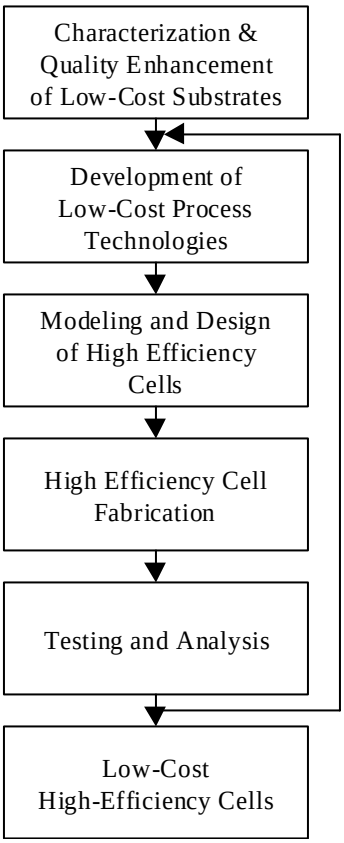

Figure 5.1. Approach toward high efficiency solar cells

The next performance step involves development of cost-effective gettering and passivation techniques that can mitigate the adverse effect of defects to enhance the bulk lifetime. The third step involves computer modeling and device design that can produce practically achievable high efficiency cells on any given material. Step four involves development of novel low-cost rapid thermal technologies for each layer of solar cell, including emitter, back surface field (BSF), antireflection coating, surface passivation, and contacts. The fifth step involves the integration of rapid thermal technologies for fabricating high-efficiency solar cells. The final step involves detailed characterization and analysis of finished devices and developing guidelines for achieving even higher efficiency cells.

Georgia Tech has a library of about 15 different computer programs to analyze and model each layer of a solar cell, in addition to the modeling and design of complete solar cells and photovoltaic systems. There are excellent capabilities for detailed characterization of finished devices, including light and dark I-V, light and dark IQE and spectral response, surface reflectance, LBIC, bulk lifetime and saturation-current density measurements. Finally, Georgia Tech has extensive cell fabrication capabilities ranging from conventional furnace processing to rapid thermal processing, belt line processing, photolithography screen-printing, PECVD SiN, and self-doping contacts.

Rapid Thermal Processing of Silicon Solar Cells

The cost of a silicon PV module must decrease by a factor of from 2-to-4 to allow the widespread implementation of photovoltaics. To accomplish this goal, Georgia Tech seeks to achieve high efficiency cells on low-cost thin silicon materials by developing and integrating rapid and cost-effective technologies. One of these techniques involves rapid thermal processing (RTP).

RTP utilizes banks of tungsten halogen lamps to radiatively heat a sample in a cold wall system. The radiation spectrum of RTP contains high energy visible and UV photons that can accelerate semiconductor processes (such as oxidation and diffusion) to reduce the cell processing time. Because of the cold wall processing and radiative heating, RTP can perform simultaneous front and back diffusion or oxidation without cross contamination. This reduces the number of processing steps. Reduced processing time and steps reduces material handling, which can significantly improve yield, especially when thin silicon substrates are used for cost reduction. In spite of the RTP advantage, successful implementation of RTP for achieving high efficiency cells poses several challenges including bulk lifetime preservation during rapid heating and cooling, achieving optimum doping profiles in a very short time, obtaining good surface passivation within a couple of minutes, and development of a continuous RTP machine. Georgia Tech is addressing all the above issues. Researchers at Georgia Tech have done pioneering work in this field by developing rapid thermal technology for each layer of silicon solar cell while maintaining high efficiency. They have fabricated record high efficiency RTP cells (see Figure 5.2) and continue to raise the efficiency by making RTP more manufacturable and adaptable to advanced cell design concepts.

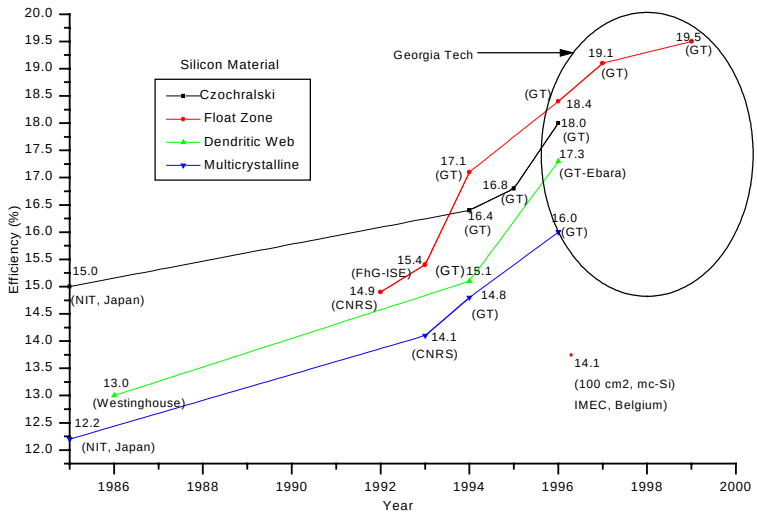

Figure 5.2. Progress of RTP cells

Rapid Screen-Printed Metallizations

One of the most difficult aspects of large-scale solar cell production is forming low-cost, high-quality front contacts. Screen-printing (SP) offers a simple, cost-effective contact method that is consistent with the requirements for high-volume manufacturing. However, the current problem with SP is that the throughput gains are attained at the expense of device performance. Literature shows considerable scatter in the fill factor values of SP solar cells. In addition, there are no clear guidelines for achieving high fill factors. Fill factors in excess of 0.78 can raise the screen-printed industrial cell efficiency by about 1% absolute. As a result of this fact, a methodology for optimizing SP metallization was developed at Georgia Tech, recognizing that fill factor can be degraded by both (1) gridline resistance and contact resistance and (2) contact formation induced junction leakage and shunting.

The first step in this methodology involves measuring metal resistivity as a function of firing temperature. For the Ag paste #3349 used in this study, metal resistivity decreased with increases in firing temperature and for a firing time of 30 sec and went below 3 m-ohm-cm for firing temperatures above 700°C. Model calculations indicated that 3 m-ohm-cm was sufficient to achieve fill factor in excess of 0.78.

The next step involved measuring shunt resistance as a function of firing temperature, which showed that for 30 sec firing time, firing temperature should not exceed 730°C to maintain Rsh in excess of 1 kΩ cm^2. The third step involved carefully tailoring the junction depth for the 730°C/30 min firing cycle in order to minimize junction leakage current (J_{02}). It was found that ~0.5 μm deep junction with a sheet resistance of ~40 ohms/sq was required to maintain J_{02} value below 10^{-8} A/cm^2 along with acceptable shunt resistance.

Finally, a 400°C/10 min forming gas anneal was required to reduce the series resistance to about 0.6 ohm-cm^2. Systematic optimization of the firing cycle and junction depth, coupled with a post contact forming gas anneal, resulted in fill factors as high as 0.795 on monocrystalline silicon (mc-Si). Preliminary results on multicrystalline silicon cells indicate that firing cycle and junction depth may have to be optimized for each multicrystalline silicon material because of the possible role of defects or past-defect interaction in causing junction shunting underneath the gridlines. Shorter firing times in conjunction with higher firing temperatures are being investigated for mc-Si cells. Georgia Tech is working with paste manufacturers to understand and mitigate the impact of paste contamination and frit content, especially when low-cost Si materials are used.

Rapid Phosphorus Diffusion with Low-Cost Spin-On Dopants

The total process for phosphorus diffusion in a conventional furnace requires on the order of one hour at 850-900°C to achieve emitters with appropriate junction characteristics for high efficiency cells. This could severely limit the throughput of a manufacturing line. In this section, emitter formation in a belt line furnace and RTP unit is described and compared with conventional furnace diffusion. Georgia Tech is investigating both belt line and RTP systems (which utilize tungsten halogen lamps) to optically heat the sample. At normal diffusion temperatures, these lamps produce high-energy photons that can significantly increase the effective diffusion of phosphorus in Si when utilized in conjunction with low-cost spin-on dopants (SOD).

In order to support this hypothesis, three different drive-in treatments were performed at 880°C after the application of SOD phosphorus. These treatments were (1) conventional furnace diffusion where the sample temperature is raised by standard resistance heating; (2) beltline furnace diffusion where the sample is heated by a combination of radiation from tungsten halogen lamps, conduction from the belt, and convection; and (3) single-wafer RTP diffusion where the sample is heated primarily by radiation from the tungsten halogen lamps. Figure 5.3 shows that after the SOD application, an 880°C/6 minute RTP drive-in produces significantly more diffusion compared to conventional furnace processing (CFP). The diffusion profile attained with belt line processing (BLP) generally falls between the other two treatments. This is consistent with the high-energy photon content of the three spectra. As a result, a 40 Ω emitter was obtained at 880°C in just 6 and 3 minutes BLP and RTP, respectively. This represents about a factor of 5 to 10 reduction in the diffusion time compared to conventional furnace processing.

Rapid and Improved Aluminum Back Surface Field

The Aluminum (Al) Back Surface Field (BSF) is widely used in commercial solar cells in an attempt to reduce back surface recombination velocity. However, it is not well recognized by the photovoltaic industry that unoptimized processing can lead to non-uniform BSF, which can degrade its quality. For example, slow ramp-up rate to reach the

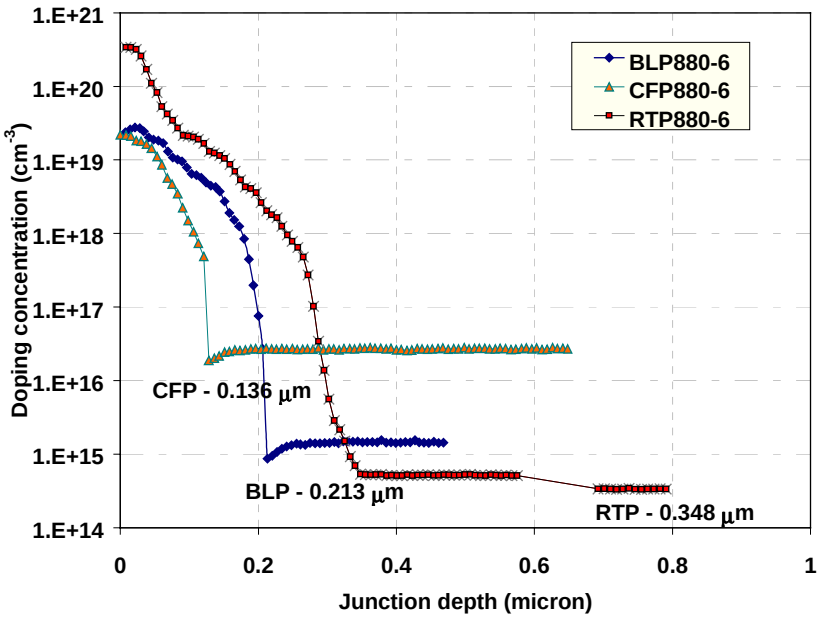

Figure 5.3. Comparison of CFP, BLP, and RTP phosphorus diffusion profiles (diffused at 880°C for 6 minutes using SOD sources) measured by spreading resistance technique.

alloying temperature can lead to local wetting or melting of aluminum. Therefore, very fast ramp-up rates in RTP should help the quality of Al BSF.

GIT has successfully integrated screen printing and rapid thermal annealing to achieve an aluminum-alloyed back surface field that lowers the effective back surface recombination velocity (S_{eff}) to approximately 200 cm/second for solar cells formed on 2.3 W-cm Si. This represents an improvement of about a factor of from 10-to-1000 when compared to devices with poor, or no, BSF. It was found that an Al BSF formed in a conventional furnace in 1-2 hour, using a slow ramp-up rate of 5°C/minute, produced a non-uniform BSF with a surface recombination velocity of 1000 cm/second. The cross section SEM micrograph in Figure 5.4 shows that the non-uniformity includes variation in BSF junction depth, loss of surface planarity, Al spiking, and possible non-formation of the p+ region. In contrast, Al BSF formed in just 2 minutes at 850°C in an RTP system, using a ramp-up rate of 1200°C/minute, produced a very uniform BSF with a back surface recombination velocity of 200 cm/second. Analysis and characterization of the BSF structures in Figure 5.4 show that this RTP BSF process satisfies the two main requirements for achieving low S_{eff} , which are deep p+ regions and uniform junctions. Screen printing is ideally suited for fast deposition of thick Al films, which upon rapid RTP alloying result in deep uniform BSF regions. Use of a rapid alloying treatment is shown to significantly improve the BSF junction uniformity, reduce S_{eff} and increase Voc (Figure 5.5). The Al BSFs formed by screen printing and rapid alloying have been integrated into both laboratory and industrial-type fabrication sequences to achieve solar

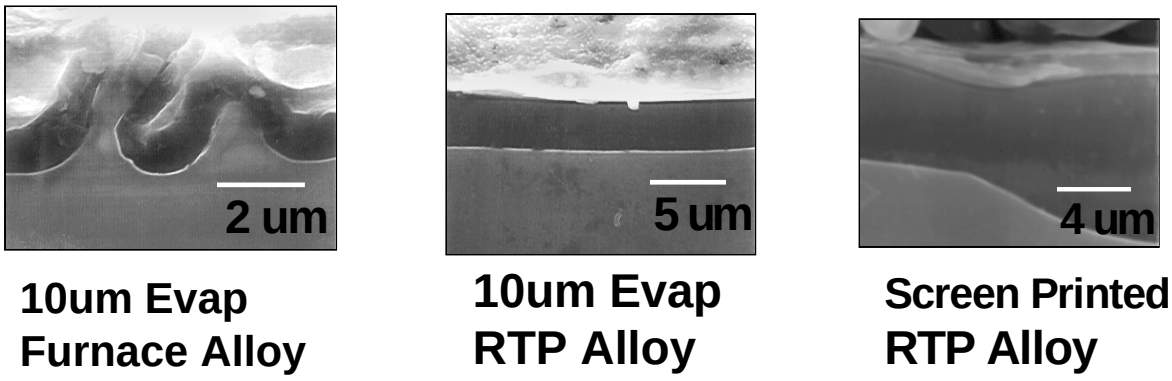

Figure 5.4. SEM images of Al BSFs formed by alloying in the furnace and by RTP.

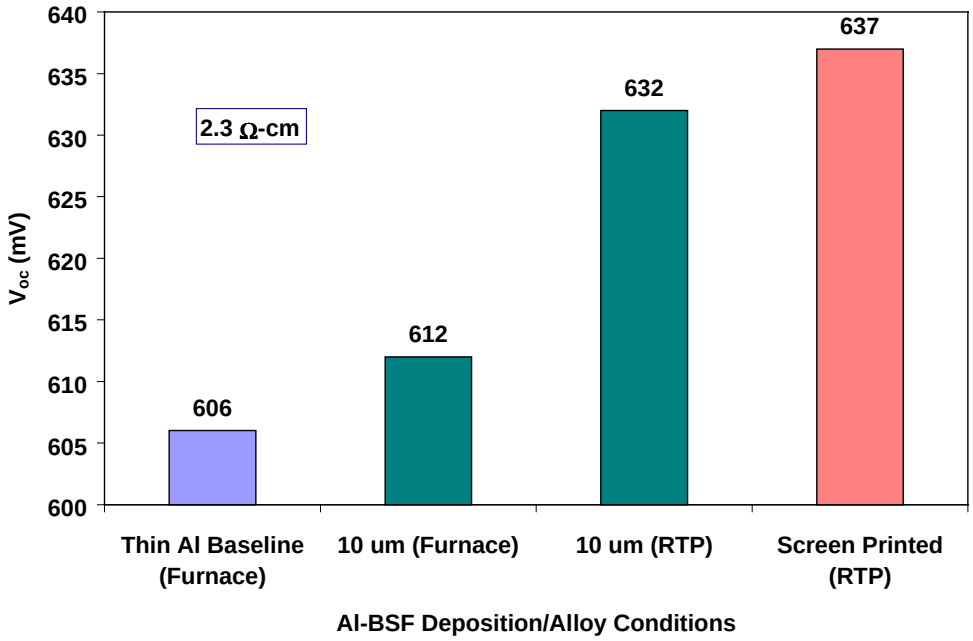

Figure 5.5. Effect of different Al-BSF processes on V_{oc}.

cell efficiencies in excess of 19.0% and 17.0%, respectively, on planar 2.3 W-cm float zone Si. For both process sequences, these cell efficiencies are 1-2% (absolute) higher than analogous cells made with un-optimized Al BSFs or highly recombinative rear

surfaces. The RTP of screen-printed Al BSF not only reduced thermal budget but also produced a higher quality back surface field.

Development of a Novel RTO/SiN Stack

A comprehensive and systematic investigation of low-cost surface passivation technologies was conducted for achieving high-performance silicon devices such as solar cells. Most commercial solar cells today use TiO2 or SiN antireflection coating and lack adequate surface passivation, while laboratory cells use conventional furnace oxides (CFOs) for high quality surface passivation involving an expensive and lengthy high-temperature step. In an effort to develop a low-cost, rapid, and effective surface passivation scheme that can also withstand screen-printed metal firing, Georgia Tech conducted a comprehensive study using all the promising dielectrics. It was found that the passivation quality of all the single layer films, including TiO2, SiN, and thermal oxide, degrades severely after the firing of screen-printed contacts (Figure 5.6). This led to the development of surface passivating technology compatible with low-cost screen printing.

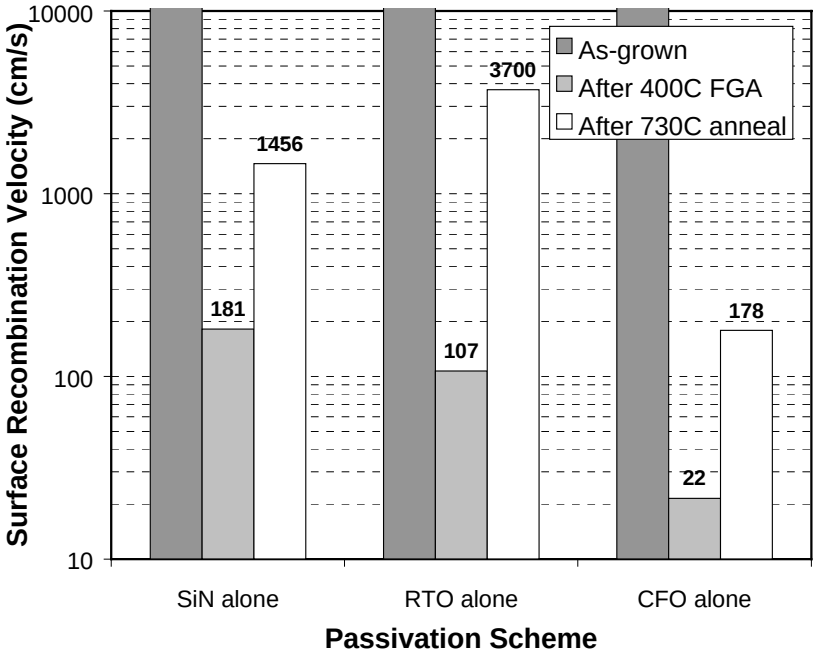

Figure 5.6. Effect of belt line annealing on the S value of individual dielectric passivation schemes.

Georgia Tech developed a rapid and novel surface-passivating scheme, which not only provides excellent front and back surface passivation and antireflection coating but can also withstand 700-800°C screen-printed contact firing. This scheme consists of thin

(100 Å) rapid thermal oxide (RTO) capped with ~750 Å direct PECVD SiN. In addition, the thin RTO is grown simultaneously during the two-minute RTP Al BSF formation. This reduces the number of processing steps and the time. Figure 5.7 shows that this RTO/SiN stack is better than any other passivation scheme, and is capable of reducing undiffused Si surface recombination velocity to less than 20 cm/sec even after the firing of screen-printed contacts. It also reduces the saturation current density of 40 ohms/square and 80 ohms/square phosphorus diffused emitters by factors of 3 and 10, respectively.

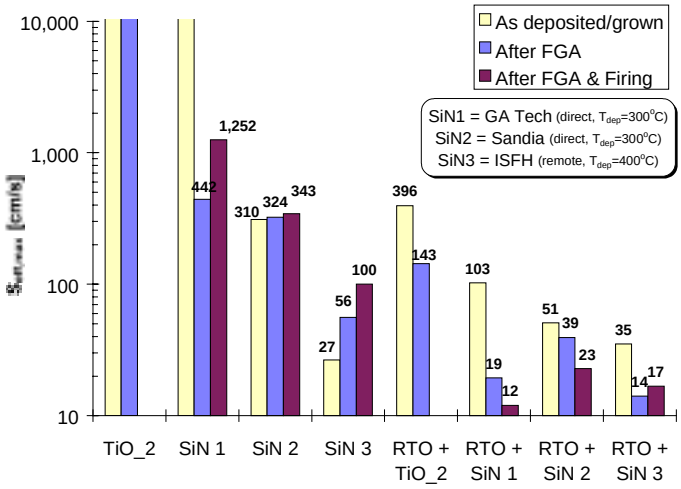

Figure 5.7. Undiffused surface passivation by various films including stack and 730^{o}C screen-printed firing.

Figure 5.7 shows that unlike the single layer passivation, stack passivation actually improves with the firing of screen-printed contacts. This thermal treatment is believed to enhance the release and delivery of atomic hydrogen from the SiN film to the Si-SiO2 interface, thereby reducing the density of interface traps. Compatibility with this post-deposition anneal makes the stack passivation scheme very attractive for next generation cost-effective thin bifacial solar cells where a similar anneal will be required to form front and back screen-printed contacts.

High Efficiency Cell Fabrication by Integration of Rapid Technologies

Georgia Tech has a very strong portfolio of cell fabrication technologies — ranging from conventional furnace processing to rapid thermal processing to belt line processing. Figure 5.8 shows the integration of low-cost rapid thermal technologies for reducing cell fabrication time while maintaining efficiency cells. Figure 5.9 shows the corresponding cell efficiencies on monocrystalline silicon.

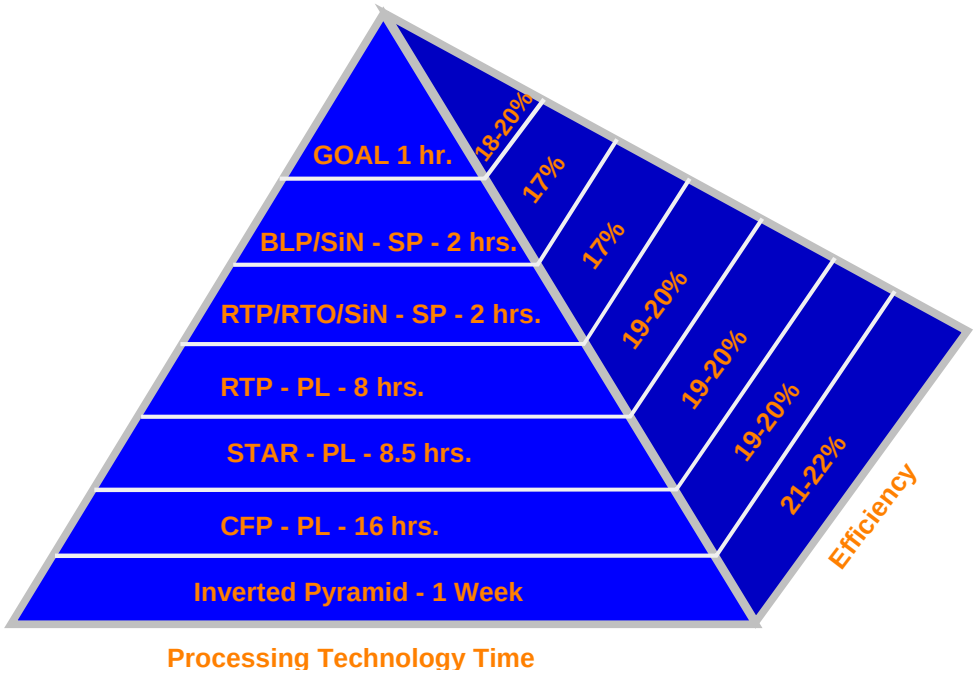

Figure 5.8. Improved technologies for reducing processing time and increasing cell efficiency

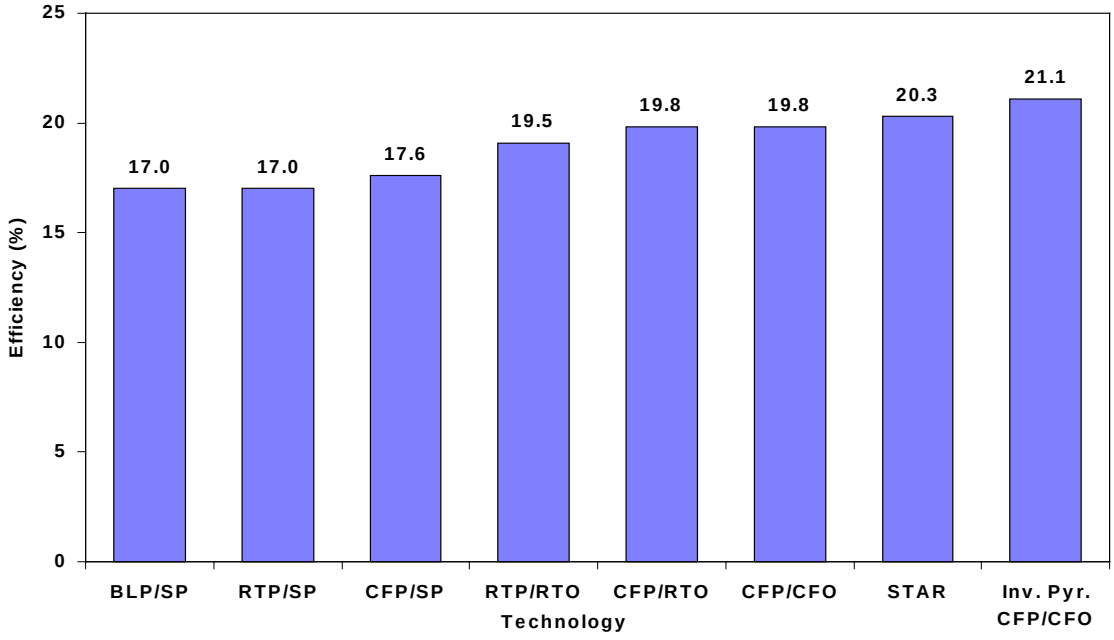

Figure 5.9. Efficiency versus techniques on mono-crystalline silicon solar cells

Conventional Furnace Processing with Photolithography Contacts. In 1993, shortly after the Center for Excellence was established, Georgia Tech achieved 21-22% efficient silicon cells by excellent optical and electrical confinement using inverted pyramid texturing and point contacts on the back. This process required multiple high-temperature and photolithography steps and took about one week of processing time, which is unacceptable for low-cost cells. Next, a simple baseline process (SBLC) was developed that involved emitter diffusion, oxide passivation, and 1μm Al back surface field formation in a conventional furnace. Contacts were formed by evaporation and photo-lithography. The SBLC process involved 6 hours of high temperature processing, 2 hours of metal evaporation and 5 hours of photolithography, resulting in 13 hours of processing time and about 18% efficient cells without any surface texturing. Figure 5.10 shows that the SBLC process gave 16-19% efficient cells on various low-cost multicrystalline silicon materials.

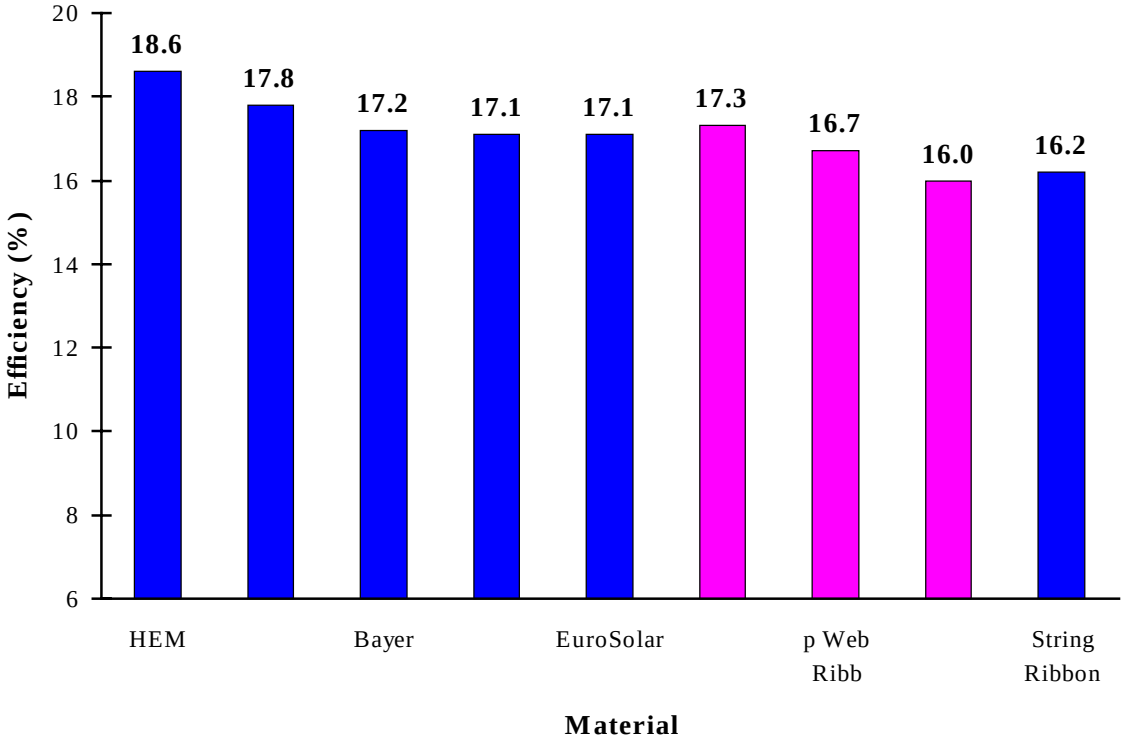

Figure 5.10. Record high efficiency on multi-crystalline SBLC/PL (areas = 1 cm^2 or 4 cm^2)

Rapid Thermal Processing with Photolithography Contacts. The above SBLC process was modified and shortened significantly by completely replacing furnace processing by rapid thermal processing in which phosphorus diffusion, screen-printed Al BSF formation, and oxide passivation were performed in a single wafer RTP system. The 80 Ω RTP phosphorus diffusion was performed in 3 minutes. Al BSF was formed by screen-printing thick Al paste in less than a minute, followed by a less than 5-minute RTP in an oxygen ambient. In addition to forming a very effective and deep BSF, this

RTP step also produced a high quality, rapid, thermal oxide on the front (simultaneously). This novel RTP sequence reduced the total high-temperature processing time from 6 hours in the case of CFP to less than 15 min. In addition to reducing the total processing time from 13 hours to 7 hours, the RTP and photolithography process produced higher efficiency cells than conventional furnace processing. The RTP cell efficiencies of 19.5% compared to 17.8% for the CFP cells.

Rapid Thermal Processing of Screen-Printed Cells. In an attempt to reduce the cell processing times further, the evaporation and photolithography contacts on the front were replaced by screen-printed Ag contacts. Because of the high contact resistance and junction shunting, the emitter sheet resistance of the SP cells was decreased from 80 to 40 ohms/sq to achieve good contacts and high fill factors (FF). This increased the emitter diffusion time from 3 to 7 minutes. An 800 Å thick PECVD SiN coating was deposited on top of RTO for stack passivation and single-layer AR coating. Ag contact grid was screen printed on the front and fired through the SiN AR coating in less than 5 minutes. This reduced the contact formation time from 330 minutes to 8 minutes. This RTP/SP process reduced the total cell processing time from 8.5 hours to less than 2 hours and produced a planar cell efficiency of 17% with a fill factor of 0.798.

Screen-Printed Solar Cells by Belt Line Processing. Because there is no continuous RTP machine available today, GIT has been trying to improve and optimize the lamp-heated belt line processing to achieve high efficiency cells in a very short time. A rapid belt line process has been developed that involves 925°C/6 min 40 ohms/sq phosphorus diffusion for the emitter, 825°C/2 min drive in air for the screen-printed Al BSF formation, and 730° C/30 sec heat treatment for the firing screen-printed Ag contact through the PECVD SiN antireflection coating. The total BLP time was less than 2 hours, resulting in 17% efficient cells on monocrystalline silicon.

Screen-Printed Bifacial Cells. Low-cost bifacial cell design involves screen-printing of metal grid on both sides. This increases the power output (due to rear illumination) and also permits the use of thin silicon without wafer warpage. However, rear-illuminated efficiency is a very strong function of back surface recombination velocity. This makes the stack passivation, developed at Georgia Tech, an ideal candidate because it provides excellent front and back passivation, even after the firing of screen-printed contacts. Few bifacial cells have been fabricated on 0.65 ohm-cm float-zone silicon by 40 ohms/sq emitter diffusion, front and back RTO/SiN stack passivation, and co-firing of front and back Ag grid through the stack. This resulted in front-illuminated efficiency of 17% and a rear-illuminated efficiency of 11.6%. Further optimization is expected to produce even higher efficiency cells.

Next Generation Solar Cells

Self-Aligned Selective Emitter by Self-Doping Screen-Printed Metals. Figure 5.11 shows the path toward 18-20%-efficient next generation low-cost screen-printed cells. In the screen-printed devices fabricated so far, the emitter sheet resistance was reduced from

80 ohms/sq to 40 ohms/sq. This lowered the cell performance by about 1% due to heavy doping effects and relatively poor surface passivation. Attempts are being made to fabricate selective emitter cells by forming 10-40 W/o emitter underneath the grid lines and 80-100 ohms/sq emitter in between the grid lines. A special Ag paste is being developed, in collaboration with industry, which upon appropriate firing will allow the heavy n+ self-doping underneath the grid lines. Initial experiments look promising. This concept should give about 1% boost in screen-printed cell efficiencies.

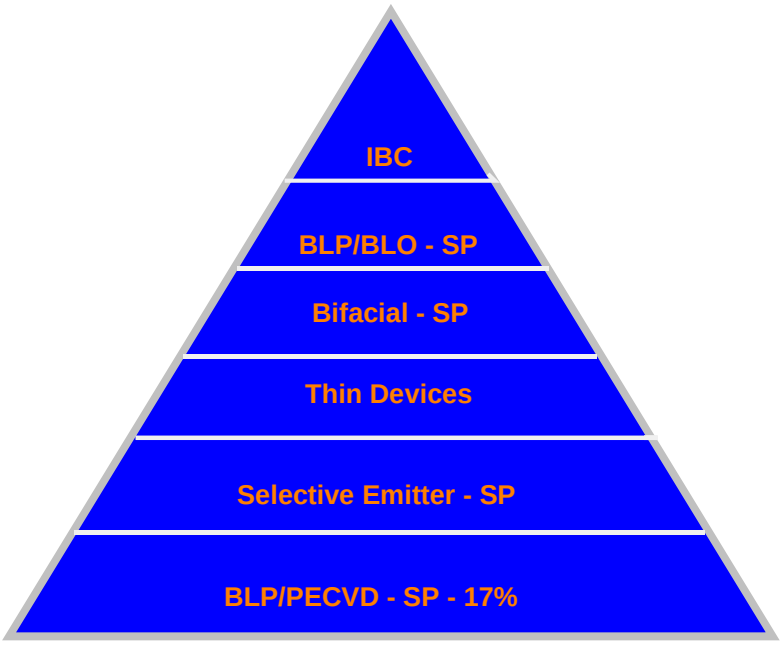

Figure 5.11. Approach toward 18-20% low-cost high efficiency solar cells

RIE Texturing for Light Trapping. The 17%-efficient screen-printed solar cells fabricated so far did not have any light trapping. GIT is working with Sandia to implement RIE surface texturing of the cells. A combination of RIE surface texturing and stack passivation could increase the screen-printed cell efficiency by another 1%. Georgia Tech is also working on porous silicon for surface texturing.

Screen Printed IBC Solar Cells Using Self Doping Contacts. Georgia Tech has recently started fabricating screen-printed interdigitated back contact (IBC) cells using self-doping Al and Ag contacts. Both contacts are on the rear surface and the diffusion is localized to regions immediately beneath the contact area. This structure eliminates contact shading and reduces resistance losses due to the large metal coverage on the back. The illuminated surface is pristine, making RTO/SiN stack passivation an attractive candidate for achieving very low surface recombination velocity. Stack passivation will also be used to passivate the silicon regions between the interdigitated fingers. IBC cells are best suited for thin devices where diffusion length-to-thickness ratio is greater than

three. Georgia Tech has succeeded in screen printing interdigitated grid lines with self doping contacts without shunting, and is in the process of finishing and testing the devices. IBC cells can significantly reduce the module assembly cost because both contacts are on the rear so large numbers of cells can be interconnected in one shot rather than one cell at a time. The fabrication sequence is also very fast and simple, requiring stack passivation on both sides and two screen printing steps on the rear, followed by individual or co-firing.

Development of a Novel Belt Line RTP Machine. Rapid thermal processing cells are slightly superior and faster than the belt line cells. However, no continuous RTP machine is available today to take full advantage of RTO/SiN stack, speed, and performance. Georgia Tech is working with an equipment vendor to custom build a belt line version of RTP in which samples will be heated by tungsten halogen lamps as well as high energy UV photons to expedite the process and reduce the cell processing time.

This belt line machine will also have the capability to grow high quality thin belt line oxide to permit the fabrication of stack passivation. It will also have the provision to avoid any belt-induced contamination to preserve bulk lifetime. This machine is expected to be delivered soon. If everything works according to its promise, then RTP could become a commercial reality, producing low-cost, rapid, and high efficiency devices with high throughput.

Georgia Tech has made considerable strides in transforming the high-cost, low-throughput, and high-efficiency technology to low-cost, high-throughput, and high-efficiency rapid thermal technology. Screen-printed monocrystalline cells with efficiency exceeding 17% have been realized. Research is in progress to further simplify the process and cell design so that even higher efficiency cells (18-20%) can be achieved on low-cost thin silicon materials.

Chapter 6. PROCESSING RESEARCH

By 1990, the PDFL was ready to begin the task of focusing on key semiconductor processing steps crucial for the fabrication of high-efficiency Si solar cells. Each of the individual processes that make up a fabrication sequence were evaluated for peak performance and compatibility with the other steps in the sequence.

Phosphorus Diffusion Process

The phosphorus diffusion is used in p-type substrate processing to form the emitter region of the solar cell. The depth to which the phosphorus dopant diffuses determines the p/n junction depth, and the dopant concentration in the emitter and at the wafer surface is important in determining the amount of unwanted recombination that occurs in this region. Previous work at universities had shown the importance of forming low-recombination passivated emitter regions while maintaining high bulk recombination lifetimes for the fabrication of high-efficiency silicon cells. Many different types of diffusion sources are available for performing the emitter diffusions for each dopant species. Each could affect device quality in a unique way, and each has particular attributes that determine its cost-effectiveness.

In this study, we compared the effects of PH_3 and $POCl_3$ diffusion sources on recombination lifetimes and emitter saturation currents. We also examined the relative costs associated with each, including material, capital, and safety costs. We found that PH3 and $POCl_3$ can both produce equivalent low-recombination emitters while maintaining high bulk lifetimes. However, PH_3 may have a higher yield in this regard. Because the safety concerns regarding PH_3 can be addressed in a cost-effective manner, it has a cost advantage over $POCl_3$ when used at multi-megawatt production levels. (SAND90-1821)

Phosphorus Gettering Process

Solar-grade silicon frequently contains large quantities of defects and impurities that can significantly degrade the excess-carrier lifetime through introduction of recombination sites. The impurities frequently include metals as well as high concentrations of carbon and/or oxygen. Defects and impurities can also degrade the electrical properties of solar cells fabricated in solar-grade silicon by causing shunt currents or excess junction current. Fabrication of acceptable solar cells from such materials requires processes that are tolerant of, or that can even improve, impure and defective material.

Gettering refers to a process step that removes deleterious impurities from active regions of the device to less important regions. Typically, gettering requires several actions to occur. First, the unwanted impurity must be placed into solid solution in the silicon crystal. Next, it must be made mobile. Finally, a site must be provided that is in a less

important region of the device and that can capture the impurity. Typically, gettering is achieved through specific surface and thermal treatments of the silicon crystal.

Phosphorus diffusion is a well-known technique for gettering of impurities in silicon. The effect of phosphorus diffusion on the excess-carrier lifetime in various silicon materials was investigated. The optimum phosphorus diffusion schedule and enhancement of lifetime was found to be material specific, with substantial (5-fold) increases found for some materials.

Table 6.1. PCD lifetime (μsec) of oxidized silicon wafers with and without phosphorus gettering. The statistics were computed on data from 10 wafers of each type that were processed in five different runs. Low-, mid-, and high-resistivity refer to 0.25, 15, and 300 Ωcm, respectively.

Wafer Type	Gettered?	Average	Std.Dev.
p, low-resistivity, FZ	Y	10.21	3.60
	N	9.25	1.82
n, high-resistivity, FZ	Y	3975	853
	N	3845	737
p, low-resistivity, MCz	Y	5.71	1.68
	N	7.10	4.98
n, high-resistivity, MCz	Y	3235	964
	N	2633	465
p, mid-resistivity, Cz	Y	240.2	117.7
	N	44.5	19.7
n, mid-resistivity, Cz	Y	487.6	260.7
	N	372.9	169.8

The FZ and MCz wafers did not show any benefit due to the phosphorus gettering step, while both the n-type and the p-type Cz wafers show a significant enhancement of the lifetime. The PH_3 and the $POCl_3$ getter diffusions were both effective. Substantial enhancement of the lifetime due to the phosphorus-diffusion gettering step was found for both gases.

The next experiment with the Solarex multicrystalline silicon material used a more conservative gettering schedule. The phosphorus diffusion at 900°C improved the lifetime of the Solarex multicrystalline samples from 1-2 ms to 4-10ms. All the multicrystalline-silicon samples degraded after the second high-temperature step. The multicrystalline samples are apparently sensitive to multiple thermal excursions. We processed multicrystalline material provided by Mobil Solar Energy Corporation with a similar process schedule and found similar results.

The FZ and the MCz materials did not respond to gettering. The high-resistivity FZ and MCz achieved long lifetimes without gettering, so these wafers may have been supplied

with less metallic contamination or they are less susceptible to contamination during processing. In any case, a general observation from this work is that the silicon materials that are more responsive to gettering have high oxygen or carbon concentrations. Also, it appears that larger oxygen concentrations can inhibit gettering and decrease the lifetime. Finally, materials with high concentrations of defects (e.g. the multicrystalline samples) are more difficult to getter.

Phosphorus Gettering and Aluminum-Alloying

Three multicrystalline silicon materials were used in experiments for a planned comprehensive gettering study on several industrial solar cell materials. Two processes commonly used to upgrade material quality were investigated: phosphorus gettering and aluminum-alloying. Microwave-detected photoconductance decay measurements of minority-carrier lifetime and detailed analyses of full solar cells were used to determine the response to the gettering processes.

Sandia embarked upon a comprehensive study of the combined effects of phosphorus diffusion and aluminum alloying in industrial multicrystalline materials. Our desire was to develop and carry out an inclusive, yet tractable experimental design for several materials that includes the essential factors for both processes. Two materials were used in these preliminary studies: electromagnetically cast (EMC) material from Osaka Titanium and directionally solidified Heat-Exchanger Method (HEM) material supplied by Crystal Systems.

Figure 6.1 depicts the results of a three-factor interaction study done on EMC material where PCD lifetime was used to monitor the gettering effects. The factors for the experiment were the $POCl_3$ diffusion time at 850°C, the aluminum alloy diffusion time, and the aluminum alloy temperature. For this particular set of data, the alloying step was done after the phosphorus diffusion (qualitatively similar results were obtained with the order reversed).

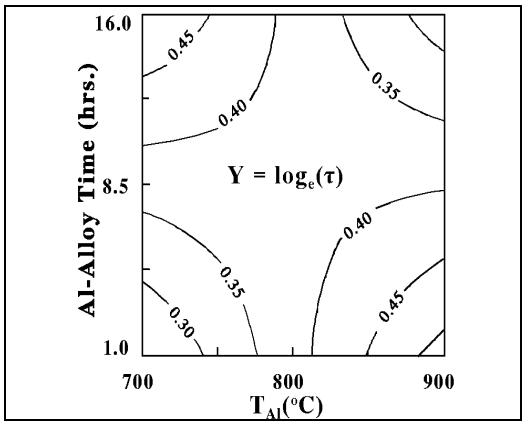

Figure 6.1. Contour plot representing the natural logarithm of PCD lifetime as a function of Al-alloying time and temperature. The 95% confidence limits span adjacent contour lines.

We examined, in preliminary experiments, the combined effects of phosphorus gettering and aluminum alloying in two multicrystalline silicon materials. Lateral nonuniformities have been shown to be significant. Such nonuniformities must be accounted for to fully understand the beneficial effects of these processes. This is especially important in materials where the grain structure is larger than the area probed by analytical techniques, but is still less than the cell size.

Low-Temperature Emitter-Passivation

Passivation of the emitter surface with a thin high-quality thermally grown oxide layer had been shown to dramatically increase the blue response of cells with a relatively light emitter diffusion. A more lightly diffused emitter region generally has longer diffusion lengths, which, together with a well-passivated surface, results in increased collection of carriers generated in the emitter by short-wavelength photons.

Sandia National Laboratories worked with Texas Instruments to develop a process that provides much of the performance improvement possible from a high-quality, high-temperature emitter passivation while remaining within the temperature and chemical constraints imposed by having the aluminum foil present during the processing. These constraints restricted our investigation to processes that require temperatures of 400°C or less and which avoid chemical treatments that would damage the aluminum foil. Our investigation focused on the low-cost approach of atmospheric- pressure chemical-vapor deposition (APCVD) of SiO_2.

Three different surface conditions were compared in this study. The first was that of a bare-Si surface after an HF etch and water rinse, similar to that of TI's Spheral cells before antireflection coating. The second was a surface that received the CVD-oxide layer. The third was a surface that underwent a high-temperature dry thermal oxidation at 950°C. A 2.6-fold reduction in the emitter recombination rate was obtained after the CVD oxide was applied to the bare Si surface. However, this represented only part of the benefit attainable by the use of a high-quality thermal oxidation.

We developed a process that provides much of the performance improvement possible from a high-quality emitter passivation while maintaining cell temperatures at or below 400°C. Using atmospheric-pressure chemical-vapor deposition (CVD) of SiO_2 at 400°C followed by a 400ºC forming gas anneal, we were able to produce a 3.1-fold increase in the blue response of cells compared to that of unpassivated cells. This resulted in an 11% increase in AM1.5G short-circuit current due to the passivating qualities of the CVD oxide.

This technique represents a low-cost approach to boost the performance of cells that do not presently employ passivating oxides. It would be of particular value to any silicon cell process in which material or other constraints preclude the use of a high-temperature thermal oxidation for the purpose of emitter passivation. This also applies to cells using material whose bulk lifetime is reduced by multiple high-temperature thermal excursions.

The Effects of Concentrated Ultraviolet Light on High-Efficiency Cells

The importance of stability in the performance of solar cells is clearly recognized as fundamental. Some of the highest efficiency silicon solar cells demonstrated at that time, such as the Point Contact solar cell and the Passivated Emitter solar cell, relied upon the passivation of cell surfaces in order to minimize recombination. It had recently been shown that exposure to ultraviolet (UV) light of wavelengths present in the terrestrial solar spectrum can damage a passivating silicon-oxide interface and increase recombination.

In this study, we compared the performance of Point Contact and Passivated Emitter solar cells after exposure to UV light. We also examined the effect of UV exposure on oxide-passivated silicon wafers. We found that Passivated Emitter designs are stable at both one-sun and under concentrated sunlight. The evolution of Point Contact concentrator cells showed a clear trend towards stability.

Chapter 7. CELL ANALYSIS AND PROCESS INTEGRATION

By the mid-1990s, the Si cell research project at Sandia had advanced to the point where individual fabrication processes had been optimized. Each process step then was integrated into complete fabrication sequences, which were tailored for high-performance, yet manufacturable cell designs. Sophisticated cell modeling and measurement tools were used to both design cells and determine performance-limiting mechanisms.

Simplified Processing for 23%-Efficient Si Concentrator Solar Cells

Concentrator cells were still seen as a cost-effective approach for PV-generated electricity. Several research groups had already fabricated different types of silicon concentrator cells with conversion efficiencies greater than 22%. These included the front and back Point Contact cells and several variations of the Passivated Emitter Solar Cells (PESC). All of these designs required multiple dopant diffusions and up to eight high-temperature furnace steps. The complexity of cell processing, especially the requirement for up to six photomask levels, made it difficult to reduce processing costs. The large number of high-temperature steps precludes the use of lower cost Cz silicon, which is easily degraded by repeated high-temperature cycling. Therefore, the use of more expensive FZ silicon had always been required to date.

In an attempt to increase cost-effectiveness, we developed a simplified processing schedule that retained most of the benefit available from high-performance cell designs while holding down processing costs. We began with a Passivated Emitter Cell design and developed a 3-photomask process that required only a single furnace step above 800°C. In comparison, the Passivated Emitter and Rear Locally diffused (PERL) cell developed by the University of New South Wales (UNSW) used eight furnace steps above 800°C and six photomask levels. While the PERL cell has achieved an efficiency of 24.8% using FZ Si at about 20 suns with the use of prism covers, the Sandia

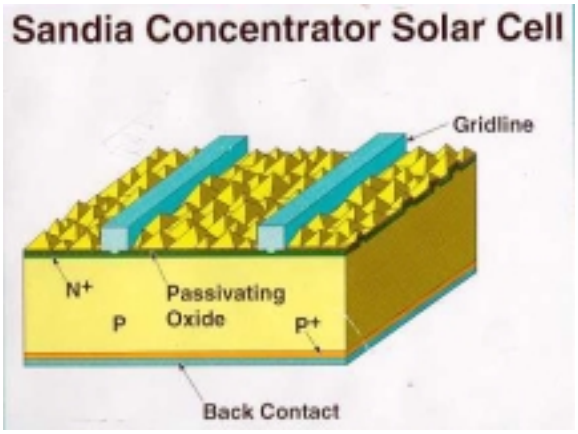

Figure 7.1. Structure of the Sandia Concentrator Solar Cell

concentrator cell process has achieved an efficiency of 22.6% on FZ Si at a concentration of 40 suns without prism covers. What is perhaps more significant is that this process resulted in an efficiency of 20.0% at 40 suns on solar-grade Cz silicon that was grown by Siemens Solar Industries. (23rd IEEE PVSC, Louisville, 1993. pp. 172-177.)

One unique feature of the Sandia concentrator cell process is the in-situ oxidation that is performed during the emitter diffusion and drive-in. This 900°C furnace step consists first of a 10-minute deposition of P_2O_5 that results from the reaction of $POCl_3$ and O_2 at the Si surface. This P_2O_5 layer reacts with the Si to form phosphosilicate glass (P-glass), which provides the source of P for diffusion into the Si. For the next 1.25 minutes, the wafers are allowed to soak in N_2 to allow a fixed amount of P to diffuse into the Si. This soak time can be varied to allow a wide range of emitter sheet resistances to be obtained.

Then, the furnace ambient is switched to 100% O_2 for 200 minutes. This grows a passivating oxide under the P-glass and provides a 110 nm total thickness that allows the diffusion oxide also to serve as the antireflection coating. This passivating oxide layer grows under the P-glass layer faster than phosphorus can diffuse through it, thereby abruptly cutting off the source of phosphorus diffusing into the Si. As a result, the concentration of phosphorus atoms at the Si surface slowly decreases during the oxidation due to finite source diffusion, just as it would if the P-glass layer had been etched away during a normal two-step diffusion and drive-in. This fact, in combination with the high-quality dry oxide growth, allows the surface to be extremely well passivated.

By experimenting with the fabrication process, we were able to improve cell performance at the cost of some added complexity. By moving the Al-evaporation and alloy steps to occur after the phosphorus diffusion, and by performing the alloy at 900°C to simulate the same Al drive-in conditions, the best cell performance was increased to an efficiency of 22.6% at 40 suns. This cell maintains an efficiency of 22.3% up to a concentration of 100 suns.

The reason for the performance improvement of cells made using the modified process becomes apparent after examination of the base diffusion lengths. Performing the Al-alloy after the phosphorus diffusion resulted in a statistically significant increase in the electron diffusion length in the base, because of the improved gettering of the combined phosphorus-diffusion, aluminum-alloying that we had optimized earlier.

A Simple Single-Photomask Process for Fabrication of High-Efficiency mc-Si Cells

In about 1993, we began to turn our attention toward low-cost one-sun cells that used even simpler processing and lower cost mc-Si materials. In so doing, our goal was to use a clear understanding of device behavior to remove performance-limiting features through clever processing.

We developed a simplified process sequence for fabrication of high-efficiency multicrystalline-silicon (mc-Si) solar cells. Photolithography is required only to define the evaporated metal gridlines. We used this fast turn-around, high-yield baseline process to evaluate different mc-Si materials and new processing procedures. The process uses a one-step emitter diffusion/drive-in and an aluminum-alloyed back surface field to provide a well-passivated cell with excellent blue and red response. Laser-scribed cell-isolation grooves are used to define both moderate-area (4, 4.6, or 10.5 cm^2) and large-area (42 cm^2) cells. We have observed minority-carrier diffusion lengths of around 300 μm in 1.4-Ωcm mc-Si material and have achieved efficiencies of 16.8% in 4.6-cm^2 cells. Large-area cell efficiencies in the same material have reached 16.4%.

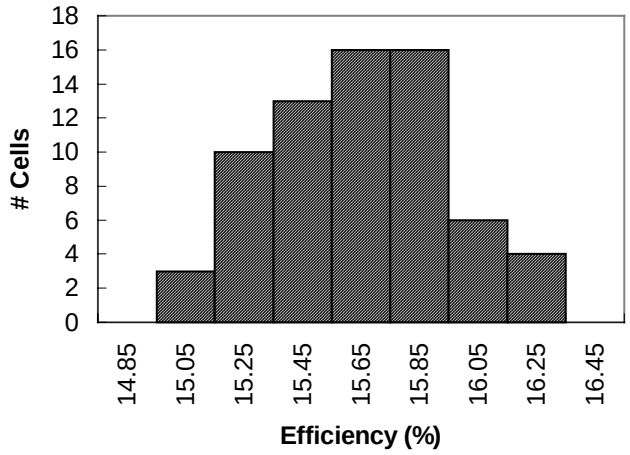

Figure 7.2. Efficiency distribution for the 68 cells produced in six processing lots.

The efficiency bin for each bar is +/-0.1% absolute. The best cells were used in prototype modules, which **demonstrated 15% module efficiency in 1994. This record efficiency for mc-Si modules still stands today**.

We demonstrated that the single-photomask process developed in the PDFL is capable of producing high-efficiency cells on mc-Si material. As applied to large-area cells in particular, the process has proven to be very robust. The relatively simple process facilitated PDFL collaborations with commercial material and cell producers. It became particularly useful in the evaluation of substrate materials and novel processes.

The World's First 15%-Efficient mc-Si Modules

The mc-Si modules produced and evaluated at Sandia established a new performance standard for commercial multicrystalline silicon. They demonstrated that the quality of industrial mc-Si wafers was not the limiting factor in module performance. Progress is continuing to be made in industry to improve the material quality while lowering the cost

per wafer. The challenge is to realize the material's potential with lower-cost commercial cell processes. Gettering effects from the emitter and back surface processing can be achieved with little change to current commercial processes. The cell metallization process appears to be the critical performance inhibitor since it is the primary difference between our cells and typical commercial cells. Buried-contact and/or all-plated metallization processes could bridge at least part of the gap between our cells and commercial mc-Si cells. Our emitter diffusion and aluminum alloy back-surface-field processes may also effectively eliminate the photon-induced changes observed when commercial cells are first exposed to sunlight.

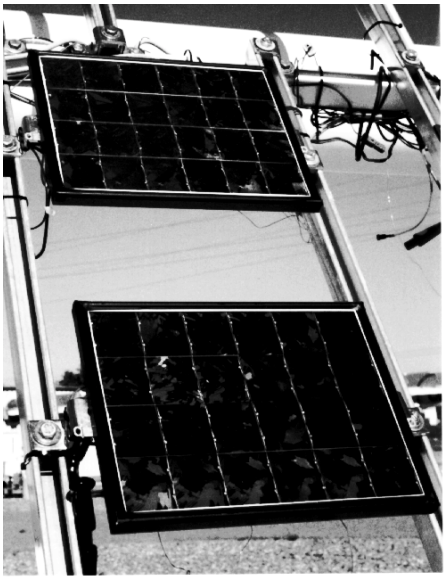

Figure 7.3. Sandia's mc-Si modules during outdoor performance evaluation at the Photovoltaic Systems Evaluation Laboratory

This accomplishment was the result of a team effort at Sandia to demonstrate the near-term performance potential for multicrystalline silicon modules using commercial mc-Si material and improved cell fabrication processes. Large-area high-performance mc-Si cells were fabricated, prototype modules were built, and world-record module efficiency was confirmed by outdoor testing at over 15% for standard test conditions.

The Emitter Wrap-Through Silicon Solar Cell

At around this time, efforts to circumvent some of the obstacles to improved cell performance at reduced cost were investigated through the use of novel cell designs and processes. This concept (Emitter Wrap Through -- EWT) wraps the emitter on the front surface through laser-drilled holes to interdigitated current-collection grids on the back

surface. The primary advantage of a back-contacted cell is elimination of the grid on the front surface, which increases cell performance through elimination of grid obscuration and reduction in series resistance. There are additional advantages for a back-contacted cell in terms of module performance, assembly, and aesthetics. Unlike other back-contact cell designs, the carrier-collection junction is on the front surface in the EWT cell; the front-surface emitter helps maintain a high internal collection efficiency in solar-grade silicon materials with modest diffusion lengths. The EWT cell can also easily include a carrier-collection junction on the back surface so that photogenerated carriers in the bulk are collected at both surfaces; such a "double-junction" cell is particularly appropriate for materials with diffusion lengths less than the device width (e.g., multicrystalline silicon solar cells). Our previous modeling calculations for an EWT solar cell with solar-grade silicon found that the double-junction structure is capable of increasing the cell efficiency by around 1% absolute compared to a front-junction cell. These calculations used conservative material parameters associated with solar-grade silicon, and also found that efficiencies of 18 and 21% are possible with multi- and monocrystalline 100-cm^2 EWT solar cells, respectively. A 36cm^2 EWT cell was demonstrated using buried-contact technology with an efficiency of 8.8%. (SAND93-1684C)

We developed a variation of our original EWT cell that uses a single n^+ diffusion and that can use screen-printed metallizations. We refer to this variation as the Screen-printed EWT cell (SEWT). Because the SEWT concept uses fabrication technologies that are already commonly used in commercial production, we believe the SEWT cell can be easily adapted for commercial production. The SEWT process is also simpler than the Buried Contact-EWT (BC-EWT) process, which should lead to a lower production cost. Solar-grade silicon should work well with the SEWT process because the SEWT cell uses only a single furnace step above 800°C. However, the process simplification of the SEWT cell is obtained at some reduction in potential performance (about 1% absolute) compared to the BC-EWT cell.

One of the most interesting features of the SEWT and BC-EWT cells is the double-junction structure that offers the possibility for enhanced collection efficiency from the bulk. Our calculations indicated that the double-junction structure can enhance the efficiency by nearly 1% absolute compared to a conventional front-junction cell; these calculations used material parameters appropriate for solar-grade silicon. The region over the n-type grid in the PhEWT cell has an n^+pn^+ structure (Figure 7.4), so that carrier collection from the p-type bulk can occur from both n^+ surfaces.

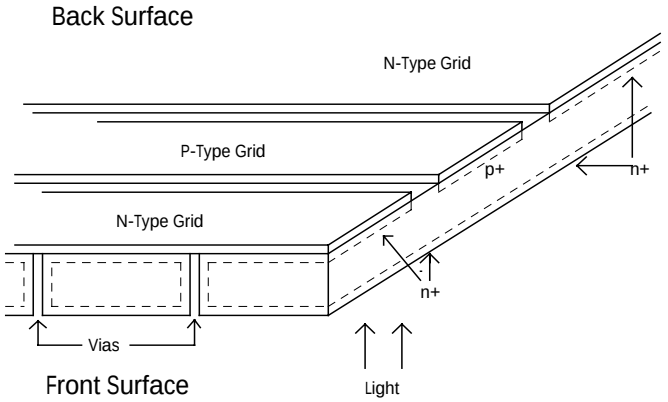

Figure 4. Schematic illustration of SEWT cell

The bottom surface is shown facing up in the diagram in order to illustrate the interdigitated grid on the back surface. Approximately 50% of the cell has an n+pn+ structure.

The Numerical Modeling of Solar Cells

A fundamental understanding of device behavior drove all of the improvements to solar cell design and performance attained during this period. This knowledge of device parameter interactions came from the highly accurate and user-friendly semiconductor device modeling program that could run on personal computers: PC-1D. This software, developed and refined by researchers at Sandia, was sought out and used by almost every Si cell research group in the world. It offered a convenient user interface with the ability to address complex issues associated with heavy doping, high-level injection, nonplanar structures, and transients. Quasi-one dimensional modeling allowed many 3D effects to be adequately addressed, while keeping the calculations simple enough to run on ubiquitous PC's, thereby increasing its usefulness. (IEEE Transactions on Electron Devices, ED-37 (2), February 1990, p. 337)

Using PC-1D, a powerful new method for identifying the performance-limiting mechanisms in silicon cells was developed and tested at Sandia. This method uses the internal quantum efficiency (IQE) of the device at both near-infrared and near-bandgap wavelengths. The conventional interpretation of IQE is expanded to accommodate textured surfaces and long diffusion lengths, and extended to near-bandgap wavelengths where internal optical effects play an important role. The information available from this extended analysis can be used to obtain a value for the internal optical reflectance of the back surface, and to separate the effects of diffusion length from back-surface recombination. Results from experimental tests verified the method. The information obtained can be used to compute recombination components for the cell, and to quantify the light-trapping effectiveness of the device.

The conventional interpretation of IQE data is obtained from a plot of IQE^{-1} versus α^{-1}, where the optical absorption coefficient, α, is a known function of wavelength. For planar cells of thickness W with a diffusion length, L, much shorter than the thickness, the plot is linear for absorption lengths (α^{-1}) greater than the junction depth but shorter than the device thickness. The inverse of this slope is equal to the minority-carrier diffusion length in the base region.

The analysis of IQE data can be extended to accommodate textured surfaces, long diffusion lengths, and weakly absorbed light. Only a few parameters are shown to be important, allowing data interpretation to be simplified significantly. To verify the method, we evaluated cells fabricated at Sandia under controlled conditions where only one cell parameter at a time was varied. Plots of inverse-IQE versus absorption length for the wavelength range 800 nm to 1120 nm have consistently displayed two linear regimes for textured high-performance silicon cells fabricated at Sandia, as illustrated in Figure 7.5.

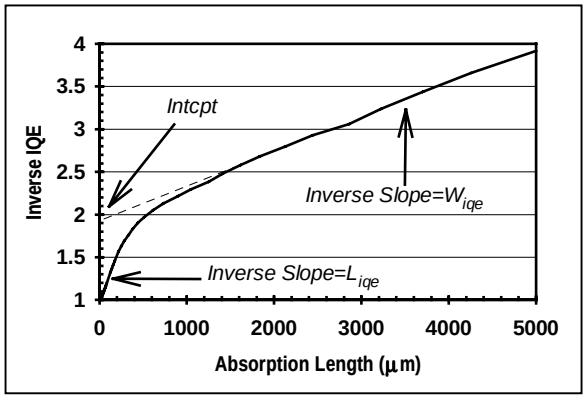

Figure 7.5. Typical Inverse-IQE data showing two linear regimes

The first linear regime occurs at near-infrared wavelengths. This is the data conventionally used to interpret IQE. But, for a textured cell such as this one, the inverse slope, L_{iqe}, cannot be directly equated to the diffusion length. The second linear regime occurs at near-bandgap wavelengths. The existence of the second linear regime was first predicted using the computer program PC-1D. The inverse slope of this region, W_{iqe}, and the extrapolated intercept of this line with the axis, Intcpt, form the basis for an "extended IQE analysis."

Analysis of internal quantum efficiency data has been extended for near-infrared wavelengths to accommodate textured cells and long diffusion lengths. The slope of the inverse IQE plot in this wavelength range gives the effective diffusion length needed to calculate the base component of the saturation current density to within about 5%. If the total saturation current density is known from dark I-V or Isc-Voc data, one can assess the relative importance of the base versus the emitter in determining the cell's voltage.

The additional information available from near-bandgap wavelengths permits the determination of the internal back-surface reflectance and the carrier collection efficiency for uniform photogeneration, to within about 5%. By combining the effective diffusion length from the near-infrared wavelengths with the collection efficiency from the near-bandgap wavelengths, it is possible to identify whether the dominant recomination mechanism in the base region of the cell is in the bulk or at the back surface.

Our experience at Sandia indicates that the extended-IQE analysis described here is the most reliable method yet devised for identifying the performance-limiting mechanisms in silicon solar cells, especially those which combine long diffusion lengths and light trapping. Most importantly, IQE analysis is performed nondestructively, on finished cells, using data that directly reflects the cell's performance.

Reflectance Control for Multicrystalline-Silicon Photovoltaic Modules Using Textured-Dielectric Coatings

We developed a new approach for controlling the reflectance of photovoltaic modules with planar-surface solar cells. The new approach used an optically thick, dielectric coating with a large refractive index and a textured surface; this dielectric coating is deposited on the planar-surface solar cell. The textured-dielectric coating (TDC) works optically with the module encapsulation to promote optical confinement of rays inside the module encapsulation structure, which reduces the net reflectance of the photovoltaic module. The advantage of our approach is that deposition of a textured-dielectric film may be less costly and less intrusive on the cell manufacturing process than texturing multicrystalline-silicon substrates. We presented detailed optical models and experimental confirmation of our new approach. (SAND94-1570C)

The TDC on the silicon cell randomizes the direction of reflected rays inside the encapsulant (glass) and inside the high-refractive-index dielectric film. The random direction of the rays creates “optical confinement” (also known as “light trapping”) in the module encapsulation and textured dielectric. We developed an optical model of a crystalline-silicon module and applied the model to three types of crystalline-silicon modules: (1) a textured silicon cell with a single-layer antireflective (SLAR) coating; (2) a planar silicon cell with a textured-dielectric coating; and (3) a planar silicon cell with a SLAR coating.

The TDC is very effective in both reducing reflectance losses and in increasing optical absorption through optical confinement in the module. The active-area solar-weighted reflectance is reduced by over a factor of two compared to the planar cell with SLAR coating, which is the present standard commercial product. In addition, the short-circuit current densities of the textured-dielectric and textured-silicon modules are very similar.

Textured-dielectric coatings have several practical advantages compared to other approaches for controlling reflectance in mc-Si modules. Suitable materials for the TDC include ZnO, TiO_2, and SnO_2. These materials have large refractive indices and have

been deposited with textured surface and with low-cost technologies. The TDC introduces no complications in the cell process if the coating is applied after the grid metallization. In contrast, mechanical texturing produces surfaces with large texture dimensions that can significantly complicate the cell fabrication process. In addition, a TDC deposited over the grids should reduce grid obscuration losses by recovering reflected light from the gridlines through optical confinement. This new method for reducing the reflectance and improving the optical absorptance of photovoltaic modules has potential cost and performance advantages over other approaches for texturing mc-Si solar cells.

The Effect of PECVD Deposition Parameters on Surface and Bulk Recombination in Silicon Solar Cells

The use of Plasma-Enhanced Chemical Vapor Deposition (PECVD) as a low-temperature surface passivation technique for silicon solar cells had become a topic of increasing importance. PECVD was widely recognized as a potentially cost-effective, performance-enhancing technique that could provide surface passivation and produce an effective antireflection coating layer at the same time. For some solar-grade silicon materials, it had been observed that the PECVD process resulted in the improvement of bulk minority-carrier diffusion lengths as well, presumably due to bulk defect passivation.

While previous results showed that certain deposition and annealing conditions could be effective, no one had yet reported a systematic optimization of deposition and annealing parameters for solar-grade silicon materials. We therefore performed a statistically designed experiment using response surface methodology to predict the optimum deposition and anneal conditions, and then tested the prediction by fabricating solar cells on cast multicrystalline solar-grade silicon. (SAND94-1557C)

We began our investigation with a main-effects experimental design to determine which parameters had the most effect on emitter-surface recombination. In this way, we intended to reduce the large number of factors by identifying those with the most influence on cell performance. Then, a quadratic interaction experiment was done to find optimum combinations of parameters that minimize emitter recombination and optimize refractive index.

We initially carried out the depositions on high-lifetime float-zone (FZ) single-crystal wafers that had the same lightly diffused phosphorus emitters we use in our high-efficiency solar cells. We chose this as an experimental vehicle because we could measure emitter saturation-current density (J_{oe}) on these structures and calculate the front-surface recombination velocity without having to fabricate a large number of complete solar cells.

The results of the main-effects experiment in Figure 7.6 shows that the emitter surface passivation provided by either PECVD oxides or nitrides can range from almost as poor as a bare or TiO_2-covered silicon surface to almost as good as the best thermal-oxide-

passivated surface. Unpassivated TiO_2-covered cells are typical of those from the commercial Si-PV industry.

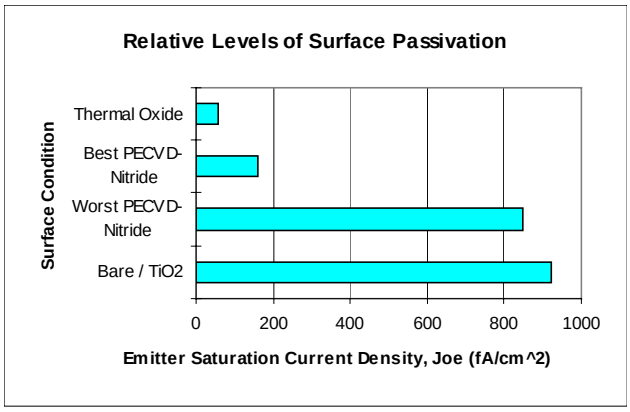

Figure 7.6. Range of J_{oe} values obtained in the nitride main-effects experiment, measured at 25ºC

We next performed the quadratic experiment and used a statistical analysis program to calculate the functional dependence of J_{oe} on the four factors varied.

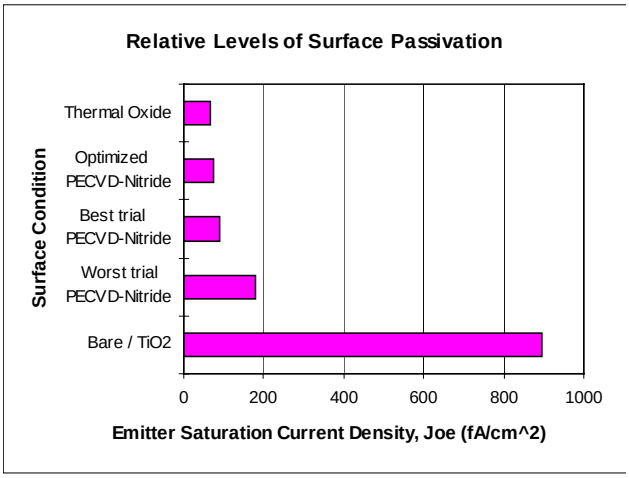

Figure 7.7. The measured and predicted Joe values for the nitride quadratic experiment.

The analysis predicted that the optimized nitride conditions should produce a film with surface passivation properties almost as good as that of our best thermal oxides, while at the same time producing optimal ARC properties. We tested this prediction by fabricating solar cells on float-zone wafers and also on cast mc-Si wafers provided by Solarex Corp. Figure 7.8 shows measured internal quantum efficiency curves for the

same surface conditions of Figure 7.7, where the optimized curve here represents measured IQE data on a cell fabricated using the predicted best deposition conditions.

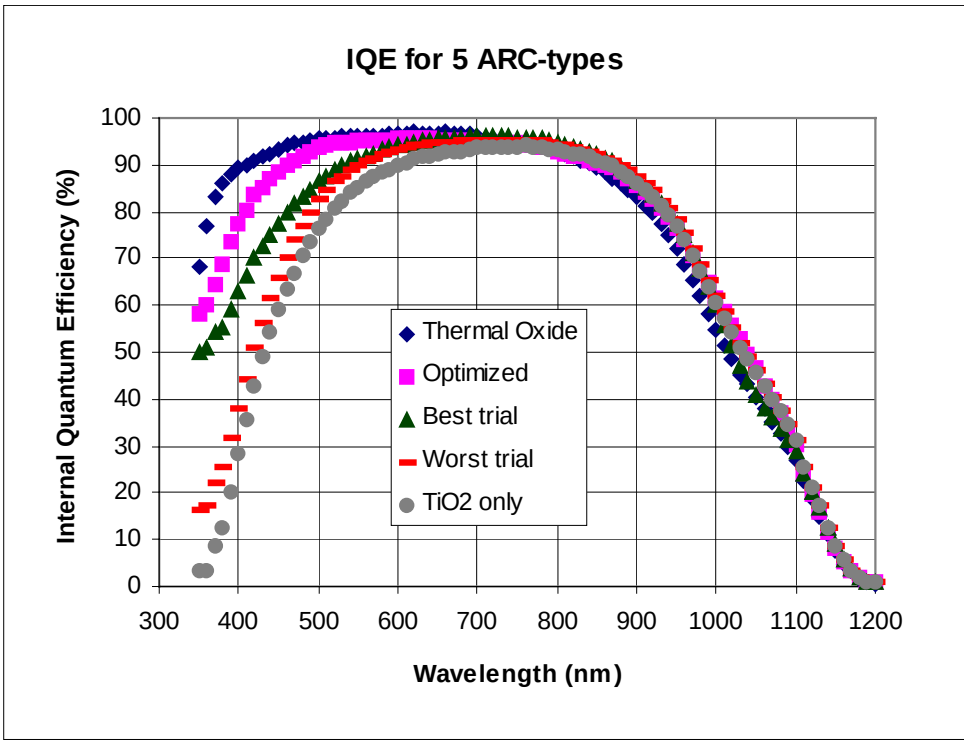

Figure 7.8. Measured IQE curves on mc-Si cells for the same five surface conditions shown in Figure 7.7

Figure 7.8 shows a continuous improvement in the blue response of nitride-passivated cells as the deposition conditions approach those of the optimized case. This is entirely consistent with the lower J_{oe} values measured earlier and proves that the predicted optimum conditions do indeed result in better-passivated emitters, even on mc-Si cells.

Finally, Figure 7.9 shows the measured short-circuit current densities of the mc-Si and float-zone Si cells fabricated using the same surface conditions as in Figure 7.7.

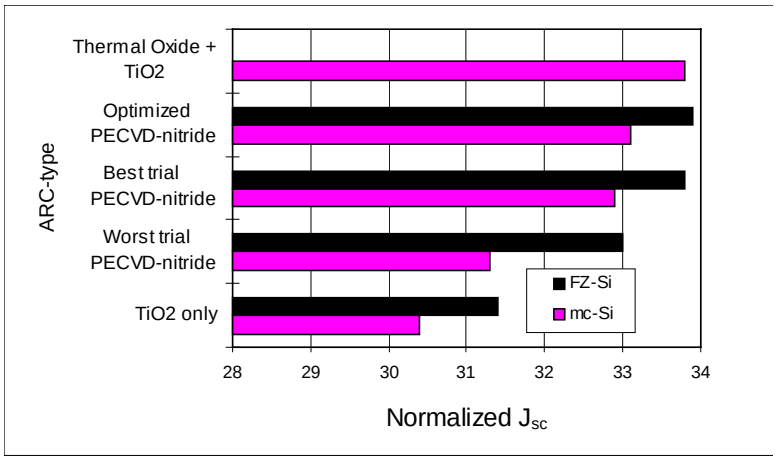

Figure 7.9. Measured short-circuit current densities, normalized to the same reflectance, for the surface conditions of Figures 7.7 and 7.8, for mc-Si and FZ-Si cells

Our goal was to define a process to optimize cell performance by minimizing recombination while also providing an effective antireflection coating. Our initial results showed that excellent emitter-surface passivation, approaching that of the best thermally grown oxides, could be obtained using a single-layer nitride coating whose refractive index was also optimized for antireflection purposes. Use of the PECVD-nitride instead of a TiO_2 ARC resulted in an 11% increase in output power.

Chapter 8. ADVANCED CELL CONCEPTS

By the mid to late 1990s, the Si cell research team had begun to work on advanced cell concepts whose purpose was to address the limitations that were holding back cell performance while maintaining simple cell processing to allow manufacturing at reasonable cost. One of the areas addressed built on the previous achievements attained in the passivation of bulk and surface defects by plasma-hydrogenation.

The Effect of Hydrogen-Plasma and PECVD-Nitride Deposition on Bulk and Surface Passivation in String-Ribbon Silicon Solar Cells

A low-cost method of cell processing which simultaneously improves material quality and provides an antireflection coating (ARC) is highly desirable. The use of Plasma-Enhanced Chemical Vapor Deposition (PECVD) as a low-temperature passivation process for silicon solar cells is of interest for this purpose. Other work has shown that different multicrystalline materials respond differently to hydrogen plasma passivation. We conducted work to study how to best use PECVD techniques to improve the performance of cells made using String Ribbon™ silicon from Evergreen Solar, a promising low-cost material.

Our process can include an in-situ hydrogen or ammonia rf-plasma treatment prior to a PECVD-nitride deposition to promote bulk defect passivation independently of surface effects. We also studied whether the predeposition of a thin silicon-nitride protective layer before performing the plasma treatment would serve to minimize surface damage. Our goal was to define a process to optimize cell performance by minimizing both surface and bulk recombination while also providing an effective antireflection coating.

We used five different deposition strategies and compared the resulting cell performance with that of cells processed using the industry-standard TiO_2 ARC: (1) 70-nm nitride layer with no pretreatments, (2) H_2-plasma pretreatment followed by a 70-nm nitride layer, (3) 20-nm nitride protective layer, followed by H_2-plasma, followed by 50 nm of nitride, (4) NH_3-plasma pretreatment followed by a 70-nm nitride layer, (5) 20-nm nitride protective layer, followed by NH_3-plasma, followed by 50 nm of nitride.

Internal Quantum Efficiency (IQE) curves for cells processed using each of the five PECVD sequences are compared with that of a cell having an evaporated- TiO_2 ARC in Figure 8.1.

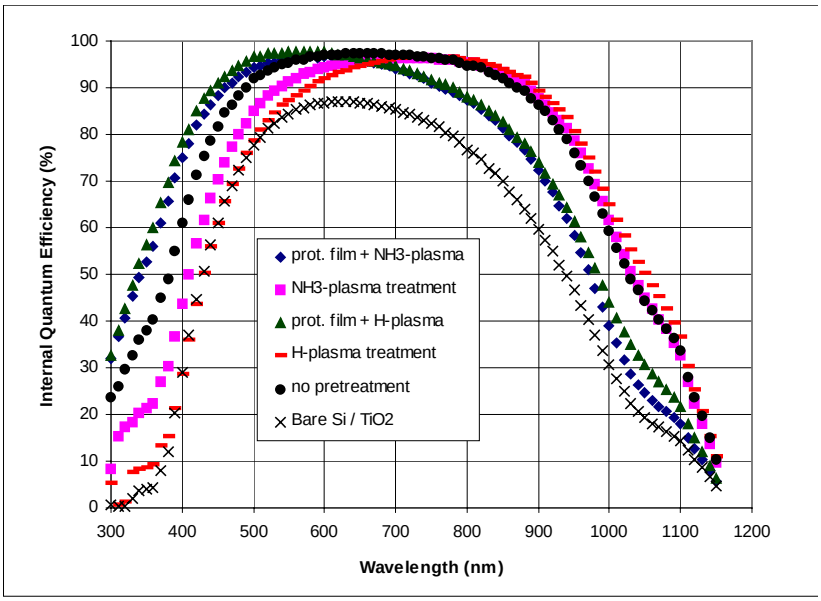

Figure 8.1. Internal Quantum Efficiency for each of the five PECVD sequences and the evaporated-TiO_2 ARC

The short-wavelength region of the IQE curves is sensitive to the degree of emitter-surface passivation and the amount of recombination within the emitter region. All the cells used in this study had identical, low-recombination emitters, so that most of the emitter-recombination occurs at the emitter surface. Well-passivated emitters have higher blue response. Figure 8.2 shows the IQE at 400 nm more clearly.

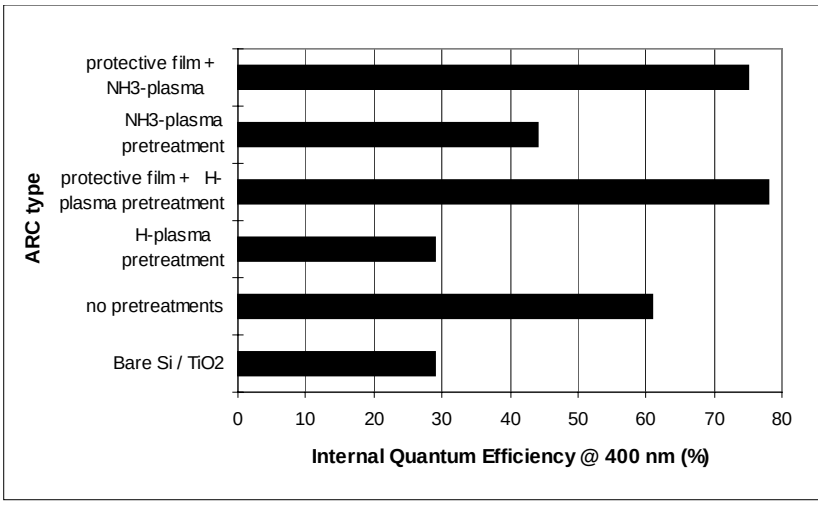

Figure 8.2. Internal Quantum Efficiency at 400 nm for each of the ARC types

The direct deposition of the PECVD-nitride without pretreatments resulted in a substantial improvement in short-wavelength response over that of the TiO_2-covered emitter, consistent with our previous work. Also consistent with that work is the indication that a hydrogen plasma pretreatment prior to the nitride deposition results in poorly passivated surfaces, presumably due to surface damage, which are no better than an unpassivated, TiO_2-covered surface. The ammonia-plasma pretreatment prior to the nitride deposition does result in some improvement of the surface, but not as much as the direct deposition. This suggests that the amount of surface damage caused by the ammonia plasma may be less than that caused by the hydrogen plasma.

When the hydrogen or ammonia plasma treatments are performed after a 20-nm protective nitride layer has been deposited, significant additional surface passivation is achieved. In fact, the 78% IQE value obtained for the H_2-plasma with the protective film is equal to the highest value that we have been able to obtain using PECVD coatings. This is certainly an indication that the protective nitride film does an excellent job of protecting the silicon surface from the damaging effects of the plasma pretreatments. This may also indicate that the presence of a thin, protective nitride film before the plasma pretreatment causes the passivating hydrogen ions to accumulate in the nitride near the silicon interface, where they are most beneficial in tying up dangling bonds and passivating interface states.

The long wavelength portion of the IQE curves is sensitive to the bulk diffusion length and the amount of back surface recombination. Since all the cells fabricated in this study used the same Al-alloyed back surface structure, differences in the long wavelength IQE curves are due to differences in bulk defect passivation. The bulk diffusion lengths were calculated using the Sandia extended IQE analysis method and are plotted together in Figure 8.3.

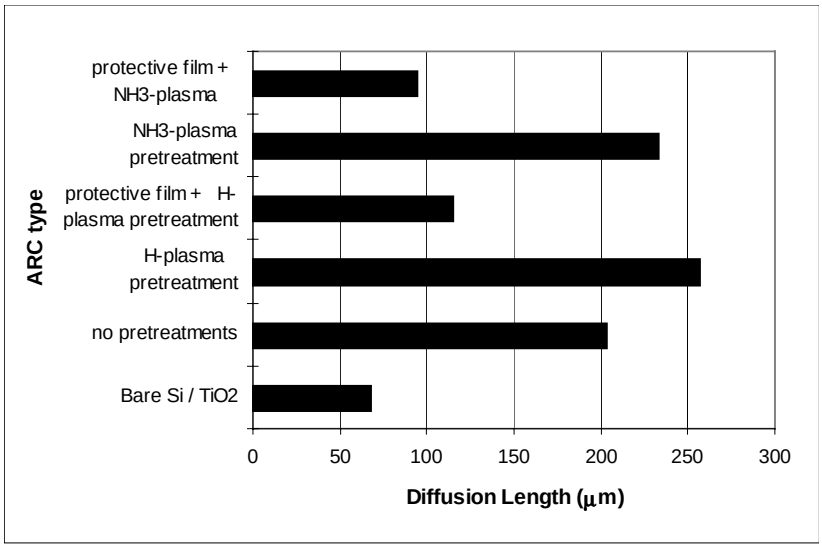

Figure 8.3. Bulk minority carrier diffusion length vs. ARC type

Here again we see that the direct deposition of the nitride without pretreatments results in a significant improvement, this time in diffusion length, over that of the TiO_2-coated control cells. However, it is evident that additional improvements are obtained by first pretreating the wafers with either an ammonia or hydrogen plasma before the nitride deposition. The diffusion length of over 250 μm obtained with the hydrogen-plasma pretreatment is as high a value as has ever been obtained on this material.

Interestingly, there is only a marginal improvement in the diffusion length over that of the control cells when the protective nitride film is deposited on the cells before a pretreatment in either the ammonia or the hydrogen plasmas. This suggests that either the film was too thick or the duration of the pretreatments too short to allow the passivating agents, presumably hydrogen ions, to diffuse in sufficient numbers through the films to penetrate the bulk of the wafers.

The overall cell performance is dependent on both surface and bulk recombination. For this reason, even though the cells fabricated with no pretreatments had only intermediate levels of surface and bulk passivation, their performance overall was superior to those that used more complex treatments and were considerably inferior in one area or the other. This is significant for the commercialization of String Ribbon and other multicrystalline Si cells and modules, where the simplest and most cost-effective method to improve the product performance is preferred. The parameters for the best cell at 25°C were Voc = 600 mV, Jsc = 31.1 mA/cm^2, FF = 0.78, and efficiency = 14.5%.

We found that for the limited set of deposition conditions investigated until then, the direct deposition of PECVD-nitride produced the best cells on String Ribbon silicon wafers at that time, with efficiencies up to 14.5%. Hydrogen and ammonia plasma pretreatments without a protective nitride layer resulted in better bulk passivation, but damaged surfaces. Pretreatments after deposition of the protective layer produced the best surface passivation, but were not effective in passivating the bulk. Further work was needed to optimize protective film thickness, pretreatment durations, and plasma pretreatment and deposition parameters to simultaneously obtain both the best surface and bulk passivation for optimum cell performance. (SAND95-2481C)

The Self-Aligned, Selective-Emitter Silicon Solar Cell

The use of PECVD silicon-nitride as a low-temperature surface passivation technique for silicon solar cells became widely recognized as a method for providing surface passivation and an effective ARC at the same time. In order to gain the full benefit from improved emitter surface passivation, it is necessary to tailor the emitter doping profile so that the emitter is lightly doped between the gridlines, but heavily doped under them. This is especially true for screen-printed gridlines, which require very heavy doping beneath them for acceptably low contact resistance.

This selectively patterned emitter doping profile had historically been obtained by using expensive photolithographic or screen-printed alignment techniques and multiple high-

temperature diffusion steps. The purpose of our work was to improve the performance of standard commercial screen-printed solar cells by incorporating high-efficiency design features without incurring a disproportionate increase in process complexity or cost. Our approach used plasma processing to replace the heavily doped homogenous emitter and non-passivating ARC with a high-performance selectively patterned diffusion covered with a passivating ARC.

The self-aligned, selective-emitter (SASE) process is outlined in Figure 8.4. Cells using Solarex cast multicrystalline silicon received standard production line processing at Solarex through the printing and firing of the gridlines. Then, the cells were sent to Sandia for reactive ion etching (RIE) to etch back the emitters between the gridlines.

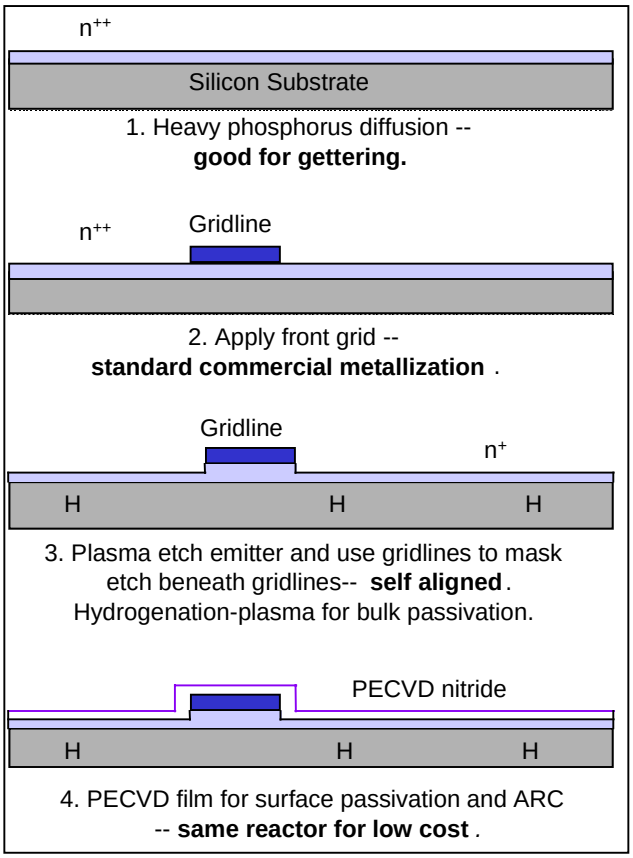

Figure 8.4. Process sequence for self-aligned, selective-emitter etchback. The emitter etchback can be performed after the hydrogenation treatment to remove surface damage.

The first experiment was a main-effects analysis that compared 1-step and 3-step depositions using six groups of full-size 130-cm^2 Solarex cells. Cells that used the 3-step deposition technique incorporating a hydrogenation step show the greatest gains in performance. These cells show efficiency gains of up to 0.2% absolute over the controls,

and 0.5% over the 1-step cells. The greatest increase in blue response is seen in the cells with the thinner protective layer, which show an IQE(400 nm) of 80%, the highest we have observed on mc-Si cells using SiN emitter passivation, with or without emitter etchback. This confirms the negligible effect of RIE surface damage on cell performance. The IQE of these cells are shown in Figure 8.5.

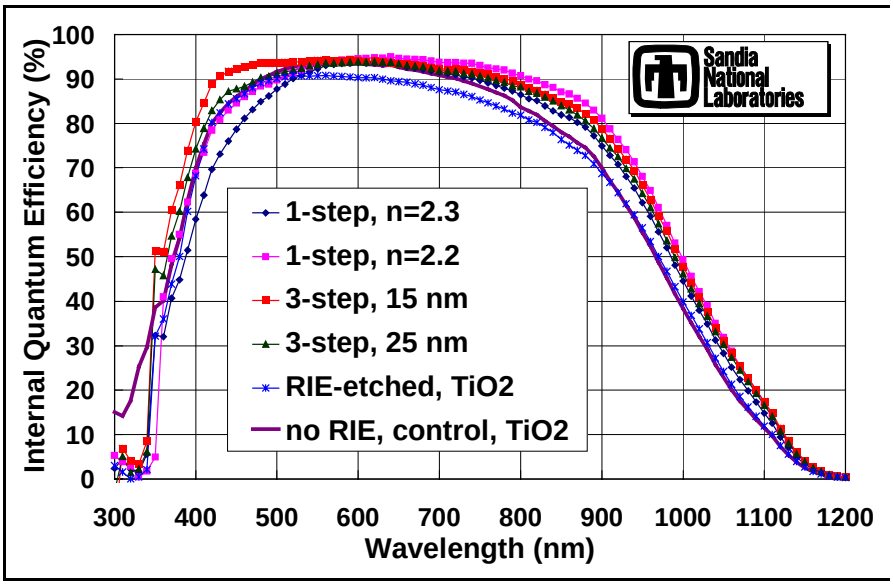

Figure 8.5. IQE curves of Solarex cells from 6 experimental groups.

The long-wavelength response of all the nitride-coated cells are consistently higher than that of the TiO_2-coated cells, presumably due to reduced bulk recombination from the plasma-nitride and hydrogenation treatments. Inverse-IQE analysis indicates that electron diffusion lengths in the bulk of the SiN cells are typically around 130 μm, while those in cells from the TiO_2-coated cells are 90 to 100 μm. This explains the somewhat higher V_{OC} values for the 3-step cells.

Because the previous results showed that the in-situ ammonia-plasma treatment in the 3-step nitride deposition process produced cells with the highest efficiency, we decided to investigate which parameters of the 3-step process would optimize cell performance. Using response surface methodology, we used a quadratic experimental design in a statistical multiparameter experiment to find the optimum parameter set. We studied the effect of 3 factors: the thickness of the silicon-nitride protective layer, and the duration and power of the plasma treatment.

The 1-step SASE cell showed no discernible difference in performance from that of the control cells. However, as predicted by the statistical model, the optimized 3-step cells have an average efficiency of 12.8%, which is half an absolute percentage point greater

than that of the control cells. The 3-step SASE cells show a slight improvement in J_{SC} as well as V_{OC} compared to the controls.

This investigation showed that the use of the SASE process in production-line fabrication of screen-printed solar cells results in improvement of half an absolute efficiency point over standard ARC controls. This has been done using a single, industrial emitter-diffusion process and no alignments. This process results in a well-passivated emitter surface, and a less heavily doped emitter between gridlines for reduced emitter recombination. It allows for heavier doping beneath the gridlines for lower contact resistance, reduced contact recombination, and better bulk defect gettering. (SAND97-2462C)

Our previous work showed that we were able to obtain better surface passivation using a 3-step nitride deposition process compared to a single continuous deposition. The 3-step process starts with deposition of a thin layer of nitride to protect the Si surface, followed by exposure to a NH_3-plasma, and finally the deposition of the remaining nitride required to attain the correct thickness for ARC purposes. We conducted a statistically designed multifactor experiment to find the 3-step parameters that would maximize surface passivation using our previous response surface methodology. We investigated whether shorter NH_3-treatments would retain the benefits of surface passivation.

The cells that received 10 minutes of NH_3-hydrogenation performed the best, exceeding the controls by almost a full percentage point due to the large improvement in V_{OC}. However, improvement in V_{OC} is reduced for the cells that received a 20-minute NH_3-exposure. These cells also suffered a loss in fill factor due to an increase in diode ideality factor. The use of an optimum-duration, NH_3-plasma hydrogenation treatment was found to be crucial to the increased performance. As the data in Figure 8.6 show, the fill factor and open-circuit voltage increase for durations up to 10 minutes, and then decrease due to higher non-ideal diode recombination, probably due to accumulated plasma-induced surface and gridline damage. (SAND98-2762C)

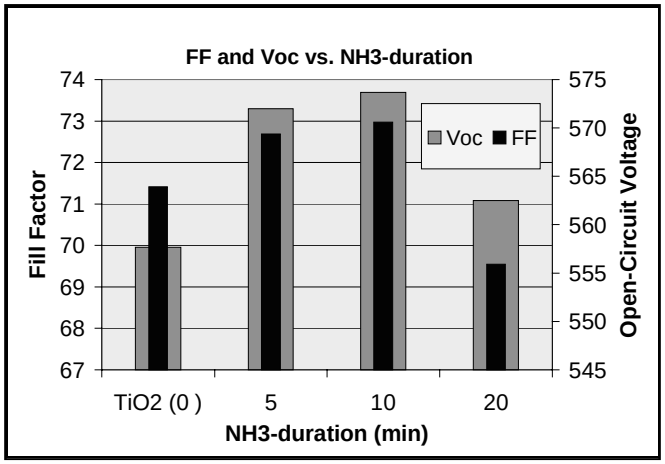

Figure 8.6. V_{OC} and FF peak at NH_3-plasma hydrogenation durations of 10 minutes

Plasma-Texturization for Multicrystalline Silicon Solar Cells

We realized that only a slight variation of the plasma etchback step previously developed was required to effectively texture mc-Si surfaces, and could significantly reduce front surface reflectance. The quality of lower cost multicrystalline-silicon (mc-Si) had increased to the point that its cell performance was close to that of single c-Si cells, with the major difference resulting from the inability to texture mc-Si affordably. This reduced the cost-per-watt advantage of mc-Si. A low-cost, large-area, random, maskless texturing scheme independent of crystal orientation is still expected to significantly impact the cost and performance of mc-Si photovoltaic technology.

Surface texturing for enhanced absorption in Si had been historically obtained by creating randomly distributed pyramids using anisotropic wet etchants, but this works well only on single-crystalline silicon because of its (100) crystallographic orientation. Various other forms of surface texturing have been applied to mc-Si in research, including laser-structuring, mechanical grinding, porous-Si etching, and photolithographically defined etching. However, these generally slow techniques may be too costly to ever be used in large-scale production.

We developed a maskless plasma texturing technique for mc-Si cells using Reactive Ion Etching (RIE) that results in much higher cell performance than that of standard untextured cells. Elimination of plasma damage was achieved while reducing front reflectance to extremely low levels. Internal quantum efficiencies higher than those on planar and wet-textured cells have been obtained, boosting cell currents and efficiencies by up to 11% on monocrystalline Si and 2.5% on multicrystalline Si cells. (SAND2000-2338C)

We developed several metal-catalyst assisted RIE-texturing techniques using SF_6/O_2 plasma chemistry. A large parameter space of power, pressure, gas ratio, flow rate, and etch time was investigated. A parameter range was found to be useful for texturing Si wafers up to 6" in diameter and mc-Si wafers of 130 cm^2. The textured surface exhibits a spectral reflectance between 1 and 5 % for wavelengths below 1 μm without the benefit of anti-reflection films as shown in Figure 8.7.

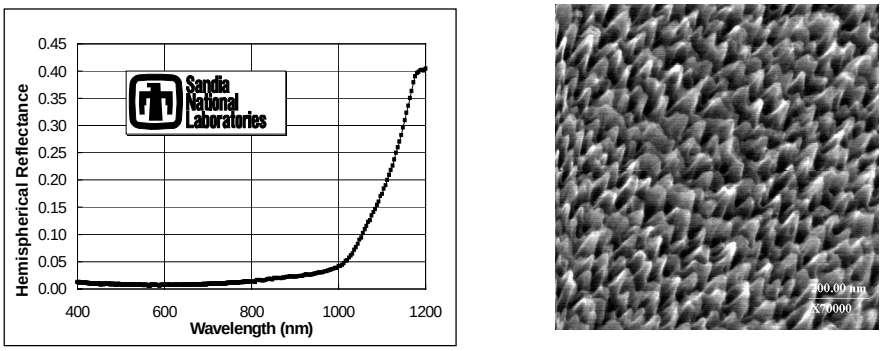

Figure 8.7. Spectral reflectance and SEM of a mc-Si wafer textured using a Cr-assisted RIE-texturing process

The challenge involved in incorporating the low-reflectance surfaces obtained from RIE-texturing into a complete solar cell has been to remove the plasma-induced contamination and surface damage without removing too much of the texture. Figure 8.8 shows results of the use of a damage removal etch (DRE) consisting of nitric/HF to remove this damaged region.

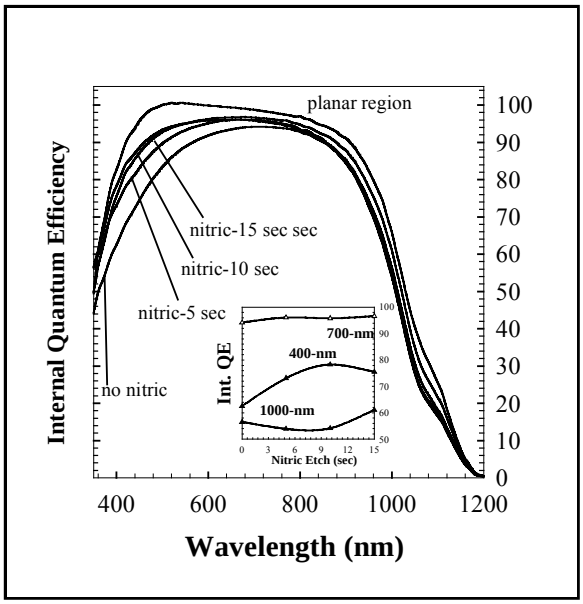

Figure 8.8. Recovery of textured cell IQE as a function of damage removal etch duration using nitric/HF

With the selection of the proper DRE and RIE-texture processes, we were able to fabricate cells on monocrystalline Si whose IQE was increased to levels as high as that of our best wet-textured cells with reflectances almost as low. Single-crystal wafers were used to compare the RIE-texturing process to both planar cells, which represent today's untextured mc-Si cells, and to high-efficiency wet-textured cells. The best RIE-textured cells had current densities of over 34.3 mA/cm^2 and efficiencies up to 16.5%, which far exceeded the 31 mA/cm^2 and 14.75% typical of the planar control cells. These results in fact slightly exceeded the average currents and efficiencies of our wet-textured single-crystal control cells.

Two promising RIE-texture processes were each applied to groups of 12 mc-Si wafers from BP Solarex, and compared with another 12 planar control wafers from the same ingot. Then all wafers were processed through the Solarex cell production line using standard industrial process schedules. The average efficiency of the cells with RIE texture increased 2.5% relative to the planar value due primarily to the higher cell currents. The textured cells show lower reflectance than the planar cell, but not as low as was obtained on mono-Si. This is because a longer-duration nitric/HF DRE was used on these cells to ensure complete damage removal, and this resulted in loss of some of the

texture. Work to optimize this process on various mc-Si materials from several US Si module manufacturers is ongoing, supported by an internal Sandia R&D program.

Record-Breaking Emitter Wrap-Through Solar Cells

Research continued to improve EWT cell performance. Back-contact solar cells have the potential to reduce module assembly costs and provide higher conversion efficiency. Such a device must be simple to fabricate on an industrial scale and be tolerant of low minority-carrier diffusion lengths. The EWT cell is a device design that can meet these goals. In this device, the diffused junction is present on both sides and is connected by laser-drilled holes through the silicon. EWT cells were frequently found to have poor fill factors due to shunt-like behavior. The holes were found to possess no defects that adversely affect device performance. However, detailed equivalent circuit modeling of the EWT cell was able to explain the shunt-like behavior. Experiments were performed to confirm the physical mechanisms described by the equivalent circuit model. Device optimization guided by the equivalent circuit model has led to the demonstration of a large area EWT cell with a fill factor of 77.6% and efficiency of 18.2%.

The EWT cell has often shown a soft-knee diode characteristic leading to poor fill-factor under illumination. The dark current-voltage curve perfectly fits a two-exponential model. However, the 2kT component is too small to explain the poor fill factor observed in the illuminated I-V curve. One effect that can explain this behavior is the existence of two different paths for collection of photogenerated current, with one path having a much larger series resistance. This is the case in the EWT cell with the two paths being either collection by the front or the rear junction. The effect is actually a manifestation of high series resistance for a portion of the photocurrent. The fill factor is determined by the width of the cell edge, as shown in Figure 8.9.

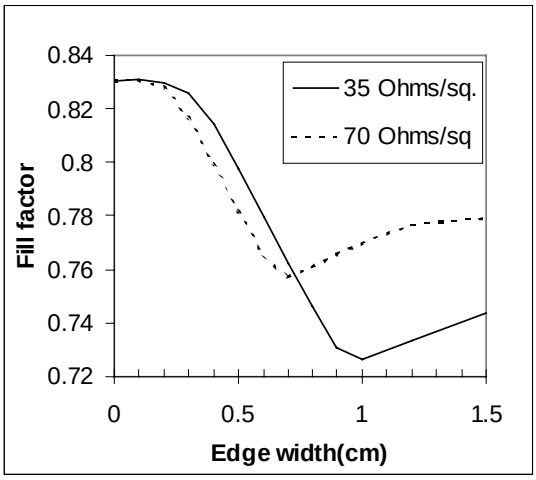

Figure 8.9. Fill factor of EWT cell calculated from model as a function of edge width for two values of emitter sheet resistance

As the edge area increases, an apparent shunt develops near the maximum-power point. Short-circuit current begins to decrease as the fill factor reaches a minimum.

Careful processing, optimized etching of the holes, and moderate passivation of the p-type surface has minimized extrinsic sources of shunt currents. The net result is that device performance is limited by the geometry of the EWT solar cell. These effects were well modeled by equivalent-circuit models. Optimization of the device geometry based on these equivalent-circuit models, and of the device processing, resulted in demonstration of a large-area back-contact EWT cell with a fill factor of 77.6% and efficiency of 18.2%.

Sandia has recently demonstrated an EWT cell using screen-printed contacts. A 41 cm^2 cell with 15.3 % efficiency under AM1.5G illumination was achieved. Several other cells had similar efficiencies. Screen-printed aluminum formed the p-contact and screen-printed silver was used for the n-contact. Emitter patterning was done by photo-lithography of a deposited mask oxide. Emitter line widths were quite large at 0.8 mm. This large line width holds open the possibility of alternative patterning techniques that can avoid photolithography.

The largest fill factor loss for this EWT cell is series resistance, contributing about 5.5% power loss, with non-ideal diode recombination contributing about 4.5 % power loss. Shunt conductance is the smallest contributor giving only a 1.5 % loss. Series resistance is approximately 0.9 Ohm-cm^2 and is dominated by contact resistance and the resistance of the holes. Recombination losses are dominated by bulk recombination in the base. The cell is approximately 280 mm thick, 41 cm^2 area, on 0.5 Ohm-cm c-Si. The emitter sheet resistance is 45 Ohm/square. Contact coverage on the back of the cell is 40 %. Fraction of p-type area on the back surface is 40 %. Quantum efficiency and reflectance data of the 15.3 % efficient cell are shown in Figure 8.10.

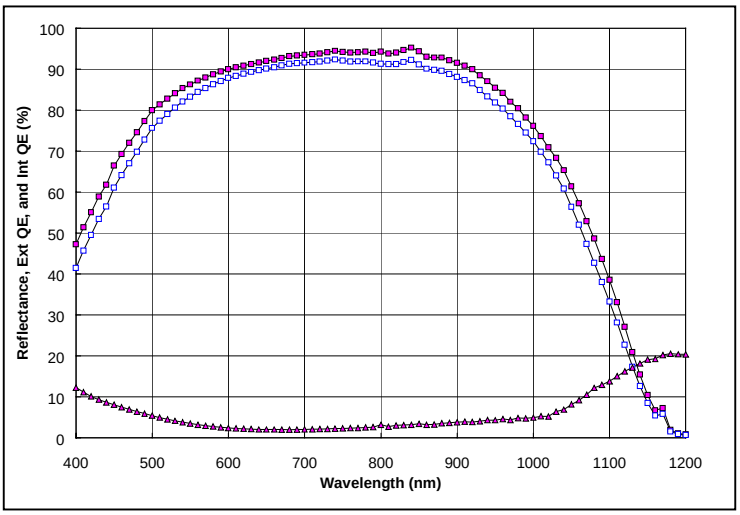

Figure 8.10. Internal, External Quantum efficiency and reflectance of 15.3 % efficient screen printed EWT solar cell

There are many opportunities to improve the EWT cell. A primary technical challenge for higher efficiency in the EWT cell is getting metal in the holes to minimize series resistance. Also, the cell would benefit from a selective emitter even more than a front contact cell due to the large junction area in the EWT. For processing lower quality materials, a gettering step is always helpful. All three of these features could be incorporated by the use of self-doping contacts.

Self-Doping Metal Contacts

The concept of a self-doping metallization allows formation of a junction or back surface field at the same time a contact metal is applied. The basic technique is to apply a carrier metal, including a dopant species, to the silicon. This would be followed by a high temperature growth cycle in which a doped layer is grown by liquid phase epitaxy, LPE. LPE is a crystal growth technique in which a solute is dissolved in a solvent. The solution is cooled, which allows the solute to grow out epitaxially on a substrate. The technique allows growth to proceed at temperatures lower than the crystal melting point. The temperature must be higher than the solute/solvent eutectic temperature. LPE has been used for silicon growth, resulting in high crystal quality.

The self-doping metal concept utilizes the same physical phenomenon as LPE. However, the carrier metal remains in place forming an ohmic contact to the grown silicon. The process steps also are analogous to the familiar screen printing process for forming contacts, in that metal is applied in a pattern and is followed by a firing step. However, the end result is very different. It is important for a screen printing fire step to be below the eutectic point of the metal-silicon system. For a self-doping metal, it is required that the firing, or growth step, occur above the eutectic temperature. The screen-printed contact requires a doped layer to be in place before contacts are applied, but the self-doping metallization forms its own doped layer.

The junction formed is therefore entirely covered by metal, i.e. the junction area equals the contact area. This, however, can be an asset in the right kind of cell structure. For example, a selective emitter on a front contacted cell could be formed from self-doping metals, which would be self-aligned. One device structure to which the self doping metal is ideally suited is the Interdigitated Back Contact (IBC) cell. This cell structure has a junction only on the back surface and interdigitated opposite polarity grid lines. This cell has demonstrated high efficiency both as a concentrator solar cell and a one-sun cell using photolithography, conventional diffused junctions, and evaporated metal contacts. Since the junction need not extend over the entire surface, it can be envisioned that a self-doping metal can form this junction.

Our approach has been to use a self-doping metal compound incorporating silicon. This raises the metal to silicon interface above the level of the remaining silicon wafer. A compound of Ag/Si/B has been used successfully for creating p on n diodes. Films were applied by sputtering. A brief period of back sputtering was used to assure good wetting.

Simple diode structures fabricated to date have shown an adequately low shunt conductance. A plot of the dark current-voltage characteristic of one of these diodes is shown in Figure 8.11.

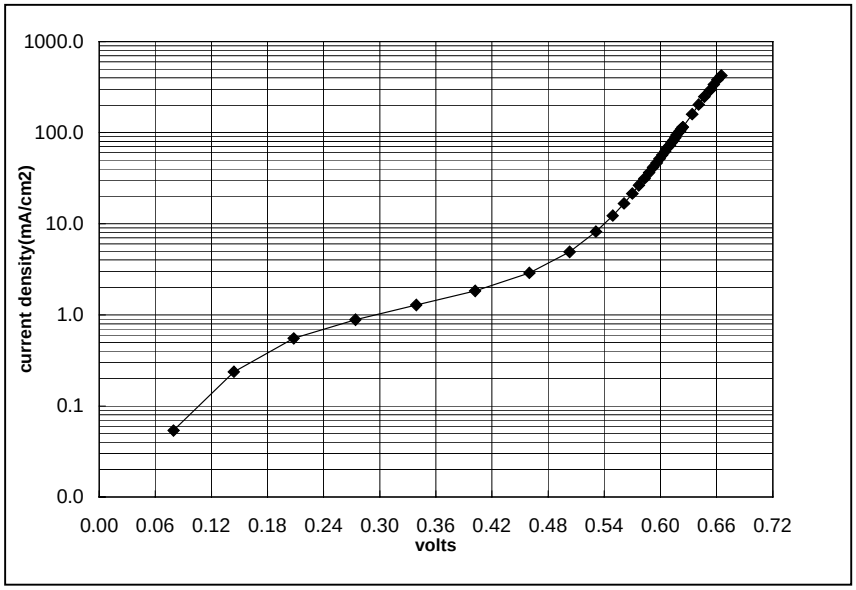

Figure 8.11. Dark I-V curve of p on n diode created from Ag/Si/B compound

Monolithic Module Assembly

The most significant advantage of the back-contact configuration is simplification of the module assembly. The conventional cell geometry with contacts on front and back surfaces is difficult to automate, and module fabrication (including labor and materials) now accounts for nearly 50% of the finished module cost. We were working on a new module assembly concept that encapsulates and electrically connects all the cells in the module in a single step. The key features of this new process include the following: (1) back-contact cells, (2) a module backplane that has both the electrical circuit and encapsulation material in a single piece, and (3) a single-step process for assembly of these components into a module (Figure 8.12). This process reduces costs by reducing the number of steps, by eliminating low-throughput (e.g., individual cell tabbing, cell stringing, layout, etc.) steps, and by using completely planar processes that are easy to automate. We referred to this process as "monolithic module assembly" since it translates many of the advantages of monolithic module construction of thin-film PV to wafered c-Si PV. Simplifications in the module fabrication have been estimated to reduce the cost of module fabrication by up to 50%, which corresponds to a reduction of around 25% in the total manufacturing cost for the module.

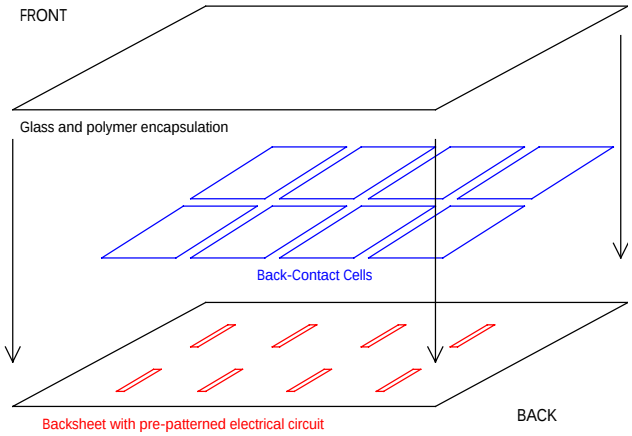

Figure 8.12. Schematic illustration of monolithic module assembly

Our first process used a conductive epoxy for the electrical attachment material. The electrical resistance of the epoxy bonds continuously increased during thermal cycling, which led us to examine other materials for the electrical attachment. We next examined solder for the electrical attachment material. Solder can make reliable, low-cost electrical attachments. However, we had to examine solders with relatively low liquiduus temperatures (<150°C) due to the use of ethylene vinyl acetate (EVA) for the encapsulant.

We examined bismuth-alloy solders with liquiduus temperatures of 100 and 138°C. We were able to make electrical bonds with both solders during an encapsulation cycle in a standard pressure-vacuum laminator and using EVA. Metallography of assembled modules found that the solder joint was not continuous. The EVA both melts and flows during the lamination cycle, which could interfere with wetting of the solder between the tinned copper electrodes and the solar cell buss bar. Changes in the geometry of the solder joint, stabilization of the copper electrode, and/or variations in the encapsulation process may improve the quality of the solder joints.

Diffraction Grating Structures in Solar Cells

Sub-wavelength periodic texturing (gratings) of crystalline-silicon (c-Si) surfaces for solar cell applications can be designed for maximizing optical absorption in thin c-Si films. We have investigated c-Si grating structures using rigorous modeling, hemispherical reflectance, and internal quantum efficiency measurements. Model calculations predict almost ~ 100 % energy coupling into obliquely propagating diffraction orders. By fabrication and optical characterization of a wide range of 1D and 2D c-Si grating structures, we have achieved broadband, low (~ 5 %) reflectance without

an anti-reflection film. By integrating grating structures into conventional solar cell designs, we have demonstrated short-circuit current density enhancements of 3.4 and 4.1 mA/cm^2 for rectangular and triangular 1D grating structures compared to planar controls. The effective path length enhancements due to these gratings were 2.2 and 1.7, respectively. Optimized 2D gratings are expected to have even better performance.

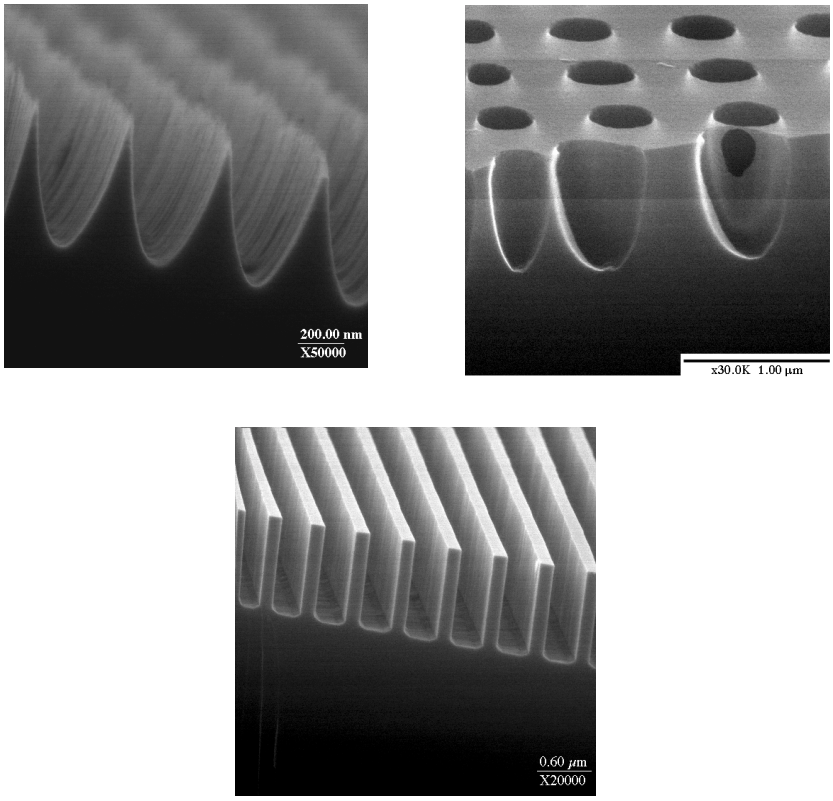

Figure 8.13. SEM photomicrographs of (a) 1D triangular, (b) 1D rectangular, and (c) 2D hole pattern grating

We refer to "effective" path length enhancement since the generation profile with the grating is a combination of different modes traveling at different angles. The effective path length enhancement for the triangular and rectangular profiles is roughly 1.7 and 2.2, respectively. For comparison, the path length enhancement with chemically textured surfaces is around 1.3 since the light is coupled into the silicon at a well-defined angle

Solar-Grade Silicon Research

Crystalline-silicon PV industry traditionally used waste material from the electronic-grade silicon industry for its silicon feedstock. The PV industry benefited from an over capacity in the electronic-grade silicon industry for many years, although there have been

periods where the PV industry had difficulty obtaining silicon feedstock when demand from the electronic industry exceeded supply from electronic-grade silicon feedstock production. Similarly, the availability of an inexpensive, high-purity silicon feedstock is an issue for the long-term growth of the c-Si PV industry.

Solar-grade silicon production had been examined during the JPL program. The progression of the industry brought the issue to the fore again, and advances in metallurgy and other fields opened possible new approaches.

We performed a thermochemical analysis of purification of silicon melts. The analysis performed chemical equilibrium calculations of situations corresponding to purification of silicon melts by injection of reactive gases. The equilibrium distributions of silicon, boron, phosphorus, carbon, nitrogen, oxygen, and iron among solid, liquid, and gas phases were calculated as a function of pressure, temperature, and reactive gas composition. The reactive gases included ammonia, oxygen, nitrogen, air, water, chlorine, and hydrogen chloride.

The calculations found a possible new method for removing the most difficult impurity in silicon – boron. Boron was found to react preferentially with nitrogen to form boron nitride (BN). BN should be a solid, which would need to be removed from the silicon melt in order to remove the boron. (SAND99-1047)

Silicon purification experiments were conducted with a vacuum induction furnace. Metallurgical-grade silicon in charge sizes of 20 kg was melted in a vacuum induction furnace. The silicon melt was blown with ammonia gas to provide nitrogen for the BN reaction.

Most of the impurities (phosphorus and metallic elements) were reduced with only a few hours of vacuum treatment, but there was no reduction noted in the boron concentration. The reduction of the other impurities was probably due to volatilization – possibly assisted with reactions of the silicon melt and impurities with residual water vapor in the chamber. The lack of boron reduction may have been due to inadequate sinks for solid BN while the silicon was still molten. Further research on slag chemistry may improve the boron purification of silicon melts. (SAND00-0821)

Chapter 9. CONCLUSIONS

Crystalline-silicon one-sun PV technology was the first PV technology to reach commercial success. It still dominates the market today despite some inherent disadvantages (large material and energy content for the c-Si) compared to thin-film and concentrator PV technologies. Crystalline-silicon PV technology has also achieved a very high level of technical sophistication – issues associated with the specific bonding structure of hydrogen in silicon are discussed at the same meetings as issues associated with requirements for achieving 100-MW/year production lines!

Past success is not necessarily a guide to future returns. Nevertheless, we believe that c-Si will remain a critical element for the continued commercial success of PV systems due to the fundamental advantages of c-Si as a PV technology that were enumerated in the Introduction. Furthermore, we believe that the future will find the following trends in c-Si technology:

- Increased plant size (100+ MW/year) with increased automation and throughput, and improved process and material yields.
- Increased use of non-wafered c-Si technologies (ribbon, sheet, thick-film, and thin-film), and use of very thin (<150 μm) wafered c-Si substrates.
- Improvement of commercial c-Si efficiencies through adoption of new processes (texturing, new metallizations and contacts, heterojunctions, BSFs, plasma processing, RTP, etc.) to 20%.
- Development of new sources of silicon that take advantage of waste materials from other industries.
- Cost reductions that follow *United States PV Industry Roadmap* targets through 2020.

The technical promise of c-Si PV remains bright and the commercial progress of c-Si PV industry and been impressive. Nevertheless, we feel that a strong government R&D role is still required to help realize the potential of this technology to meet the needs of US customers for clean, reliable, affordable energy. Government R&D investment is required for PV solar energy in general because PV is a very technically sophisticated product to manufacture while the energy industry generally features low margins and R&D investment. The *PV Industry Roadmapping* workshops, *Workshop on Crystalline-Silicon Solar Cell Materials and Processes,* and workshop on *Basic Research Opportunities in Photovoltaics* have all identified a number of research needs for c-Si PV in order to help c-Si PV achieve its full potential as outlined in the above trends.

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