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AlGaN Materials Engineering for Integrated Multi-function Systems

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Abstract Follows

Abstract

This LDRD is aimed to place Sandia at the forefront of GaN-based technologies. Two important themes of this LDRD are: 1) The demonstration of novel GaN-based devices which have not yet been much explored and yet are coherent with Sandia's and DOE's mission objectives. UV optoelectronic and piezoelectric devices are just two examples. 2) To demonstrate front-end monolithic integration of GaN with Si-based microelectronics. Key issues pertinent to the successful completion of this LDRD have been identified to be 1) The growth and defect control of AlGaN and GaN, and 2) strain relief during/after the heteroepitaxy of GaN on Si and the separation/transfer of GaN layers to different wafer templates.

Key Words: GaN, AlGaN, Wide bandgap semiconductors, porous GaN, porous Si, strain engineering, epitaxial growth, MOCVD, MOVPE

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I. Introduction

In response to a world-wide interest in wide-bandgap III-nitride devices and the recent progress in the development of metal-organic chemical vapor deposition (MOCVD) growth of (Al,Ga)N materials at Sandia, we propose to explore the multi-functional usage of GaN to meet various mission requirements and to position Sandia at the technological forefront of this strategically important material family. Over a wide range of possible applications, we have identified the development of compact ultra-violet (UV) optoelectronic devices (emitters and detectors), piezoelectric devices (surface acoustic wave (SAW) sensors), and the integration of GaN with silicon as the initial thrust areas. All of these areas have thus far remained relatively unexplored and yet are well aligned with Sandia's mission objectives. In addition to maintaining a broad portfolio, this LDRD will explore the full potential of the ceramic-like nature of the III-nitride materials (namely the physical robustness, chemical inertness and tolerance to structural defects), to achieve chip level integration into microsystems containing various nitride devices and possibly between nitride devices and silicon-based electronics.

II. Strain engineering of III-nitride films in Si (111)

The integration and growth of gallium nitride (GaN) on silicon (Si) has proven to be a challenging problem due to the thermal expansion differences between GaN and Si. Typical GaN grown on Si(111) at standard temperatures and pressures encounters its most significant problems during the cooling step after growth. As the wafer starts to cool the thermal expansion mismatch between the GaN and Si puts the GaN in tension (~0.3% tensile strain). To relieve this tension in the GaN film macroscopic cracks are formed.

To alleviate this tensile strain and thereby reduce/eliminate the cracks formed during cool down one can design a multilayer system where an intermediate HT $Al_xGa_{1-x}N$ layer is grown on a Si(111) wafer with an HT AlN buffer layer. An upper Al_yGa_{1-y} N layer with a lower composition of Al or a GaN layer (with no Al) then follows this intermediate AlGaN layer. During growth this upper layer will be under compression if the percentage of Al (y%) in it is less than the percentage of aluminum in the layer below it (x%). Upon cool down the total strain in the upper film will be the amount of

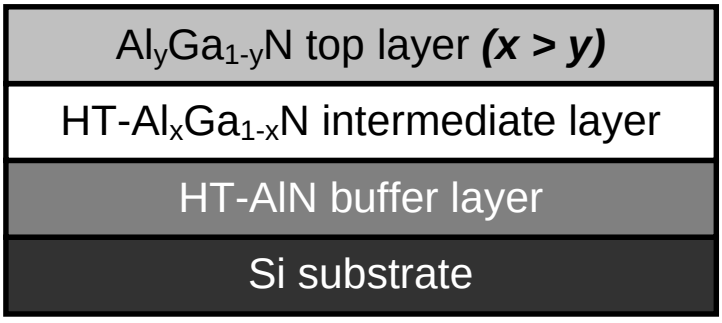


Figure 1. Schematic of strain-relieving intermediate AlGaN layer.

compressive strain induced during growth plus the amount of tensile strain normally seen during GaN on Si(111) growth. This will result in a reduced amount of overall tensile strain after cool down.

This technique is different from existing techniques in that it uses AlGaN interlayers grown compressively to counteract some of the tensile strain experienced by the layer during cool down. To our knowledge this technique has not been reported. When perfected, this technique will allow the growth of GaN on Si(111) on large area substrates (2" or greater). GaN has been shown to be a highly useful material for many optoelectronic and electronic devices that can be used in high-temperature and harsh environments. The addition of Si as a substrate not only reduces the cost over more conventional Al_2O_3 and SiC substrates, but it opens up entirely new avenues of device development. The possibility of combining devices commonly manufactured in Si with V-III optoelectronic and electronic devices is an area just beginning to be explored.

III. Epitaxial Growth of GaN on Porous GaN

Hexagonal GaN is widely used in applications involving short wavelength (green, blue and UV) optoelectronics and high-temperature or high-power electronics. A key issue for these applications is the growth of high quality GaN. Single-crystal GaN substrates are not readily available and epitaxial deposition of GaN on other semiconductors has proven difficult because of large lattice mismatches. Most GaN-based devices employ costly sapphire (Al_2O_3) substrates or even costlier 6H-SiC. It would be very useful to expand the set of substrates that are capable of supporting "device-quality" GaN epitaxy for increased device performance or lower cost. Integration between GaN and Si could enable new applications for both materials. Although the thermal conductivity is not as high as in silicon carbide, silicon substrates can outperform silicon carbide in heat removal for high-power applications because micromachining techniques for silicon are well developed. Silicon offers a conducting substrate, as opposed to sapphire, which would lead to reduced fabrication cost of devices such as LEDs and lasers. Additionally, silicon substrates are much less expensive than sapphire or 6H-SiC, and are available in large wafer diameters and high quality.

Recently, there have been reports of epitaxial growth of GaN on {111} Si. However, the presence of cracking networks due to the thermal expansion mismatch appears to limit the practical device implementation. The largest crack-free areas reported to-date[1] are about 500 μm x 500 μm.

The work described here is the use of porous gallium nitride (PGaN) over porous silicon (PS) to produce device-quality $AlGa_{1-x}N$ (to be referred to as GaN) material. These GaN layers are grown onto a composite porous silicon/PGaN. This composite is formed by epitaxially depositing a thin (ca. 0.1 μm) GaN layer onto a fully dense {111} silicon wafer. Because the GaN is so thin, no cracks form in the GaN on cool down from deposition temperatures. The GaN and the underlying silicon are made porous in one step by electrochemical anodization in hydrofluoric acid electrolytes. The PS layer serves to reduce the thermal expansion mismatch stress between the Si substrate and

hence mitigate cracking of the GaN layer. The PGaN layer serves as a template for further GaN epitaxial growth.

Porous silicon is a sponge-like material formed by anodization of Si wafers in hydrofluoric (HF) acid solutions. Being spongy, porous silicon is expected to be less stiff and likelier to crack than fully-dense silicon. The porosity and microstructure, and hence the resulting mechanical properties of the porous silicon, can be controlled by tailoring the anodization conditions and silicon doping.

Since the thermal expansion coefficient of GaN is greater than that of Si, on cool-down after deposition at high temperatures the GaN layer attempts to shrink more than the Si substrate. The adhesive forces between the GaN film and the Si substrate cause the GaN to stretch to the wafer diameter resulting in cracking of this layer. The use of an intermediate PSL between the GaN film and the Si substrate will partially absorb the misfit between the top face of the Si substrate and the bottom face of the GaN film. Additionally, any micro-cracking of the PS layer will decrease the stress transmitted to the GaN layer.

GaN is deposited directly onto PGaN, which covers a porous silicon underlayer. The porous silicon serves as a compliant substrate to prevent cracking while the porous GaN serves as a template for epitaxial GaN growth (see Figure 2).

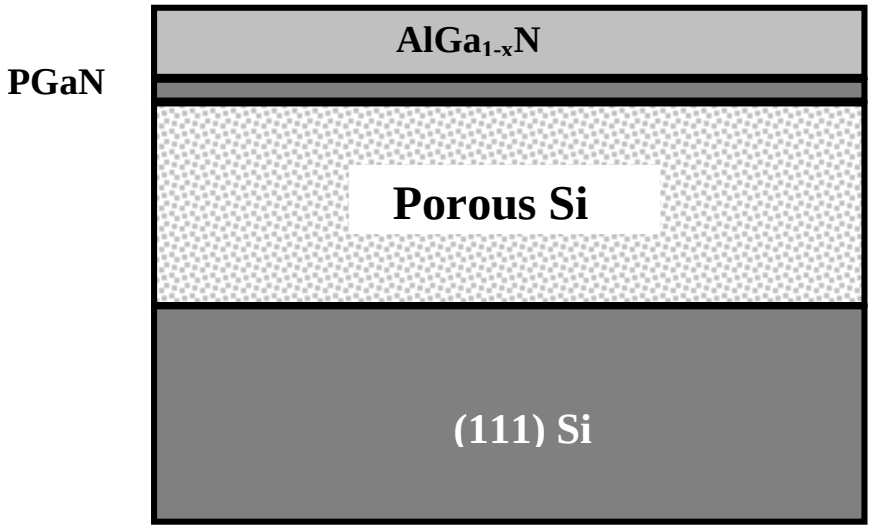


Figure 2. Schematic of GaN on Porous Si.

A trenched porous GaN/porous silicon substrate may also offer a wider process window for some applications. The trenches offer additional stress relief between the Si substrate and the GaN.

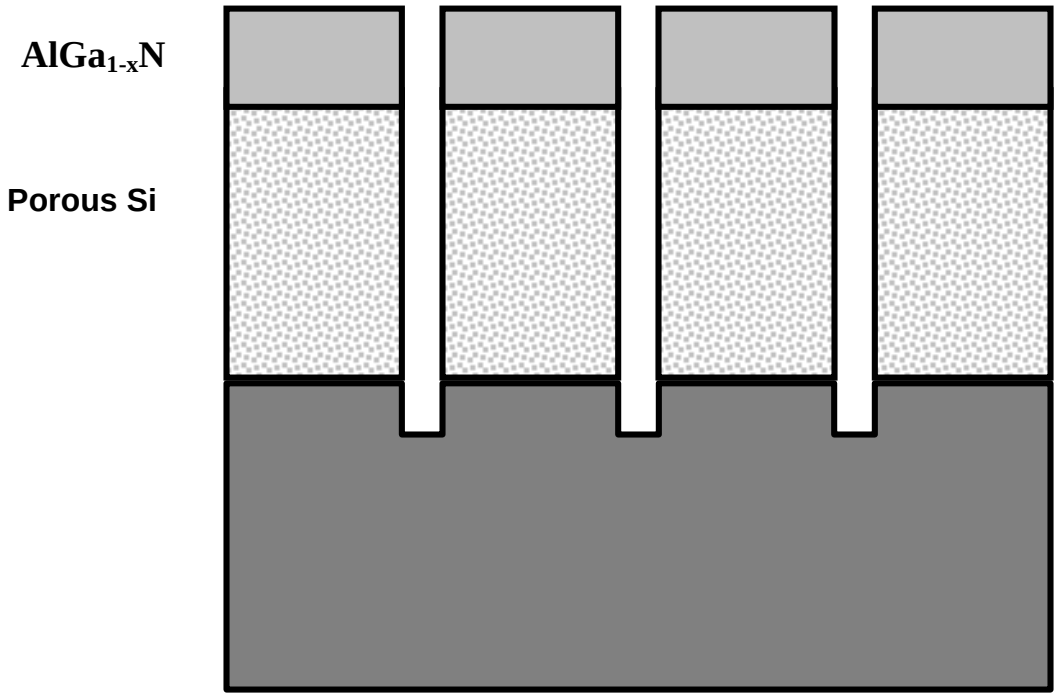


Figure 3. Schematic of trenched porous silicon substrate.

In another embodiment, porous silicon (capped by a porous GaN layer) is used as a sacrificial layer and is removed after deposition of a thick GaN film (on the order of 100 microns or greater) able to mechanically support its own weight.

On cool-down from GaN deposition (perhaps by hydride vapor phase epitaxy-HVPE), the PS layer may itself crack causing separation of the thick GaN film from the Si substrate. Any remaining PS adhering to the bottom of the GaN can be etched off easily and selectively. The GaN film may also be detached from the substrate by selective etching of the PS layer. Because of its porosity, PS can be etched off much faster than the fully-dense Si substrate. Existing technologies to grow GaN have not used porous GaN over porous silicon as part of the Si substrate.

Existing technology to relieve thermal expansion mismatch stresses during growth of GaN on Si includes use of compliant substrates such as silicon-on-insulator.

Seeding techniques such as LEO (lateral epitaxial overgrowth) or pendeo-epitaxy to confine cracks to particular areas have also been shown to mitigate stress effects on GaN device fabrication.

Large free-standing GaN substrates have been obtained by hydride vapor phase epitaxy and laser-induced liftoff.[2] Use of the PGaN/PS layer is an improvement over existing technology as it can lead to a greater reduction of the transmitted stress from the substrate. It is also less costly to implement than many other substrate options such as sapphire or silicon carbide.

Figure 4. Schematic of free-standing GaN concept.

IV. GaN Epitaxial Growth on Porous Silicon

In the last year of this LDRD project, attention was given to a new concept, namely the epitaxial growth of GaN on compliant substrates. The use of a surface porous layer as a compliant substrate for the growth of semiconductor films has been reported for Si on porous Si[3,4,5], GeSi on porous Si[3], GaAs on porous Si,[4] diamond on porous Si,[5] GaN on porous GaAs,[6] and GaN on porous GaN.[7] However, the integration of GaN with Si through MOCVD growth onto a porous Si substrate has not yet been reported. The compliant layer serves to reduce the thermal expansion mismatch stress between the Si substrate and hence mitigate cracking of the GaN layer.

Porous silicon is a sponge-like material formed by anodization of Si in hydrofluoric (HF) acid solutions. Being spongy, porous silicon is less stiff and less likely to crack than fully-dense silicon. The porosity and microstructure, and hence the resulting mechanical properties of the porous silicon, can be controlled by tailoring the anodization conditions and silicon doping.

Since the thermal expansion coefficient of GaN is greater than that of Si, on cool-down after deposition at high temperatures the GaN layer attempts to shrink more than the Si substrate. The adhesive forces between the GaN film and the Si substrate cause the GaN to stretch to the wafer diameter resulting in cracking of this layer. The use of an intermediate porous Si layer between the GaN film and the Si substrate will partially absorb the misfit between the top face of the Si substrate and the bottom face of the GaN film. Additionally, any micro-cracking of the porous Si layer will decrease the stress transmitted to the GaN layer.[8]

Previous work in this LDRD project had shown that device-quality GaN could be grown by MOCVD on fully-dense (111) Si. An AlN buffer layer was first deposited on the Si to aid in nucleation of the hexagonal nitride material. Epitaxial GaN was then grown on the AlN buffer layer. Cracking was observed due to the differing thermal expansions of GaN and Si; nonetheless, the material between the cracks was examined by TEM and was found to have a microstructure very similar to that of the widely-studied GaN on sapphire heterostructure. The density and character of the dislocations was also found to be similar to the GaN/sapphire heterostructure that has been successfully used to fabricate visible and UV lasers and LEDs. The goal of the work described in this section, namely the deposition of GaN onto compliant porous Si substrates, was to determine if crack-free GaN of similar quality could be produced.

We completed one attempt to deposit GaN onto a compliant substrate. The result is seen in Figure 5, which shows a cross-section SEM of MOCVD AlN/GaN grown on porous silicon. The details of the fabrication process steps which preceded the AlN and GaN epitaxy are as follows:

1. Porous silicon was formed in p-type, 0.002-0.0035 Ω-cm, single crystal (111) Si. The silicon was anodized in 49 wt.% HF for 5 minutes at a current density of 45 mA/cm^2, producing a silicon layer that was approximately 49% porous and 12 μm thick.
2. The porous silicon sample was cleaned in a sulfuric acid/hydrogen peroxide mixture at ~ 90 ^oC. The purpose of this step was to remove organic contamination from the surface of the porous silicon, as well as from the pore walls beneath the surface.
3. The porous silicon layer was stabilized by low temperature (350 ^oC) oxidation in dry oxygen for 1 hour. The purpose of this step was to oxidize the surface of the pore walls to an extent that stabilizes them against collapse when the sample is exposed to higher temperatures during subsequent AlN and GaN deposition steps. There is evidence in the literature[5] that this oxidation does not completely convert the porous silicon layer to an oxide, and this is important because it is essential to have a crystalline porous silicon framework as a template for the AlN and GaN epitaxial growth steps.
4. The wafers were cleaned in a 100:1 H_2O:49% HF mixture for several minutes, using ultrasonic agitation to improve the efficiency of the cleaning step.

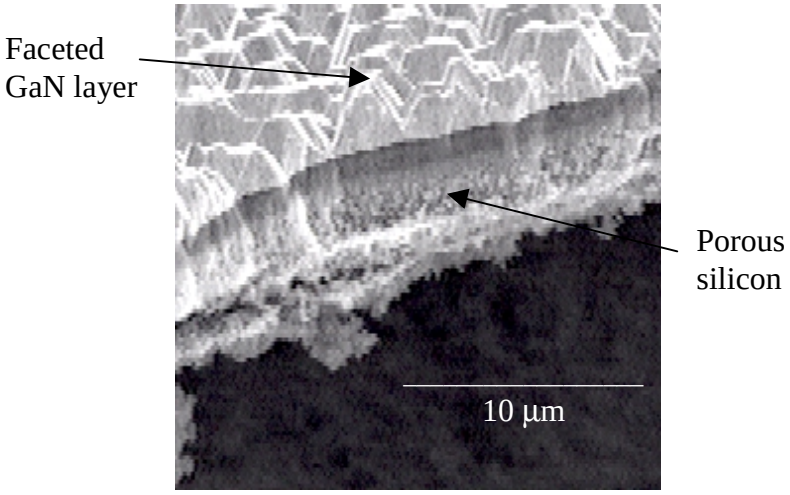


Figure 5. Cross-section SEM of MOCVD GaN on porous silicon.

In Figure 5, the AlN apparently forms to some depth in the porous Si layer, does not appear to form a continuous layer on top of the layer, and is not readily observed in the micrograph. Cracking was observed to occur in the porous silicon layer rather than in the GaN layer itself, thus demonstrating that stress relief can be made to occur in the more compliant layer of the structure. Islands of crack-free GaN larger than 400 μm by 800 μm were observed in these samples; however, the GaN was not of high crystalline quality. We have several hypotheses as to why the GaN layer was of poor crystalline quality. Addressing these concerns should be the focus of future research involving GaN deposition onto porous Si substrates. As a first course of study, we recommend the following changes to the process steps:

1. In the dilute HF cleaning step, the wafers should only be briefly dipped in the dilute HF. We recommend attempting a 30-second etch in 100:1 H_2O:49% HF, without ultrasonic agitation. The goal is to remove only the surface oxide, but not the oxide on the pore walls beneath the surface. In the sample shown in Figure 5, we believe that the stabilization oxide grown in the low-temperature oxidation step was substantially or completely removed during the extended ultrasonic cleaning step in dilute HF. Therefore, there is a good possibility that the porous structure coarsened or collapsed during the high temperature AlN and/or GaN deposition steps, thereby degrading the quality of the porous silicon as a compliant substrate for epitaxy.
2. Following the dilute HF clean, the wafers should be annealed in dry hydrogen for 3 minutes at 1100 ^{o}C. There is evidence in the literature[5] that this process anneals the surface of the porous silicon layer so that a continuous, crystalline surface layer is formed. Our hypothesis is that this layer now combines the desirable features of a compliant substrate (due to the nature of the porous silicon) with a continous template for epitaxial growth (i.e., the uniform silicon surface). This step can be performed in the same reactor where the AlN and GaN depositions are performed, and should be done immediately prior to AlN deposition.

3. Finally, attempts should be made to accurately control the temperature of the porous silicon surface during AlN and GaN epitaxy at temperatures similar to those used in high-quality epitaxial growth on fully-dense silicon (111) substrates. In the sample shown in Figure 5, we believe that poor thermal conduction from the MOCVD reactor susceptor to the porous silicon surface (likely due to the low thermal conductivity of porous silicon compared to fully-dense silicon) led to epitaxial deposition of AlN and GaN at surface temperatures below the optimum temperature for high-quality deposition.

Two additional paths were identified for further research. The first path involves a compliant substrate consisting of a thin layer of epitaxial (111) silicon deposited over the porous silicon. This fully dense layer could provide a better template for GaN deposition than the porous silicon alone. The second path involves depositing an ultra-thin layer of GaN on (111) silicon.[9] Because the layer is so thin, the GaN does not crack on cool-down. The GaN layer and silicon could then be made porous in a second step to provide an epitaxial substrate that combines the advantages of compliancy (of the thick porous layer) and crystal nucleation (of the hexagonal GaN material).

For lack of time and resources, experiments with epitaxial silicon deposited onto porous silicon were not further pursued. We focused our efforts on the porous GaN/porous silicon substrate. It was found that the GaN layer could be made porous thus allowing HF access to the silicon substrate where a thicker porous silicon layer could be formed during an extended anodization process. The samples used in these experiments consisted of ~ 0.1 μm thick, crack-free GaN layers deposited onto p-type (111) silicon substrates of two different resistivities (0.002-0.0035 Ω-cm and 0.062-0.065 Ω-cm). A porous GaN/porous Si substrate was formed by anodization of these samples in 49 wt.% HF at current densities between 5-45 mA/cm^2. At this writing, GaN deposition has not been performed on these wafers. We believe that this approach has considerable promise since porous GaN should provide a better template for GaN nucleation and growth than porous Si.

V. Epitaxial Growth of GaN on Patterned Substrates

The integration and growth of gallium nitride (GaN) on silicon (Si) has proven to be a challenging problem due to the thermal expansion differences between GaN and Si. Typical GaN grown on Si(111) at standard temperatures and pressures encounters its most significant problems during the cooling step after growth. As the wafer starts to cool the thermal expansion mismatch between the GaN and Si puts the GaN in tension. To relieve this tension in the GaN film macroscopic cracks form. For a crack to form and propagate there has to be sufficient strain in the film and a crack nucleation source has to be present. By dividing a 2 inch silicon wafer into small regions (~1000 μm^2) it may be possible to grow an uncracked GaN film thick enough to make a device.

The procedure for this experiment is to take a Si(111) wafer and etch posts of varying sizes using Bosch etching (Figure 6). A matrix of each size of post is made which makes measurement and analysis easier.

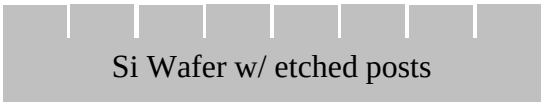


Figure 6. Si(111) with etched posts.

The trenches that separate the posts are 50 – 80 μm deep. The goal is to make the largest possible area of non-cracked GaN. High quality GaN is grown on top of the posts using an MOCVD process. The process includes a HT AlN buffer layer, LT GaN buffer layer, and HT GaN epilayer (Figure 7). Figures 8 and 9 show 1.4 μm GaN grown on a 75 μm and 100 μm silicon post.

Figure 7. Schematic of Si(111) posts with GaN growth.

Figure 8. 1.4 μm GaN on 75 μm x 75 μm post.

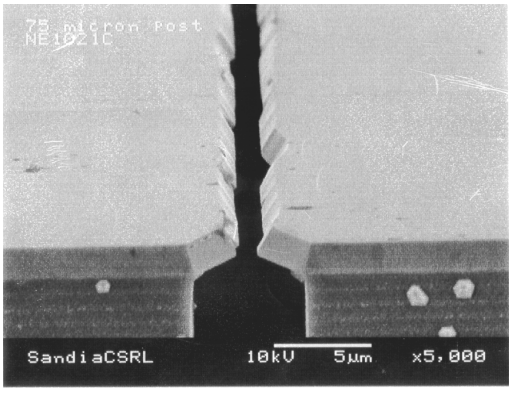
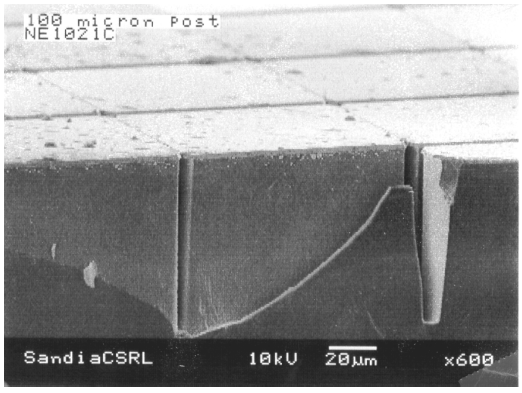


Figure 9. 1.4 microns GaN on 100 μm x 100 μm post.



For an array of 75 μm x 75 μm posts 83% of the GaN covered posts did not crack. This is an excellent yield on a surface large enough to make an electronic device. The sizes of posts tested are 2500 μm^2, 5635 μm^2, 10000 μm^2, 22500 μm^2, and 40000 μm^2.

The percentage of uncracked squares follows a Poisson distribution and decreases as the area increases. The probability that a square will crack is shown in Equation 1 where P(A) is the probability that a square will crack and $\overline{A}$ is defined as the area per post, A (μm^2), divided by the area per defect, A_0 (μm^2).

$$P(A) = 1 - e^{\overline{A}} \qquad \frac{A}{A_o} = \overline{A} \qquad (1)$$

The results of this equation are illustrated in Figure 10 for three different cases. The three different cases show situations where ten crack nucleation sites (origin yet to be determined in this system) are randomly distributed over a 1000 μm^2 area that has been divided into different size posts. For all of these cases A_o, the area per defect, is 100 μm^2.

Case 1 shows the area as a single post with an area of 1000 μm^2. The probability of a post cracking that is 1000 μm^2 in a system where the area per defect is 100 μm^2 is 1, it will crack 100% of the time. Case 2 shows the total area divided into posts with an area of 100 μm^2. For this case the probability that a post will crack is 0.623. Case 3 shows the total area divided into posts that have an area of 10 μm^2. The probability of cracking in this case is 0.095.

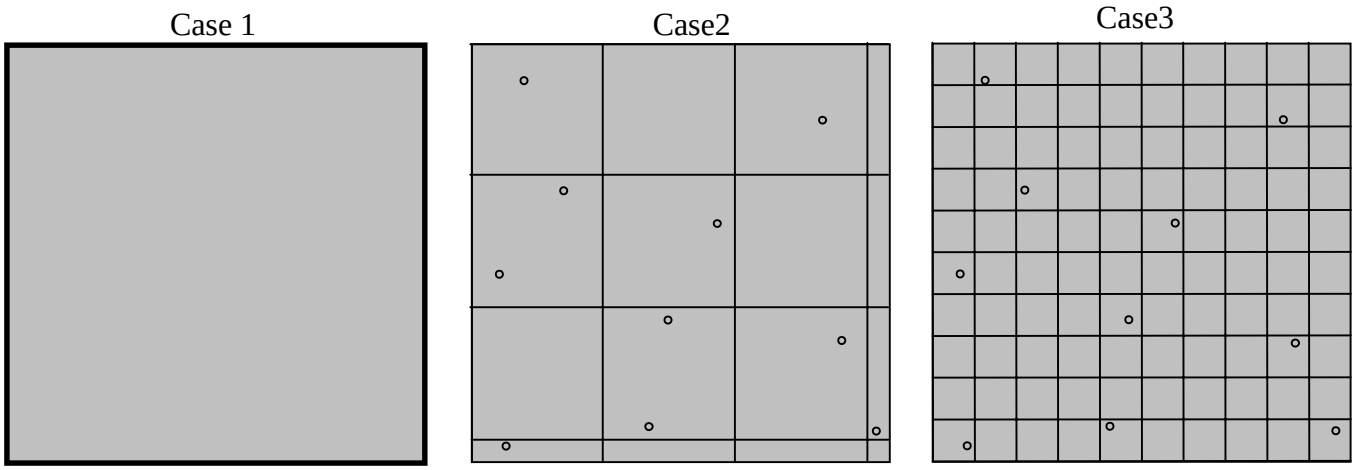


Figure 10. Illustration of random defects affecting the cracking of GaN grown on various size silicon posts.

This probability of a square cracking compared to our experimental data is shown in Figure 11. This figure shows that the functional form of our experimental data fits the theory of randomly distributed crack nucleation points.

When $\overline{A}$ is scaled to fit the experimental data the experimental crack nucleation site density (ρ_o) can be found. For our data, $\rho_o = 4 \times 10^{-5}\ \mu m^{2\ -1}$ or we have one crack nucleation site for every 25000 μm^2 of material. It can also be stated that an array of squares 158.1 μm on a side would yield a success rate of 37.7%.

Currently existing techniques used to grow GaN on Si(111) can not produce uncracked films of sufficient thickness to make good quality device material. This is a problem that is being tackled from many different directions but to our knowledge this is the first time that the use of patterned substrates has been used for GaN/Si growth.

VI. Smart Cut: GROWTH OF GaN ON THIN SI {111} LAYERS BONDED TO SI {100} SUBSTRATES

We are interested in developing integrated systems able to process information, sense, act and communicate. Eventually, all these capabilities will co-exist on a single die. At present, we are able to integrate Si-based electronics with various sensors and Si surface micromachined actuators. However, silicon's indirect band gap makes it unsuited to the manipulation of light for photonics and communications applications. GaN and its alloys are emerging as important optically active materials. They are relatively chemically and physically stable and defect insensitive. These unique properties, and reports that growth of GaN on {111} Si is possible[10-12] have motivated us to try to integrate GaN with silicon technologies. However, while growth on {111} Si has been proven, typical CMOS technologies are based on {100} and not {111} silicon. As a first step, we have demonstrated the bonding of a thin layer of Si {111} material onto a thin silicon dioxide layer on a Si {100} substrate. This was done using a process developed by the French and often referred to as "Smart-Cut" [10-12] in which, in our case, a {111} wafer undergoes a high dose H implant. The dose is sufficiently high to nucleate bubbles at the range of the implant during heating. The stresses generated are sufficient to slice off a thin layer of silicon. Wafer bonding is initiated after implantation and the bond is strengthened by later heat treatments. We have subsequently used such hybrid substrates to grow epitaxial GaN. In order to address the potential problem of Ga diffusing into the silicon and degrading the CMOS we have demonstrated the insertion of a thin SiN diffusion barrier between the two layers of silicon.

Our final objective is the integration of standard CMOS technology with GaN. We proposed to achieve this through the combination of CMOS fabrication on Si{100} and the deposition of GaN on Si{111}. This is schematically outlined in Figure 12. This will require the integration of two different Si orientations and the introduction of Ga diffusion barrier between the Si layers. SiN has been demonstrated to be an effective Ga barrier[10] and we have used integrated this material in the work presented here.

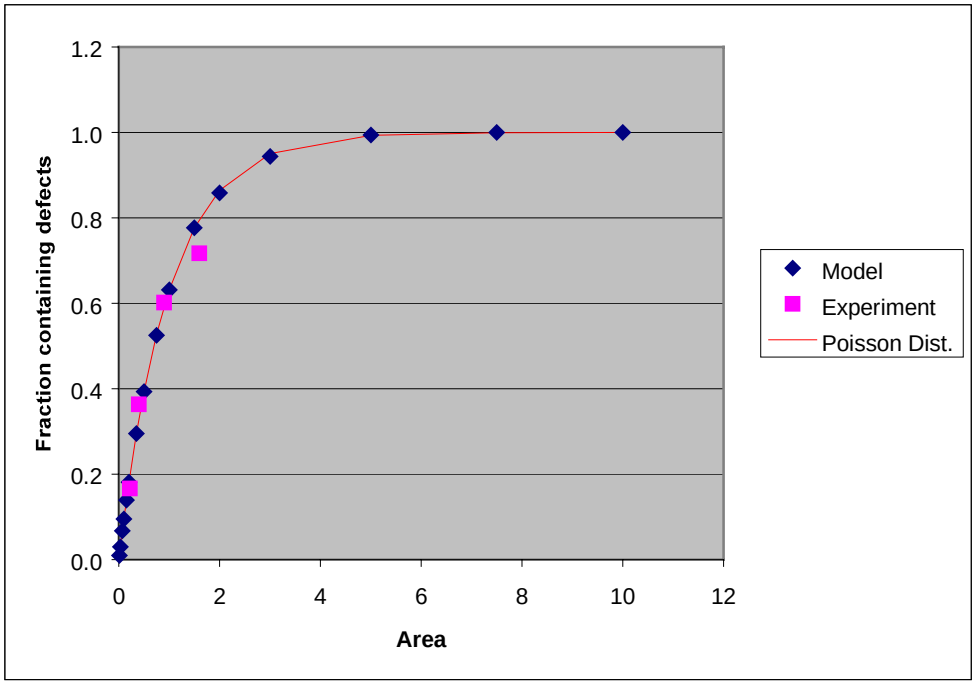


Figure 11. Fraction of posts that contain defects and their relation to a theory of randomly distributed crack nucleation points

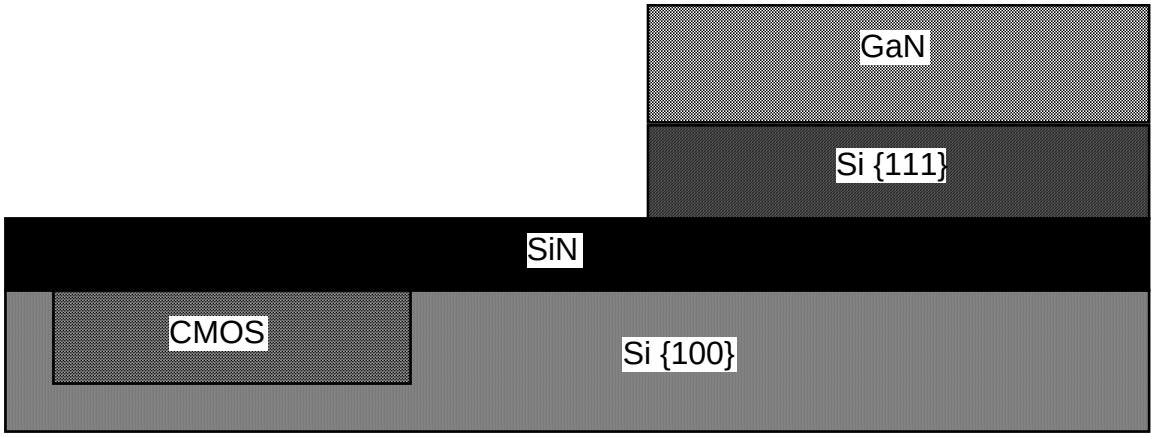


Fig. 12 Schematic of our proposed approach, CMOS will be fabricated on Si {100} and will be protected by a thin layer of SiN. The GaN will then be grown on a thin layer of Si{111} bonded to the Si{100}.

The “Smart-Cut” process is the technology we have explored to integrate the two different orientations of Si onto a single substrate. The process is schematically rendered in Fig. 13. In our work we have typically used a dose of $4x10^{16}$ of H_2^+ at 60keV. This results in layers which are ~350nm thick. We have used interlayers of either thermal silicon dioxide or silicon dioxide coated silicon nitride. The silicon dioxide samples were bonded as grown following a combination of a SC-1/megasonics (1:4:9, ammonium hydroxide: hydrogen peroxide: water, 5 minutes, 45 C) followed by a SC-2 (1:1:10, HCl: hydrogen peroxide: water, 5 minutes, 40 C) clean of both wafers. Upon being brought together, the wafers remain joined as a result of hydrogen bonding. We then heated the joined wafer stack to 900°C for 1 hour in N_2. We did not separate out the cutting heat treatment from the bonding heat treatment. The process works well over the vast majority of the wafer. Unbonded regions result from particles on the surface or physical defects, such as wafer scribe marks. In the unbonded regions the silicon cleaving process still takes place, however here the silicon delaminates and shatters into small fragments. Periodically there are also millimeter diameter size bubbles present. In these cases we speculate that the areas remained bonded up through the delamination process, however, at higher temperatures some other contaminant began to desorb, debonding the layer and forming the bubbles. Figure 14 shows an oblique SEM cross section of a bonded stack.

The same process was used to integrate a thin SiN layer between the two sheets of silicon. However, due the surface roughness of this deposited film, additional surface preparation was required. The silicon nitride was deposited onto the handle {100} wafer using a chemical vapor deposition process at 800°C. The reactants were dichlorosilane and ammonia. The ratio of reactants was adjusted to result in a slightly silicon rich film (refractive index of 2.1) which has a lower level of stress than stoichiometric silicon nitride. The thickness of the layer was 400nm. The as-deposited film was sufficiently rough to prevent bonding. This problem was addressed through the addition of a chemical mechanical polishing (CMP) step, Fig. 15. This eliminated the grosser surface roughness. In order to create a thin oxide surface layer to aid in bonding, the wafers were then subjected to a 900°C, 30 minute steam oxidation process. The wafers were then cleaned, bonded and heat treated as described above. Again, the process was successful on the whole; however, there were numerous small unbonded regions spread across the wafer. The origin of these defects is unclear. They may be the result of CMP slurry remaining on the surface of the wafer, or residual film roughness. This problem was addressed through the deposition of a thin film of silicon dioxide on top of the polished silicon nitride layer. The silicon dioxide was deposited by plasma enhanced chemical vapor deposition using a TEOS (tetraethoxysilane) precursor. The film was 120nm thick and, following deposition, was stabilized by a 1050°C, 20 second rapid thermal anneal in a Ar/O_2 ambient. Approximately half of this thermal oxide film was then polished back using CMP. The motivation behind this was that the thin oxide layer would bury any small defects on the wafer surface. The wafers were then bonded using the process outlined above. In this case, the bonding was successful and there were no small circular unbonded regions.

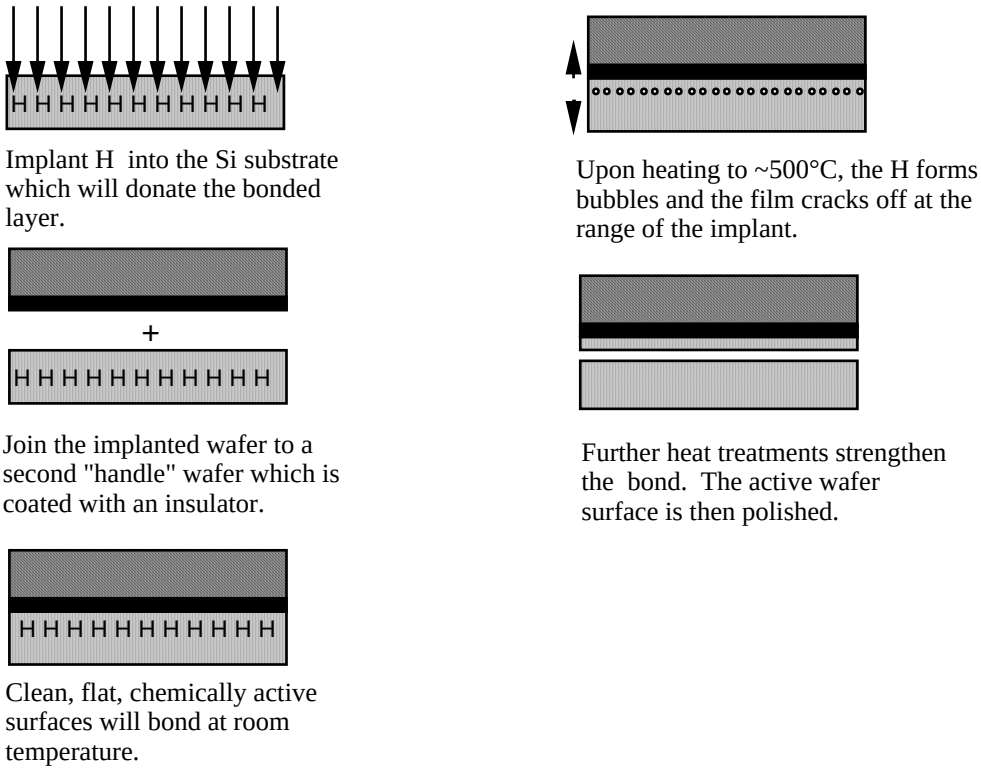


Figure 13. The "Smart-Cut" process after M. Bruel[13].

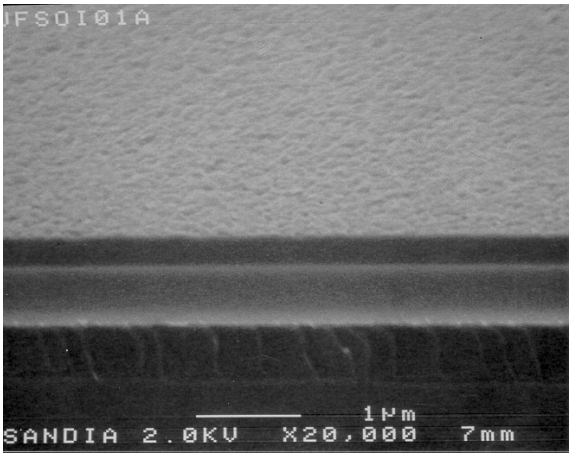


Fig. 14. Oblique cross section scanning electron micrograph showing oxide interlayer and the bonded layer.

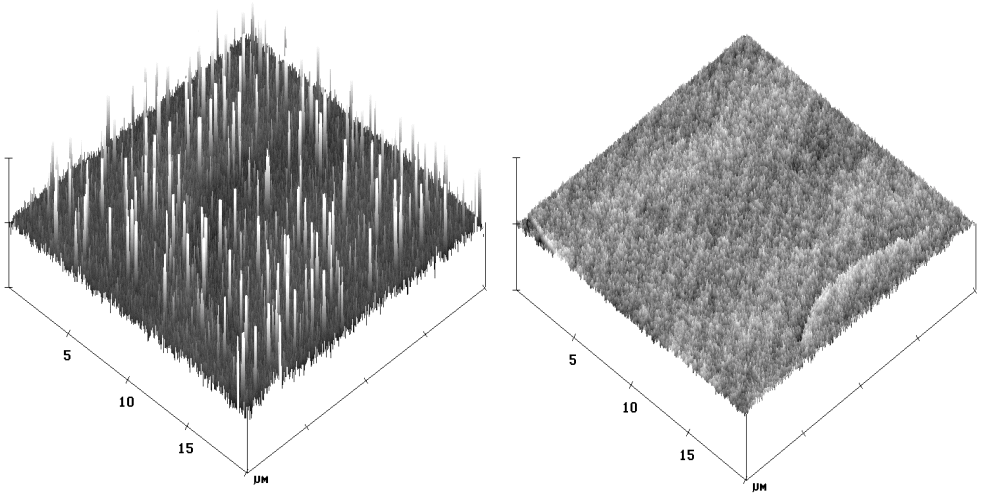


Fig. 15. AFM traces of pre and post CMP on a 400nm thick low stress SiN film. The horizontal scale is 10 nm.

Following the cleaving process, the surface of the wafers was specular to the naked eye. However, scanning electron microscopy revealed a regularly roughened surface on both {100} and {111} substrates, Fig 14. AFM measurements determined the RMS roughness to be ~6nm. In order to prepare the samples for deposition, the {111} bonded layers were subjected to a ~5 second etch in a 6M 65°C KOH solution. KOH effectively does not etch {111} Si planes. However, the {111} substrates used were ~3.5 ° off the {111} and as a result the surface consisted of a series of scalloped steps, Fig. 16.

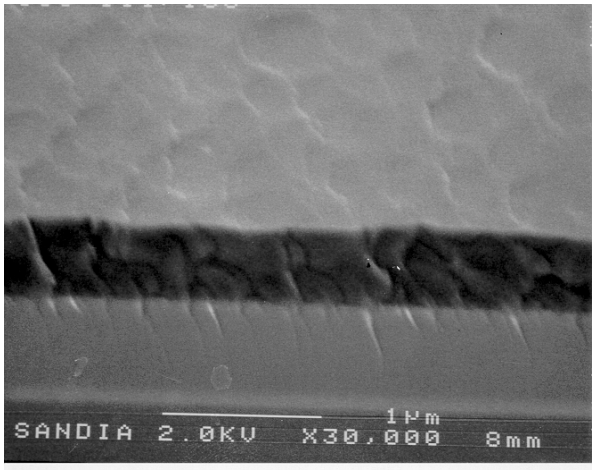


Fig. 16. SEM micrograph showing the surface morphology of a stack following a KOH treatment to remove damage at the cleavage interface. The {111} wafer was cut ~3.5 ° off orientation resulting in a scalloped-step morphology.

Layers of GaN/AlN (buffer) were grown in a high speed (~ 1000 rpm) rotating disc MOCVD reactor. Two-inch diameter substrates were placed on a molybdenum (Mo) susceptor that is RF inductively heated using a SiC-coated graphite coupling block. Temperature was monitored by a pyrometer focusing on the Mo susceptor surface, which is nearly co-planar with the wafer surface. Ammonia, TMGa (Trimethlygallium), and TMAl (Trimethylaluminum) were used as the N, Ga, and Al precursors, respectively. Hydrogen was used as the carrier gas and to supplement the ammonia in making up the required flow rate as determined by the reactor pressure and rotation rate. Metal-organic precursors were separated from hydride gases before being injected into the top of the growth chamber. An *in situ* reflectometer used to monitor surface roughness and layer thickness used a tungsten lamp as a light source. The source illuminates a spot, of 6 mm in diameter, on the sample surface through a reactor port window. Both AlN and GaN were grown at a pressure of 30 Torr. The temperature for GaN growth was varied from 1050 to 1080C and for AlN growth was varied from 1050 to 1150^{o}C. The temperature for GaN growth was varied from 1050 to 1080^{o}C and for AlN growth was varied from 1050 to 1150^{o}C. GaN was deposited on AlN on Si {111} on thermal oxide on Si {100}. The major problem encountered has been cracking due to thermal expansion mismatch between the GaN and the Si. The cracks were observed to go through the GaN and Si nucleation layer. However they stopped in the oxide layer, probably due to the compressive nature of the oxide stress. The presence of the oxide did reduce the crack length, however, cracking did still occur.

In conclusion GaN has been successfully deposited on Si{111} bonded to Si{100} with either oxide or silicon nitride interlayers. This process was enabled using "Smart-Cut" technology. The next step in the process will be the reduction in cracking, possibly using epitaxial overgrowth techniques to create isolated islands of GaN instead of continuous sheets.

VII. Conclusions

GaN has been shown to be a highly useful material for many optoelectronic and electronic devices that can be used in high-temperature and harsh environments. The addition of Si as a substrate not only reduces the cost over more conventional Al_2O_3 and SiC substrates, but it opens up entirely new avenues of device development. The possibility of combining devices commonly manufactured in Si with V-III optoelectronic and electronic devices is an area just beginning to be explored. We have also explored alternative substrates, such as porous GaN, and believe that these approaches show considerable promise since porous GaN should provide a good template for GaN nucleation and growth. Porous silicon was also explored, and promise was also found. Currently existing techniques used to grow GaN on planar Si(111) can not produce uncracked films of sufficient thickness to make good quality device material. This is a problem that is being tackled from many different directions but to our knowledge this is the first time that the use of patterned substrates has been used for GaN/Si growth. GaN has been successfully deposited on Si{111} bonded to Si{100} with either oxide or silicon nitride interlayers. This process was enabled using "Smart-Cut" technology. The

next step in the process will be the reduction in cracking, possibly using epitaxial overgrowth techniques to create isolated islands of GaN instead of continuous sheets.

VIII. References

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