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SETEC/Semiconductor Manufacturing Technologies Program: 1999 Annual and Final Report

John McBrayer

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SETEC/Semiconductor Manufacturing Technologies Program: 1999 Annual and Final Report

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Abstract

This report summarizes the results of work conducted by the Semiconductor Manufacturing Technologies Program at Sandia National Laboratories (Sandia) during 1999. This work was performed by one working group: the Semiconductor Equipment Technology Center (SETEC). The group's projects included Numerical/Experimental Characterization of the Growth of Single-Crystal Calcium Fluoride (CaF_2); The Use of High-Resolution Transmission Electron Microscopy (HRTEM) Imaging for Certifying Critical-Dimension Reference Materials Fabricated with Silicon Micromachining; Assembly Test Chip for Flip Chip on Board; Plasma Mechanism Validation: Modeling and Experimentation; and Model-Based Reduction of Contamination in Gate-Quality Nitride Reactor. During 1999, all projects focused on meeting customer needs in a timely manner and ensuring that projects were aligned with the goals of the National Technology Roadmap for Semiconductors sponsored by the Semiconductor Industry Association and with Sandia's defense mission.

This report also provides a short history of the Sandia/SEMATECH relationship and a brief on all projects completed during the seven years of the program. And as such, this is the final report for the Sandia/SEMATECH Cooperative Research and Development Agreement (CRADA), SC92/01082.

Acknowledgments

I wish to thank the Sandia and SEMATECH project leaders and team members for their efforts this past year. The names of project contributors for the 1999 projects are listed at the beginning of the individual project descriptions found in Section 2.

Specifically, the following 1999 project leaders are worthy of gratitude:

> Sandia National Laboratories: M. W. Cresswell (National Institute of Standards and Technology), S. Everist, A. Geller, S. E. Gianoulakis, G. Hebner, J. Johannes, and D. W. Peterson

I would also like to thank the many other project leaders who, over the last seven years, have made this program successful.

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Acronyms and Abbreviations

ADC	automatic detect classification
AGA	AG Associates
Al	aluminum
Al_2O_3	aluminum oxide (sapphire)
Ar	argon
ASCI	Accelerated Strategic Computing Initiative
ATC	assembly test chip
BESOI	Bonded Etched-back Silicon-on-Insulator
BGA	ball grid array
C	Celsius
C_2F_6	hexafluoroethane, perfluoroethane
C_4F_8	octafluorocyclobutane, perfluorocyclobutane
CaF_2	calcium fluoride
CD	critical dimension
CDE	chemical downstream etcher/etch
CF	fluoromethylidyne
CF_2	difluoromethylene
CF_3	trifluoromethylene
CFM	Contamination-Free Manufacturing
CFMRC	Contamination-Free Manufacturing Research Center
CHF_3	trifluoromethane
cm	centimeter
CMOS	complementary metal oxide semiconductor
CMP	chemical mechanical planarization/polishing
CRADA	Cooperative Research and Development Agreement
CTMC	Cluster Tool Module Communications
CVC	conserved vector current, also CVC Products, Inc. (a company)
CVD	chemical vapor deposition
CY	calendar year
DCA	direct chip attach
DOE	Department of Energy
DP	Defense Programs
DPS	decoupled plasma source or detached plasma source
ECR	electron cyclotron resonance
EDSC	Equipment Design and Support Center
EIC	Equipment Improvement Center
ESC	electrostatic chuck
ETAB	Executive Technical Advisory Board
FCOB	Flip Chip On Board
FEM	finite element method
FRACAS	Failure Reporting and Corrective Action System
FTAB	Focus Technical Advisory Board
FTIR	Fourier transform infrared
g	gram

Acronyms and Abbreviations (continued)

g	gravitational acceleration
GEC	Gaseous Electronics Conference
HDP	high-density plasma
HIBS	Heavy-Ion Backscattering Spectrometry
HRTEM	high-resolution transmission electron microscopy
IC	integrated circuit
ICD	ion current density
ICP	inductively coupled plasma
IDDQ	quiescent power-supply current
ILS	intracavity laser spectroscopy
IMRL	Integrated Materials Research Laboratory
I/O	input/output
IR	infrared
ITRI	Interconnection Technology Research Institute
ITRS	International Roadmap for Semiconductors
JDP	Joint Development Project
K	Kelvin
KOH	potassium chloride
kW	kilowatt
LA	laser absorption
LIF	laser-induced fluorescence
LPCVD	low-pressure chemical vapor deposition
Maglev	magnetically levitated
MDL	Microelectronics Development Laboratory
MEMS	Micro-Electrical-Mechanical Systems
MESC	Modular Equipment Standards Committee
MF	mole fraction
MIMO	multi-input multi-output
MIT	Massachusetts Institute of Technology
mm	millimeter
NFE	Non-Federal Entity
NIH	National Institutes of Health
NIST	National Institute of Standards and Technology
nm	nanometer
NMP	n-methyl pyrolidone
NTRS	National Technology Roadmap for Semiconductors
O_2	oxygen
ORNL	Oak Ridge National Laboratory
PBL	polysilicon-buffered local oxidation of silicon
PB LOCOS	same as PBL
PBMS	particle beam mass spectrometer
PCB	printed circuit board
ppb	parts per billion

Acronyms and Abbreviations (continued)

ppt	parts per trillion
PTAB	Project Technical Advisory Board
QFP	quad flat pack
RAMP	Reliability Analysis and Modeling Program
rf	radio frequency
RIE	reactive ion etching
RTP	rapid thermal processing/process/processor
Sandia	Sandia National Laboratories
SAW	surface acoustic wave
SBFR	small-batch, fast-ramp
SC-1	standard clean 1
sec	second
SEM	scanning electron microscopy
SEMATECH	SEmiconductor MAnufacturing TECHnologies, Inc.
SEMI	Semiconductor Equipment Manufacturing Industry
SETEC	Semiconductor Equipment Technology Center
SiC	silicon carbide
Si_3N_4	silicon nitride
SIF	fluorosilylidyne
SiH_4	silane
SIMOX	Separation by IMplantation of OXygen
SiO_2	silicon dioxide
SIV	Sensors in Vacuum
SMIF	Standard Mechanical InterFace
SOI	Silicon On Insulator
SPI	Sofware Process Improvement
SUNY	State University of New York
SVG	Silicon Valley Group
SVGL	Silicon Valley Group Lithography Systems, Inc.
TAB	tape-automated bonding
TCP	tape carrier package
TEM	transmission electron microscope
TEOS	tetraethelorthosilicate
TMAH	tetramethylammonium hydroxide
TXRF	total x-ray fluorescence
W	watt
WFO	Work for Others
2-D	two-dimensional
3-D	three-dimensional

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SETEC/Semiconductor Manufacturing Technologies Program: 1999 Annual and Final Report

1 Executive Summary

This report summarizes work performed on five projects during the seventh year of a Cooperative Research and Development Agreement (CRADA) between Sandia National Laboratories (Sandia) and SEMATECH. The five projects employed a wide variety of resources from within Sandia and support from several universities. Funding for each project during the year ranged from $160,000 to $440,000. A project was considered small if funding was less than $250,000 and medium if the funding was over that amount. This report also provides historical information about the CRADA and all other projects that were completed over the lifetime of the CRADA.

The report is divided into four sections. Section 1 contains executive summaries of the five projects in calendar year (CY) 1999 that were performed for the Semiconductor Equipment Technology Center (SETEC), and also an overview of the overall program. Detailed descriptions of the projects are given in Section 2, following the same order of presentation as in the first section. Section 3 gives a short history of the seven-year CRADA. A synopsis of the projects completed from 1993 through 1998 under the CRADA is provided in Section 4. Note that works cited in text for all projects are listed numerically in the References section at the back of the report.

SETEC projects developed and tested new equipment and technologies for semiconductor manufacturing. Topics for CY 1999 included annealing-process modeling, linewidth reference materials, assembly test chips, equipment models for plasma and thermal processing, and reduction of wafer defects.

1.1 Numerical/Experimental Characterization of the Growth of Single-Crystal Calcium Fluoride (CaF_2)

The next two generations of lithography exposure tools will most likely use 193 nanometer (nm) and 157 nm illumination, respectively. At 193 nm, fused silica exhibits some undesirable characteristics, including compaction and increased bulk absorptivity, relative to 248 nm. Compaction is the densification of the bulk material, which alters the optical characteristics. One possible alternative to fused silica for high-fluence elements in 193 nm tools is CaF_2. Being crystalline, CaF_2 does not exhibit compaction. The bulk absorptivity of CaF_2 is also significantly less than that of fused silica at 193 nm. An additional benefit of CaF_2 is that its thermal conductivity is approximately eight times larger than fused silica. An increased thermal conductivity has been shown to reduce the thermally induced aberrations, which result from the absorption of illumination power. At

157 nm, fused silica is essentially opaque and CaF_2 is the material of choice for lens elements.

One of the issues limiting the use of CaF_2 in modern large lithography lenses is the residual stress-induced birefringence that results from the manufacturing process. Current manufacturing practices result in birefringence of approximately 5–6 nm/cm for large single crystals. The desired specification is less than 1 nm/cm for the 193 and 157 nm lithographic applications. Smaller crystals have been successfully made to the tighter specification.

State-of-the-art modeling has been applied to study the annealing process used to manufacture CaF_2. As a result of this effort, a clear understanding has been gained of the material response during annealing and has led to the development of furnace modifications and operational changes, which should reduce birefringence by an order of magnitude.

1.2 The Use of HRTEM Imaging for Certifying Critical-Dimension Reference Materials Fabricated with Silicon Micromachining

The International Technology Roadmap for Semiconductors (ITRS) has called for metrology reference materials to meet the requirements of current- and future-generation integrated circuit (IC) technologies [1]. With this objective, electrical test structures in silicon have been generated that provide correlation between electrical, critical-dimension (CD) linewidth measurements and the atomic lattice spacing, a known physical constant. The design for electrical CD test structures, oriented with respect to the silicon lattice, was provided by the National Institute of Standards and Technologies (NIST) and implemented by Sandia. The test structures were fabricated at Sandia's Microelectronics Development Laboratory (MDL) in (110) Silicon-On-Insulator (SOI) material, using bulk micromachining techniques. Patterned (110) silicon was etched with potassium hydroxide (KOH), resulting in linewidth structures with vertical sidewalls and a consistent sample width. The test structures were then electrically characterized at NIST and physically characterized at the Integrated Materials Research Laboratory (IMRL) at Sandia by high-resolution transmission-electron-microscopy (HRTEM) imaging of the silicon lattice.

1.3 Assembly Test Chip for Flip Chip on Board

The Assembly Test Chip (ATC) for Flip Chip on Board (FCOB) project is a continuation of the ATC for Ball Grid Array/Direct Chip Attach project. This work focused on the development of test vehicles for demonstration of high-input/output (I/O) flip chips on organic substrates that use nonreinforced epoxy "build-up" layers over conventional glass-reinforced printed circuit boards (PCBs). These high-circuit-density boards contain "micro-vias" that are fabricated into the build-up layers using photolithographic and laser-ablating techniques. The ATC4.2/3 and ATC4.4/5 stress-measurement test vehicles on 250 and 150 μm pitch, respectively, were designed, fabricated, and assembled to

concurrently designed micro-via build-up layer BGA substrates that were supplied by various contributing members of the Interconnection Technology Research Institute (ITRI). Parts were assembled by Celestica and Universal Instruments and underwent stress and life testing at Auburn University and Sandia. Experimental measurements of mechanical deformation were compared to analytical and high-fidelity finite-element-method (FEM) thermomechanical calculations. These results were used to better understand the different classes of mechanical failure observed during stress testing.

1.4 Plasma Mechanism Validation: Modeling and Experimentation

Detailed chemical-reaction mechanisms have been developed for the hexafluoroethane (C_2F_6) and trifluoromethane (CHF_3) plasma etching of silicon dioxide. There is good overall agreement between computational simulations using these mechanisms and a large set of experimental measurements, including etch rates, electron densities, negative ion densities, and fluoromethylidyne (CF), difluoromethylene (CF_2) and fluorosilylidyne (SiF) relative densities in three different plasma reactors. Validated mechanisms improve confidence in the plasma models, which in turn will allow simulations to be used in future reactor designs and process improvements.

1.5 Model-Based Reduction of Contamination in Gate-Quality Nitride Reactor

In partnership with SEMATECH, Sandia is applying numerical modeling to predict the formation and transport of contaminants in semiconductor manufacturing processes, thereby reducing defect production. The system chosen as an application project for the year was Applied Materials' Centura nitride reactor. By combining Sandia's capability for simulating particle transport in chambers with MicroTherm LLC's experimental expertise on measuring particle concentrations at low pressure, improvements to the particle performance of the reactor are being generated and the numerical models employed for the study are being validated against the empirical data. Currently, the numerical model has been constructed and the equipment for measuring particle concentration is being installed at SEMATECH.

1.6 Overview of the Sandia/SEMATECH Relationship

This seven-year CRADA resulted in the successful completion of 152 projects. Projects were selected by their relevance to Sandia's defense mission and to the National Technology Roadmap for Semiconductors (NTRS), which is now ITRS. Projects covered essentially every aspect of fabricating ICs. The program spent $110,750,000.00 of which $21,897,000.00 was funds-in to Sandia from SEMATECH, $35,178,000.00 was in-kind funds spent at SEMATECH, and the remaining $47,675,000.00 was Department of Energy (DOE) funds spent at Sandia.

2 Semiconductor Equipment Technology Center (SETEC)

The SETEC mission is to develop methods and tools for reducing the equipment design cycle, improving equipment reliability and control, and characterizing and evaluating equipment-processing capabilities. This section describes five SETEC projects performed in CY 1999. Four of the projects were small sized: Numerical/Experimental Characterization of the Growth of Single-Crystal Calcium Fluoride (CaF_2), The Use of HRTEM Imaging for Certifying Critical-Dimension Reference Materials Fabricated with Silicon Micromachining, Assembly Test Chip for Flip Chip on Board, and Model-Based Reduction of Contamination in Gate-Quality Nitride Reactor. One project was medium sized, Plasma Mechanism Validation: Modeling and Experimentation.

2.1 Numerical/Experimental Characterization of the Growth of Single-Crystal Calcium Fluoride (CaF_2)

Sandia Project Leader: S. Gianoulakis (505) 844-0450; SEMATECH Project Leader: C. Van Peski (512) 356-3330

• Objective

The objective of this project is to optimize the annealing process for large single crystals of CaF_2 using validated models. These crystals are most likely to be used as an alternative material to fused silica for the high-fluence lens elements in 193 nanometer (nm) lithographic steppers. CaF_2 does not compact in the same manner as fused silica, and its thermal conductivity is approximately eight times larger than fused silica. However, the use of CaF_2 in modern large lithography lenses has been limited because of residual stresses resulting from annealing of the crystals. Annealing is required to bring the crystal temperature down from the growth temperature to room temperature with minimum residual stresses. Such stresses can result in unacceptable levels of birefringence that degrade the optical performance of the lens. Current levels are 5–6 nm/cm. The required level of birefringence is approximately 1 nm/cm for lithographic applications, a specification that previously has been met only for smaller crystals (less than six inches in diameter). By developing a better annealing process, CaF_2 manufacturers may be able to fabricate large single crystals with residual birefringence to meet the tighter specification.

• Approach

Historically, the development of anneal processes for CaF_2 has been accomplished by empirical testing. This approach is somewhat impractical due to the long cycle time to grow and anneal a crystal (up to six weeks). Also, this approach does not provide any information as to what the crystal experienced during the process. Only the final state can be examined and history has to be inferred. To provide detailed information of what the crystal experienced during annealing, a thermal-mechanical finite element model was

developed. This model predicts the temporal and spatial temperature, stress, and strain distributions during the entire annealing process. The model also predicts the birefringence distribution based on the state of the residual stress.

The model used a one-way coupled approach to estimate the response of the crystal. First, the thermal response was computed, and then the temperature data was used to compute the stresses within the crystal. This approach assumes that the mechanical response of the crystal does not appreciably impact the thermal response.

To compute the thermal response, a thermal model was used that includes all necessary furnace components, as well as the thermal characteristics of the crystal. The decision to include the entire furnace was made because the only known boundary condition was the total power dissipated in each heater as a function of time. It was also decided not to estimate boundary conditions within the furnace so that the size of the model could be minimized, as any optimized processes based on this type of model would be difficult to extend to the shop floor. Therefore, to compute the thermal response of the furnace and the crystal, the heat source within the furnace had to be determined first. Determining the heat source was accomplished by modeling the transfer of heat in the same way that electrons are transferred in an electrical current transfer model. With this approach, a detailed map of the power dissipation distribution was computed over the volume of each heater. The dissipation map was then scaled in time based on the proposed anneal cycle and used as the heat source within the furnace.

The thermal model also included heat conduction and radiation. The furnaces typically operate in a vacuum, and thus convection is not present. Power from the heater was transported to the crucible via radiation and then conducted to the crystal. The semi-transparent nature of CaF_2 was also included in the model. The important data from the thermal model was the temporal and spatial temperature distributions within the crystal. The temperature gradients within the crystal are responsible for the formation of thermal stresses. If the crystal could be annealed isothermally, then thermal stresses would not form. It is only in the presence of temperature variations that stresses can form.

Following computation of the thermal response, the temperature data was used to compute the transient stress distribution within the crystal. Only the crystal is included in the stress model. To predict the stresses that result from a temperature distribution, a material model is needed to relate the stresses to the thermal strains. The material model had to simulate the relaxation mechanisms within the crystal that control the mechanical response. When the localized stress within CaF_2 reaches a certain level, dislocations begin to move to relieve the stresses back to the critical level. This critical stress level is temperature dependent. In fact, the critical stress drops to approximately 10% of its room temperature value when the crystal reaches 200°C. A practical approach to simulate dislocation is to use a thermal-elastic-plastic model. To populate the material model, temperature-dependent data such as the elastic modulus, plastic modulus, and yield stress had to be measured. **Figure 1** shows schematically the temperature dependence of critical stress of CaF_2. The objective of the anneal process optimization is to determine a method such that the peak stress within the crystal never exceeds the critical stress. This may not be practical but one should attempt to minimize the time that the peak stress is above the

critical stress. The reason for keeping the stress below the critical stress is that plastic deformations will occur when the stresses are above this level. It is plastic deformation that results in residual stresses, which manifest as birefringence.

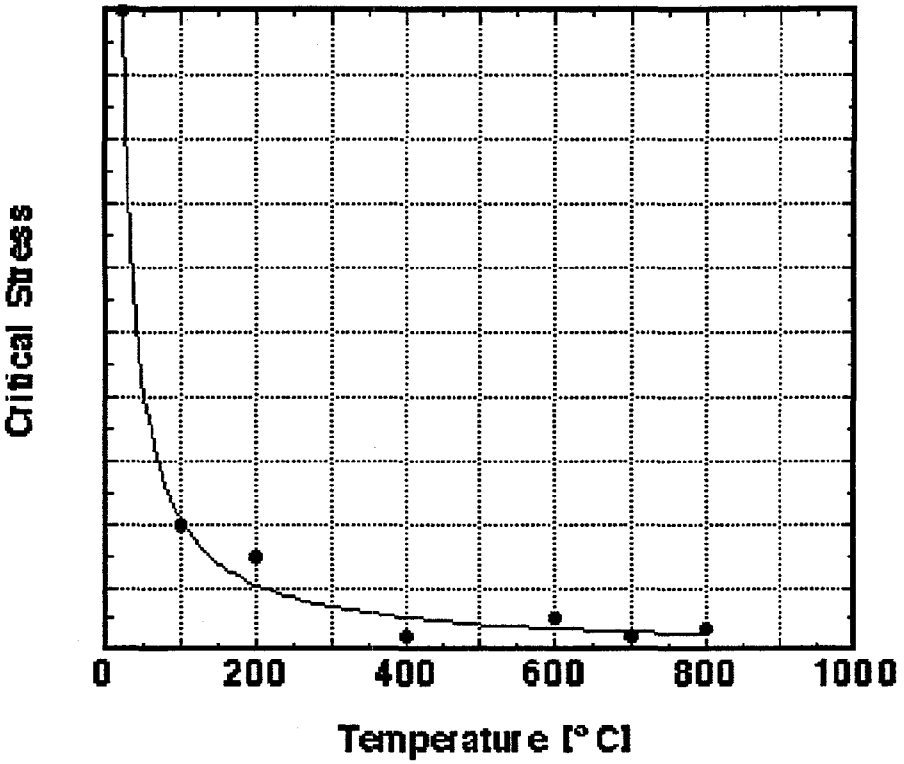

Figure 1. Critical stress vs. temperature for CaF_2. Symbols are data and the curve is a model line fit.

• Status/Results

This program was designed to support the individual CaF_2 manufacturers by examining their specific equipment, material, and processes. Therefore, the equipment-specific input to the models (geometry), boundary conditions (anneal cycles), and material properties are proprietary and cannot be discussed in this report. The following is a list of the participating CaF_2 manufacturers and contacts where additional information may be solicited:

Corning, North Brookfield	Rob Sparrow	(508) 867-6444
Bicron	Mike Mendicino	(440) 349-6960
Schott ML	Christoph Berndhaeuser	49(0) 613166-7283

As previously mentioned, the objective of this program was to reduce the birefringence in CaF_2 crystals from the current 5–6 nm/cm to less than 1 nm/cm. The models described above were applied to current furnace designs to determine whether the birefringence could be reduced with operational changes or whether hardware modifications were needed. The conclusion was that a combination of both operational changes and hardware

modifications was needed to control the response of the crystal during annealing and minimize the stresses. **Figure 2** compares the birefringence distribution in a crystal using existing processes with that using a modified furnace design. From this figure it can be seen that the birefringence has been reduced by over an order of magnitude to well below the specified level. Furnaces with these design modifications are currently being fabricated and should be online shortly.

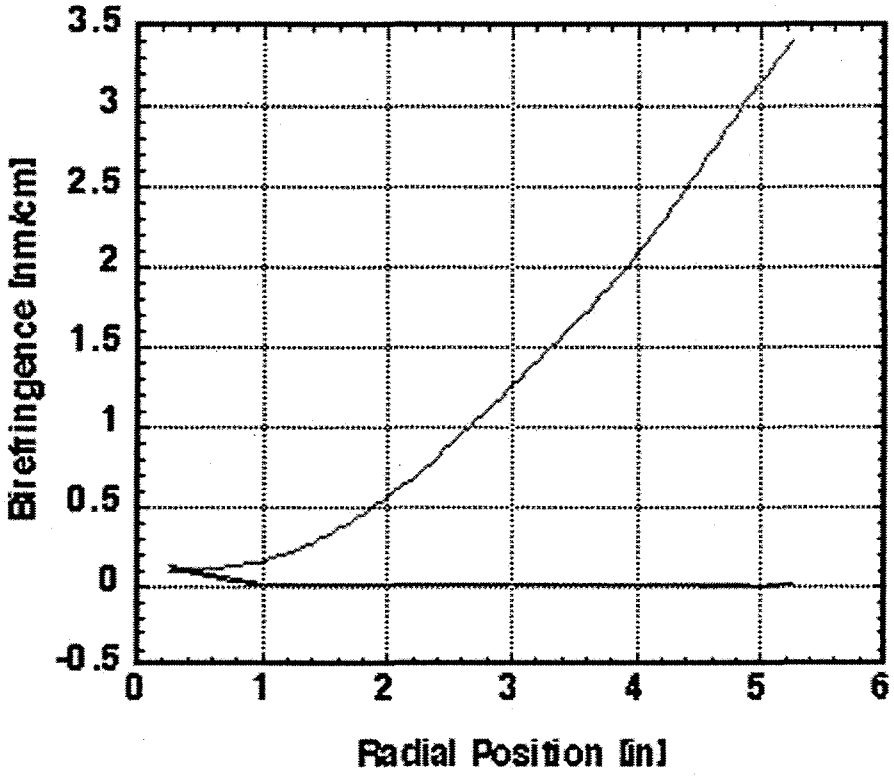

Figure 2. Birefringence vs. radial position predictions for a typical 12-inch CaF_2 furnace. The high-slope prediction curve (red) matches well with real furnaces. The flat curve (blue) suggests ways to improve the furnace.

• Benefits/Impact

High-volume production of single-crystal CaF_2 that meets the birefringence specification is considered critical to the success of 193 nm exposure tools and is an enabling technology for 157 nm lithography. Without CaF_2, 193 nm tools have to operate at a reduced power level to minimize the effects of compaction on the material. This has a significant impact on throughput and thus the cost of ownership. The lack of a robust supply of quality CaF_2 would effectively prevent the insertion of 157 nm lithography. This project has identified the cause of excessive stresses in CaF_2 and developed solutions that are currently being implemented. Once these furnace changes are proven, then anneal-induced birefringence should no longer affect the yield of CaF_2.

2.2 The Use of HRTEM Imaging for Certifying Critical-Dimension Reference Materials Fabricated with Silicon Micromachining

NIST Project Leader: M. W. Cresswell (301) 975-2072: Sandia Project Leader: S. Everist (505) 844-0023; SEMATECH Project Leader: H. Bogardus (512) 356-3456; Other Participants: R. A. Allen, L. W. Linholm, R. N. Ghoshtagore, and N. Guillaume (NIST); T. Headley, D. Renninger, C. Reber, D. Rieger, J. Wendt, P. Shea, P. Chavez, and P. Maldonado (Sandia)

• Objective

The objective of this project was to demonstrate the fabrication and certification of sub-0.18 μm reference-feature critical dimensions (CDs) in silicon by generating traceability to the known atomic lattice spacing using electrical test-structure metrology and high-resolution transmission electron microscopy (HRTEM). Feature sizes were targeted with linewidths greater than or equal to 0.10 μm.

• Approach

The approach to meet these objectives consisted of five tasks:

1. Obtain Silicon-On-Insulator (SOI) material
2. Develop alternative, nonlithographic procedures to reduce linewidths
3. Evaluate these alternative nonlithographic methods in SOI
4. Evaluate a hybrid ebeam/optical lithographic methodology to produce sub-0.18 μm features
5. Generate fully processed samples and evaluate them with standard electrical test methodology and HRTEM

A potential industry partner was also identified and invited to participate in technology and problem-solving issues.

• Status/Results

The National Institute of Standards and Technology (NIST) provided the starting material, which consisted of (110) Separation by IMplantation of OXygen (SIMOX) and Bonded Etched-back Silicon-on-Insulator (BESOI). NIST also provided the designs for reticles that corresponded to (110) SIMOX and BESOI orientations and that could be used in a hybrid process consisting of both e-beam and optical lithography.

Two fabrication process methodologies were developed to reduce linewidths by nonlithographic methods. Bulk (100) silicon, which forms 54.737° sidewalls when etched in KOH (potassium hydroxide), was used as the starting material for developing these methodologies. In the first methodology, 500 nm of amorphous polysilicon was deposited over 60 nm of thermal oxide. The polysilicon was photo-patterned, etched, and stripped

of resist. Exposed polysilicon lines were re-etched in an isotropic chemical etch to reduce the feature size. The underlying oxide was wet-etched, stopping on silicon, with the polysilicon functioning as a *hard mask*. The remaining oxide features were subsequently used as a hard mask to define features in the bulk silicon. The linewidth was reduced by as much as 80% (see **Figure 3**).

In the second methodology, a 50 nm layer of nitride was deposited, followed by a 350 nm layer of deposited oxide. The deposited oxide was patterned using a photomask with a gradient of pitch sizes ranging from 1.0 to 4.0 μm, and etched with reactive ion etching (RIE). Conformal oxide, 350 nm, was deposited over the patterned oxide lines, and oxide spacers were formed by RIE, resulting in a narrowed space between the original patterned lines. The spaces were filled with 300 nm of deposited, amorphous polysilicon. After chemical-mechanical polishing (CMP) of the polysilicon, and a wet oxide etch, a polysilicon plug remained in the formerly open space. As in the previous method, the oxide was removed by a wet etch. The polysilicon plug was used as a hard mask for the underlying nitride. The remaining nitride features were subsequently used as a hard mask to define features in the bulk silicon. Reduced linewidths were obtained (see **Figure 4**). Production of sub-0.25 μm features by nonlithographic methods was demonstrated in bulk (100) silicon.

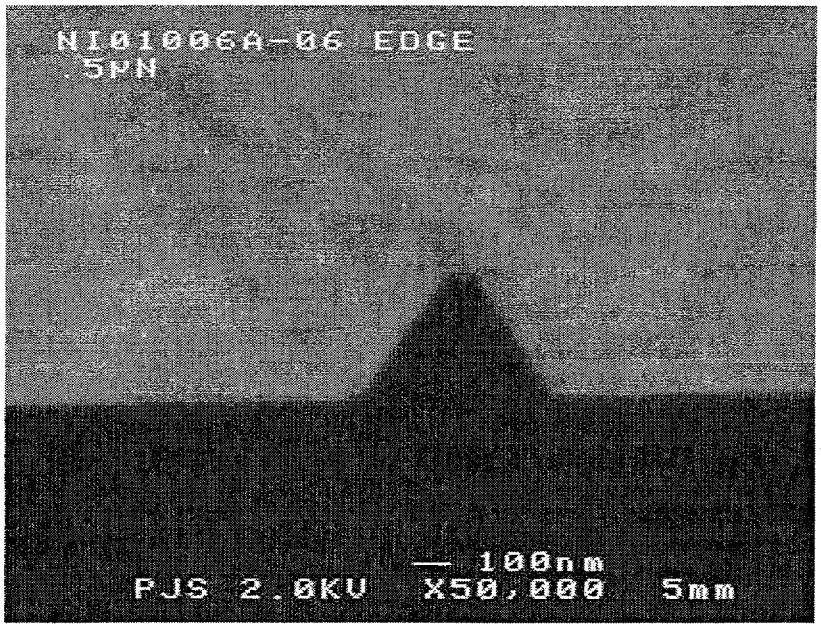

Figure 3. SEM of KOH-etched (100) silicon. The hard mask, still in place, was a 0.5 μm polysilicon line over oxide, reduced to ~ 0.1 μm by RIE and wet etching.

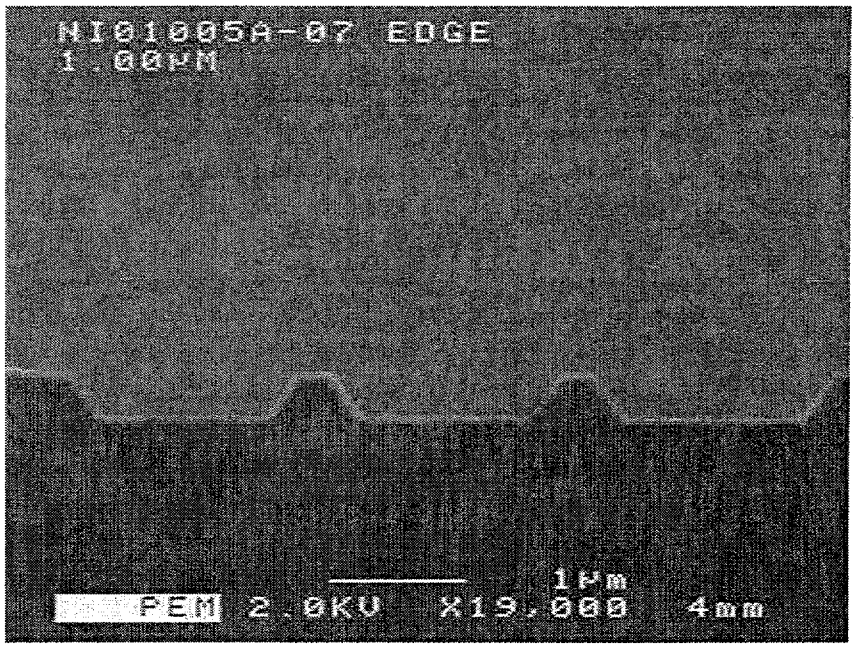

Figure 4. SEM of KOH-etched (100) silicon. The hard mask, which has been removed, was a filled space between an oxide line with an oxide spacer. The original 1.0 µm space was reduced to ~ 0.25 µm.

Feasibility was established for a hybrid direct-write ebeam/optical lithography process. A methodology for performing the mix-and-match optical/ebeam lithography process was developed. Samples in bulk silicon were prepared, and the initial optical lithography and patterning were performed. Due to the demonstration of reduced feature linewidths solely from optical lithography and KOH etching of silicon, hybrid ebeam/optical lithography processing was not further pursued.

Fabrication of electrical CD reference structures, patterned in the active silicon layer of SOI material and aligned to the silicon lattice, has been previously demonstrated in an earlier phase of this project. As part of the current year's project, arrays of the test structures were fabricated on (110) SIMOX and BESOI substrates. The active silicon layer was patterned with standard bulk-micromachining techniques, resulting in reference features with vertical sidewalls.

Unresolved process issues include unetched silicon, which remained on the SOI insulating oxide after KOH etching (see **Figure 5**), and pitting of the silicon sidewalls, which was observed by scanning electron microscopy (SEM) and HRTEM (see **Figure 6**) after fabrication completion. Although cosmetically undesirable, the unetched silicon did not affect electrical functionality of the test structures. Longer etch times in KOH reduced the features to an undesirable size but did not remove the unetched silicon. Using tetramethylammonium hydroxide (TMAH), NIST was able to remove the excess silicon. NIST also used TMAH to clean up the sidewall pitting, which was observed in BESOI but not SIMOX material.

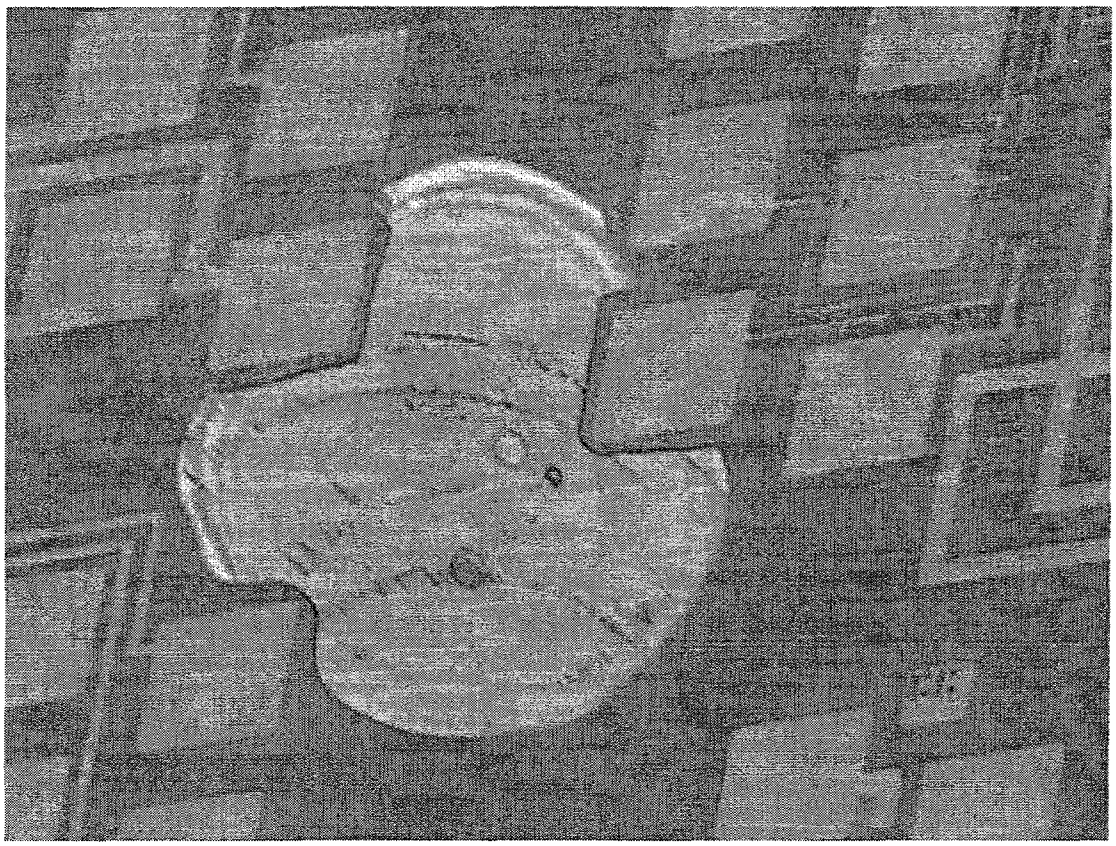

Figure 5. Patterned features and unetched silicon after KOH etching of (110) BESOI material.

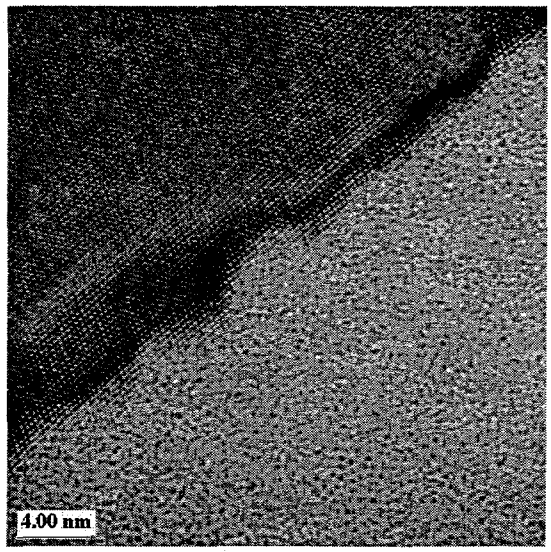

Figure 6. HRTEM image of a (110) BESOI 0.5 μm line with a pitted sidewall. The upper left portion of the figure shows the silicon lattice, while the lower right portion shows the oxide overlayer deposited as part of the HRTEM sample preparation.

Linewidth measurements of the CD reference structures were performed at NIST by standard electrical methods. Following electrical testing, HRTEM was used to image lattice planes of features in the active silicon layer in the SIMOX samples and in previously fabricated BESOI samples. A methodology was developed to prepare the (110) SIMOX and BESOI samples for HRTEM. Deposition of an oxide overlayer was performed to ensure sidewall protection of the silicon lines during final ion milling. This overlayer was polished down to a depth into the silicon lines to planarize, and a 2 mm x 2 mm square, centered on the linewidth structure, was diced from the die. The 2 mm x 2 mm square was dimpled, polished, and ion-milled from the back until a hole formed adjacent to the line of interest. It was then ion-milled from both front and back until the line was suitably thin for plan-view HRTEM.

Techniques for HRTEM imaging, processing, and analysis for lattice-plane counting were developed, resulting in the measurement of lattice planes across the drawn 0.75 μm line in (110) SIMOX (see **Figure 7**) and the 0.5 μm and 1.0 μm lines in (110) BESOI. In the transmission electron microscope (TEM), the target (110) silicon line was oriented so that the HRTEM image contained only the set of {111} lattice fringes lying parallel to the line length. The HRTEM image was captured on a negative at a magnification that allowed the full linewidth within the frame of the negative. A slice of the image across the line width was scanned from the negative at 3000 dpi, reproducing the lattice fringes at sufficient clarity for subsequent image processing and analysis. The scanned image was imported into the National Institutes of Health (NIH) Image software, and black fiducial lines were drawn and numbered on the image at appropriate spacing across the full linewidth. A 20- or 30-pixel-wide portion of the image between each pair of fiducial lines was selected, as shown in **Figure 8**, and the integrated plot profile was generated, as shown in **Figure 9**. The number of peaks corresponding to the number of lattice fringes between fiducial marks was counted for each profile and summed over the total linewidth. The total line-width was then calculated as (total no. lattice spacings) x (0.31356006 nm/lattice spacing) = total linewidth in nm.

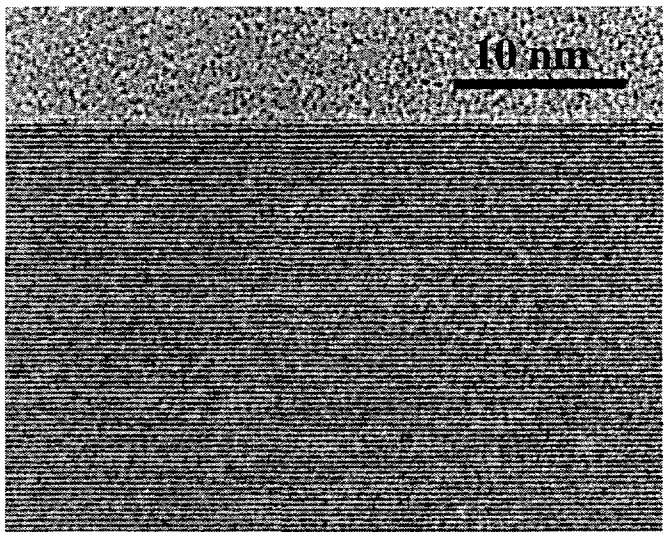

Figure 7. HRTEM image of a single set of {111}-lattice fringes, taken from a (110) SIMOX 0.6 μm line.

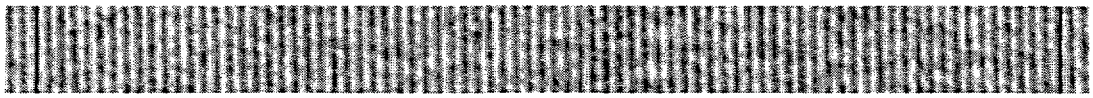

Figure 8. HRTEM partial image of a 3000 dpi scan with fiducial lines, taken from a (110) BESOI 0.5 μm line.

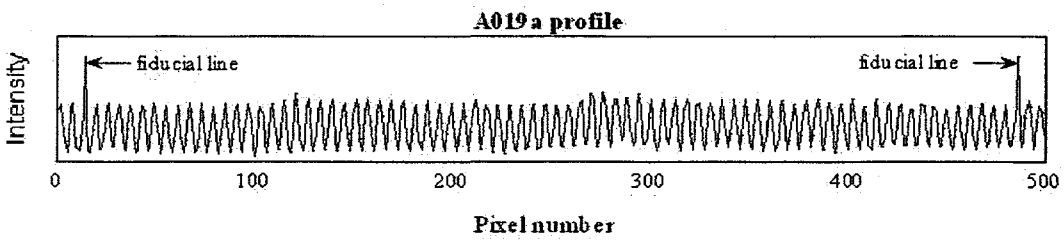

Figure 9. Integrated plot profile of Figure 7.

Lattice-plane counts were completed on drawn 0.75 μm lines in SIMOX and 0.5 μm and on 1.0 μm lines in BESOI samples. HRTEM images were taken in plan view of the lines. Since the lines from BESOI material showed pitting attack at the sidewalls, measurements were made to avoid the etchpits. This was done by selecting two different points along each line and measuring from what was perceived to be the outermost surfaces. A different number of lattice planes was obtained for the two measurements for each sample, and it was assumed that the larger number was more likely to represent the original width prior to any planes being removed from processing-induced pitting.

Papers on this work were written for the Spring SPIE Microlithography Symposium [2] and for the March IEEE/ICMTS Conference [3]. Other published documentation on this work is also included at the end of this report [4-6].

• Benefits/Impact

Although the current generation of IC technologies is at 0.18 μm and below, metrology reference features at sub-0.50 μm are not readily available. Low-cost, sub-0.18 μm, NIST-traceable CD reference materials are intended to meet this need. Statistical correlation between electrical results on 100% of the reference features and HRTEM measurements of a smaller sample of reference features will provide traceable reference materials to industry at a reasonable cost.

Sandia was able to provide a unique set of capabilities, combining design layout, test structure fabrication, packaging, SEM, and HRTEM analysis. The methodology for the fabrication of electrical CD reference structures in SOI by bulk micromachining has been established. Fabrication of sub-0.18 μm structures was demonstrated. Methodologies for HRTEM sample preparation and measurement of submicrometer structures on SOI were developed and demonstrated on features greater than or equal to 0.5 μm. More work is needed to demonstrate HRTEM sample preparation and analysis of sub-0.5 μm features.

With the intent of facilitating a technology-transfer process, NIST and SEMATECH have participated in a series of meetings with VLSI Standards. The meetings have resulted in plans for a parallel wafer-processing activity by an independent laboratory working under contract to VLSI Standards. This contractor will use the same NIST-provided BESOI starting material but will employ oxide hard masking and pattern delineation by TMAH instead of the baseline nitride hard-mask/KOH etching used at Sandia. A simplified test-chip layout, oriented towards application rather than research, was designed and provided to the commercialization partner.

2.3 Assembly Test Chip for Flip Chip on Board

Sandia Project Leader: D. Peterson (505) 844-6009; SEMATECH Project Leaders: B. Werner (512) 356-7543, E. Sorongon (512) 356-3528, and J. DeRosa (512) 356-3075; Other Participants: J. Sweet, M. Tuck, R. Mitchell, and S. Burchett (Sandia)

• Objective

The major objective of this project was to develop a family of common test vehicles that can be married with appropriate organic substrates, including ball-grid arrays (BGAs), to facilitate the assessment of underfill materials and processes as well as the thermomechanical and electrical performance of assembled devices. A secondary objective was the correlation of thermomechanical measurement data resulting from these activities to computer models for the purpose of identifying and characterizing tools that would be most useful to the member companies in the development of packaging technology and for the control of manufacturing processes.

• Approach, Status, and Results

Sandia followed the same approach to test-vehicle design, construction, and validation that was used in previous years. This year's work is a continuation of this approach for new designs. During calendar year (CY) 1999, the work consisted of two main task areas: supporting design of the ATC4.2, 4.2/3 and 4.4/5 test chips, and reliability testing of the ATC4.2/3 test chip. A description of these tasks and their associated activities and results follows. Additional information on the ATC4.2 test chip can be found in the references cited at the end of this report [7, 8].

— ATC4.2 Design

A flip-chip stress-measurement test chip was fabricated by redistributing the perimeter input/output (I/O) pads of the existing ATC04 test chip into an area array of 975 eutectic solder bumps on 250 μm pitch. The redistribution and bumping of Sandia-supplied 150 mm quartz demonstration wafers and silicon wafers, which contained active circuits, were done both by Aptos Corporation using a copper-polyimide process and by Flip Chip Technologies using a copper-benzocyclobutene process. A matching substrate was designed by Zukan-Redac and fabricated in development quantities for board-level environmental testing. Sandia coordinated

testing at the Naval Surface Warfare Center in Crane and the University of Maryland Electronic Packaging Center.

— ATC4.2/3 Design

A second 250 µm pitch-redistribution design for the ATC04 was completed at Sandia that improved interconnect routability at the substrate level. This design used the "clamshell" approach described by Intel at the 44th Electronics Components and Technology Conference. The design variant intended for redistribution of active circuitry on the ATC04 die was identified as the ATC4.2, and a passive daisy-chain complementary design for use on unpatterned wafers was identified as the ATC4.3. Quartz and silicon wafers were redistributed and solder-bumped by Aptos and Flip Chip Technologies, and organic substrates were fabricated by Merix, MMS, Ormet, Altron, Sheldahl, Hadco, and IBM using a clamshell board design laid out by Zukan-Redac. Flip-chip assembly of ATC4.2 and ATC4.3 parts was accomplished by Celestica using a test matrix of underfill materials identified by the SEMATECH Underfill Interfacial Integrity Enhancement Project Technical Advisory Board (PTAB) and substrates provided by the SEMATECH BGA Substrate PTAB and Interconnection Technology Research Institute (ITRI) Chip Carrier Team.

— ATC4.2/3 Reliability Testing

ATC4.3 BGA assemblies were surface-mounted to test boards fabricated by Altron. These assembled units were tested at Sandia for electrical continuity and at Auburn University for environmental robustness. ATC4.2 BGA assemblies in nine experimental groups underwent thermal cycle testing at National Semiconductor, with periodic electrical testing at Sandia up to a total of 2500 temperature cycles between – 40 and +125°C. Sandia performed extensive failure analysis on these parts and used the results of thermomechanical stress modeling to better understand the three principle failure modes of die cracking, edge delamination, and underfill-fillet radial cracking.

— ATC4.4/5 Design

A 150 µm pitch test-vehicle was designed and fabricated at Sandia. This device contained 2104 flip-chip connections on a 150 µm pitch 77 x 77 array. Since the micro-via build-up infrastructure was not capable of fully routing to this density, a partially routed design was developed to provide access to daisy chains, heaters, ring oscillators, and stress-measurement circuitry. This design used a 35 mm BGA substrate containing a 34 x 34 array of solder connections on 1.0 mm pitch with a depopulated center for a total of 960 I/Os. Fujitsu fabricated substrates and ATC4.4 and ATC4.5 die were flip-chip–assembled to these substrates by Universal Instruments using two of the three experimental underfills that were being evaluated in the ATC4.2/3 reliability test. These devices were subsequently electrically tested by Sandia but did not undergo reliability testing because the project was terminated.

• Benefits/Impact

For SEMATECH member companies, this project has provided access to active and passive 250 and 150 μm flip-chip, BGA, integrated test vehicles for use in internal and shared experiments. In addition, the project has enabled solder-bump and substrate build-up process development to meet the 2001 NTRS requirements. For Sandia's Defense Programs, the test-vehicle development process has provided valuable experimental validation of Sandia's Accelerated Strategic Computing Initiative (ASCI) computational tools, which will be used in the simulation of nuclear events and has provided important information for packaging future microsystems.

2.4 Plasma Mechanism Validation: Modeling and Experimentation

Sandia Project Leaders: J. Johannes (505) 844-1994 and P. Ho (505) 844-3759, Modeling Task, and G. Hebner (505) 844-6831, Diagnostics Task; SEMATECH Project Leader: P. Ryan (865) 574-1133; Other Participants: R. Buss (Sandia)

• Objective

The purpose of this work is to develop and validate detailed chemical-reaction mechanisms for the hexafluoroethane (C_2F_6) and trifluoromethane (CHF_3) plasma etching of silicon dioxide. These mechanisms are based on independently determined physical and chemical parameters, within the limits of the cross section and chemical kinetic data available in the literature. The use of fundamentals-based mechanisms, validated with a variety of experimental measurements, should lead to predictive computational models of these plasma processes.

• Approach/Status/Results

The project's approach is to combine available fundamental chemical data, diagnostic data, and plasma modeling to develop predictive chemical mechanisms and models validated with data from commercial reactors. This project is part of a larger project in which other researchers are carrying out cross-section determinations and a host of experimental measurements. The experiments done at Sandia are described in this section; the work at other institutions is not covered here. The modeling work described is a continuation of work done in previous years; further model and mechanism validation continued this year using detailed diagnostic data and etch rates taken on Gaseous Electronics Conference (GEC) research reactors at Sandia, the University of New Mexico, and the State University of New York (SUNY) for C_2F_6 and/or CHF_3 plasmas. Simulations were performed to validate the mechanisms and improve them where necessary. In addition, oxide etch-rate data taken on these research reactors and a Lam 9100 commercial reactor were compared to zero-dimensional model predictions.

— Modeling Task

Version 1 of the reaction mechanism for C_2F_6 plasma etching of blanket oxide was formally released on May 12, 1999, and Version 2 on September 10, 1999. Version 1 of the CHF_3 reaction mechanism was also delivered on September 10, 1999. The CHF_3 reaction mechanism is based on Version 2 of the C_2F_6 mechanism. The mechanisms are in the form of input files for CHEMKIN and Surface-CHEMKIN, and include information on the sources of the kinetic data used. The mechanisms are sizable: the gas-phase part of the C_2F_6 mechanism involves 28 species and 132 reactions, while the surface part involves 2 materials, 6 species, and 85 reactions. The mechanisms are not given here because of their size, but have been transferred to SEMATECH and will be published in the open literature.

The results of comparisons between model and experiment for C_2F_6 plasmas are summarized in **Table 1** for etch rate data and **Table 2** for diagnostic measurements. The overall agreement between the model predictions and the large body of experimental data is very good, but imperfect. In general, worse fits to any individual data set were accepted in order to get a better overall fit to the entire set of data. If good agreement (✔) is scored as 3 points, okay agreement (**O**) is scored as 2 points, and poor agreement (✖) is scored as 1 point, the average is a very favorable 2.6. The details of these comparisons, including figures, will be published separately in the open literature.

The results of a smaller set of comparisons between model and experiment for CHF_3 plasmas are summarized in **Table 3** for both etch rates and diagnostic measurements. The overall agreement between the model predictions and the large body of experimental data is again good, but imperfect. If the scoring system discussed above is followed, the average in this case is slightly lower value at 2.5.

Table 1. Summary of Model Comparisons to Etch Rate Data for C_2F_6 Plasmas

Reactor	Parameter Varied	Direction of Trend	Magnitude of Trend	Absolute Number	Comments
Lam	Overall	✔	✔	✔	
Lam	flow rate	✔	O	✔	
Lam	bias power	✔	✔	✔	
GEC	Overall	✔	✔	✔	
GEC	power	O	✔	✔	Trend sometimes correct, sometimes not.
GEC	pressure	O	✔	✔	Trend sometimes correct, sometimes not.
GEC	bias power	✔	✔	✔	
SUNY	Overall	✔	O	✔	Pressure dependence off.
SUNY	power	✔	✔	✔	
SUNY	pressure	O	O	✔	Model has peak, too steep.
SUNY	flow rate	✔	O	✔	Model too shallow.
SUNY	bias voltage	✔	✔	✔	Model too shallow.

✔ = Good, **O** = Okay, ✖ = Poor

Table 2. Summary of Model Comparisons to Diagnostic Data for C_2F_6 Plasmas

Reactor	Species	Parameter Varied	Direction of Trend	Magnitude of Trend	Absolute Number	Comments
GEC	e^-	power	O	✔	✔	Model flat at high power.
GEC	e^-	pressure	O	✔	✔	Model peaks at low pressure.
GEC	e^-	bias power	O	✔	✔	Experiment rises at high bias.
GEC	F^-	power	O	✖	✔	Model peaks at low power, not steep enough.
GEC	F^-	pressure	✔	✔	✔	
GEC	F^-	bias power	O	✔	✔	Experiment drops at high bias.
GEC	CF (LIF)	power	✔	✔	---	
GEC	CF (LIF)	pressure	O	✔	---	Model flat at high pressure.
GEC	CF (LIF)	bias power	✔	✔	---	
GEC	CF (LA)	power	✖	O	✖	Two experiments show opposite trends, model too high.
GEC	CF (LA)	pressure	✔	O	✖	Model too high, too steep.
GEC	CF_2 (LIF)	power	✔	O	---	Model too steep.
GEC	CF_2 (LIF)	pressure	✔	O	---	Model too steep.
GEC	CF_2 (LIF)	bias power	✔	✔	---	
GEC	CF_2 (LA)	power	✖	O	✔	Two experiments. show opposite trends, model too steep.
GEC	CF_2 (LA)	pressure	✔	O	✔	Model too steep.
GEC	CF_3 (LA)	power	O	O	✔	Model too steep.
GEC	CF_3 (LA)	pressure	✔	O	✔	Model too steep.
GEC	Gas Temp.	power	✔	✔	O	Model a bit low.
GEC	Gas Temp.	pressure	✔	✔	O	Model a bit low.
GEC	Gas Temp.	bias power	✖	✔	O	Experiment decreases with bias, model flat, low.
GEC	SiF (LIF)	power	✖	✔	---	Experiment up, model up then down.
GEC	SiF (LIF)	pressure	O	O	---	Model drops too much at high pressure.
GEC	SiF (LIF)	bias power	✔	✔	---	
GEC	SiF (LIF)	C_2F_6/O_2 MF	✔	✔	---	

Reactor	Species	Parameter Varied	Direction of Trend	Magnitude of Trend	Absolute Number	Comments
SUNY	ICD	power	✔	✔	✔	
SUNY	ICD	pressure	O	O	✔	Model has peak, too steep.
SUNY	ICD	flow rate	✔	O	✔	Model not as flat.

✔ = Good, O = Okay, ✖ = Poor,
LIF = laser-induced fluorescence, LA = laser absorption, ICD = ion current density, MF = mole fraction

Table 3. Summary of Model Comparisons to Etch Rate and Diagnostic Data for CHF_3 Plasmas

Reactor	Species	Parameter varied	Direction of trend	Magnitude of trend	Absolute number	Comments
GEC	e^-	power	O	O	✔	Model too flat at high power.
GEC	e^-	pressure	✔	O	✔	Model drops too much at low pressure.
GEC	e^-	bias power	O	✔	✔	Experiment rises at high bias.
GEC	F^-	power	✔	✖	✔	Model not steep enough.
GEC	F^-	pressure	✔	✔	✔	
GEC	F^-	bias power	✖	O	✔	Experiment drops at hi bias
GEC	CF (LIF)	power	O	✔	---	Model dips at low power; data noisy.
GEC	CF (LIF)	pressure	✔	✔	---	
GEC	CF (LIF)	bias power	O	✔	---	Model rises at low bias.
GEC	CF_2 (LIF)	power	✔	✔	---	
GEC	CF_2 (LIF)	pressure	✔	O	---	Model too steep.
GEC	CF_2 (LIF)	bias power	O	✔	---	Model rises at low bias.
GEC	SiF (LIF)	power	✖	✔	---	Experiment up then flat, model up then down.
GEC	SiF (LIF)	pressure	✔	O	---	Model too steep.
GEC	SiF (LIF)	bias power	O	✔	---	Experiment rises at high bias.
SUNY	Etch Rate	Overall	O	O	✔	
SUNY	Etch Rate	power	O	O	✔	
SUNY	Etch Rate	pressure	✖	✔	✔	
SUNY	Etch Rate	flow rate	✔	O	✔	

Reactor	Species	Parameter varied	Direction of trend	Magnitude of trend	Absolute number	Comments
SUNY	ICD	power	✔	✔	✔	
SUNY	ICD	pressure	O	O	✔	Model flat at high pressure.
SUNY	ICD	flow rate	O	O	✔	Model higher at low flow rather than lower, also too flat.

✔ = Good, O = Okay, ✖ = Poor
LIF = laser-induced fluorescence, LA = laser absorption, ICD = ion current density

— Experimental Measurements in Support of Validation Task

As part of the plasma diagnostic program, Sandia hosted visiting scientists from the University of New Mexico, the University of Wisconsin and Penn State University in our laboratory and also conducted our own measurements. The university work brought in visiting scientists to measure the line-integrated radical concentrations for fluoromethylidyne $(CF)_x$ gas-phase species using infrared (IR) absorption and mass spectroscopy. That work will be reported by those institutions. The Sandia work focused on microwave measurements of the electron and negative ion density as well as laser-induced fluorescence (LIF) of the spatial density distributions of CF, difluoromethylene (CF_2), and fluorosilylidyne (SiF). In addition, the rotational temperature was determined for CF and SiF.

In detail, LIF has been used to measure the rotational temperature of CF and SiF, as well as the relative CF, CF_2 and SiF density as a function of plasma reactor conditions. The rotational temperature of the CF is important since, in most cases, it strongly correlates with the gas temperature. The gas temperature is used to calculate the absolute density in the center of the plasma (Ideal gas law) and is an important part of the partition function to calculate the absolute density from the line-integrated diode-laser measurements. In C_2F_6, the CF temperature increased from 450 to 700 Kelvin (K) for inductively coupled plasma (ICP) powers of 100 to 300 watts (W), was constant at 600 K with changes in pressure from 5 to 20 mTorr, and decreased from 600 K to 500 K with an increase in bias power from 20 to 100 W. Measurements at both the center of the GEC chamber, r = 0 cm and r = 5 cm, yielded the same values to within the uncertainty in the measurement (about 50–75 K). Temperatures were calculated assuming fully saturated LIF transitions. These temperatures are higher than one might first expect based upon a wall temperature of 450 K and suggest that additional heating mechanisms are important. Similarly high temperatures and higher were observed for argon metastables, our previous measurements. For the case of argon metastables, the higher temperature was primarily attributed to charge-exchange-induced heating of the neutrals. Temperature measurements of SiF were in the 500 K range.

Spatially resolved LIF measurements of CF_2 showed that there is a large amount of CF_2 outside the measurement volume. In fact, the amount outside the glow region was at least three to five times larger than the volume within the glow region. More

than likely, this is a lower bound since we have not measured the CF_2 density all the way to the walls or windows. Within the glow region, the CF_2 density was fairly constant as a function of radial position in C_2F_6 and CHF_3. However, for octafluorocyclobutane (C_4F_8), the CF_2 density was strongly peaked in the center of the glow. The reason for the different spatial shapes is not currently known.

• Benefits/Impact

Successful comparison of simulation results to a wide range of experimental data helps in developing a robust chemical-reaction mechanism that can be applied to a variety of plasma reactors. Validated mechanisms improve confidence in the plasma models, which in turn will allow simulations to be used in future reactor designs and process improvements both for commercial and defense applications.

2.5 Model-Based Reduction of Contamination in Gate-Quality Nitride Reactor

Sandia Project Leaders: A. Geller (505) 844-7795; SEMATECH Project Leader: R. Worley (512) 356-3755; Other Participants: M. Louis (SEMATECH), D. Rader and R. Rao (MicroTherm, LLC)

• Objective

The goal of this project is to develop and apply analytic, computational, and experimental methods to predict the formation and transport of contaminants in semiconductor manufacturing processes, thereby reducing defect production. The ultimate purpose is to supply equipment designers with models for optimizing process conditions and developing tool designs that reduce defect formation by preventing contaminant generation or by isolating the wafer from contamination. General-purpose models are being developed to accept geometry, flow rates, chemistry, and environmental conditions as input and to provide local contaminant concentration, formation rates, deposition rates, and size distribution as output. During the last year, the application of the work was to the Applied Materials Centura platform configured with a reactor performing a silicon nitride deposition process. Although this project focuses on applying models to specific process tools, the models are flexible enough to be applicable to other tools as well.

• Approach

The approach taken in executing this project has three parts:

1. Apply the best-available numerical modeling techniques to understand particle transport in the Applied Materials Centura reactor using a SEMATECH nonproprietary recipe.
2. Apply novel particle-sampling methods to measure particle concentration and formation rate in the interior of the Applied Materials Centura nitride deposition chamber located at SEMATECH.

3. Combine the results of parts 1 and 2 above to improve the particle performance of the SEMATECH Centura tool and validate the results of the Sandia modeling effort. An essential component of this task is close cooperation among Sandia, SEMATECH, member companies, process equipment manufacturers, and universities.

• Status/Results

— Particle Transport Modeling

The Centura nitride-reactor chamber is a rotating-disk, cross-flow reactor. In this configuration, there are no symmetry planes or axes (such as the axis of symmetry in an Applied Materials 5000 chamber); so it is necessary to model the chamber in three dimensions. However, a number of simplifying assumptions may be made:

1) *Gas flow is incompressible, laminar, and steady.* Incompressibility is satisfied because gas velocities in the Centura reactor are much less than the speed of sound. At the low operating pressures typical of this tool, low gas densities result in low Reynolds numbers that are well within the laminar regime. Although the steady-flow assumption prevents extending the current analysis to process transients that affect the gas flow, such as pressure and/or flow changes, these varying conditions may be considered as a series of steps with as many steps along the transient modeled as a quasi-steady state.

2) *Variable gas properties.* Temperature-dependent variations in gas properties are allowed but pressure-dependent properties are excluded. This restriction is insignificant due to the low velocities in the chamber (see the first assumption). Temperature gradients will be used as a driving force for particle thermophoresis.

For the interior domain of the Centura nitride reactor, the governing equations for flow and temperature are the conservation of mass:

$$\nabla \cdot U = 0 \ , \tag{1}$$

conservation of momentum:

$$\rho\left(\frac{\partial U}{\partial t} + U \cdot \nabla U\right) = -\nabla P + \mu \nabla^2 U + \rho g \ , \tag{2}$$

and conservation of energy:

$$\rho C_p\left(\frac{\partial T}{\partial t} + U \cdot \nabla T\right) = k \nabla^2 T \ . \tag{3}$$

where U = fluid velocity vector (cm/sec), P = pressure (dynes/cm^2), ρ = fluid density (grams [g]/cm^3), μ = fluid viscosity (g/cm sec), g = gravitational acceleration (cm/sec^2), T is the fluid temperature, (K), C_p is the heat capacity of the gas at constant pressure (cm^2/sec^2/K), and k is the thermal conductivity (g-cm/sec^3/K). Because of the three-dimensional (3-D) nature of the problem, the vector notation is used for brevity; an expanded version of these equations in component form is available in

Bird *et al.*, 1960 [9]. Solving these equations will provide the fluid velocity and temperature fields, which are the basis for particle transport calculations.

To complete the problem specification, boundary conditions must be imposed. In treating the reactor, no-slip conditions are taken at all solid walls (i.e., on the quartz reactor top, wafer, chamber bottom, and sidewalls). For all surfaces except the wafer, this translates to zero velocity. For the wafer, the adjacent fluid is assumed to undergo pure rotational motion with rotation rate equal to that of the wafer and no radial and vertical velocity. Horizontal flow is assumed at the inlets, and zero traction is assumed at all outflows. The inlet flow rate, wafer rotation rate and wafer temperature are those specified in the SEMATECH operating recipe. Applied Materials provided the temperatures of the other surfaces.

The numerical method used for calculating the fluid velocity and temperature field is the commercial fluid dynamics analysis code FIDAP (Version 8, Fluid Dynamics International, Evanston, Illinois, USA). This general-purpose finite-element code allows steady-state or transient simulations of fluid and thermal transport in two-dimensional (2-D), 3-D, and axisymmetric geometries. The input for the numerical simulation, including the reactor geometry and boundary conditions, has been completed and preliminary calculations are currently being performed.

— Particle-Sampling Experiments

MicroTherm, LLC has been contracted to perform in situ particle monitoring of the Centura nitride system using a particle beam mass spectrometer (PBMS) on loan to this project from the University of Minnesota. The PBMS is being installed on SEMATECH's Applied Materials Centura nitride reactor, where it will be connected downstream of the chamber to permit in situ particle monitoring. MicroTherm is responsible for the following tasks related to this project:

1) Preparation of the University of Minnesota PBMS for field measurements
2) Transport of the University of Minnesota PBMS to SEMATECH
3) Installation of the PBMS at SEMATECH
4) Collection of representative particle data for baseline process recipes on the Applied Materials Centura reactor.
5) Analysis and reporting of particle-monitoring data to SEMATECH

MicroTherm, LLC has completed tasks 1 and 2 from the above list and is in the process of completing task 3 (awaiting final approval from SEMATECH to modify a gas cabinet to allow the final hook-up of the PBMS). As illustrated in **Figure 10**, the PBMS relies on electrical detection and sizing of particles. Installed downstream of the process tool, the PBMS samples gas flow from the process chamber through an aerodynamic focusing inlet fitted with aerodynamic lenses. Particles entrained in the flow are focused into a narrow beam (<1 mm), accelerated to high speeds, and injected with high transmission efficiency into a turbo-pumped detection chamber. Particles entering the detection stage are charged by electron impact using an electron

gun and then detected and sized in an electrostatic energy analyzer consisting of a 90° deflector, Faraday cup, and electrometer. Previous use of this instrument in the field had indicated that the PBMS suffered from problems such as poor beam alignment, short-lived electron emission filaments, etc. In preparing the University of Minnesota's portable PBMS for field measurements, MicroTherm has implemented several design improvements to address these issues:

- A newly designed long-life electron gun and energy analyzer unit has been designed, fabricated, installed, and tested using laboratory-generated calibration aerosols. The new electron gun enables the PBMS to be operated for long periods (several weeks) without replacement of the electron emission filament used for generating electrons in the electron gun.

- The particle-beam generation and shaping system was modified to ensure robust beam alignment. The modified design uses aerodynamic lenses that are locked into place and also a self aligning nozzle-skimmer system to achieve beam alignment without adjustment. The nozzle-skimmer system has also been designed to achieve adjustment-free alignment with downstream components such as the electron gun and the energy analyzer. The self-aligning design has been fabricated, installed, and tested successfully using calibration aerosols.

- A rack-mountable electrometer with pre-amplifier head was fabricated to replace a malfunctioning electrometer that was previously used for measuring the on-axis current of collected particles. The new electrometer is used to verify beam alignment during the initial PBMS setup.

These modifications will benefit this project by providing more reliable operation and more accurate data. The modifications are expected to benefit SEMATECH and its member companies in the future by providing a more robust and portable instrument for taking such measurements at member-company sites.

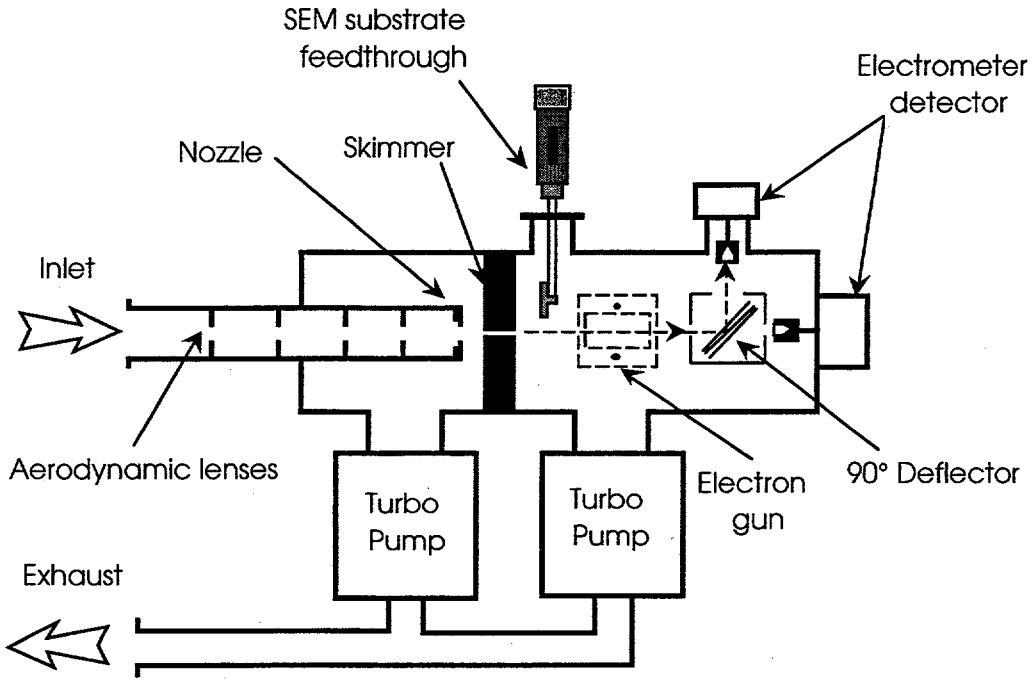

Figure 10. Schematic diagram of the particle beam mass spectrometer (PBMS).

• Benefits/Impact

The results of the work performed under this project benefit SEMATECH and the member companies in three ways. First, through the application of numerical and experimental methods, improved particle performance in the Applied Materials Centura reactor will be accomplished. Second, both modeling and experimental tools are being improved under this project and will be available to SEMATECH member companies. These improved capabilities will make further improvements in particle performance on the Centura and other reactors possible in the future. Third, fundamental understanding of particle generation and transport mechanisms is being uncovered through this research. This understanding will benefit Sandia and SEMATECH by allowing rapid improvements to a range of process equipment through application of generic guidelines not tied to a specific application.

This work is also applicable to defense program applications, such as radiation hard microelectronic processes. It also adds to the advance of creating complete simulation of plasma processing.

3 History of the Sandia/SEMATECH Relationship

This section highlights various aspects of the Sandia/SEMATECH relationship, with primary emphasis on the seven-year Cooperative Research and Development Agreement (CRADA) from 1993 through 2000. Topics addressed include the historical background of the relationship, reasons for partnering, level of effort, CRADA results, observations on the process, and future work and plans.

3.1 Background

SEMATECH was established in 1987 as a unique venture in cooperation between the U.S. government and the U.S. semiconductor industry. The goal of this new cooperative venture (**SE**miconductor **MA**nufacturing **TECH**nology, Inc.) was to help the United States regain a competitive position in semiconductor manufacturing. Thirteen high-tech companies were incorporated as part of SEMATECH, representing 85% of the nation's capacity in semiconductor manufacturing. These companies, referred to as SEMATECH "member companies," were Advanced Micro Devices, AT&T, Digital Equipment Corp., Harris Corp., Hewlett-Packard Co., IBM Corp., Intel Corp., LSI Logic Corp., Micron Technology Inc., Motorola Inc., National Semiconductor Corp., Rockwell International Corp., and Texas Instruments Inc. [10]. One year later, NCR became the 14th member company in SEMATECH [11]. During the early stages of SEMATECH's development, the member companies determined that their first priority would be to strengthen the technical capabilities of their U.S. suppliers of semiconductor manufacturing equipment—a priority that has remained as the primary thrust of SEMATECH.

Sandia's relationship with SEMATECH began during SEMATECH's first two years of operation. At that time, SEMATECH held workshops on a large number of technical topics, and Dr. Wayne Johnson of Sandia participated in five of these workshops. Subsequently, Johnson and Dr. Jim Gerardo submitted a proposal to SEMATECH that culminated in the establishment of the Semiconductor Manufacturing Technology Center (SETEC) at Sandia in 1989. The decision was made to initially fund three generic tasks through SETEC: 1) equipment reliability, 2) equipment enhancement, and 3) modeling and advanced manufacturing methods. These three tasks were fully funded by SEMATECH under the terms of a funds-in Work for Others (WFO) agreement at a cost of $8 million and covering a 30-month period [10].

Sandia chose Dr. Chuck Gwyn, a former executive in the semiconductor manufacturing industry, as the first manager of the SETEC program. During the first 30-month period of SETEC operations, Gwyn was able to expand the SETEC program to include foreign equipment benchmarking and other activities and thus increase SEMATECH funds-in to Sandia from $8 million to $13 million. Following this initial contract, Sandia and SEMATECH signed two simultaneous one-year CRADAs valued at $10 million. During that time, a second program was established at Sandia, called the Contamination-Free Manufacturing Research Center (CFMRC), to conduct and coordinate research in

contamination-free manufacturing at universities, national laboratories, supplies, and member companies.

In 1993, the focus of the continuing Sandia/SEMATECH relationship changed with the signing of a five-year CRADA between SEMATECH and the Department of Energy (DOE). This CRADA, with two subsequent one-year extensions and a total value in excess of $110 million, governed the Sandia/SEMATECH relationship until the CRADA's termination on April 5, 2000. Partial funding by DOE required that the needs of both SEMATECH and Sandia be given equal weight. Thus, in the selection of projects, attention was also given to how such work would benefit Sandia's defense microelectronics program. Other programmatic changes also occurred at Sandia during the seven-year CRADA. Sandia established the Equipment Manufacturing Center as a third program area, in addition to SETEC and CFRMC; and Dr. Chuck Gwyn left Sandia and was replaced by Dr. John McBrayer, who served as the project manager from 1997 through 2000.

On the SEMATECH side there were also changes that impacted the Sandia/SEMATECH relationship. Gene Feit, the initial program manager, moved to another area at SEMATECH and Chris Daverse took over responsibility for the Sandia/SEMATECH relationship in 1997. In addition, the composition of SEMATECH changed to include both U.S. and international companies. In 2000, the SEMATECH member companies were Advanced Micro Devices, Conexant, Hewlett Packard, Hyundai, Infineon Technologies, IBM, Intel, Lucent Technologies, Motorola, Philips, STMicroelectronics, TSMC, and Texas Instruments.

3.2 Multiple Reasons for Partnering

The basic goal of the seven-year CRADA was to help SEMATECH member companies (a consortium of the majority of U.S. chipmakers) improve the quality of the processing tools used for fabricating integrated circuits (ICs). This goal has allowed the normally very competitive members of SEMATECH an arena where they could work together for mutual benefit in a pre-competitive environment.

From Sandia's perspective, the Sandia/SEMATECH partnership provided opportunities for Sandia to

1. Develop advanced semiconductor manufacturing equipment to produce next-generation ICs that are needed for defense applications
2. Meet and maintain Sandia's microelectronics Defense-Programs (DP) priorities
3. Leverage more than $4 billion a year in industry investment in equipment and processes
4. Ensure alignment of the DOE microelectronics core-competency with industry directions and the NTRS

5. Ensure efficient application of microelectronics development resources to DP-specific applications
6. Expose Sandia to the best industrial practices
7. Improve core competency directly and with spin-off industrial agreements

And through Sandia, the CRADA offered DOE the opportunity to maintain a microelectronics capability at a lower cost and at a higher quality.

3.3 Level of Effort

Over the lifetime of the seven-year CRADA, the Semiconductor Manufacturing Technologies Program spent $110,750,000.00 of which $21,897,000.00 was funds-in to Sandia from SEMATECH, $35,178,000.00 was in-kind funds spent at SEMATECH, and the remaining $47,675,000.00 was DOE funds spent at Sandia (see **Table 4**, where Project Year [PY1] corresponds to 1993). The program was well matrixed throughout Sandia. In fact, over the seven years of this CRADA, no one individual worked on the program exclusively.

Table 4. Project Funding History ($k)

	PY1	PY2	PY3	PY4	PY5	PY6	PY7
Total DOE	7500	10000	13175	10200	12100	1200	carry over
Total SEMATECH	7500	10000	13175	10200	12100	3600	carry over
Funds-in	4000	5000	5238	3254	3205	1200	
In-kind	3500	5500	7937	6946	8895	2400	500
Total Funding	15000	20000	26350	20400	24200	4800	500

By the conclusion of the CRADA, all projects were managed using technical project-management techniques. At the beginning of each year, Sandia published a book (the "Statement of Work") that provided SEMATECH and technology transfer offices with a one-page project summary and a Gantt chart of the work to be performed during the year. The success of each project was, in part, determined by how well the project was implemented according to plan. The projects followed all DOE rules, including Conflict of Interest, Environmental Safety and Health, Construction or Modification of Facilities, Use of Classified or Sensitive Information, Export-controlled information, Foreign Nationals, Proprietary Information, and Background Intellectual Property. Each project published a detailed final report at the end of each calendar year, and an annual report was also published summarizing the work performed by all projects during the year.

3.4 CRADA Results

During the seven-year CRADA, approximately 152 projects were completed. These projects have enhanced the quality of semiconductor processing equipment in many technical areas, and great strides in the modeling of IC processing equipment have been made. And, in some cases, model-based control systems have been developed. Overall, the CRADA has resulted in a general increase in semiconductor knowledge. The CRADA has also resulted in specific and shared benefits to industry, Sandia, DOE, and taxpayers, as briefly discussed below.

- **Benefits to Industry**

  The semiconductor industry has had the use of first-rate facilities and a complete range of science-based expertise upon which to call when faced with real industry problems. The industry has also had direct access to new and improved technologies that can increase productivity and yield and generate greater revenues. This access has allowed IC fabricators to concentrate their resources on production while using Sandia's science-based expertise to solve crisis problems and generation of next-generation tools. Equipment suppliers generally aren't large enough to provide the overall science needed for the creation of improved tools. Interacting with Sandia allows these smaller semiconductor companies to benefit from Sandia's larger investment in science-based solutions.

- **Benefits to Sandia and DOE**

  CRADA projects were selected based on DP relevancy and industry need. The projects have been technically challenging and have accessed Sandia's unique pool of expertise. The technical-challenge aspect has helped in making Sandia more interesting to potential new hires, as well as offering benefits to existing employees to further their technical expertise and project management skills. The Sandia/SEMATECH relationship has also been instrumental in upgrading Sandia's microelectronics facilities by exposure to best industry practices—decreasing costs to DOE and improving the quality of the facilities for DOE work. Projects have always included involvement of the U.S. semiconductor-equipment-supplier industry and of U.S. universities when appropriate, thus bridging university research concepts into engineering applications for industry and DOE use. Both Sandia and DOE have benefited from improved contacts with industry and academia.

- **Benefits to Taxpayers**

  Taxpayers have also benefited from the CRADA work. Approximately $50 million of enhancements in facilities and tools at Sandia and $1 million at Oak Ridge National Laboratory (ORNL) have been made with no cost to DOE. And an improved U.S. semiconductor industry impacts our economy in numerous beneficial ways, such as providing more higher-paying jobs for Americans, increased information access, and improved lifestyle through innovative consumer products.

- **Shared Benefits**

The CRADA has resulted in a number of technical publications and the creation of intellectual property that benefits Sandia, DOE, and SEMATECH, as well as the competency of the worldwide semiconductor industry. The following are a few statistics of the things created by this interaction:

- 40+ technical patent disclosures
- 7 patents awarded through December 1999
- 62 licenses
- 8 copyrights
- 50+ technical papers

Under the terms of the Sandia/SEMATECH CRADA, Sandia owns all intellectual property, and SEMATECH and its members are provided with a user license for anything invented under the CRADA. Sandia has honored all requests for licensing suppliers.

Figure 11 further illustrates how the Sandia/SEMATECH microelectronics synergy has resulted in a shared technological benefit, building a strong U.S. microelectronics industry to support a world market and future U.S. defense needs.

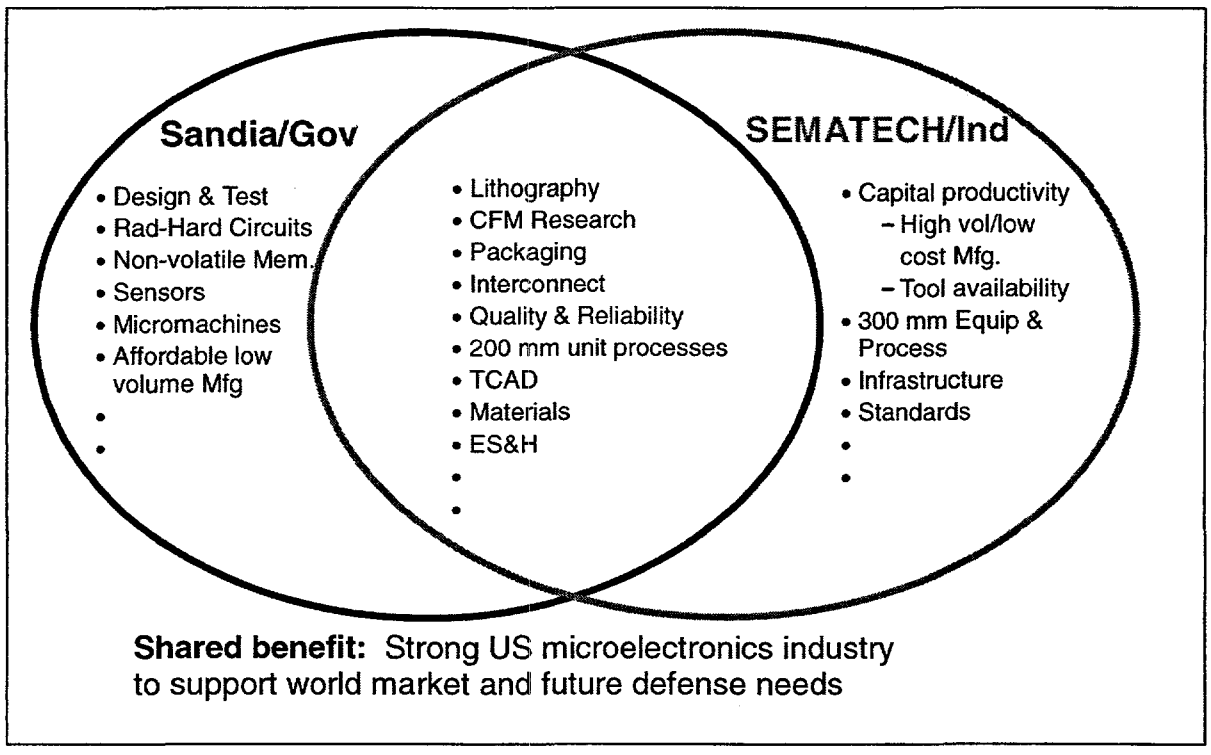

Figure 11. Sandia/SEMATECH microelectronics synergy.

3.5 Observations on the Process

The SEMATECH/Sandia partnership was influenced by the organizational structure of SEMATECH and the organizational structure of Sandia, and the working relationships between personnel at SEMATECH and Sandia were often impacted by the differences in their respective organizational cultures. Below, an overview of the two organizational structures is given, followed by some major lessons learned by Sandia from this dynamic partnership with SEMATECH.

3.5.1 About the SEMATECH Organization

SEMATECH is a unique and evolving consortium of member companies who cooperate in a precompetitive fashion to accelerate development of advanced technologies in the semiconductor industry. SEMATECH has its own employees as well as personnel from member companies who come to work at SEMATECH, generally for two-year assignments. As illustrated in **Figure 12**, the SEMATECH organization consists of a three-tiered hierarchy of boards that were implemented to reach consensus on the work pursued by SEMATECH. At the top level is an Executive Technical Advisory Board (ETAB), which is composed of representatives from the member companies (typically executive-level) and other organizations such as SEMATECH, SEMI/SEMATECH, and the Semiconductor Research Corporation. The president of SEMATECH is the chairperson of the ETAB. The ETAB is responsible for determining the areas on which SEMATECH will focus, for setting the overall budget in each area, and for recommending members at the next board level, which is composed of middle-level managers who are considered experts in their focus area.

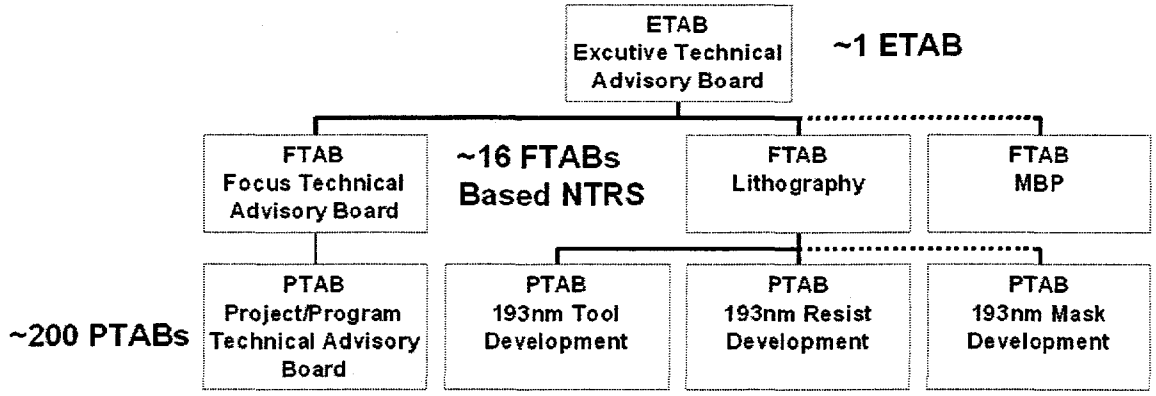

Figure 12. SEMATECH organization.

At the second tier of SEMATCH's structure, there is one FTAB for each focus area. In 2000, there were approximately 16 FTABs, each composed of representatives from member companies who typically are from middle management. Each FTAB has its own work force and is responsible for recommending projects and/or programs in its area of concentration. The technical director of an FTAB is either a SEMATECH employee or an assignee from a member company who has a number of project/program leaders who

report to him (or her) and work in the particular focus area. These project/program leaders (who may also be SEMATECH employees or assignees from member companies) are responsible for interfacing with outside organizations such as Sandia and equipment suppliers and also for creating Project Technical Advisory Boards (PTABs) at the next organizational tier. Note that these project/program leaders are the ones who served as co-project leaders, typically in a guidance capacity, on the CRADA projects.

At the third tier of SEMATECH's structure are the PTABs. Each PTAB is composed of representatives from member companies, typically technical staff of first level managers, who meet several times a year. A PTAB may be responsible for one or more programs. Some PTABs are working groups, while others are advisory. On several CRADA projects, PTABs participated in the work.

In addition, SEMATECH provided an overall Sandia/SEMATECH program manager (Chris Daverse) who, along with his Sandia counterpart (John D. McBrayer), guided the entire program.

3.5.2 About Sandia's SETEC/Semiconductor Manufacturing Technologies Program

CRADA projects were selected from prioritized lists prepared by the FTABs, PTABs, and individuals at both Sandia and SEMATECH. These lists were then reduced to a list congruent with Sandia's DP microelectronics needs. The program manager of the SETEC/Semiconductor Manufacturing Technologies Program at Sandia coordinated all CRADA activities at Sandia and also interfaced with the counterpart program manager from SEMATECH. The work was performed in many different departments and managed through a matrix structure throughout Sandia by the SEMATECH/Sandia program manager. Each project had a Sandia project leader, as well as a corresponding SEMATECH project leader, and some number of participants. The participants came from Sandia, equipment supplier companies, universities, ORNL, and/or SEMATECH.

3.5.3 Lessons Learned

Of the approximately 152 projects completed under the CRADA, all but 4 were completed in an outstanding manner, and those 4 projects ended with moderate success. From both the outstanding project successes and those that were only moderately successful, Sandia has learned some valuable lessons. Some of the most important lessons learned are discussed below.

- Sandia must control all resources needed to complete a project, as opposed to SEMATECH controlling project resources. This lesson was learned during the beginning of the CRADA when a SEMATECH project leader placed a contract directly with a university in support of a Sandia/SEMATECH project. The work called out in the CRADA project was superseded by the SEMATECH contract manger's requests for information from the university. Thus no funds were left to

complete the agreed-upon work. Sandia was then "blamed" for not properly completing the project.

- A detailed but flexible project plan is essential to address any potential changes in leadership during the duration of a project. This lesson is particularly important when there are co-project leaders from different organizations on a project. For example, each CRADA project had a project leader from SEMATECH and one from Sandia. And given the way that the SEMATECH personnel system works, it was not uncommon that a project leader would start a project but at some point would return to his company, leaving the direction of the project to another SEMATECH project leader who was unfamiliar with the project objectives and approach. A well-documented project plan can eliminate radical changes in direction that such a situation could invite.

- Partners with radically different organizational cultures need to respect the differences in their respective cultures. To facilitate this process, the Sandia program manager prepared a set of guidelines that helped Sandia project members interact with SEMATECH personnel. The guidelines emphasized that Sandia and SEMATECH were partners in CRADA projects and thus should make decisions together.

- Some companies have preconceived negative impressions of federal laboratories that must be overcome with earned respect. It was discovered that the best way to create trust and respect of Sandia by SEMATECH was to negotiate reasonable goals for the project, document these goals in the form of project plans, and then complete the project on time, for the predicted cost, and in fulfillment of the goals.

- Companies must realize they need help and want assistance. Good communication and results help with this realization.

- Federal laboratory personnel must take the initiative and provide hands-on assistance.

- Corporate partners must be directly involved in team activities.

- Information transfer is best handled at the working level through one-on-one relationships.

- The federal laboratory must put together a top-quality team that quickly earns the respect of the corporate partners.

3.6 Future Work and Plans

Although the long-term CRADA has been discontinued, the Sandia/SEMATECH relationship will continue under a 100% funds-in Non-federal Entity (NFE) WFO agreement. For CY 2000, $500,000 was committed to this new agreement.

4 Project Briefs

This section presents a summary of the projects completed under the Sandia / SEMATECH Cooperative Research and Development Agreement (CRADA) for the years 1993 through 1998.

4.1 Projects Completed in 1993

1. **Reliability Consulting**: The Reliability and Analysis Modeling Program (RAMP) was expanded to support six redundancy options and improved usability access to data libraries and import/export capabilities. Software Quality Improvement courses were updated and presented to member companies and Semi/SEMATECH companies. Ergonomics analysis was provided to FSI, ergonomic guidelines were published, and support was given to the creation of Semiconductor Equipment Manufacturing Industry (SEMI) standards.

2. **Vertical Furnace Modeling**: Extensive modeling and simulation, using the TWAFER and OVEND codes, were performed for the design of a Silicon Valley Group (SVG) Thermco advanced vertical processor. The simulations included verifying the tetraethelorthosilicate (TEOS) reaction rates and products.

3. **Resist Stripper Reactor Modeling**: Simulations were performed and design modifications were suggested for the Applied Materials P5000E stripper reactor to provide uniformity improvements of 9% to 22%.

4. **Lithography Equipment Modal and Vibrational Analysis**: Extensive modal and vibrational analysis was performed for the GCA XLS lithography tool. An experimental modal and structure dynamics analysis of the Silicon Valley Group Lithography Systems, Inc. (SVGL), series 92 lithography tool was completed, and design recommendations were suggested.

5. **RTP Reactor Modeling**: Basic rapid-thermal-process (RTP) models were developed to evaluate the Texas Instruments MMST and 65 kilowatt (kW) reactors and to provide suggestions for improving future designs.

6. **Materials and Process Analysis**: A number of oxidized aluminum samples, typical of those used in showerhead construction for plasma reactors, were evaluated. The aluminum anodization studies highlighted the lack of anodization standards and the variability of the coatings used in plasma reactors.

7. **Tungsten Reactor Analysis**: The use of the Genus 8720 reactor for selective tungsten deposition identified a number of sources of particles. To perform selective tungsten deposition, several major design changes must be implemented.

8. **Pressurized Sulfuric Acid Tank Failure:** Root-cause analysis of an explosive failure of a pressurized chemical tank provided recommended design changes and created an inspection procedure to prevent future failures.

9. **ECR Equipment Benchmark**: A Hitachi electron-cyclotron-resonance (ECR) plasma etch tool was evaluated for process capability, reliability, maintainability, and long-term process performance. The tool demonstrated excellent process control and reliability.

10. **Center for Contamination-Free Manufacturing (CFM)**: The CFM Research Center was created in mid-1992 at the request of SEMATECH member companies. From the Infrastructure and New Initiatives Project, four technical projects were defined and initiated. These projects involved modeling to reduce particles on wafers, sensors to improve detection sensitivity of contaminants in process equipment, wafer environment control through microenvironments, and advanced wafer cleaning.

11. **CFM – Particle Trajectory Modeling in Low-Pressure Reactors**: Commercial software was extended to model trajectories and capture efficiency of particles from the showerhead of the Applied Materials 5000 low-pressure chemical vapor deposition (LPCVD) tungsten reactors. Calculations indicated that thermophoretic forces can be made sufficiently strong to repel particles from the wafer surface under properly chosen reactor operating conditions.

12. **CFM – High-Sensitivity Sensor Development**: Development of trace moisture sensors was initiated during the third quarter using three approaches: 1) intracavity laser spectroscopy (high sensitivity, high cost), 2) Fourier transform infrared spectroscopy (moderate sensitivity, moderate cost), and 3) solid state sensors (moderate sensitivity, low cost).

13. **CFM – Microenvironments:** A survey of the methods used to characterize microenvironments was completed, and a summary of potential test methods for measuring microenvironment out-gassing was compiled.

14. **CFM – Wafer Cleaning Efficiency Enhancement Using Megasonics**: Pressure-wave agitation of wafer surfaces in a Verteq Sunburst Megasonic Cleaner was shown to enhance the removal efficiency of sub-0.15 μm particles when used in conjunction with industry-standard SC-1 (hydrochloric acid/hydrogen peroxide/water) chemical-cleaning solutions.

15. **RAMP Version 2**: RAMP version 2 provided software upgrades, including the addition of new execution, editing, and BLOCS routines. Version 2 was beta-tested at Genus, Inc., Lam Research Corp., Applied Materials, IBM, Kulicke & Soffa Industries, Inc., Varian & Associates, and Teradyne, Inc.

16. **Software Process Improvement**: Guidelines for software process improvement were developed and published. The guidelines were beta-tested at Varian

Associates, Teradyne, Inc., Plasma & Materials Technology, Inc., Eaton Corp., and Applied Materials.

17. **Ergonomics of Computer-Directed Equipment**: Ergonomics consulting was performed to improve the human-tool interfaces for several manufacturers. The companies (with specific tools as noted) included the following: GCA (XLS), SVG (9x series track & microscan), Genus (8722), and FSI (Excalibur II), Dryden, RealTime Performance, Advantage (Edge 3000), Eaton, KLA, and The Mcilvaine Company.

18. **Aluminum Anodization Characterization**: Process-variation sample testing was performed for a variety of anodized samples. A dissipation factor measurement was created and patented to characterize the anodized layer quality. A working group was formed with industry to monitor progress and provide technical direction.

19. **Quartz Acid Tank Failure**: An analysis, performed on the cracking failure of a quartz tank, identified the cause of the failure and provided suggestions for eliminating this type of failure in the future. Finite-element analysis indicated the failure was caused by excessive corner stress produced by a constrained fixture.

20. **Simulation, Design, and Control of Low-Pressure Chemical Vapor Deposition (LPCVD) Furnaces**: LPCVD models were applied to the design and optimization of SVG-Thermco and Semitherm furnaces. A model-based control approach was developed with Relman, Inc.

21. **Simulation of the Texas Instruments MMST Rapid Thermal Processor (RTP)**: Thermal models were calibrated and validated using experimental data for the Texas Instruments RTP tool. The codes were also used to aid CVC Products, Inc., in developing a commercial RTP tool.

22. **Plasma Process and Equipment Modeling - Plasma Modeling I**: The infrastructure was established for a three-year integrated modeling approach for plasma processes. This approach provided an evolving suite of codes to simulate and model high-density plasmas through a distributed computer system. Each module was developed independently and used to solve current industry problems.

23. **Magnetically Levitated (Maglev) Stage Development**: The Massachusetts Institute of Technology (MIT) Maglev technology was employed, and an associated control system was developed to provide an improved six-degree-of-freedom fine stage for the GCA (XLS) lithography tool.

24. **Lithography Stage Materials Development**: Light-weight, rigid, low-thermal-expansion materials were investigated for possible use in the fabrication of reticle stages. The materials investigated included aluminum-silicon carbide (Al-SiC) composites, SiC graphite epoxy composites, and alumina.

25. **Neutral-Beam Etching**: Two workshops were held to evaluate the present status of neutral-beam technology for low-damage cleaning and etching. The main issues identified were slow etch rate due to low flux, pressure/pumping in large systems, contamination, and lack of surface kinetic data needed for a system design.

26. **Electrostatic Chucks (ESCs)**: Existing ESCs were benchmarked and alternate materials investigated, including anodized aluminum that was sprayed with alumina, titania, spinel, and anodic aluminum oxide coatings and that was painted with a polyimide, polytetrafluoroethylene, dielectric silicone, thermal-management silicone paint or spin-on-glass siloxane preparation.

27. **Hitachi ECR Benchmark Follow-on**: The electron-cyclotron-resonance (ECR) etcher was characterized using additional chemistries to optimize selectivity, and the cost of ownership was determined.

28. **Chemical Downstream Etcher (CDE) Benchmark**: A Shibaura CDE etch tool was evaluated for process capability, reliability, maintainability, and long-term process performance. The tool demonstrated excellent process control and reliability. The cost of ownership was determined for an optimized etching process.

29. **American Challenge Benchmark**: In response to the Hitachi ECR benchmark project (number 27 above), an Applied Materials 5000 etch tool was evaluated for process capability, reliability, maintainability, and long-term process performance, and was compared with the Hitachi. The tool demonstrated excellent process control and reliability, as well as lower cost of ownership.

30. **CFM – Gas-Phase Nucleation in Chemical Vapor Deposition (CVD) Reactors**: Predictive models of reactor processing conditions that lead to gas-phase nucleation of particles were developed, including nucleation-kinetics modeling. Results were implemented into flow codes for plasma TEOS deposition.

31. **CFM – Particle Transport Modeling Incorporating Plasma and Electrostatic Effects**: Numerical models were generated for Lam Rainbow 4720 tungsten etchers, resulting in suggestions for particle reduction that the industry partner propagated to the installed base through retrofit kits. A particle measurement technique in plasmas was also developed and used to verify modeling predictions.

32. **CFM – Contamination Sensor Development**: An intracavity laser spectrometer demonstrated sensitivity for trace moisture in nitrogen and helium at the 10 parts-per-billion (ppb) level. A direct absorption spectrometer was developed that exhibited a detection sensitivity for trace moisture at the 15 ppb level.

33. **CFM – Organic Contamination Detection in Wafer Environments**: Analytical measurement of out-gassing from wafer cassettes from Fluoware and Asyst was completed, and development was initiated for a surface acoustic wave (SAW)

sensor that could continuously detect submonolayer concentrations of molecular contamination.

34. **CFM – Effects of Frequency and Location on Sonic-Assisted Cleaning**: The ultimate cleaning limits of sonic agitation were evaluated with respect to frequency of sonic waves, location of transducer, and spacing between wafers. For this evaluation, researchers used a contaminant, such as silicon nitride, that is known to be difficult to remove. This project also developed a reproducible particle-generation and application technique for cleaning experiments.

4.2 Projects Completed in 1994

35. **Plasma Modeling II**: The second year of the three-year project focused on producing flexible simulators for inductively coupled plasma (ICP) processing equipment with chlorine and chlorine-rare-gas chemistries. Model validation was performed on an ICP source for the Gaseous Electronics Conference (GEC) radio-frequency reference. Individual simulations were used to provide solutions to the plasma tool industry.

36. **Rapid Thermal Processor (RTP) Modeling**: Simulations combining thermal, fluid flow, and chemically reacting flow models were used to support CVC Products, Inc., in developing a commercial RTP system. The models were applied to the concurrent design and testing of a real-time, multivariable temperature-control system. Fundamental chemistry work supported development of an improved chemical reaction mechanism for depositing silicon dioxide (SiO_2) from tetraethoxysilane (TEOS).

37. **Characterization of 248 nm Precision Optical Lens Subjected to Thermal Load**: A model was developed to predict the aberrations occurring in precision optical components subjected to thermal loads. This analysis simulated the thermal, mechanical, and optical response of components to predict the aberration induced by the illumination source and was applied to several generic optical components.

38. **Equipment Design and Support Center (EDSC)**: The EDSC was established to provide designers of semiconductor manufacturing equipment (Gasonics, Matrix, Semitherm, Silicon Valley Group/Tracks, Varian, and Watkins-Johnson) access to equipment models and computer hardware for performing computer simulations of semiconductor fabrication equipment.

39. **Tool Improvement**: Reliability modeling support was provided for Brooks Automation and CFM Technologies. This support included training and assistance in predicting the performance benefits to be gained from tool upgrades. Support was also provided to AG Associates (AGA) in developing a direct software linkage between the SEMATECH Failure Reporting and Corrective Action

System (FRACAS) software and the Reliability Analysis and Modeling Program (RAMP).

40. **Electrostatic Chucks (ESCs)**: Two approaches were followed in developing ESC coatings for use in aggressive chemistries at high temperatures: 1) painting, dip-coating, and plasma-spraying the insulating polymeric or ceramic materials on aluminum-based substrates and 2) fabricating a textured silicon chuck with insulating coatings.

41. **Small-Batch, Fast-Ramp Furnace**: Computational models were developed and applied as part of a team effort to define and study the feasibility of a set of technical specifications for a small-batch, fast-ramp furnace.

42. **Heavy-Ion Backscattering Spectrometry (HIBS)**: A HIBS system was designed and built to measure trace amounts of high-atomic-weight contamination on the surface of wafers. The HIBS system provides approximately a two-order-of-magnitude improvement over the conventional total x-ray fluorescence (TXRF) method.

43. **Software Improvement Program**: Assistance was provided for two projects during 1994 to improve the software delivered and used by suppliers in the semiconductor equipment manufacturing industry. Software Process Improvement (SPI) Initiatives were established at Plasma and Materials Technologies, Inc., Varian Associates, and Teradyne, Inc. Support was also provided to AGA by applying the SEMATECH SPI approach for the RTP Installed User Base Project.

44. **Photolithography Stage Materials Research**: A wafer-stage support structure and chuck were selected as components for evaluating the use of advanced materials (graphite, epoxy composite, alumina, silicon carbide). Modal, thermal, and structural analyses were conducted to verify that the stage components met performance specifications.

45. **Neutral Beams**: A third workshop was held to identify the state of development and application of neutral beams for low-damage etch-processing applications. Support was provided for neutralization modeling by Lawrence Livermore National Laboratory, for surface studies with halogen beams by Los Alamos National Laboratory, for oxide etch chemistry by the University of California at Berkeley, and for test-bed construction at SEMATECH.

46. **Connector Failure Rapid Response Study**: A study was performed to determine the reason for a quartz-lined acid-bath-triggered fire. The study attempted to develop an inspection process to avoid such fires in the future. The cause of the event was related to bolted connectors in the heater wiring. Although the cause of the failure was confirmed and sufficiently well understood to predict future failure of similar tanks, no method was found to reliably inspect suspect baths other than disassembly.

47. **Chemical Downstream Etch (CDE)**: Basic models were developed for analyzing the Shibaura CDE-80 benchmark system. These models were used to help Applied Materials and Matrix in the design of new CDE tools.

48. **Automated Defect Classification** [Project Implemented at Oak Ridge National Laboratory (ORNL)]: The state of the art in automatic defect classification (ADC) technology for semiconductor wafers was determined through interviews and on-site evaluations of five commercial and university suppliers. An unbiased procedure was developed to evaluate ADC products. Two on-site evaluations were completed.

49. **Manufacturing Systems Development - Equipment Control** [Project Implemented at ORNL]: Two staff members were assigned as national laboratory associates to SEMATECH to assist the Manufacturing Systems Development thrust in equipment control areas. These associates supported control hardware and systems integration, with emphasis on control standards and applications for cluster tools as well as technical assistance to the Cluster Tool Module Communications (CTMC) tester project. Consulting on control systems was also provided to three equipment suppliers.

50. **Electrostatic Chuck (ESC) Materials Evaluations** [Project Implemented at ORNL]: Various dielectric materials were investigated for use as high-temperature coatings (up to 600°C) on ESCs. Thermal-spraying methods were developed to apply the materials on chuck surfaces, and techniques for evaluating the electrical behavior of the coatings over a range of temperatures were developed.

51. **Chemical Downstream Etcher (CDE) Applications**: A process was developed for the Shibaura CDE-80 to replace wet stripping of polysilicon-buffered local oxidation of silicon (referred to as PB LOCOS or PBL) mask stacks and oxynitride films. The cost of ownership was determined.

52. **Current Wire-Bond Capabilities**: A survey of SEMATECH member companies was performed to determine the manufacturing capabilities and performance of current fine-pitch wire-bond products.

53. **Current Surface Mount Technology Assembly Data**: A survey of SEMATECH member companies and vendors was performed to benchmark quad-flat-pack (QFP), ball-grid-array (BGA), and tape-carrier-package (TCP) manufacturing assembly data.

54. **CFM – Particle Reduction in Lam ICP Plasma Etch Tools Through Modeling**: Models of particle transport in inductively coupled plasma (ICP) etch reactors were applied to Lam Research etch tools. Previous studies in modeling particle movement in Applied Materials' chemical vapor deposition (CVD) tungsten reactors were extended to include the transient heating effects of wafers on susceptors, and the leading particle sources in these reactors were calculated.

55. **CFM – Moisture Sensor Development**: Refinements to both the intracavity laser spectroscopy (ILS) and Fourier transform infrared (FTIR) sensors made possible the detection of moisture in corrosive gas (hydrochloric acid vapors) at the sub-10 ppb level. A surface acoustic wave (SAW) sensor was completed and tested at a moisture detection limit of 100 ppb. A procedure for simulating load-lock operations was designed and implemented on the Sensors-in-Vacuum (SIV) test stand.

56. **CFM – Organic Contamination Detection and Impact in Wafer Environments**: An experimental test matrix was developed to determine the effect of gaseous and liquid organic contamination on the gate-oxide integrity of IC devices. The development of the SAW sensor was extended and integrated in Standard Mechanical InterFace (SMIF) pods for real-time measurement of organic condensation. This sensor demonstrated the capability to detect and differentiate specific organic species among several classes of molecular contaminants.

57. **CFM – Efficacy of Ultradilute Cleaning Solutions**: The cleaning efficiency of full-strength and diluted standard-clean 1 (SC-1) solutions was evaluated in cleaning studies. Researchers concluded that dilution of greater than 1000:1 in SC-1 constituents had no negative effect on cleaning efficiency over a variety of conditions—a finding that allowed for the possible reduction in costs associated with acquiring and disposing of the cleaning chemicals. Evaluation of particle adders from spin-rinse dryers was completed, and the cause/cure of industry's long-standing "sulfuric-rinsing residue particle problem" was identified.

4.3 Projects Completed in 1995

58. **Alternate Interconnect**: The trade-off point between peripheral and array input/output (I/O) designs was determined by computing the cost for three different interconnection technologies: wire-bond, tape-automated bonding (TAB), and flip-chip.

59. **Chemical Downstream Etch (CDE) Benchmarking and Follow-On Support**: Follow-on activities evaluated a water-cooled sapphire source as an alternative to the original air-cooled quartz source to minimize discharge-tube erosion, and investigated an etching mechanism for silicon nitride (Si_3N_4).

60. **Plasma Diagnostics**: Plasma diagnostics were created to measure charge in low-charge-density (n_i) plasma environments, e.g., in a CDE reactor.

61. **rf Plasma Studies**: Advancements in the excitation of plasma reactors by radio frequency (rf) power included the following: 1) performing an experiment to provide understanding and thus control of the harmonic generation of an inductively coupled research reactor at the chuck, 2) taking measurements at AT&T Bell Labs of components in the tee match of a Lam Alliance high-flow

reactor, and 3) conducting tests of the rf voltage and current sensors developed by ORNL.

62. **rf-Power Measurement and Control** [Project Implemented at ORNL]: This project focused on developing an rf-power measurement and control system for use on plasma etch tools. An rf-power sensor was designed; a prototype was fabricated and tested; and a boot-strapped preamplifier and band-pass filter were designed, simulated, fabricated, and tested.

63. **Electrostatic Chucks (ESCs)**: Cost-effective techniques were identified for improving the performance of ceramic coatings that are widely used as dielectrics in high-temperature ESCs. A novel silicon-pin chuck was designed, manufactured, and evaluated.

64. **Investigation of Thermally Sprayed Coatings for High-Temperature ESCs** [Project Implemented at ORNL]: Thermally sprayed aluminum oxide (Al_2O_3) was investigated as a potential coating material for high-temperature ESCs.

65. **Tool Improvement - Brooks Automation and Silicon Valley Group Lithography Systems, Inc. (SVGL)**: Reliability modeling support was provided to Brooks Automation (Chelmsford, Massachusetts) and SVGL (Wilton, Connecticut). An approach was developed to identify the optimal spare-parts inventory for a specified number of tools to meet a specified budget or downtime goal. A baseline reliability model was also developed for the Micrascan II lithography system based on failure data imported into the Reliability Analysis and Modeling Program (RAMP) from SVGL's failure-reporting database.

66. **Plasma Modeling III**: A suite of simulation tools was developed for modeling various aspects of plasma etch and deposition reactor performance. The tools were validated with spatial data taken for pure argon and pure chlorine plasmas discharges in a Gaseous Electronics Conference-Inductively Coupled Plasma (GEC-ICP) reference cell without a wafer.

67. **Chemical Downstream Etch (CDE) Modeling and Joint Development Project (JDP) Support**: Support was provided for SEMATECH JDPs with Matrix Integrated Systems, Applied Materials, and Astex Corporation in the development of new CDE reactors for wafer cleaning and stripping processes. Models were developed to simulate the gas flow, chemistry, and transport in CDE reactors and to address the essential components of the CDE system (i.e., a microwave source, transport tube, showerhead gas inlet, and downstream etch chamber). Data for model validation was obtained from Sandia's molecular-beam mass spectrometry experiments, the literature, the CDE Benchmark Project, and the JDP partners.

68. **Rapid Thermal Processor (RTP) Modeling**: Fabrication of the first conserved-vector-current (CVC) RTP reactor was completed. Numerical models were applied to the design and evaluation of the new axisymmetric RTP reactor. Sandia, CVC Products, Inc., and Microelectronics Control and Sensing Inc.

teamed to develop and test a multi-input multi-output (MIMO) controller using a detailed finite-element thermal model as a surrogate for the actual hardware.

69. **Small-Batch, Fast-Ramp Furnace**: Computational models were developed and applied to accelerate development of small-batch, fast-ramp furnaces at Semitherm and Silicon Valley Group (SVG) Thermco. Modeling results were used in the SEMATECH cost-resource-modeling studies and in defining optimum process trajectories.

70. **Heavy-Ion Backscattering Spectrometry** (HIBS): The HIBS user facility was established for use by specialists from SEMATECH member companies. The detection limits of contaminants were lower than those achieved by any other ion-beam technique.

71. **Equipment Improvement Center (EIC) Support**: The Equipment Design & Support Center (EDSC) functions were expanded, and the EIC was established to improve tool design and operation by supporting computer simulations for semiconductor fabrication equipment manufacturers. The EICS was located at two sites: Albuquerque, New Mexico, and Livermore, California. Both sites provided computers, software, and experts to help run the simulations either locally or remotely through the Internet. The EIC supported the following companies: FSI, Gasonics, Semitherm, SVG/Tracks, Varian, and Watkins-Johnson.

72. **CFM – Numerical Modeling Applications for Improved Equipment Performance**: A list of "Ten Commandments" for the design and operation of semiconductor deposition and etch tools, based on modeling and verification results, was published. The list included 1) particle generation by nucleation, 2) particle transport in plasma etch reactors, 4) particle jetting through CVD reactor showerheads, 5) reduction of resuspended particles, 6) particle transport in load locks, and 7) particle reduction during wafer-handling steps.

    By determining the factors that limit the efficiency of water use in overflow rinse tanks, researchers were able to recommend (to Santa Clara Plastics) a retrofit kit for improving the SCP 9200 rinse tank. The recommendations included a method for reducing wafer usage by 41% without a corresponding reduction in cleaning efficiency.

73. **CFM – Trace Moisture Sensor Development**: The intracavity laser spectroscopy (ILS) sensor demonstrated a detection sensitivity of 100 parts-per-trillion (ppt) for moisture, and was commercialized by Innovative Lasers Corporation of Tucson, Arizona. A dual-beam Fourier transform infrared (FTIR) accessory for moisture in corrosive gases was successfully commercialized in partnership with Axiom Analytical of Irvine, California. A new porous-silicon-capacitor solid state sensor was designed, fabricated and tested for use in the detection of trace moisture in vacuum (sputter-system) applications. An

investigation was completed of the sensitivity and pressure-dependent sensitivity of the Ferran Micropole Analyzer toward water vapor over the full working range.

74. **CFM – Molecular Contamination in Wafer Environments**: Three techniques were studied that are capable of measuring organics on wafers at levels to 10^{12} carbon atoms per square centimeter. Measurements of contact angles were taken to evaluate the impact of molecular contamination on surface tension. A calibration procedure for SAW sensors was developed for n-methyl pyrolidone (NMP) and calibrated to 100 ppb. A hand-held molecular contamination monitor was also developed using a quartz crystal microbalance, and a trace amine sensor was evaluated for feasibility. A clean-room assay was completed for trace airborne contaminants.

75. **CFM – Development of Post-CMP Cleaning Techniques**: An evaluation of megasonically assisted, dilute solution cleaning of chemomechanically polished (CMP) wafers was conducted with and without surfactant additives. Measurement of particle adhesion to surfaces was demonstrated using a liquid-cell atomic force microscope, and the results were used to improve cleaning efficiency. A micromachined pressure sensor was developed for performing in situ measurement of the intensity of sonic wave energy.

76. **CFM – Environmental Safety and Health - Reduction in Wafer Use**: The first phase of this multiyear project began by assessing the availability of online sensors and technology for detecting acetone, ethylene glycol, and isopropanol in water.

77. **CFM – Defect Data Reduction** [Project Implemented at ORNL]: Techniques for image processing and pattern recognition were used in conjunction with optical inspection of defect patterns on wafers to help diagnose problems with manufacturing equipment.

4.4 Projects Completed in 1996

78. **Lithography Stage System Dynamic Modeling**: A dynamic model for the Silicon Valley Group Lithography Systems, Inc. (SVGL), advanced Micrascan II exposure tool was developed to enable simulation testing of proposed tool advancements and help equipment designers determine optimal choices in areas such as electrical and mechanical design and control strategies and algorithms. The six-degree-of-freedom dynamics model of the SVGL Microscan lithography tool provided complete simulation and was identified as a tool for future design.

79. **Lithography Reticle Stage Development**: Advanced materials were used to manufacture an advanced SVGL reticle stage to reduce the stage weight and enhance the thermal stability. An acceptable new material that meets all of the needed criteria was not available. The available materials could only be used in applications where the optical surface was not rigidly attached to the structure.

80. **Tool Improvement-SVGL**: The Reliability and Analysis Modeling Program (RAMP) capability was transferred to SVGL. The baseline model was consistent with observed field performance. SVGL was trained in fault-tree methodology.

81. **Silicon-On-Insulator (SOI) Material Screen Test**: Separation by IMplantation of OXygen (SIMOX) buried-oxide SOI wafers were characterized at the wafer level by, I-V and C-V property measurements to determine an electrical-screening technique for qualifying SIMOX wafer lots.

82. **IDDQ/Burn-In Effectiveness**: Static IDDQ (quiescent power-supply current) testing was evaluated with optimized stress voltage and frequency for high-defect coverage as part of a full electrical test that identified failing, or potentially functional failing, die prior to burn-in.

83. **rf Power Measurement & Control Standards** [Project Implemented at ORNL]: Radio-frequency (rf) system components were optimized, and the hardware was evaluated by the National Institute of Standards (NIST) as a possible high-rf-power standard.

84. **NIST/Sandia Precision Critical-Dimension Metrology Structures**: Micromechanics technology was used to create SOI high-precision electrically certified CD reference artifacts for deep submicrometer metrology.

85. **Optical Index of Refraction Measurement with Temperature at 193 nm**: A novel interferometric technique was developed for measuring the change of the index of refraction for 193 nm candidate optical-lithography lens materials.

86. **Optical Degradation from 193 nm Illumination**: An analysis environment to characterize the performance of optical materials for 193 nm illumination was created. This analysis environment consisted of a suite of tightly integrated software packages that together estimated the Zernike polynomials in the wave front exiting an optic or group of optics. The simulations included color center formation, absorption, and compaction of several 193 nm candidate lens materials. The model was used to predict performance of an operating tool.

87. **SOI Buried- & Gate-Oxide Integrity**: Experiments using SOI wafers, created by implanting a buried-oxide layer, showed correlation between buried-oxide integrity and gate-oxide integrity.

88. **Known-Good-Die & Chip-Scale-Packaging Process Cost Resource Modeling**: The relative costs of chip-scale packages were compared to conventional surface-mount packages. This comparison helped in deciding whether to use conventional packages versus chip-scale packages versus chip-on-board known good die.

89. **Improved Manufacturing of Low-Cost Liquid Encapsulants**: Standardized metrology tools and techniques were developed to characterize liquid encapsulants. These tools and techniques provided an understanding of the factors

affecting wetting, flow, and the role of materials variables to manufacturing and the reliability of cavity-fill and underfill packages.

90. **Ball Grid Array (BGA)/Flip-Chip Addendum to Assembly Test Chips**: The ATC04 stress-measurement test chip was modified with an additional metal layer to distribute the existing perimeter bond pads to an area array. The completed test chip, designated ATC04.1, contained daisy chain and solder-ball Kelvin measurement structures, along with access to all ATC04 test structures, and provided the necessary data to evaluate flip-chip packages.

91. **Lead-Free BGAs & Jetting**: A lead-free manufacturing process for BGA packages was developed, along with a prototype novel jetting machine that created the BGAs with superior cost-ownership numbers than were presently available in the industry.

92. **Wire Sweep During Solid Molding**: Experiments were performed to determine shear stress and molding-compound viscosity for optimizing the epoxy-molding process and minimizing wire sweep. The extent and details of wire sweep were compared with the measured viscosity of molding compounds taken at the manufacturing process temperature, duration, and shear-stress levels.

93. **Probe Card Evaluation Laboratory**: Sandia created and performed alternating current, direct current, and mechanical metrologies for advanced probe cards. This work prepared Sandia to use and evaluate the probe card technology for the next generation of ICs.

94. **rf Studies '96**: Improved performance and understanding of plasma reactors was accomplished by reducing the chamber-to-chamber variability in an IBM production line, by developing and analyzing an rf equivalent-circuit model for Lam Research, and by developing and validating a harmonic-generation model at the chuck of an inductively coupled reactor.

95. **Wafer-Level Charge Flux Analyzer**: A real-time, wafer-level energy analyzer and Faraday collector for use in plasma process/tool design and analysis was designed and fabricated. The analyzer performed as expected.

96. **Linking Topographic Simulation to Reactor Modeling for Silicon Dioxide (SiO_2) Deposition in Lam's Deep Submicron Tool**: Software was developed to interface a compact reactor model and a commercially available topographic simulator, Terrain. The software included gas-phase chemistry for silane (SiH_4), oxygen (O_2,) and argon (Ar) plasmas, and SiO_2 deposition, ion recombination, and ion milling. The integrated simulator was validated using industry-provided data. Lam modelers were trained to use the integrated simulator.

97. **Guidelines for Simulator-Based Control System Testing** [Project Implemented at ORNL]: A validated Cluster Tool Module Communications (CTMC) tester was developed to allow suppliers to determine product compliance with the Modular Equipment Standards Committee (MESC)/CTMC standards and to identify areas

requiring modifications. Equipment reliability is improved by the promotion of simulator-based controller testing.

98. **Small-Batch/Fast-Ramp (SBFR) Furnace Modeling**: The SBFR furnace modeling was extended to include control. Model-based control lowers cost and improves performance.

99. **Numerical Simulation of New Rapid Thermal Processing (RTP) Systems**: Closed-loop control was demonstrated and shown to be a critical element of the RTP design process. Specific designs were evaluated for High Temperature Engineering Corporation (Eaton) and Peabody.

100. **CFM – Modeling-Based In Situ Particle Monitor Placement Optimization**: To resolve issues noted in industry regarding locational dependence on measured sensor-particle density, the particle trajectories in an experimental Lam reactor were modeled and sensor measurement discrepancies were explained in terms of proximity to particle-rich flow regions. In support of SEMATECH and member-company interests in nonaqueous tool development, one-dimensional cleaning mechanisms in cryogenic aerosol jets were determined.

101. **CFM – Sensors for Improved Overall Equipment Effectiveness:** Progress was made in creating an advanced sensor to measure and reduce contaminants in plasma etch tools, with development of an in situ real-time chamber-wall residue monitor based on a fiber-optic reflectometer. An optical emission spectrometer was also developed and demonstrated as an effective sensor for real-time etch-endpoint determination. In addition, a point-of-use purifier for hydrofluoric-based liquids was developed and demonstrated.

102. **CFM – Molecular Contamination Control:** The feasibility of an Attenuated Total Reflection Surface State Monitor was evaluated. The effect of modifying pregate cleans to reduce the use of chemical and process steps (while still adequately removing organic contamination) was evaluated.

103. **CFM – Effect of Transducer Frequency, Location, and Wafer Spacing Through Modeling of Megasonic Energy Fields**: A mechanistic model of megasonics agitation effects, developed with the University of Minnesota and compared to previous experimental CFM wafer-cleaning projects, showed good agreement. The postulated cavitation phenomenon was verified as the most likely cleaning (particle-removal) mechanism.

104. **CFM – Real-Time, On-Line Sensors for Semiconductor Water Systems**: Commercial availability of water system sensors with respect to on-line/in-line monitoring, time of response, and speciation of organic compounds was improved. Prototype sensors for organic contaminants in semiconductor water systems were developed and demonstrated.

105. **CFM – Spatial Signature Analysis** [Project Implemented at ORNL]: A spatial signature analysis tool was developed that can be transferred to fabrication personnel for analyzing process signature events found during wafer processing.

106. **Hydrogen Peroxide Cleaning Station Fire**: A site investigation, root-cause analysis, and recommended procedural changes were completed in response to a request from a member company that experienced a fire in a hydrogen peroxide wet-cleaning bench.

4.5 Projects Completed in 1997

107. **Interferometric Mix/Match Lithography**: A mix/match system was being developed for use as an interferometric technique for the "difficult" layers of less than 0.18 mm CMOS (complementary metal oxide semiconductor) technology and for use as a conventional optical-stepper technology for all other layers. This machine was used for advanced development in Sandia's Microelectronics Development Laboratory (MDL).

108. **Wafer Prober Enhancement & Control**: This project improved the performance of the ElectroGlas wafer prober through the development of a closed-loop control system and the addition of an enhanced temperature-controlled chuck.

109. **Tungsten Chemical-Mechanical Planarization (CMP)**: This project determined an integrated cost-of-ownership for tungsten CMP and post-CMP cleaning with a focus on pad and slurry performance. Recommendations for CMP consumables, based on measurement, were provided.

110. **DPS Metal Etch Tool Characterization**: The Applied Materials detached-plasma-source (DPS) tool was completely simulated and characterized. A 0.25 μm etching process was developed and commercialized. This tool was subsequently used in Sandia's MDL for advanced development.

111. **Dielectric Etch Mechanisms for High-Density Plasma (HDP) & Etch System Modeling**: The previously developed plasma-modeling codes were specialized to model the Applied Materials HDP reactor. Results showed good agreement between the models and the data provided by the industry.

112. **Oxide Etch Diagnostics**: This project determined the oxide etch parameters needed to predict and simulate dry-etch fabrication processes.

113. **New Film Development for Fluorescent Microthermal Imaging**: Fluorescent microthermal imaging uses fluorescing materials that are not environmental friendly. This project identified alternative materials and instructed member companies in the use of this failure analysis with the new materials. The resulting process was both cheaper and safer.

114. **193 nm Optics Degradation Modeling Enhancements and Pilot-Tool Modeling**: Codes to model the degradation of optic components in 193 nm lithography tools were developed. These codes were combined to provide a full-tool simulation of the optics system.

115. **Enhanced Measurement of Index of Refraction Change with Temperature in Fused Silica and Calcium Fluoride**: 193 nm optical models need accurate materials parameters such as the change in refraction with temperature of the 193 nm candidate lens materials. This project provided even more accurate answers than those provided in the previous year.

116. **Silicon Micromachining for Dimensional Metrology Support**: This project continued the effort, with NIST, to create electrical subnanometer metrology standards.

117. **Advanced Small-Batch Fast-Ramp Furnaces & Numerical Evaluation of Rapid-Thermal Chemical Vapor Deposition Equipment**: Sandia continued to perform optimization analysis with a finite-element thermal model of the Silicon Valley Group Thermco 300 mm furnace. The model was being used to explore different heater configurations and the resultant effect on flat-zone size and heater-power utilization.

118. **Compact Models of Wafer Stresses**: Sandia created and enhanced PC platform codes that predict the maximum-allowable furnace ramp rate as a function of mean wafer temperature to avoid stress-related breakage.

119. **Clean-Room Ergonomic Stressors**: This project collected semiconductor equipment maintenance data by observation. The analysis provided guidance in maximizing productivity for both equipment manufacturers and existing maintenance procedures.

120. **Plasma-Modeling Pilot**: The Aurora model, using specific reactor descriptions and operating parameters, as well as previously developed chemistry sets for etching semiconductor materials, allowed prediction of the optimum flow rates to minimize exhaust emission rates.

121. **Model-Based Reduction of Process Tool Exhaust**: This project optimized the exhaust gas flow while still providing sufficient flow to adequately handle hazardous material transport in and around microelectronic processing equipment.

122. **Wafer Ion Flux Analyzer**: This work was a continuation of an earlier project. Adjustments in the fabrication process yielded higher breakdown voltages. The redesign of one mask level allowed stripping of the resist before the long wet etch and shortened the process while still retaining characteristics of high-breakdown voltage.

123. **Radio-Frequency (rf) Harmonic Control**: Sandia worked with the IC industry to improve the control of IC fabrication tools that use rf sources to perform their processing functions.

124. **Assembly Test Chips for Ball-Grid Array (BGA) /Direct-Chip Attach (DCA)**: Using its assembly test chip (ATC), Sandia further developed the use of BGA and DCA packaging techniques. Sandia took data acquired from the ATCs and found it to compare favorably with model predictions.

125. **Improved Manufacturing of Low-Cost Liquid Encapsulants**: Sandia used its computational analysis and science base to improve the performance and cost of packaging ICs with liquid encapsulants.

126. **Validation of Water Recycling Models**: The objectives of this project were to demonstrate reliable models for the design of water recycle systems and to use these models in Sandia's MDL water-conservation plans.

127. **Reducing Water Usage In Semiconductor Manufacturing**: This project conducted a worldwide solicitation for "innovative technology" from the supplier community and began evaluating the most promising in Sandia's MDL.

128. **Combustible Environment Sensor**: New deposition techniques were used to place the sensing films on the surface of the detector. Model predictions agreed well with the measured data. A deposition control system was investigated that integrates the model for improved deposition control.

129. **Comb-Drive Particle Detector**: This project investigated the possibility of using Sandia's micromachining capability to detect particles. The technique looked promising but only for larger particles, i.e., those greater than 1 μm.

130. **Model-Based Reduction of Particle Contamination in Leading-Edge Interconnect Tools**: Sandia worked with several IC equipment manufacturers to make model-based reductions in particle contamination generated by the tool.

131. **Sensors for Fault Detection and Model-Based Process Control**: Sandia continued to develop and commercialize many sensors that aid in IC fabrication processes and in the development of new tools.

132. **Defect Removal**: Sandia continued to advance wafer-cleaning technologies. Both wet and dry cleans were investigated. Under particular scrutiny were the cleaning processes for pre- and post-CMP (chemical-mechanical-polishing) cleans.

133. **Minimum-Feature-Size Silicon On Insulator (SOI) Advanced Technology**: SOI wafers were processed in Sandia's MDL to evaluate the current status and viability of routinely using commercial SOI material.

134. **CMOS Analog IC Development**: A radiation-hardened analog CMOS (complementary metal oxide semiconductor) technology was developed and demonstrated exciting positive results.

135. **SVGL Cup Seal**: Sandia responded to an industry request to investigate and recommend a new or improved cup seal that would not generate particles in the tool.

4.6 Projects Completed in 1998

136. **CaF_2 Anneal Characterization & Simulation:** Earlier work showed that the material of choice for 193 nm lithography optical lens systems is calcium fluoride (CaF_2). This project characterized and was able to simulate the anneal process for this material. As a result of this work, better-quality CaF_2 is now becoming available.

137. **SVGL Thermal Modeling - Extension**: This work made specific recommendations for the Silicon Valley Group Lithography Systems, Inc. (SVGL), lens systems regarding issues of heat transfer in a production environment.

138. **Silicon Micromachining for Dimensional Metrology Support - Follow-on**: Overlay structures were developed to add to the critical-dimension (CD) structures. Work continued to create a National Institute of Standards and Technology (NIST)-certifiable nanometer measurement both for registration and for overlay.

139. **The Use of HRTEM Imaging for Certifying Critical-Dimension Reference Materials**: This project investigated the use of high-resolution transmission electron microscopy (HRTEM) of critical-dimension (CD) and overlay Micro-Electrical-Mechanical Systems (MEMS) structures as a way to create NIST-certifiable electrical nanometer measurements. All indications pointed to the success of this approach, and plans were made to continue the effort to make NIST-certified nanometer measurements.

140. **Numerical Evaluation of Rapid Thermal Processing (RTP) Equipment - Follow-on**: Sandia used numerical techniques to provide recommendations for improved RTP equipment—both for existing designs and for 300 mm designs.

141. **Model-Based Reduction of Copper Contamination**: Sandia used the codes developed for the reduction of particle contamination in IC processing equipment to investigate the possibility of copper contamination of CMOS (complementary metal oxide semiconductor) IC lines. The project showed that copper contamination is not a concern.

142. **Sensors and Modeling - Extension**: Sandia provided sensor data for improving several pieces of existing processing equipment. The sensor data was also used to model and simulate this equipment.

143. **Reduction of Water Usage - Follow-on**: This project used innovative and commercial sensor technologies to develop ultrapure water recycling models. Sandia verified these models in a recycling test bed at Sandia's MDL.

144. **Dielectric Etch Modeling & Diagnostics - Follow-on**: Researchers continued to develop mechanisms through diagnostic experimentation for modeling and simulating the etching of dielectrics. The effects of photoresist began being incorporated.

145. **DPS Metal Etch - Extension**: Delays in delivery of the detached-plasma-source (DPS) etch system required an extension to complete the milestones originally defined for this project. Additional diagnostic and model work was added to better characterize the 0.25 μm metal etch process. This process was transferred to industry. The tool became part of Sandia's development of a 0.35 μm four-level metal radiation hardened CMOS process.

146. **rf Studies 98 – Extension**: Work continued as needed to support rf issues that fall under Sandia's unique expertise in this area.

147. **Assembly Test Chips for Ball-Grid Array (BGA)/Direct-Chip Attach (DCA) - Follow-on**: Sandia continued to make outstanding progress in developing BGA/DCA technologies for both the industry and Defense Programs applications. Sandia's assembly test chip (ATC) has provided a unique vehicle for making these advances.

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