Performance of Front-end Readout System for PHENIX RICH

K. Oyama[1], H. Hamagaki[1], S. Nishimura[1], K. Shigaki[1], R. S. Hayano[2], M. Hibino[3], S. Kametani[3], J. Kikuchi[3], T. Matsumoto[3], T. Sakaguchi[3], K. Ebisu[4], H. Hara[4], Y. Tanaka[4], T. Ushiroda[4], C. G. Moscone[5], A. L. Wintenberg[5], and G. R. Young[5]

[1]Center for Nuclear Study, School of Science, University of Tokyo
3-2-1 Midori-cho, Tanashi, Tokyo 188-0002, Japan
[2]Physics Department, School of Science, University of Tokyo
7-3-1 Hongo, Bunkyo, Tokyo 113-0033, Japan
[3]Advanced Research Institute for Science and Engineering, Waseda University
3-4-1 Okubo, Shinjuku, Tokyo 169-8555, Japan
[4]Department of Electronics and Information technology,
Graduate School of Engineering, Nagasaki Institute of Applied Science
Nagasaki 851-0193, Japan
[5]Oak Ridge National Laboratory, Oak Ridge, TN 37831-6006, USA

Abstract

A front-end electronics system have been developed for the Ring Imaging Čerenkov (RICH) detector of the PHENIX experiment at the Relativistic Heavy Ion Collider (RHIC), Brookhaven National Laboratory (BNL). A high speed custom back-plane with source synchronous bus architecture, a full custom analog ASIC, and board modules with FPGA's and CPLD's were developed for high performance real time data acquisition. The transfer rate of the back-plane has reached 640 MB/s with 128 bits data bus. Total transaction time is estimated to be less than 30 μs per event. The design specifications and test results of the system are presented in this paper.

I. Introduction

The RHIC is the first colliding accelerator dedicated to high-energy heavy-ion collisions [1]. The PHENIX is a major experiment of the RHIC [2][3]. Primary goals of the PHENIX are studies of properties of nuclear matter at extremely high energy densities, and search for a new phase of hadronic matter called Quark Gluon Plasma (QGP). The RICH detectors are the main device for electron identification in the PHENIX [4].

The PHENIX has two RICH vessels. Each vessel is filled with a radiator gas of C_2H_6 or CO_2. The average number of photons is estimated to be $\sim$ 20 per electron track with C_2H_6. Produced Čerenkov photons are reflected by spherical mirrors, and detected by photo-multiplier tubes (PMT's) array. Each vessel houses 2,560 PMT's. The signals from the PMT's are fed into fast pre-amplifier cards mounted on the outside wall of the vessel. The gain of PMT is 10^7 typically, rise and fall time is 2 $\sim$ 5 ns. The amplified signals are carried via coaxial cables to the front-end electronics (RICH FEE) in the electronics racks on the detector carriages.

The RICH FEE measures the amount of charge and pulse timing information from the RICH PMT's at each Beam Crossing (B.C.) of the RHIC, of which frequency is around 10 MHz. The charge information is used to measure the number of photons. From the single to 10 photon de-

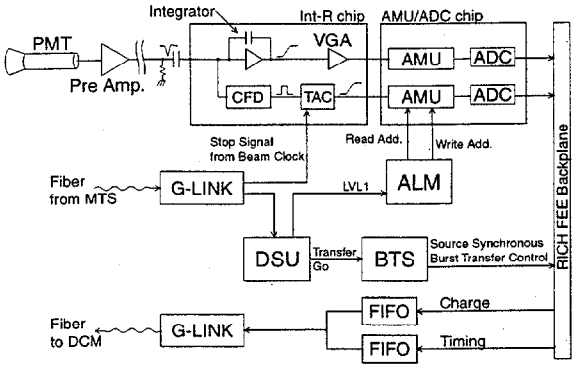

Figure 1: Block diagram of the data flow of RICH FEE.

tection is required. The input charge to the FEE is around 16 pC per photo-electron. For reasonable counting of number of photo-electrons, around 1 pC charge resolution were required. Therefore, bit resolution of charge measurement should be 8 bits or more. The timing information is used to reduce background. Because the flight velocity of electron emitted from heavy ion collision is the speed of light, the arrival time of the electron will be held in a small time range ~1 ns. To ensure the extraction of proper electrons, the time resolution of around 200 ps is needed. To satisfy those requirements, a full custom analog ASIC, modules, and back-plane were developed.

II. Overview of the RICH FEE

Figure 1 shows the data processing diagram of the RICH FEE. The RICH FEE receives amplified (gain ~ 10) PMT signal and digitize them and send them to the PHENIX Data Collection Module (DCM) via the G-LINK optical fiber. The G-LINK is giga-bits rate data transfer media developed in Hewlett Packard. The electrical isolation and high speed data transmission are achieved by the G-LINK.

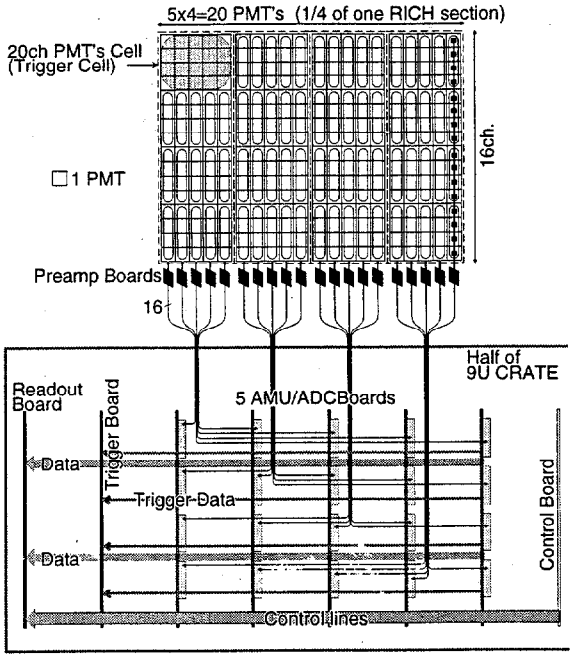

Figure 2: Mechanical block diagram of the RICH-FEE. Components in the half of crate are shown. The Controller board is placed in the center of the crate and commonly used to control both left and right half of the crate.

Also the RICH FEE receives control commands, trigger decision, and beam clock of the RHIC from the Master Timing System (MTS) of PHENIX via G-LINK.

The Signal from a pre-amplifier is fed into a Int-R chip. This chip is an analog ASIC developed by ORNL for the RICH FEE [5]. And it integrates active charge integrators and constant fraction discriminators (CFD).

Charge and timing data at every B.C. are stored in analog memory units (AMU) on the AMU/ADC chip which has 32 channels of analog memory units and 32 channels 12 bits Wilkinson type ADC's. The AMU/ADC chip was developed in ORNL [6][7]. Each analog memory unit has 64 memory cells. And cells which contain physically important data will be specified by first level trigger (LVL1

trigger) around 40 B.C. later, and be converted to digital data and sent to the back-plane. The AMU/ADC chip is commonly used for subsystems in PHENIX.

Unlike ordinary shift register or CCD image sensor, AMU is randomly accessible. Therefore, complex address management is indespensable for operation of AMU. Until LVL1 trigger decision comes or during the AD-conversion (takes ≥ 3 μs), cells are occupied and can not be used to store new data. The Address List Manager (ALM) manages the write and read address of the AMU and contains status of all cells [8].

For the implementation of all above functions required for RICH FEE as a system, the RICH FEE consists of AMU/ADC module, Control module, Readout module, Trigger sum module, and 9U crate with special back-plane. Figure 2 shows block diagram of RICH FEE.

An AMU/ADC module has eight Int-R chips and four AMU/ADC chips. An AMU/ADC module can digitize 64 channels of PMT signal. The digitized data by AMU/ADC module are sent to readout module via back-plane. A RICH FEE crate has 10 AMU/ADC modules corresponds to 640 PMT's, two Readout modules, and a Control module.

The data size from a RICH FEE will be more than 160 KByte per event. Event rate at RHIC will be around a few KHz to a few MHz and it depends on particle species. Then the RICH FEE has to send digitized data to DCM at around 160 MByte/s to 160 GByte/s. Of course 160 GByte/s is impossible. PHENIX decided that maximum trigger frequency should be less than 30 KHz, it corresponds to 480 MByte/s.

Because of the requirement of the high speed data transfer rate, a custum back-plane was designed and the source synchronous data transmission method was employed. The data transfer speed of the back-plane is around 640 MByte/s at maximum.

The Control module has timing receiver circuit, clock distribution circuit, ALM, scheduler, burst transfer controller and ARCNET controller. The ARCNET is simple network protocol and used to configure FEE on the startup.

The Readout module receives the digitized data from the five AMU/ADC modules, formats them, and sends them to DCM via G-LINK. Maximum instantaneous transfer speed from the Readout board to DCM exceeds 800 Mbps.

III. AMU/ADC MODULE

A. The Int-R chip

Int-R chip is an eight channel multi-function integrated circuit. The Int-R chip is preceded by a PMT and fast preamplifier and followed by an AMU/ADC chip. In the Int-R chip, the signal from each preamplifier is converted to two voltage values corresponding to charge and timing information.

Figure 3 shows the block diagram of the Int-R chip. The Int-R chip consists of charge integrating amplifier (CIA) and variable gain amplifier (VGA) for charge measurement, constant fraction discriminator (CFD) and TAC for timing measurement.

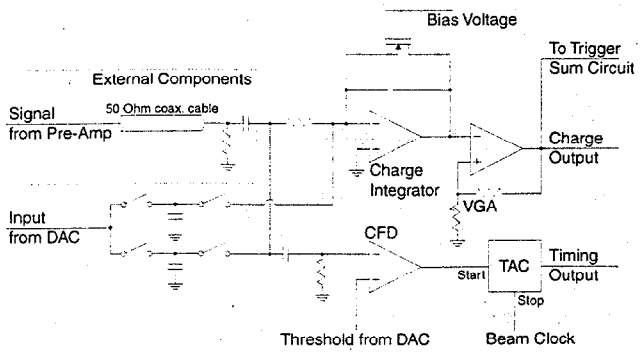

Figure 3: Block diagram of Int-R.

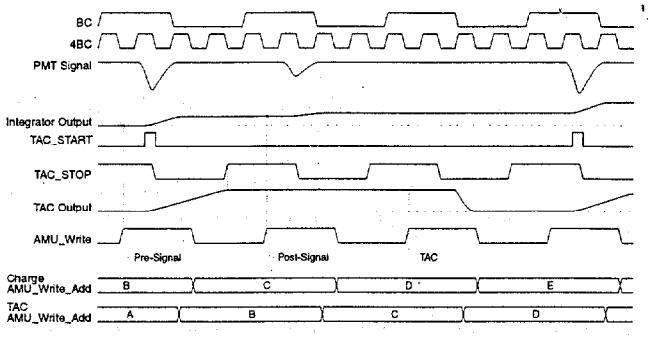

Figure 4: Typical operation timing diagram.

The maximum outputs of both VGA and TAC were adjusted to be 3.25 V that match the input dynamic range of AMU/ADC chips. The eight bits ADC resolution which corresponds to 500 ps is required for TAC. The chip also contains two four-channel signal summing circuits, calibration circuit and various DAC's. DAC's are configurable by serial control and eliminate the need of any external adjustment.

Figure 4 shows typical timing diagram of the Int-R chip. The CIA is always integrating amplified PMT signal. The deay constant of the CIA is adjusted by bias voltage supplied to the CIA.

The integration is quite effective to measure charge amount and to reduce high frequency (more than 100 MHz) continuous noise. However, very low frequency noise (less than 100 KHz) can not be removed by the integration. To remove the low frequency noise, we take two points of data for an event; Pre-Signal data and Post-Signal data. At the analysis stage, we take correlation of these two data, and low frequency noise are removed.

1) Performance Test for VGA

A test fixture board for Int-R was developed in ORNL to perform the overall test of Int-R chip.

The VGA tests was devided into three categories; the linearity test of V_{post}, V_{pre} and $V_{post} - V_{pre}$ of VGA outputs, the gain code (5 bits) test which changes the gain of amplifier from 4 to 12, the calibration voltage code (6 bits) test for calibration.

Figure 5 shows the linearities of VGA outputs from channel 1 through 8 as a function of input pulse voltage. The gain code is fixed at 0, 15 and 30.

The solid lines show the mean value (100 point) of $V_{post} - V_{pre}$, and the dashed lines show the RMS, respectively. The input pulse has the width of 10 ns, the rise time and the fall time of 5 ns, respectively. It is seen that the VGA keeps the good linearity up to 1.4 V which corresponds to seven photoelectrons. The RMS values vary from 10 to 20% of mean value independent to the input pulse voltages. Because of the noise of the test fixture board, these values are supposed to show the performance of the chip in the worst condition.

2) Performance Test for TAC

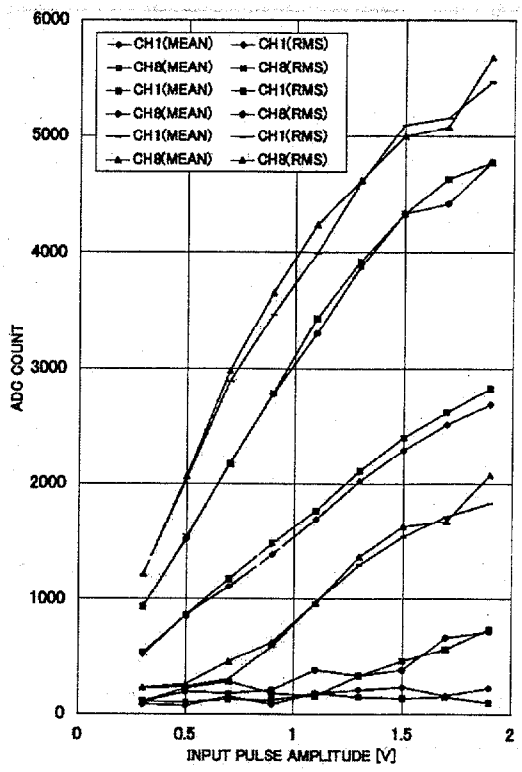

Figure 5: VGA Linearity

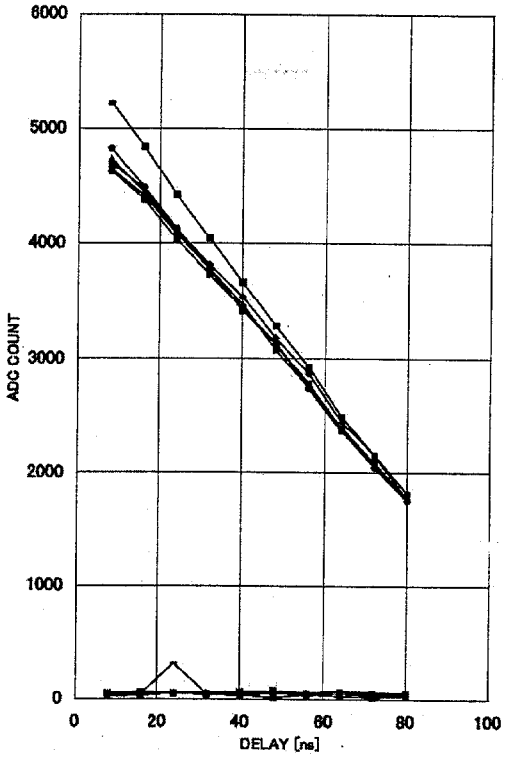

Figure 6: Delay vs. TAC output

Three different tests were applied to TAC; the TAC output measurement for linearity test, the calibration voltage test, the ramp code test. The delay of the input signal was changed from 8 ns to 80 ns. The CFD threshold code was set to be 60 not to be triggered by the baseline noise. Fig. 6 shows the linearities of the TAC's for eight channels. The solid lines show the mean value, and the dashed lines show the RMS, respectively. The TAC's have the excellent linearity. The RMS of each channel was about 50 ADC counts which corresponds to the resolution of 1.2 ns. With taking the noise from board into account, it can be said that the TAC has enough performance for RICH FEE.

B. Implementation of ASIC's

The four AMU/ADC chips and eight Int-R chip were implemented on the AMU/ADC module. Sixty-four signals, are fed into the single AMU/ADC module from behind of the back-plane.

The ADC on the AMU/ADC chip is operated in 10 bits conversion mode and at 100 MHz conversion clock which is generated by Synergy's PLL syntheizer chip and provided by PECL differential micro strip pair lines. AMU read/write address are managed by controller module and sent via back-plane.

AMU/ADC module has also burst transfer controller chip (ABC) built on an Altera MAX7000 CPLD. The ABC controlls output of AMU/ADC chips and generate data transfer clock for source synchronous data transfer to the

readout module via back-plane.

IV. Controller Module

The Control module is a mostly challenging part of the RICH FEE, and a highly integrated circuit of FPGA's, CPLD's, G-LINK optical link, and ARCNET.

The Control module distributes data acquisition timing to all other modules, manages the write and read address of the cells in the AMU, arbitrates data transfer from AMU/ADC modules to Readout modules, and controls the serial configuration lines on system initialization.

Figure 7 shows the block diagram of the Control module. The Control module consists of Clock Distribution daughter board (CDB), Generic ARCNET daughter board, Address List Manager (ALM), Decoder/Scheduler Unit (DSU), and Burst Transfer Sequencer (BTS).

The CDB receives four signals from MTS via G-LINK optical network; the Beam Clock (BC) timing generated from the beam transfer clock of RHIC accelerater, first level trigger bit (LVL1), mode bits, and ENDAT signals. Hewlett Packard's G-LINK optical module (HDMP-53D5) and receiver controller (HFBR-1024) were used to receive the data from MTS.

The Control module uses BC as system clock and provides it to all AMU/ADC modules as low jitter (less than 200 ps) timing signal of TAC stop via PECL differential point-to-point transmission lines. 100K ECL logic devices of Synergy Semiconductor Corporation and Category-5 twisted pair line were used for transmission of the timing signal.

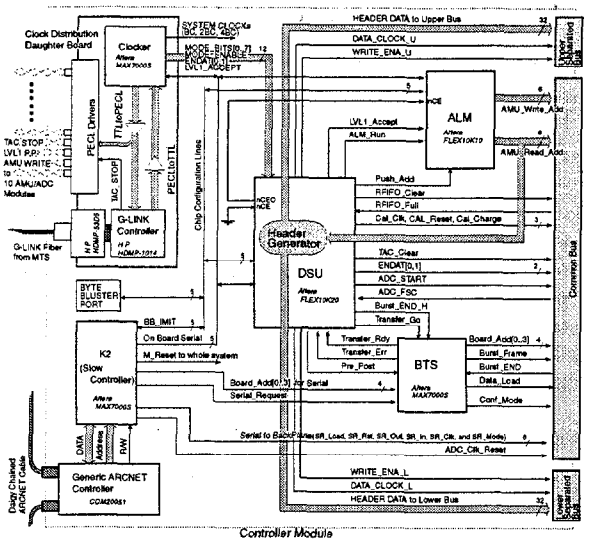

Figure 7: Block diagram of the Controller module

A LVL1 trigger bit is issued within 40 BC counts after an physically important event has happened. The RICH FEE have to keep the data for maximum 40 BC counts after the events to see if the LVL1 trigger is issued. The data in the AMU cell will be overwritten by new analog data after 40 BC counts. Mode bits consist of mode control data of the system, for example RUN, STOP, or INITIALIZE. LVL1 and mode bits are fed into DSU and ALM. ENDAT bits are sent to the Readout modules via back-plane and used as a start signal of G-LINK data transmission from Readout to DCM.

ALM has the logic to generate the read and write address of the AMU cells. The signals from VGA and TAC are written in the AMU cell addressed by ALM on each BC, and the only data that LVL1 triggers have been issued are readout from the corresponding cell and converted to the digital data. During the AD conversion of the analog data, ALM does not assign the corresponding cell to the write

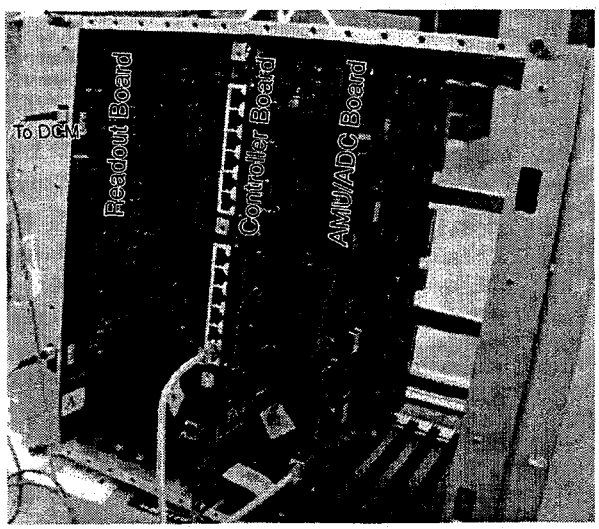

Figure 8: The RICH-FEE crate being evaluated.

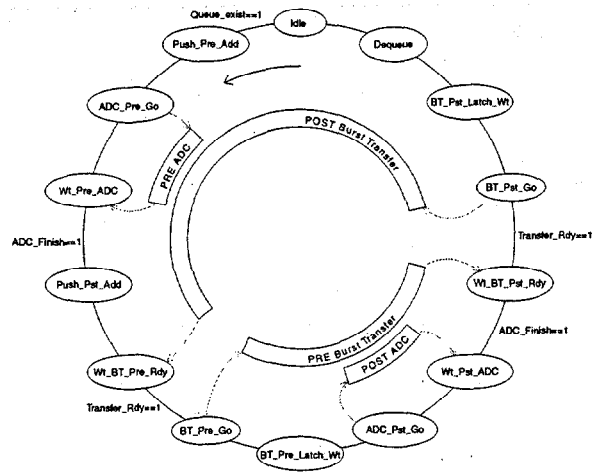

Figure 9: State transition diagram of the DSU and BTS. Outer loop is DSU state, next inner loop is ADC state in the AMU/ADC module, most internal loop is burst transfer state in BTS.

cell. The logic of ALM was build on Altera FLEX10K20 FPGA.

DSU receives mode bits and LVL1 signal from CDB, analyzes them, and controls whole system except for configuration serial lines synchronizing with BC. When the LVL1 trigger has been issued, DSU queues it on the event list to be digitized and prompts ALM to generate the read address of the corresponding AMU cell. DSU counts the number of BC and LVL1 trigger generated after the latest initialization, and sends them to the Readout module as a part of header data of the corresponding event. The logic of DSU was also build on FLEX10K20 FPGA.

BTS controls the burst transfer from AMU/ADC modules to Readout module. Figure 9 shows state machine transition diagram of the RICH FEE. The data transmission is based on the clock frequency of around 40 MHz, which is four times of the BC frequency. Since the transmission is needed to be done in high frequency and the clock skew in the back-plane is not negligible in the case, the RICH FEE employed the source synchronous data transfer method. In the source synchronous data transfer method, the BTS allows AMU/ADC modules to control the data send bus, and specified AMU/ADC module generates both data and transmission clock in itself. The same sources of data and strobe realize the skew free transmission. It is possible to realize the very high speed data transmission of 640 MByte/s after the optimization of BTS and transmission clock is achieved. BTS is implemented on Altera MAX7128S CPLD.

The RICH FEE is inaccessible and place in radiation area when the accelerator is in operation. Therefore, downloading of setting parameter of VGA gain, CFD threshold, configuration of FPGA, system wide reset and etc., is done through the ARCNET (Attached Resource NETwork).

V. Readout Module

The Readout module collects data from AMU/ADC modules, and sends the formatted data to the DCM. Two Readout modules are installed in one RICH crate, one each to the left and right 2 × 32-bits separate buses. A Readout module has two identical circuit, one each in the upper and lower parts, corresponding to the pairs of AMU/ADC chips for charge and TAC measurement. Header information and charge data are transferred to the upper and lower Charge FIFO's in parallel. The header information and TAC data are also transferred to the upper and lower TAC FIFO's. The data packet is built by the Readout Controller in the order of : the header, charge data and TAC data. Although both the pre- and post- data are sent to the FIFO's, the pre-TAC data are thrown out at this readout stage. The readout controller sends the data packet to Phase Shifter/Trailer Generator chips where longitudinal parities are calculated and added to the end of the data packet. The packet data are sent to the G-Link after being shifted by a half clock cycle in order to keep setup/hold time away from the rising edge of the 4BC. Finally the trailer bit information is added.

The readout is driven by the ENDAT0 or ENDAT1 signal received from the controller module when the Readout FIFO's are not empty. In the initial implementation of PHENIX, the data are transmitted via a single G-Link port. Data from upper and lower halves are sent sequentially under control of ENDAT0 and ENDAT1, respectively. The Readout Controller and the Phase Shifter/Trailer Generator are implemented in ALTERA FLEX 10K10 and MAX7128 CPLD's, respectively.

VI. Bus Architecture

A. Back-plane

Since the RICH FEE system need to digitize timing and charge information of 640 channels PMT data and transfer them to Readout module, ordinally VME or other back-plane can not be adopted for this. For this purpose, full costom back-plane and source synchronous bus architecture were introduced [11].

For the burst data transmission, the RICH back-plane has four independent separated bus (Upper-Left, Upper-Right, Lower-Left, Lower-Right) and each bus has 32 bits width, a clock line, and an enable line. Clock line is driven by 40 MHz in maximum. Then the maximum instantaneous transfer speed is 32 bits $\times$ 4 buses $\times$ 40 MHz $\sim$ 640 MB/s.

B. Source Synchronous Bus Architecture

Recently, the source synchronous bus is actively discussed for the high clock rate board design or the VME bus extension.

Usually in the common clock timing mode, the clock is generated elsewhere in the system and is used to launch data out of the driver and latch it into the receiver. The delay of the system clock is different from data, and the defference strongly depends on characteristics of signal line and capacitance of inserted modules on the back-plane.

In the source synchronous bus architecture, since both clock and data are generated by transmittter module, the time difference between clock and signal is compensated each other. The bus arbitorator does not generate common clock to system. If differences of electrical characteristics between driver/receiver elements for data and clock is smaller than clock period, speed of source synchronous bus system can be much higher than common clock timing mode, and 40 MHz bus clock speed have been achieved in RICH FEE.

VII. Conclusions

The RICH detector sub-system is in the final stage of construction. The RICH FEE development has been completed.

The serial programming with ARCNET, address management of AMU cells, and burst transfer have been achieved by complex FPGA and CPLD based circuit. A very high speed data transmission and data acquisition have been achieved.

A full custom ASIC was fabricated and was tested. It has good performance for the RICH FEE. Final prototype was fabricated and its evaluations are now in progress.

More tests with Data Collection Module and Master Timing Module are needed and now being prepared. PHENIX data acquisition will start in July 1999.

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