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TITLE: LEDA BEAM DIAGNOSTICS INSTRUMENTATION: BEAM CURRENT MEASUREMENT

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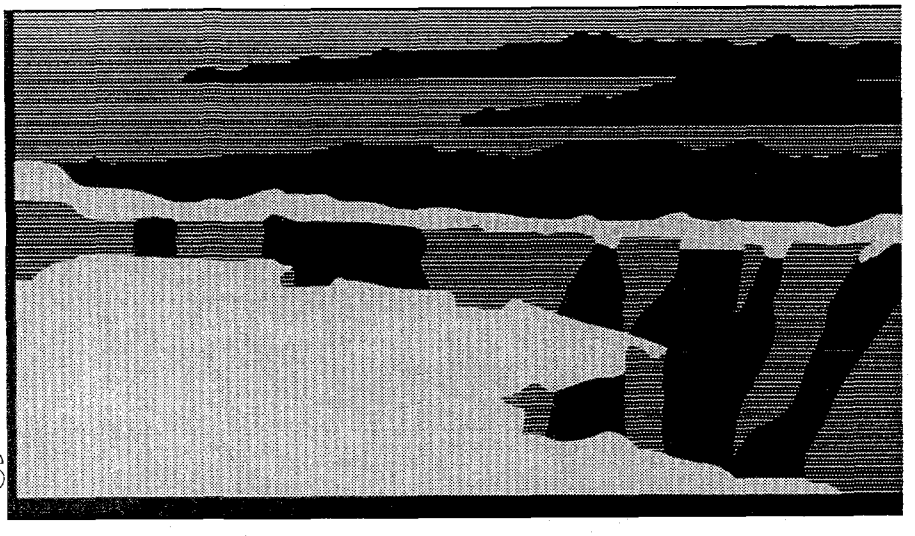

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LEDA Beam Diagnostics Instrumentation: Beam Current Measurement*

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Abstract. The Low Energy Demonstration Accelerator (LEDA) facility located at Los Alamos National Laboratory (LANL) accelerates protons to an energy of 6.7-MeV and current of 100-mA operating in either a pulsed or cw mode. Two types of current measurements are used. The first is an AC or pulsed-current measurement which uses three LANL built toroids. They are placed in the beamline in such a way as to measure important transmission parameters and act as a differential current-loss machine protection system. The second system is a DC current measurement used to measure cw beam characteristics and uses toroids from Bergoz Inc. There are two of these systems, so they can also be used for transmission measurements. The AC system uses custom processing electronics whereas the DC system uses a modified Bergoz® electronics system. Both systems feature data acquisition via a series of custom TMS320C40 Digital Signal Processing (DSP) boards. Of special interest to this paper is the operation of these systems, the calibration technique, the differential current loss measurements and fast-protection processing, current droop characteristics for the AC system, and existing system noise levels. This paper will also cover the DSP system operations and their interaction with the main accelerator control system.

INTRODUCTION

LEDA uses two types of current measurements: ac- or pulsed-beam, and dc- or average-beam. Pulsed or transient beam-current measurements provide transient-current information during startup, off-normal event recovery, and pulsed-beam commissioning [1]. These systems operate over a 10-Hz to 200-kHz bandwidth. The toroids consist of a single, high-permeability core with one multi-turn winding that acts as the secondary winding of a transformer with the beam acting as the primary winding. Average current measurements are most useful during normal facility operation. These systems operate over a dc to 100 Hz bandwidth. Average beam currents will be acquired with a dc-current transformer that consists of a multiple saturable-core beamline device and an electronics processor [2].

The pulsed beam current measurements use a single toroidal transformer core with two sets of secondary windings: one set for beam current detection and another set for an in situ calibration. The current detection-winding signals are initially processed using a simple analog feedback amplifier to increase the innate transformer L/R time

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constant, therefore, reducing the droop of the transformer signal [3]. The droop is a linear decay with a slope measured to be 6% per ms.

The dc beam current measurements use a modular parametric current transformer (MPCT) sensors and electronics modules from Bergoz®.

A VXI module has been developed to interface the analog sensors to the accelerator control system, EPICS (Experimental & Physics Industrial Control System). The same VXI module can be used for either type of sensor (ac or dc) and contains an on-board calibrator. Two internal TMS320C40 DSP modules control the calibration, data processing, and general operation of the VXI module.

An additional important feature of the ac beam current measurement system is to measure the current difference between any two adjacent toroids in real-time, and to use this information to calculate any integrated charge loss and to drive the accelerator fast-protect hardware. Each VXI module will have digital inputs and outputs that allow for various combinations of sensors to be used for this fast-protect mode. The integrated charge calculations and comparisons will be done in each of the DSP modules. Due to real-time timing considerations, it is necessary to limit these types of digital connections to adjacent VXI modules within the same crate.

DATA ACQUISITION AND PROCESSING

VXI Module

A single VXI motherboard design was developed for both the ac and dc measurement systems. A modular approach allows for the replacement or revision of sub-circuits to avoid the expense and time required in fabricating a full VXI module. Various plug-on modules include the ac AFEs (Analog Front End), dc Bergoz® AFEs, calibration current generator, dual output DAC circuit, two DSP modules, and the VXI interface circuit. Each motherboard supports two channels of beam current measurement. Electronics associated with the motherboard include various gate arrays for interfacing the modules; two 14-bit ADC channels, timing generation gate arrays, and power supply components. Two commercial DSP modules (TMS320C40), one per channel, control the operation of the module.

Most of the plug-on modules are connected with an eight-bit bus whose purpose is to allow set-up and control data to flow between them and either the DSP modules or the VXI interface. Separate dedicated buses control the flow of the real-time data streams. Figure 1 shows a block diagram of the VXI module.

The analog front-end circuits in the VXI module contain 14-bit ADCs that are clocked at 500 kHz. Each ADC is configured for ±2.5-volt full scale, straight binary (-FS is all zeros, +FS is all ones). The current-measuring circuit will present a voltage to the ADC such that ±2.5 volts equals ±200 mA of beam current. The transfer function is therefore, 40.96 counts per milliamp. The accuracy of the front-end circuits is limited to around ±2% due to gain uncertainties; so online calibration is required to achieve the system specifications of ±0.25 mA, or 0.2% of peak (for 0 to ±130 mA). The calibration system is covered later in this paper.

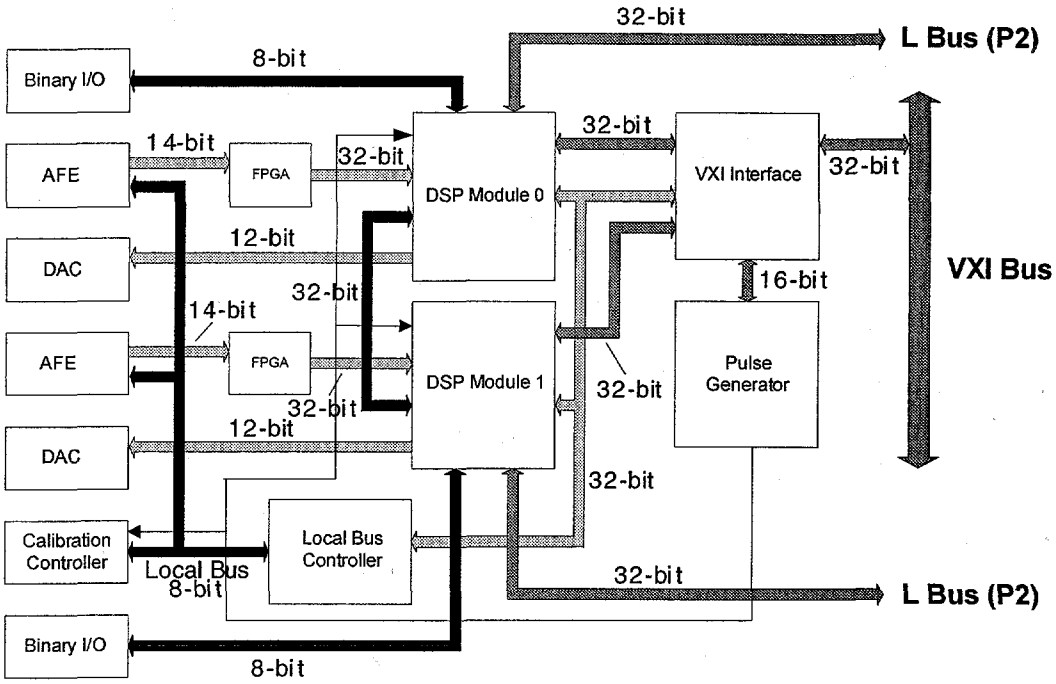

FIGURE 1. Block diagram of the VXI module.

Digital Signal Processor

The DSP modules act as the central processor for the VXI module. Each module contains a TMS320C40 chip from Texas Instruments and 2 MB of RAM. Spectrum Signal Processing® makes the modules. The various aspects of the DSP module performance and control are examined below.

DSP Functionality and Specifications – AC System

It is required that the DSP firmware performs the following tasks. Acquisition of data at 0.5 MS/sec rate. Perform calibration control and acquisition of known analog calibration pulse including calibration vector storage, gain and offset extraction, and correction of data for calibration values. Calculation of values for the fast-protect system including integrating lost charge from one toroid to the next thus determining the loss through the Radio Frequency Quadrupole (RFQ) and the loss through the HEBT (High-Energy Beam Transport). Keeping a running "box-car" integrator over 21 points taken at 100 μs intervals (which produces a trip point at approximately 21.6 μC). Signaling master fast-protect system by sending a hardware interrupt out the front of the VXI DSP board. Acquisition and output of waveforms on demand when called for by the external VXI control system.

The DSP firmware had to be written to include the fast-protect system requirements for the ac system. Since the sampling rate for data coming from the AFE was 0.5 MS/sec (every 2 μs), it was necessary to design the firmware with multi-leveled interrupts. For the initial prototype firmware without the additional fast protect code, it

was possible to devote principal processor time to any user requests (via the VXI bus). Using this approach, it was possible and acceptable to miss incoming data as long as the user's request for contiguous data was fulfilled. This approach also allowed enough processor time to perform other tasks such as filtering, housekeeping chores, etc. In the fast-protect approach, the highest priority had to be given to data collection, and hence, the DSP processor was not allowed to miss any incoming data points. Now data collection (with or without a specific user request) took a very high priority with only a fast-protect check at 100 μs intervals taking precedent. Since data was being taken every 2 μs, the DSP processor had little time to perform other tasks. It was found that user requests for data and downloading of data through the VXI bus could be accomplished in the background at about a 2 Hz rate for 2000 data points.

To compensate for these transfer rate problems, a new Direct Memory Access (DMA) operation was added to the DSP firmware. This DMA operation allowed the transfer of data from the AFE directly into memory located on the DSP module without the need of the DSP processor itself. This lessened the burden on the processor and allowed more time for data processing and VXI transfers.

DSP Functionality – DC System

The dc system processing constraints are much more relaxed than the ac system. This is due to the fact that the dc system has a lower frequency response and hence a lower necessary sampling rate. Additionally the dc system is not required to do fast-protection duty. The sampling rate used is 25 μs per sample or 4 kS/s. This is overkill for our 100 Hz bandwidth, but was much easier to implement given certain hardware constraints. Other than these differences, the dc system uses the same interface and DSP firmware as the ac system.

Basic Structure of DSP Operations

Figure 2 shows the function block diagram of the DSP module on the VXI motherboard.

From the point of view of the DSP module, the board consists of channels leading to either the front panel via the Digital-to-Analog Converter (DAC) or Analog Front End (AFE) via an FPGA, or through the VXI interface. In reality there are six of these channels, technically referred to as Communication Ports (CPs). The other CPs are used to talk to other DSP modules either on the same VXI board or on an adjacent VXI board (via the L Bus), a pulse generator/calibration controller, and a local bus (via a local bus controller).

As mentioned previously, the DAC continuously takes data at a 2 μs-sampling rate for the ac system. With a proper anti-aliasing filter on the AFE, this produces a signal band-limited to approximately 200 kHz. The dc system samples at a 25 μs-sampling rate. The data exits the ADC as 14-bit words. The gate arrays on the VXI DSP board encode these into 32-bit words with each word holding two sample points. Since the DAC is a 12-bit device, the highest order 12 bits of 16-bit DSP are sent to it when necessary.

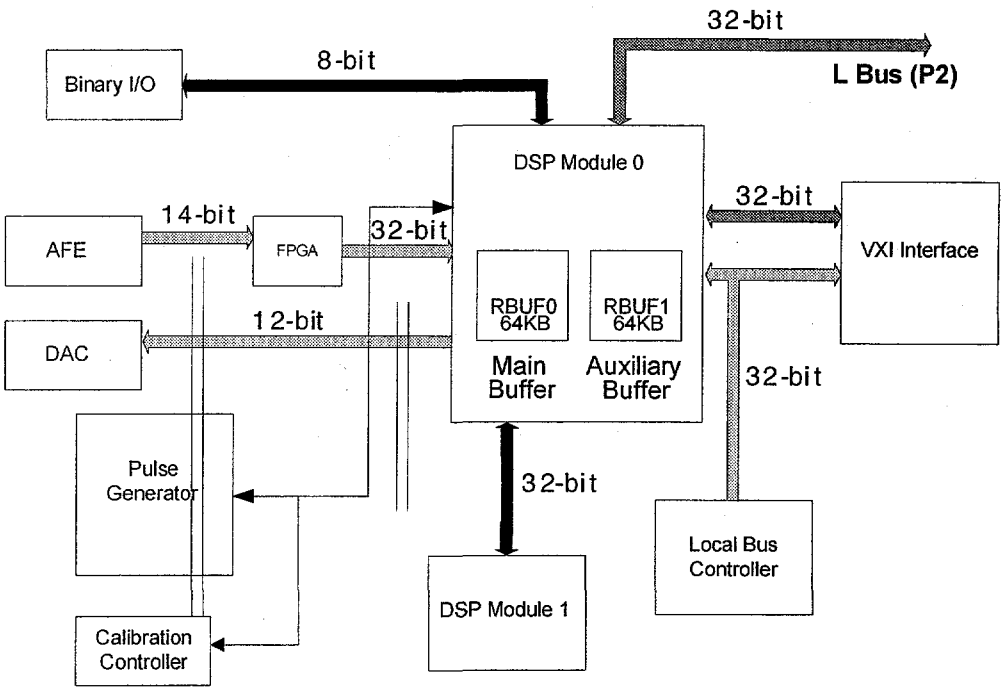

FIGURE 2. Functional block diagram of the DSP module on the VXI motherboard.

Calibration

Normally, the highest priority item for the DSP is data acquisition. System calibration, however, takes precedence on a limited basis. A user request for calibration causes the system to acquire data using a known calibration pulse as input to the toroid and then read the output through the normal input channels of the AFE. This information is used to calculate a gain and offset value based on the simulated "known" current values. The gain and offset are then used to calculate a calibrated data point from raw data whenever calibrated data is required. Each of the toroid DSPs have their own calibration routines that are based on the different characteristics of the toroids, and hence must be calibrated separately. The default calibration values are a gain of one and an offset of zero. The standard calibration equation is

$$Calibrated\ Data = (raw\ data + offset) \leftarrow gain\,. \tag{1}$$

Once the new gain and offset are calculated, they can be recalculated any number of times. There is also a user function that uncalibrates a DSP or re-sets its gain and offset to the default values.

Each VXI module supports two independent current measurements and contains a single calibration current source. The calibration source is triggered via the built-in timing channel in the module. The amplitude of the calibration current pulse is

programmable from zero to 127.5 mA via an 8-bit control bus (0.5 mA steps). The width of the pulse is fixed at 400 μs, and is delayed 400 μs from the leading edge of the trigger pulse for the ac system and fixed at 40 ms and delayed 40 ms for the dc system. In reality, the dc system should use a dc calibration signal, but because of the way the calibration signal was designed, it was much easier to use a very long calibration pulse to emulate a dc calibration signal. The 40 ms pulse works well in this regard. This calibration pulse will pass through the calibration windings on the two sensors connected to the VXI module.

The measurement system is designed for bipolar operation. The calibration will be done with a unipolar source, such that the design specifications are met over the 0 to ±128-mA range with slightly degraded performance over the full ±200-mA range. The response of the system is assumed to be symmetric, so the calibration for positive current will be "mirrored" for negative currents.

The calibration process makes a few assumptions regarding the response of the system. Most important is that the response is essentially linear at all current values between 0 and 128 mA. In particular, we assume that Equation 1 can describe the transfer function at any point. The calibration current source is used to measure the response of the system at two points, zero current and 127.5 mA. Note that the beam must be turned off during calibration.

For the ac system, knowing the droop rate for the calibration pulse it is possible to calculate the average value of the calibration pulse over the range of sampled points and compensate for the droop in the calibration software. Note that the dc calibration pulse as well as the dc system in general does not experience a current droop as the ac system does.

The data correction is always done at the maximum sampling rate of 500 kS/s for the ac system and 4 kS/s for the dc system. This allows each measurement channel to pass corrected data to another module to be used for high-speed beamloss measurement and fast-protect functions in the ac system. This will be covered in the section on the fast-protect system.

Differential Fast-Protect System – AC System Only

The differential current fast protect system is designed to protect the machine from being damaged by the beam. There are three AC toroids being used for this system. Toroid #1 is located just before the RFQ. Toroid #2 is located just after the RFQ and at the beginning of the HEBT. Toroid #3 is located at the end of the HEBT right before the beam stop.

By measuring any current lost between toroids #1 and #2 and toroids #2 and #3, it is possible to determine if any damage is being done to either the RFQ or the HEBT. The property of interest is the lost current integrated over time that is the lost charge. It has been determined [4] that 21.6 μC of focused beam in one area will cause unacceptable damage to the machine. It is therefore a requirement to shut the beam down if the charge lost between toroids #1 and #2 (RFQ) or toroids #2 and #3 (HEBT) approaches the 21.6 μC threshold within a boxcar integration time of 2.1 ms.

In order to determine the lost charge in either section (RFQ or HEBT), the lost current must be integrated over time. This is done with a running boxcar integrator.

Since each VXI board holds two DSP modules, two VXI boards are needed for the three-toroid setup.

The DSP module for toroid #1 (hereafter referred to as DSP #1) calculates its calibrated data from toroid #1 (using Equation (1)) and on a 100 μs timeout generated by DSP #1 itself (asynchronous to any other process), it passes the data point to the DSP module for toroid #2 (hereafter referred to as DSP #2). DSP #2 generates a hardware interrupt caused by the incoming data from DSP #1. DSP #2 now calculates a calibrated current data point (the latest acquired; calculated using Equation (1)) and subtracts it from the data point received from DSP #1. This difference is placed in a running twenty-one point boxcar sum. The new value for the sum is now compared to the threshold of 21.6 μC to determine if a fast protect trip should be generated. Twenty-one data points or 2.1 ms was chosen as the integration time since this is the theoretically shortest time over which a distributed charge accumulation can damage the machine [4].

After DSP #2 acquires calibrated current data from DSP #1 it passes its most recently acquired calibrated data to the DSP module for toroid #3 (hereafter referred to as DSP #3). This requires the use of the L Bus that passes data to an adjacent VXI module using the P2 connector of the VXI bus as shown in Figures 1 and 2. Note that VXI board #2 MUST be in an adjacent VXI slot just to the right of VXI board #1.

The damage point of 21.6 μC is converted to counts for the internal DSP comparison. The boxcar integrator sums the twenty-one points (2.1 ms of data sampled at 100 μs intervals) of data using 32-bit integer addition. If any contiguous sum of a sequence of twenty-one data points exceeds this set point in counts, the fast protect system is tripped by dropping an output pin of the DSP module low (TTL) which is sent to the VXI card front panel (the binary I/O blocks shown in Figure 1) and piped to the master fast protect module via a local patch panel. This shuts down the accelerator. Note that the trip is active low hence forcing a trip if system integrity should be lost.

SYSTEM RESULTS

An example graph of data is shown in Figure 3. This graph shows the output of an ac toroid positioned just before the RFQ. Note that the pulse was 825 μs long. The graph shows roughly the last 180 μs of the pulse. It is possible to archive data over each macropulse or to archive the averages from each macropulse over time. The repetition rate was between 2 and 10 Hz. The average data could be saved at set intervals (say once every 30 seconds) depending on need and data storage space.

Depending on the tune of the machine, the variation from pulse to pulse could vary from less than a percent to a few percent. When the data in Figure 3 was taken, the pulse-to-pulse standard deviation was 3.3 percent, though deviations of less than one percent are more common for a typical tune. The standard deviation within the pulse was 0.74 percent.

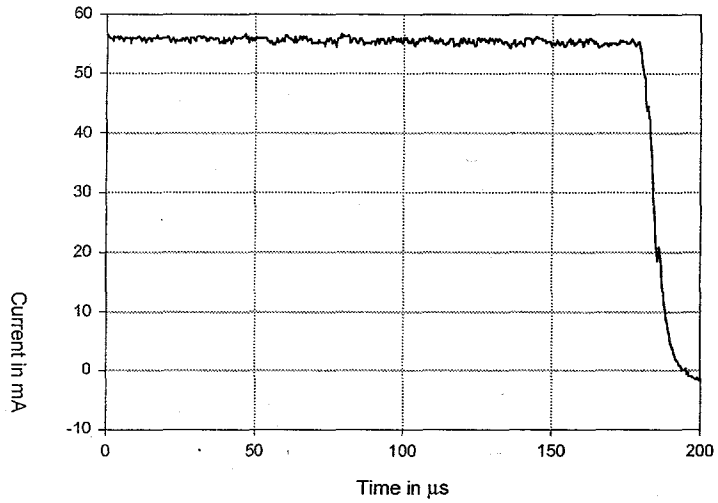

FIGURE 3. Graph of current measured at the ac toroid just before the RFQ during a typical beam run.

CONCLUSION

The beam current measurement systems for LEDA, including both the ac and dc systems, worked very well for the first year of operations. All systems, including calibration and fast-protect, have been implemented and meet or exceed design specifications. The fast-protect system trips consistently in both simulated and real spill conditions. The DSP-motherboard design has proven to be both easy to maintain and very robust. This system will continue to be used for future current measurement systems as well as other diagnostic systems.

ACKNOWLEDGMENTS

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REFERENCES

1. Gilpatrick, J. D., et al, *LEDA and APT Beam Diagnostics Instrumentation*, Proceedings of the 1997 Particle Accelerator Conference, Vancouver, B.C., Canada, pp. 2232-2234.
2. Power, J., et al, *Beam Current Measurements for LEDA*, Proceedings of the 1999 Particle Accelerator Conference, New York, 1999.
3. Gilpatrick, J. D., et al, *Low Energy Demonstration Accelerator (LEDA) Beam Instrumentation: RFQ-Accelerated Beam Results*, Proceedings of the 1999 Particle Accelerator Conference, New York, 1999.
4. William Sellyey – Private Communication.