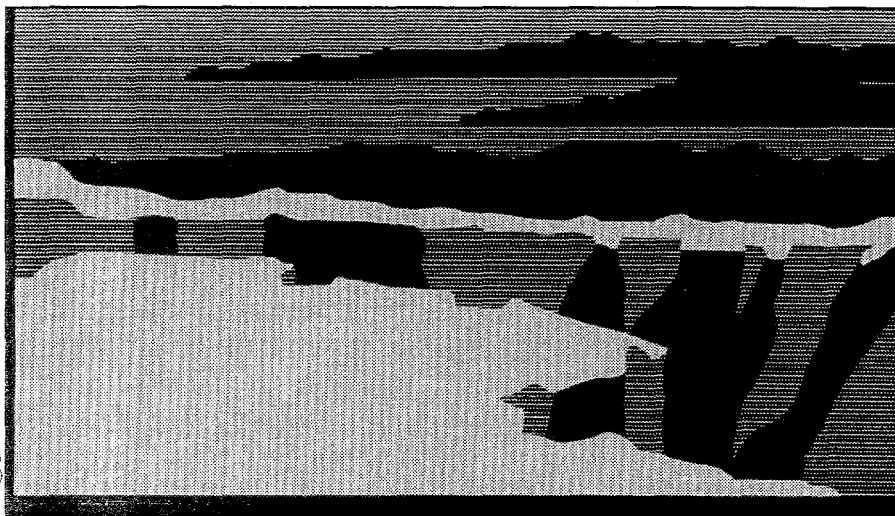LA-UR-00- 2359

TITLE: LEDA BEAM DIAGNOSTICS INSTRUMENTATION: BEAM
POSITION MONITORS

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LEDA Beam Diagnostics Instrumentation: Beam Position Monitors[*]

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Abstract. The Low Energy Demonstration Accelerator (LEDA) facility located at Los Alamos National Laboratory (LANL) accelerates protons to an energy of 6.7-MeV and current of 100-mA operating in either a pulsed or cw mode. Of key importance to the commissioning and operations effort is the Beam Position Monitor system (BPM). The LEDA BPM system uses five micro-stripline beam position monitors processed by log ratio processing electronics with data acquisition via a series of custom TMS320C40 Digital Signal Processing (DSP) boards. Of special interest to this paper is the operation of the system, the log ratio processing, and the system calibration technique. This paper will also cover the DSP system operations and their interaction with the main accelerator control system.

INTRODUCTION

The LEDA BPM system provides several services to the commissioning team. First, it provides information that allows the centering of the beam in the HEBT and into the beamstop. Secondly, it allows verification of the quadrupole magnetic field settings by offsetting the beam position from magnetic lattice center.

The position measurement systems consist of micro-stripline BPMs, coaxial cables, analog front-end (AFE) processing systems including Analog Devices AD8307 logarithmic amplifiers, real-time error correction via digital hardware, digital signal processing chips, and control system interfaces. The beamline probes themselves are a four-electrode micro-stripline design. For more details and a photograph see [1]. For details of the AFE and AD8307 log-amplifier see [2].

It is possible to use one of several common processor transfer functions for implementing a beam position measurement system. These include difference-over-sum, arctan, log ratio, and normalized power difference functions [3, 4]. The LEDA system uses the log-ratio technique. Advantages of the log-ratio system over other systems include improved sensitivity and linearity. The main drawback is ripple errors due to the approximation nature of real-world log amplifiers [5]. They use a cascade of nonlinear cells to approximate the logarithmic function in series of piecewise-linear segments. This error is corrected using the calibration technique detailed in a later section of this paper.

It is necessary to understand the individual characteristics of each beam probe before they are placed in the beamline. A mapping technique performed in a well-equipped laboratory is necessary to understand the sensitivities needed for the log ratio calculation [1].

SIGNAL PROCESSING AND DATA ACQUISITION

A VXI module has been developed to interface the analog beamline sensors to the accelerator control system, EPICS (Experimental & Physics Industrial Control System). The same VXI module can be used for all beam position measurements and contains an on-board calibrator. Two internal TMS320C40 DSP modules control the calibration, data processing, and general operation of the VXI module.

Figure 1 shows a block diagram of the VXI module design.

FIGURE 1. Beam position monitor VXI module block diagram.

The signal from the upstream ports of the BPMs are run over long-length (approximately 170 feet) rf coaxial cables and fed into the inputs labeled in Figure 1. The BPM AFE processes this raw 350 MHz signal through various stages including the logarithmic amplifier ending up at a 14-bit A/D converter. See [2] for more details. Only twelve bits are used [2]. This signal is used to address a 4096 location RAM look-up table (RAMLUT). These RAMLUTs are located on the AFEs themselves and are addressed using Field-Programmable Gate Arrays (FPGAs). The RAMLUTs are

twelve bits wide, but the values are sign-extended to sixteen bits before being passed to another set of FPGAs downstream labeled DSP FPGA #1 and #2. These FPGAs are used to calculate the sum and/or differences of the raw lobe signals as shown in Figure 2.

FIGURE 2. AFE Look-Up Tables (RAMLUTs) and DSP Field-Programmable Gate Arrays (FPGAs).

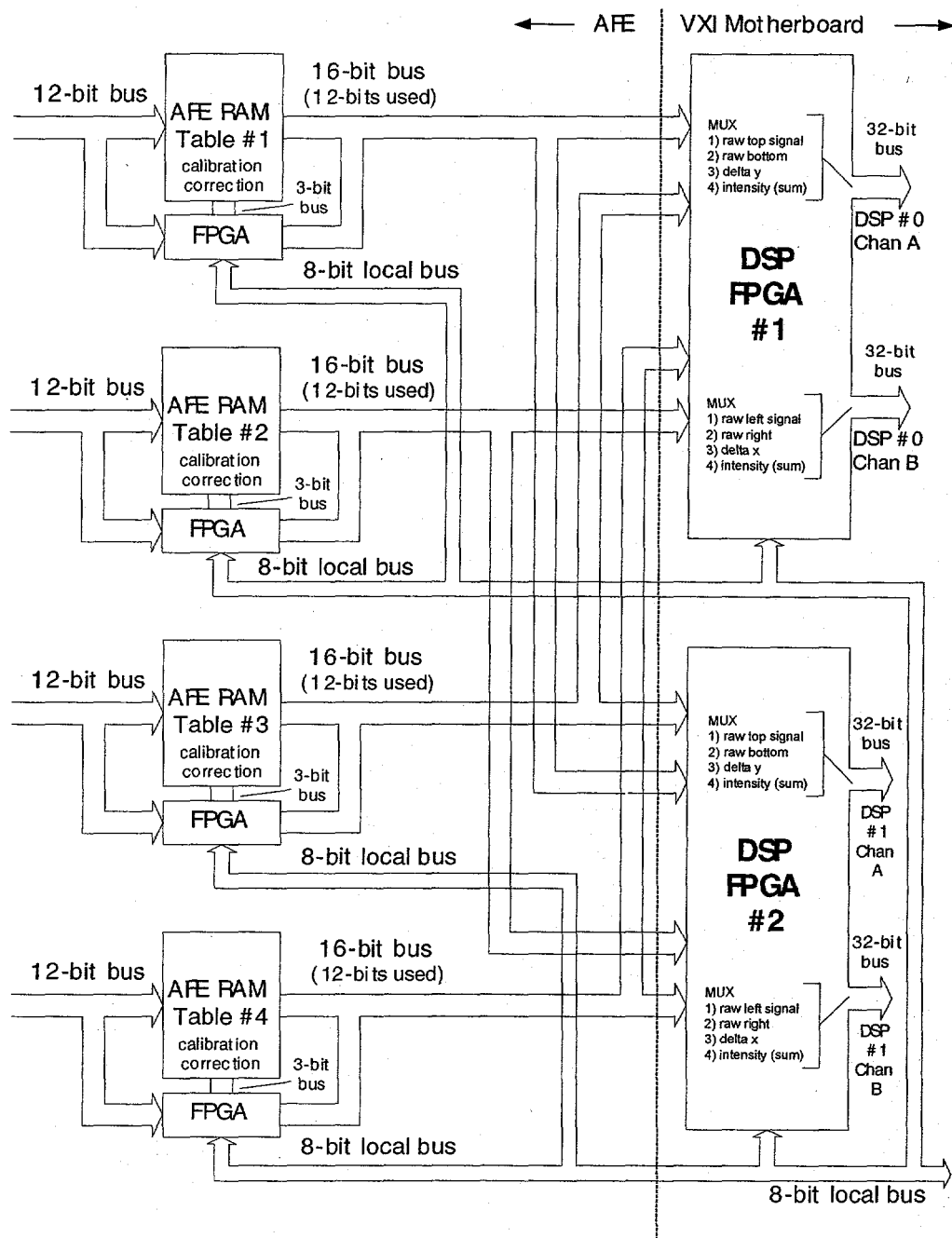Each DSP has two input channels 32-bits wide. These are labeled in Figure 2 as DSP#0 Chan A, DSP#0 Chan B, DSP#1 Chan A, and DSP#1 Chan B. The inputs for

each input channel are selectable using a muxes in each of the DSP FPGAs. These muxes are controlled by the 8-bit local bus (shown in Figures 1 and 2) that is controlled by the Local Bus Controller in Figure 1. The Local Bus Controller is controlled in turn by either DSP module. Note that a 3-bit bus runs from another set of FPGAs to each AFE RAM Table. This bus is used to select one of eight possible RAMLUTs located in each AFE RAM Table chip in Figure 2. As suggested in Figure 2, the RAMLUTs are used to perform calibration correction. The use and construction of these tables will be covered in the next section of this paper, entitled "System Calibration". It is noted that the RAMLUTs need to be initialized and loaded after each VXI module power cycle. This is accomplished using the 8-bit local bus shown in Figures 1 and 2.

Each of the AFE RAM Tables receives input from one lobe. AFE RAM Table #1 is the top lobe, AFE RAM Table #2 is the left lobe, AFE RAM Table #3 is the bottom lobe, and AFE RAM Table #4 is the right lobe. Each DSP FPGA receives input from each RAMLUT. Call these RAMLUT_TOP, RAMLUT_LEFT, RAMLUT_BOTTOM, and RAMLUT_RIGHT, respectively. Each DSP FPGA output channel can output one of four values as specified in Figure 2. The raw signals equate to each of the RAMLUT_? values. Delta x is just RAMLUT_LEFT minus RAMLUT_RIGHT. Delta y is RAMLUT_TOP minus RAMLUT_BOTTOM. The intensity or sum is just RAMLUT_TOP plus RAMLUT_RIGHT plus RAMLUT_BOTTOM plus RAMLUT_LEFT. A standard operating mode may use DSP#0 Chan A for delta y, DSP#0 Chan B for delta x, and DSP#1 Chan A for intensity. Alternatively, DSP#0 Chan A could be used for raw top signal, DSP#0 Chan B for raw left signal, DSP#1 Chan A for raw bottom signal, and DSP#1 Chan B for raw right signal. In this case, the difference and sum calculations would have to be done in either the DSP modules or by a software program located in the computer controlling the VXI crate.

SYSTEM CALIBRATION

The ideal response of a logarithmic amplifier can be stated as

$$\overline{\qquad} \tag{1}$$

where v_{in} is the amplitude of the input signal, v_{ref} is a reference voltage, and K is an amplitude constant [6]. Both v_{ref} and K are dependent on the particular log amp chosen. Since the log amp is non-ideal, there are small perturbations in its transfer function and distortion effects at the upper and lower ends of its dynamic range. By using digital error-correction the non-ideal performance in the log amps and other system non-linearities can be taken out of the overall transfer function of the system. The system calibration provides a method to determine the error correction values.

As stated in the previous section, the error correction takes place in the RAMLUTs. The 12-bit digitized lobe signals from the analog section are used as an address for the

4096-point (12 bit) deep RAMLUT. The 12-bit wide output word is used as the new corrected lobe input into the DSP FPGAs.

The system calibration is a method for placing known values into the downstream ports of the BPM and measuring the generated output signal at the DSP. The RAMLUT tables are bypassed for this measurement. This calibration output data is compared to the theoretical values that would be obtained at the DSP with the known input power levels. These theoretical values take into account the individual characteristics of the attenuators used in the calibration process. They are known a priori by measurements made in the laboratory using a precision network analyzer. Since the response of the system transfer function depends so much on the dynamic range of the log amp, the calibration must be done over a large range of power levels. This is accomplished by means of a bank of attenuators on the calibration board. A fixed amount of power is generated at 350 MHz on the calibrator board and then attenuated in 1-db steps over a range of 128 steps. With an input power of 25 dBm (which translates to about 17 dBm due to the cable and splitter), it is possible to calibrate over the full dynamic range of the log amplifiers. See [2] for details on the log amp's dynamic range. Once this data is collected, a linear interpolation routine is used to generate the remaining values in the 4096 deep RAMLUT. This effectively fills in the gaps between the 1-dB steps. Figure 3 shows a block diagram of the systems used in this process.
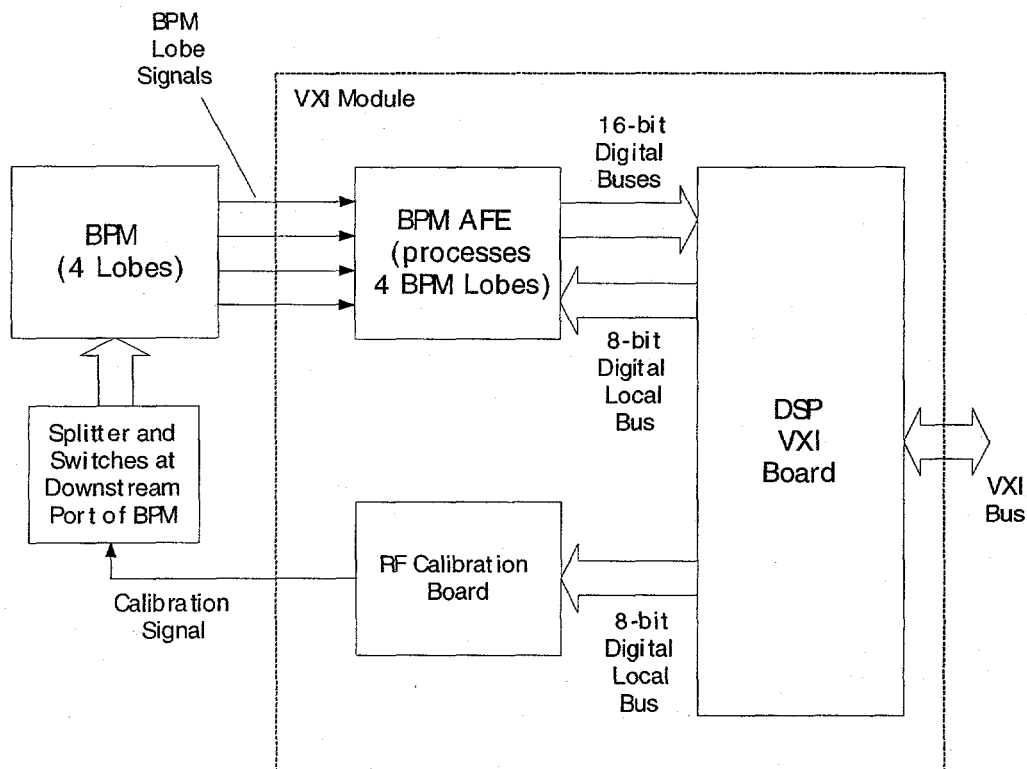

FIGURE 3. The position measurement system including the calibration process components.

The RAMLUT tables are calculated offline using LabVIEW® System Software from National Instruments®. The table values are loaded into the RAMLUTs using the 8-bit local bus shown in Figures 1, 2, and 3. A test routine was written to check how well the RAMLUTs work once loaded. This "test calibration" routine is performed immediately after a successful calibration and works as follows. A range of signal powers is placed into the downstream ports by means of the attenuators on the calibrator board. The values for these signals are measured at the DSPs as with the calibration. The main difference is that now the RAMLUTs are used to process the data. This measured data is subtracted from the theoretical values that would be obtained at the DSP with the known input power levels. These values are now plotted versus attenuation thus obtaining an estimate of system performance over the full dynamic range. An example graph of the system calibration and test calibration is shown in Figure 4. The graphs on the right side of the figure show the calibration system response for each of the four lobes of one BPM. The abscissa lists attenuation in dB (0 dB corresponds to 17 dBm) and the ordinate displays output signal response in counts (from 0 to 4095 or a 12-bit range). The graphs on the left of the figure show the corresponding test calibration output. The abscissa is attenuation in dB and the ordinate displays output signal error in dB. An ideal graph would have a zero value for all power levels. Note that the usable dynamic range of the system is from about 10 dBm to about –35 dBm. This is typical of the BPM systems at LEDA.
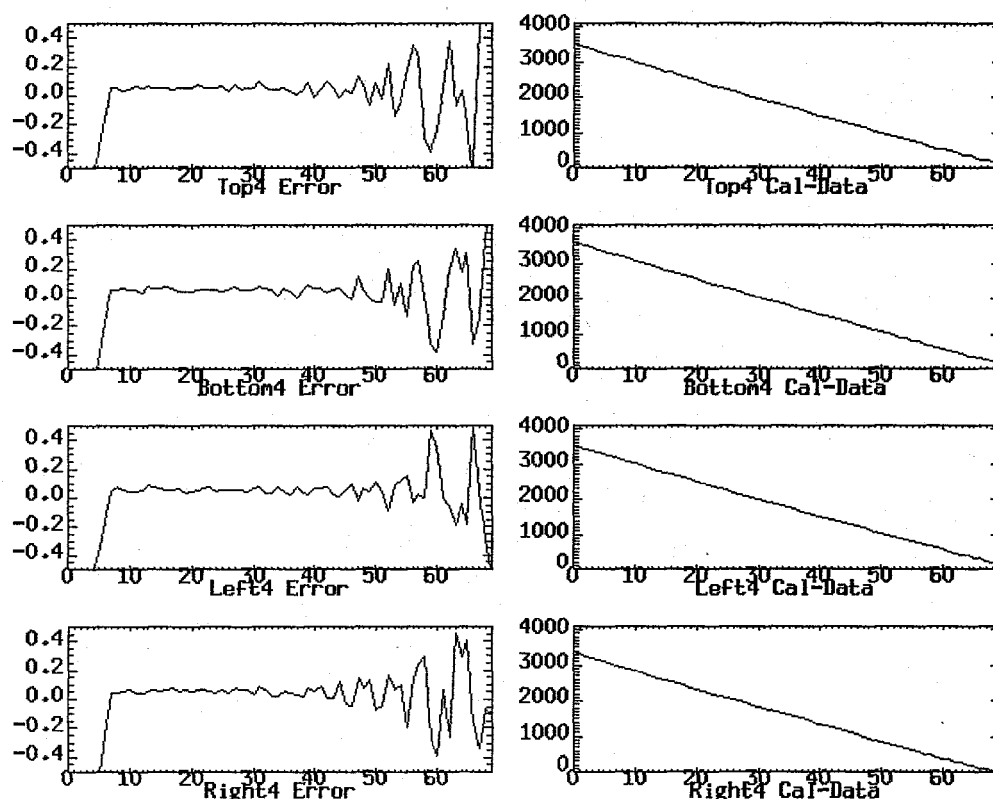

FIGURE 4. Calibration response in dB of attenuation versus counts (right side) and test calibration response in dB of attenuation versus output error in dB (left side) for four probes of a typical system.

SYSTEM CONTROL AND DATA ACQUISITION

One of the problems faced during the design and implementation of the position monitoring system was that of system control and data acquisition. The BPM VXI module is capable of handling one beamline sensor. Two DSP modules collect a total of four channels of data. After the DSPs collect and process the data, it is necessary to get the data into the EPICS control system for further processing, display, and data storage. If this is done with a 680x0 Kinetics system slot-zero controller for the VXI crate, these responsibilities fall on the shoulders of the EPICS system application programmers. This can be problematic as programming resources can be scarce at times. In addition to this is the fact that a LabVIEW® program script (or Virtual Instrument (VI)) needs to be written by the design engineer for testing and debugging of the system hardware. Now two programs need to be written and debugged that accomplish virtually the same task.

It is obvious that the ideal solution is a programmable interface that will allow LabVIEW® VIs to interface with an EPICS database. K. U. Kasemir has solved this problem by designing an ActiveX interface into LabVIEW® that allows the manipulation of EPICS process variables. This interface is known as Portable Channel Access (PCA). High-level operator screens are written by EPICS application programmers and provide a transparent connection to low-level LabVIEW® VIs. These VIs can be written by the design engineer, EPICS applications programmer, or others, as LabVIEW® is fairly simple to learn.

LabVIEW® runs on a multitude of systems, but the easiest to use and interface with is a PC running Microsoft Windows NT®. The PC can be interfaced to the VXI crate via a PCI/MXI-2 bus extender. This extender, available from National Instruments®, allows a VXI crate to appear to a PC as an extension to the PCI bus. LabVIEW® easily incorporates the VXI cards into its functionality. This allows integration of the BPM VXI module into the PCs architecture. Simple LabVIEW® VIs are used to interface with the DSP modules. Firmware is written in the C programming language, compiled, and loaded in EEPROMs on the DSP Modules. This firmware tells the DSP chips how to operate on data coming from the BPM AFEs and interface with the PC and LabVIEW® VIs. The LabVIEW® VIs then talk to the EPICS system via PCA.

CONCLUSION

The beam position measurement systems for LEDA worked very well for the first year of operations. All systems, including system calibration, been implemented and meet or exceed design specifications. The DSP-motherboard design has proven to be both easy to maintain and very robust. Integration to EPICS via Portable Channel Access has worked extremely well and most of the bugs have been worked out of the system. For more results see [7].

The next version of the beam position system will be used in the upcoming beam Halo measurements later this summer into next fiscal year. Planned upgrades include a

new AFE design as well as a new switching scheme for integrating the calibration signal into the beamline probes. The beam position measurement systems will also be used for a local project entitled the Isotope Production Facility (IPT). New improvements to the system for IPT will include a calibration system that will operate at all times by producing and measuring calibration pulses between actual beam pulses.

ACKNOWLEDGMENTS

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