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Title: Design of the SNS Normal Conducting LINAC RF Control System

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DESIGN OF THE SNS NORMAL CONDUCTING LINAC RF CONTROL SYSTEM

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Abstract

The Spallation Neutron Source (SNS) is in the process of being designed for operation in 2004. The SNS is a 1 GeV machine consisting of both a normal-conducting and super-conducting linac as well as a ring and target area. The linac front end is a 402.5 MHz RFQ being developed by Lawrence Berkeley Lab. The DTL, being developed at Los Alamos National Laboratory, is also a copper structure operating at 402.5 MHz, with an 805 MHz CCL structure downstream of it. The expected output energy of the DTL is 87 MeV and that of the CCL is 185 MeV. The RF control system under development for the linac is based on the Low Energy Demonstration Accelerator's (LEDA) control system with some new features. This paper will discuss the new design approach and its benefits. Block diagrams and circuit specifics will be addressed. The normal conducting RF control system will be described in detail with reference to the super-conducting control system when appropriate.

1 RF CONTROL FUNCTION OVERVIEW

The RF system for the SNS linac is well described in M. Lynch's paper in these proceedings [Ref. 1]. Specifically of interest to the RF Control System (RFCS) is the fact that one control system is required for each klystron. The RF control system must support operation of 402.5 MHz and 805 MHz normal conducting (NC) cavities, as well as 805 MHz superconducting (SRF) cavities. The intent of the RF Control system design is to provide a system which requires minimal changes to support all three cavity types. For each, the governing specification is to provide cavity field control within ±0.5% amplitude and ±0.5° phase.

The functions required of the RF Control System are as follows: Cavity Field Control; Cavity Resonance Control; HPRF Protection; and Reference generation and distribution. Figure 1 shows a block diagram of the RFCS. VXIbus is the selected architecture for the first three functions.

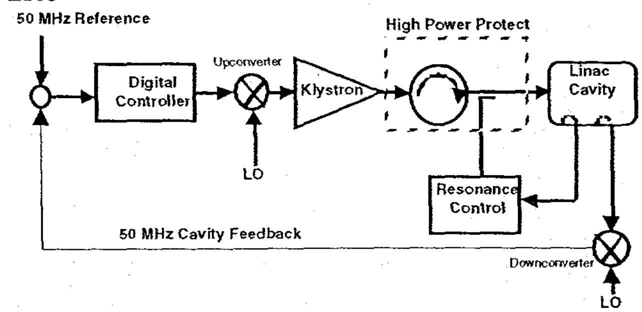

Figure 1: RF Controls for SNS

The present design combines cavity field control and resonance control into a single double-wide VXIbus module. The HPRF Protect function will be performed by another VXI module. Both are supported by a Clock Distribution Module. Physically this design differs from its basis (the Accelerator Production of Tritium RF control system) where Resonance Control and Field Control are individual modules and the HPRF Protect function requires a VXI module plus multiple chassis. Experience on LEDA has allowed us to reduce the number of channels supported by the HPRF Protect circuitry in such a way as to perform all required functions in a single VXI module only. We have also seen that combining the Field and Resonance Control functions into a single VXIbus module reduces the amount of backplane cross-communication and simplifies the module-to-module interconnections. A conceptual VXIbus crate layout is shown in Figure 2. Due to the physical location of the klystrons for the NC cavities, we are only putting one RF Control system into a VXI crate. However, the SRF cavities' klystrons are located close enough together to encourage savings in crate and rack cost by co-locating two control systems in a single crate. We cannot do this for the NC systems however because the distances between adjacent klystrons is large enough to detrimentally affect our control margin due to increased signal group delay.

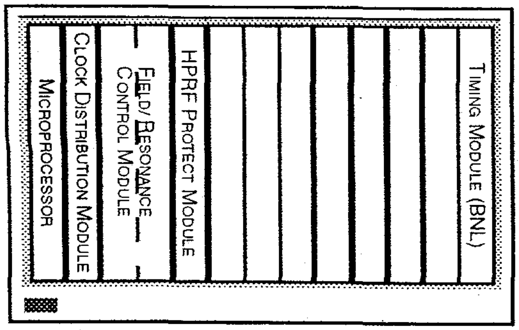

Figure 2. VXIbus RF Control System Crate Layout

2 VXIBUS MODULE DESIGNS

2.1 Clock Distribution Module

The Clock Distribution Module (CDM) is quite similar to that of LEDA. It receives a phase stable signal from the Reference Distribution system and phase locks a 40 MHz ADC (analog-to-digital converter) clock and a 50 MHz IF for use by the Field/Resonance Control Module and the HPRF Protect Module. A block diagram of it is presented in figure 3. It should be noted that the Timing System developed by Brookhaven National Laboratory provides each RFCS with a Timing Module for data synchronization of each RFCS with the rest of the accelerator. The CDM receives information from the BNL Timing Module and distributes it to the rest of the RFCS.

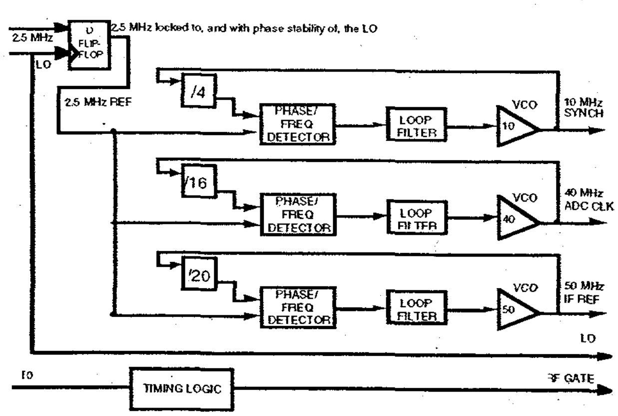

Figure 3. Clock Distribution Module Block Diagram

2.2 Field/Resonance Control Module

The Field/Resonance Control Module performs two main functions. 1) It determines the resonance condition of the cavity and sends the correct error signal to the Cavity Resonance Control System (water cooling for the NC cavities) to bring the cavity back on resonance and keep it there. We also generate a correct off beam resonance drive frequency for way-off-resonance conditions when necessary [Ref 2]). 2) It samples the cavity field and determines correct control signals for the klystron in order to keep the cavity field within specification. It provides these control signals with proportional-integral-differential (PID) feedback in addition to an adaptive feedforward algorithm (based on error feedforward which we refer to as an Iterative Learning Controller [Ref.3]).

Figure 4 is a simplified block diagram of the Field/Resonance Control Module. This module is almost completely digital circuitry. Downconversion of RF signals foe the resonance control function, and the upconversion of the controlled RF drive signal for the klystron are the only analog circuits on the board. Significant basic digital components are two digital signal processors (DSPs) and four Complex Programmable Logic Devices (CPLDs). The TI C60 family DSPs are used for Resonance Control and Field Control (one each).

The Resonance Control algorithm is the same as used in LEDA [Ref. 2]. In the fast field control signal path, multi-rate digital processing is performed in CPLDs for optimized throughput. The Field Control DSP performs the slower, pulse-to-pulse, adaptive feedforward and gain scheduling features, while the field control CPLD does the actual fast feedback proportional-differential-integral (PID) algorithm.

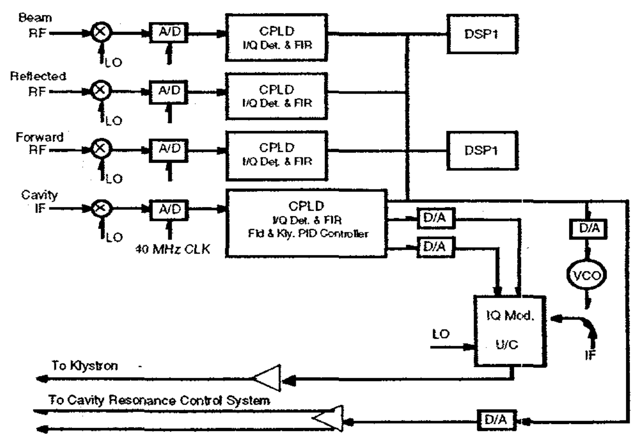

Figure 4. Simplified Control Module Block Diagram

The CPLD family we will be using is the Altera EP20KE series in a 672 FineLine BGA Package. Three of the four CPLDs are identical, containing a multiplexer/ multiplier (I/Q detector), digital filter, 2x2 rotation matrix and a controller (e.g., PID). The I and Q output data rate is 20 MHz, and the expected delay/latency through the CPLD is 23.5 cycles (1174 ns). Figure 5 shows a block diagram of the basic CPLD and the associated delay/latency at each step. The fourth CPLD in the Control Module includes this basic structure as well as the functionality to perform klystron phase control.

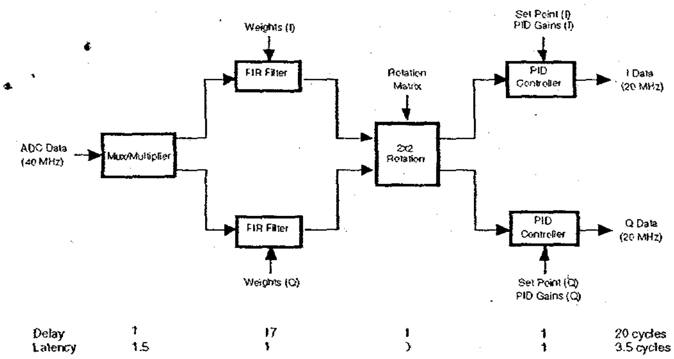

Figure 5. Basic CPLD Structure and Expected Delay

2.3 *HPRF Protect Module*

The HPRF Protect function is fulfilled by a single VXIbus module. It is based on the HPRF Protect system for LEDA, which consists of a VXIbus module and four different chassis. Based on lessons learned on LEDA, we have been able to dramatically simplify this function. The module's basic purpose is to provide a signal which turns off the RF drive to the klystron should a fault occur within the HPRF transport line, be it arcing in the waveguide or unexpected high reflected power. There are 6 RF channels per module for monitoring RF power. There are inputs from the fiber optic arc subsystem for allowing for monitoring waveguide arcs. Instead of simply turning off the drive to the klystron on any g8iven fault, logic is built into each channel to allow for a certain number of faults within a certain period of time before declaring an RF-off state. Also, besides just the waveguide arc monitoring, logic is built into the module to interpret when a cavity arc occurs based on RF power signal from directional couplers at the cavity itself.

The signal processing done on the HPRF Protect Module involves the following. There is a 20 MHz bandwidth input filter at the RF frequency (402.5 or 805 MHz). This is the only part that will need to change between cavity type. This filter is followed by a true RMS power detector (AD8361). A 6 Ms/s analog-to-digital converter (Zilog XRD 6418 with 6 channels used) with 10 bits of resolution is used to transfer the input signal to a digital version. After that all comparators are digital, and with a simple Altera PLD for decode/actions, the expected total response time is 5 μs. A block diagram of a single RF channel (which is duplicated six times on the board) is given in figure 6.

I'm still working on it. Word is being unco-operative.

Figure 6. Single RF Channel Block Diagram

3 SUMMARY

The design of the RF Control System for the Normal Conducting SNS linac is well underway. Individual modules have been identified, specified, and are mostly through the initial design phase. In the next few months we will begin bread-boarding these modules and putting together an initial test system.

REFERENCES

[1] M. Lynch, et al "The Spallation Neutron Source (SNS) Linac RF System", Linac 2000, August 2000.

[2] Y. Wang, et al, "Algorithms and Implementations of APT Resonant Control System", PAC 1997, May 1997.

[3] S. Kwon, et al, "An Iterative Learning Control of a Pulsed Linear Accelerator", Linac 2000, August 2000.