Worst-Case Bias During Total Dose Irradiation of SOI Transistors

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***Abstract*—The worst case bias during total dose irradiation of partially depleted SOI transistors from two technologies is correlated to the device architecture. Experiments and simulations are used to analyze SOI back transistor threshold voltage shift and charge trapping in the buried oxide.**

I. Introduction

THE last two years have seen the development of Silicon On Insulator (SOI) technologies for high performance and low power circuits addressing the growing market of communication, fast computers and consumer electronics [1]. SOI is used by several companies to improve their product characteristics [2, 3]. SOI is also referenced in the 1999 international roadmap of semiconductor technologies [4]. This evolution from military and space market to mainstream applications has been possible thanks to the drastic improvement of the SOI substrate quality which allows yield improvement and cost reduction for complex circuits.

However, commercial SOI technologies are not fully adapted to hardened applications. The buried oxide isolation and the small volume of silicon present many advantages for speed, density, and hardness to transient irradiation [5]. But, unless radiation hardened [6], the buried oxide introduces an additional path for total ionizing dose leakage currents [7]. Worst-case bias conditions have been partially described in [6] for 0.35µm gate length transistors processed on standard SIMOX (Separation by IMplanted OXygen). Extrapolation to other gate lengths and buried oxide thicknesses has only been studied with device simulation without modeling the total dose induced charge trapping in the buried oxide. The purpose of this paper is to determine the worst-case bias of unhardened SOI NMOS transistors through extensive experimental analysis. Simulations of the total dose trapping in the buried oxide, and comparison of two different SOI technologies will also be used to show the influence of the SOI process and architecture.

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II. Device and Experiment Description

The studied NMOS/SOI transistors were fabricated either by CEA/LETI [8], or by Sandia National Laboratories (SNL) [9]. The technologies are both partially depleted, but they have different features, such as gate length, buried oxide and silicon film thicknesses. Table I summarizes the respective features of each technology. In particular, the CEA/LETI transistors were processed on UNIBOND® [1], or medium dose SIMOX, or low dose SIMOX. The SNL transistors were processed on standard dose SIMOX.

Tested devices are either edgeless floating body transistors (without body tie), or transistors with external body contacts [10]. Transistors were irradiated with 10 keV X-rays at a dose rate of 1 krad(SiO_2)/s.

The bias conditions under irradiation are consistent with usual bias of transistors in digital circuits (Table II). They correspond to on-state (ON) and off-state (OFF) in inverter gate, and transmission-gate (TG) like access transistors in memory cells. We also tested two other bias conditions, with the source, drain, gate and body, either at 0V (0V all) or at the supply voltage (2V-all). For all cases, the substrate is grounded.

The nominal supply voltage of the SNL and CEA/LETI technologies are different: 5V for the SNL technology, and 1.8V for the low voltage low power CEA/LETI technology. However, to be able to compare our experimental results, all devices were biased at the same supply voltage $V_{DD} = 2V$ during irradiation. It corresponds to the maximum supply voltage applied on a 1.8V technology with a 10% precision.

III. Experimental Results

The use of external body contacts and edgeless transistors avoids the appearance of lateral leakage current induced by trapping in isolation oxides, LOCOS (Local Oxydation of Silicon) [11] or shallow trench. Moreover, using either LOCOS or trench isolation with body contacts prevents any interaction of the gate bias on the buried oxide as occurs with mesa [12]. Furthermore, the front gate oxides of both technologies are thin enough to avoid any significant

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modifications of the front transistor characteristics. The front gate threshold voltage shift at 1 Mrad(SiO_2) is lower than 100 mV for CEA/LETI transistors and 300 mV for SNL ones. The source of leakage current comes from the threshold voltage shift of the back transistor due to charge trapping in the buried oxide. In the following, we concentrate on the buried oxide total dose behavior as a function of bias during irradiation and transistor geometry (gate length and buried oxide thickness).

A. Influence of Bias During irradiation

Figure 1 shows the threshold voltage shift of the back transistor with different bias conditions after irradiation of SNL transistors. The case 2V-all induces the smallest shift. Biasing the entire silicon film (source, drain and body) to a positive voltage drives the holes created during irradiation towards the back interface of the buried oxide reducing the number of holes trapped at the top interface, while electrons escape to the top silicon film. Holes trapped near the back interface have a small electrical influence on the silicon film and do not induce an important shift.

The ON case shows the same shift as the 0V-all case. This demonstrates that the threshold voltage shift of the back transistor only depends on the silicon film bias (source, drain, body), and is not influenced by the gate bias during irradiation.

The TG case is the worst case bias up to 1 Mrad(SiO_2). At higher dose the TG curve saturates and the OFF curve rejoins the TG curve. The TG and OFF curves of the 0.5µm SNL NMOS rejoins precisely at 1 Mrad(SiO_2). This competition between OFF and TG will be investigated further by looking at the transistor architecture.

B. Influence of Gate Length

Figure 2 shows the back transistor threshold voltage shift of CEA/LETI transistors with different gate lengths, irradiated in the TG configuration. The shift is strongly influenced by gate length with a maximum shift for the 0.6µm transistor. Shorter transistors (0.25µm) show a smaller shift with an earlier saturation. Longer transistors also show a smaller shift, but generally, as gate length increases, the saturation phenomenon seems to be postponed to higher doses.

The back transistor threshold voltage shift at 1 Mrad(SiO_2) is plotted in Fig. 3 for different bias conditions on CEA/LETI transistors with either floating body or external body contacts. As expected, and already seen on SNL transistors (Fig. 1), biasing the silicon film with the 2V-all bias condition on transistors with body contacts induces the smallest shift since trapping mainly occurs near the back interface of the buried oxide. The floating body transistors with the TG configuration have the same behavior. This is because the floating body potential is controlled by the source and drain potential (2V), and thus without a body contact, the body potential also goes to 2V.

The cases ON and 0V-all for both types of transistors (floating body and body contacts) are quite similar since in both cases the silicon film is grounded. Trap sites are located in the volume of the buried oxide, and trapping is determined by built-in field and space charge effects as dose increases [13].

For the OFF case both transistors with floating body and external body contacts have the same behavior. This suggests that the voltage drop is across the drain-body junctions and that the potential distribution of both transistors are similar.

The TG case of the transistor with external body contacts is the worst case, except for the shortest gate length, 0.25µm. The TG and OFF shifts at 1 Mrad(SiO_2) cross at a gate length of 0.3µm. The same phenomenon (identical TG and OFF shifts at 1 Mrad(SiO_2)) occurs on 0.3µm CEA/LETI transistors and on 0.6µm SNL ones (Fig. 1).

We note that adding body contacts to a transistor avoids lateral leakage, but induces the worst back-gate threshold voltage shift with the TG case for a wide range of gate lengths. For floating body transistors, OFF state is the worst case irradiation bias and TG case only induces a weak shift.

C. Influence of Buried Oxide Thickness

Fig. 4 shows the competition between TG and OFF for transistors with external body contacts. For the 0.25µm gate length transistor, OFF state is the worst case bias when processed on UNIBOND. However, if the transistor is processed on a thinner buried oxide (medium SIMOX), TG is the worst case.

IV. Simulations and Discussion

2D simulations with Dessis from ISE (Integrated Systems Engineering) [14] are used to analyze hole trapping in the buried oxide during total dose irradiation. A specific module has been developed in cooperation with ISE, to self-consistently solve trapping equations with Poisson and carrier continuity equations in the oxide. It models the field collapse and enhancement effects [15].

In the presented simulations, only hole trapping on neutral traps, and electron recombination on trapped holes [16], are simulated since they are the dominant phenomena at low dose, below 1 Mrad(SiO_2). To determine the hole trap density N_{tp} and capture cross-section σ_{pt}, specific experiments were realized with a high positive voltage on the back gate and other terminals grounded. We used the method published in [17] to extract N_{tp} and σ_{pt} on our UNIBOND® samples. We found $N_{tp} = 5\times10^{18}$ cm^{-3}, and $\sigma_{pt} = 6.8\times10^{-14}$ cm^2. The effective hole and electron mobilities are respectively set at $\mu_n = 10^{-5}$ cm^2/Vs and $\mu_n = 20$ cm^2/Vs [18]. The cross-section of electron recombination on trapped holes is $\sigma_{pr} = 10^{-12}$ cm^2.

A. Bias Cases During Irradiation

Figure 5 shows the trapped hole concentration in the buried oxide of a floating body 0.5 µm gate length SOI/NMOS processed on UNIBOND buried oxide after irradiating to 1

Mrad(SiO_2). Trapped charge profiles in the buried oxide, 6 nm under the silicon film interface, are plotted on Fig. 6.

1) OFF state

When a floating body transistor is OFF biased, the field lines (Fig. 5a) induce hole trapping near the back interface and under the body region, and few holes are trapped in the bulk of the oxide. Trapping at the back interface has a weak electric influence. However hole trapping under the body region determines back gate transistor conduction. Trapping spreads under the source as dose increases because of electric field modification during irradiation.

OFF biased grounded body transistors have similar potential and electric field cartographies than floating body transistors. The body potential in the OFF state remains at 0V, even without grounded body contact. This shows the good behavior of the back transistor (no snap-back due to floating body effects). Fig. 6 also shows that OFF biased grounded and floating body transistors have the same trapped charge profiles. This identical behavior was observed experimentally (Fig. 3).

2) TG state

If a floating body transistor is TG biased, trapping occurs also near the back interface and under the body region (Fig. 5b). However, the electric field confines charge trapping under the body and prevents any spreading. It should be noticed that for the TG biased floating body transistor, the electric field in the buried oxide is only due to the doping difference between the body and the source or drain regions. The doping induced voltage drop can be close to 1V near the junctions. Trapped charge density under the front interface (Fig. 6) is symmetric, at about 1×10^{18} cm^{-3} with local maxima under the source and drain junctions.

When considering a TG biased transistor with grounded body contacts, the voltage drop is higher, up to 3V under the junctions, since external bias (2V) adds to the internal doping voltage drop (up to 1V). Charge trapping is then more efficient (Fig. 6). It is about 3 times higher when the body of the TG transistor is grounded rather than floating (3×10^{18} cm^{-3} instead of 1×10^{18} cm^{-3}).

3) Comparison with experiments

The simulations (Fig. 6) confirms the experimental results of Fig. 3:

- The TG case of a 0.5µm gate length grounded body transistor shows the largest trapping because both junctions (source and drain) are biased.
- The OFF case for grounded *and* floating body transistors shows lower trapping because only the drain junction is biased.
- The TG case of the floating body transistor shows the less important trapping. We can also notice on Fig. 3 the same ratio of 3 between the back gate threshold voltage shifts of the floating and grounded body TG transistors.

B. L / t_{BOX} ratio

Considering grounded body transistors, and comparing Fig. 3 and Fig. 4, it appears that the OFF state is the worst case bias for short gate lengths transistors processed on thick buried oxide. Otherwise TG is the worst-case bias configuration. This can be expressed by using the ratio gate length on buried oxide thickness L/t_{BOX} [15]: if $L/t_{BOX} \ll 1$, OFF state is the worst-case; if $L/t_{BOX} \gg 1$, TG is the worst-case.

Fig. 7 shows schematic field lines and hole trapping in SOI devices with varying L/ t_{BOX} ratio in the OFF configuration.

If $L/ t_{BOX} \gg 1$, trapping occurs mainly below the drain junction where the electric field drop is maximum. It also occurs under the source junction because of the doping induced voltage drop. But under the body, far from the drain, a region of low field prevents high trapped hole concentration. The low field under the body is only due to the doping difference between P-type substrate and P+ body. It is schematically represented by red arrows on the simulated 10µm gate length transistor on Fig. 8. 2D effects in long gate length transistors makes them less sensitive to total dose than short gate length transistors (Fig. 2 and 3).

If $L/ t_{BOX} \ll 1$, the back transistor threshold voltage shift decreases. This can be explained by the fact that the neutral part of the body is reduced as gate length decreases, while the body-drain and body-source space charge regions remain roughly unchanged. The turn up of field lines towards the neutral region of the body tends to be less important.

When L/ t_{BOX} is close to 1, the field lines turn up from the drain to the body, and trapping occurs with a maximum efficiency under the body. The maximum shift of TG and OFF curves on Fig. 3 occurs at different gate length: about 0.3-0.4 µm for the OFF curve ($L/ t_{BOX} \approx 1$), and 0.5-0.8 µm for the TG case ($L/ t_{BOX} \approx 1.5$). The TG configuration implies that both drain and source are biased at VDD, while the body is grounded (symmetric configuration). The neutral body part is then more reduced to the benefit of the source and drain space charge regions than in the OFF case. The TG case needs a longer gate length for the field lines to turn up efficiently.

The TG and OFF curves at 1 Mrad(SiO_2) (Fig. 3) cross at short gate length. This crossing point occurs at a gate length of 0.3µm on the CEA/LETI transistors. A cross point also occurs on the 0.6µm gate length SNL transistors when the TG and OFF curves rejoin at 1 Mrad(SiO_2) on Fig. 1. The TG shift decrease for short gate length seems to be a general behavior. It occurs at different gate length for each technology. This must be due to different doping profiles in the body, which modulates the effective gate length of the back transistor.

C. Body Doping Influence

Transistors with different body doping, from 2×10^{17} to 1.1×10^{18} cm^{-3} have been simulated to study the influence of the body doping on trapping in the buried oxide. The process and device simulations are calibrated according to CEA/LETI devices with a doping of 1.1×10^{18} cm^{-3}.

Fig. 9 shows the simulated back-gate threshold voltage (open symbols) before irradiation and at 1Mrad(SiO_2). As expected, the experimental data on CEA/LETI transistors exactly fit the simulation. The threshold voltage shift is equal to –48V at 1Mrad(SiO_2) for a OFF biased 0.5µm gate length transistor.

For lower body doping, the simulated threshold voltage before irradiation, and at 1Mrad(SiO_2), decrease. The SNL transistors have a body doping of 2×10^{17} cm^{-3}. At this value of doping, the simulated threshold voltage before irradiation and at 1Mrad(SiO_2) fit with the SNL data without any adjustment. The SNL transistors have a threshold voltage shift of –31V, lower than the CEA/LETI ones.

The experimental and simulated data set on Fig. 9 clearly show that the threshold voltage shift decreases for low body doping. Charge trapping in the buried oxide under the body region is lower for low body doping.

This can be easily understood by considering the electric field which results from both the applied voltage (2V in our experiments) and the internal voltage drop due to doping differences between body and source or drain regions (close to 1V). At low body doping, this internal voltage drop decreases. As a consequence, the initial electric field in the oxide, which condition the amount of trapped charge under the channel, is also significantly reduced. Thus, the lower the doping level, the lower the back-gate threshold voltage shift.

However, Fig. 9 also shows that, at low body doping, the back transistor threshold voltage is close to 0V. This suggest that a leakage current flows through the back transistor. With high body doping, we get an increase of the pre-rad back-gate threshold voltage that more than compensates for the larger threshold voltage shift at 1Mrad(SiO_2).

V. Conclusion

In this paper, we analyzed the worst-case bias during total dose irradiation on SOI technologies as a function of device architecture. The worst-case irradiation bias depends on several factors. These include the total dose level, body potential, transistor architecture (i.e., with or without body contacts), ratio of the gate length to buried oxide thickness, and doping concentration of the body region. For the conditions examined here, either the OFF or TG bias condition can be worst case. For the body contacted CEA and Sandia technologies examined, worst-case irradiation bias was determined to be the TG bias configuration for total dose levels less than 1 Mrad(SiO_2). For CEA floating body transistors, the worst-case irradiation bias was determined to be the OFF bias configuration.

VI. References

[1] A. J. Auberton-Hervé, "SOI: Materials to Systems," 1996 *IEEE IEDM Technical Digest*, pp. 3-10.

[2] E. Leobandung, E. Barth, M. Sherony, S.-H. Lo, R. Schulz, W. Chu, M. Khare, D. Sadana, D. Schepis, R. Boiam, J. Sleight, F. White, F. Assaderaghi, D. Moy, G. Biery, R. Goldblatt, T.-C. Chen, B. Davari, G. Shahidi, "High Performance 0.18µm SOI CMOS Technology," *IEDM 1999*, pp. 679.

[3] J. Ahn, H.-S. Kim, T.-J. Kim, H.-H. Shin, Y.-H. Kim, D.-U. Lim, J. Kim, U. Chung, S.-C. Lee, K.-P. Suh, "1GHz Microprocessor Integration with High Performance Transistor and Low RC Delay," *1999 IEDM*, pp. 683.

[4] "The International Technology Roadmap for Semiconctors: 1999 edition", Semiconductor Industry Association, 1999.

[5] J. L. Leray, E. Dupont-Nivet, J. F. Péré, Y. M. Coïc, M. Raffaelli, "CMOS/SOI Hardening at 100 Mrad(SiO_2)", *IEEE Trans. Nucl. Sci.*, Vol. 37, No. 6, 2013, Dec. 1990.

[6] S. T. Liu, S. Balster, S. Sinha, W. C. Jenkins, "Worst Case Total Dose Radiation Response of 0.35µm SOI CMOSFETs," *IEEE Trans. Nucl. Sci.*, Vol. 46, No. 6,1817, Dec. 1999.

[7] V. Ferlet-Cavrois, O. Musseau, O. Flament, J. L. Leray, J. L. Pelloie, C. Raynaud and O. Faynot, "Total dose induced latch in short channel NMOS/SOI transistors", *IEEE Trans. Nucl. Sci.*, Vol. 45, N°6, 2458 Dec. 1998.

[8] V. Ferlet-Cavrois, P. Paillet, O. Musseau, J. L. Leray, O. Faynot, C. Raynaud, J. L. Pelloie, "Total Dose Behavior of Partially Depleted SOI Dynamic Threshold Voltage MOS (DTMOS) for Very Low Supply Voltage Applications (0.6 - 1V)," *IEEE Trans. Nucl. Sci.*, Vol. 47, No. 3, 613, June 2000.

[9] J. R. Schwank, M. R. Shaneyfelt, P. E. Dodd, V. Ferlet-Cavrois, R. A. Loemker, P. S. Winokur, D. M. Fleetwood, P. Paillet, J. L. Leray, B. L. Draper, S. C. Witczak, L. C. Riewe, "Correlation between Co-60 and X-ray Radiation-Induced Charge Buildup in Silicon-on-Insulator Buried Oxides," *IEEE Trans. Nucl. Sci.*, Vol. 47, No. 6, Dec. 2000.

[10] V. Ferlet-Cavrois, E. Dupont-Nivet, J. C. Vildeuil, O. Musseau, J. L. Leray, "Transient Radiation Effects in CMOS/SOI Transistors and Circuits," RADECS'97 proceedings, pp. 360-365, 1997.

[11] C. Brisset, V. Ferlet-Cavrois, O. Flament, O. Musseau, J. L. Leray, J. L. Pelloie, R. Escoffier, A.Michez, C. Cirba, G. Bordure, "Two-Dimensional Simulation of Total Dose Effect on NMOSFET with Lateral Parasitic Transistor," *IEEE Trans. Nucl. Sci.*, Vol. 43, N°6, 2651, Dec. 1996.

[12] R. J. Milanowski, M. P. Pagey, L. W. Massengill, R. D. Schrimpf, M. E. Wood, B. W. Offord, R. J. Graves, K. F. Galloway, C. J. Nicklaw, E. P. Kelley, "TCAD-Assisted Analysis of Back-Channel Leakage in Irradiated Mesa SOI nMOSFETs," *IEEE Trans. Nucl. Sci.*, Vol. 45, N°6, 2593, Dec. 1998.

[13] H. E. Boesch, G. A. Brown, "Charge Buildup at High Dose and Low Fields in SIMOX Buried Oxides," *IEEE Trans. Nucl. Sci.*, Vol. 38, N°6, 1234, Dec. 1991.

[14] ISE (Integrated Systems Engineering) TCAD manuals, Release 6, 1999.

[15] J. L. Leray, P. Paillet, V. Ferlet-Cavrois, C. Tavernier, K. Belhaddad, O. Penzin, "Impact of Technology Scaling in SOI Back-Channel Total Dose Tolerance. A 2D Numerical Study Using Self-Consistent Oxide Code", *RADECS99 proceedings*, Fontevraud, 13-17 sept. 1999.

[16] J. L. Leray, "Total Dose Effects: Modeling for Present and Future," *1999 IEEE NSREC Short-course*, section III.

[17] P. Paillet, D. Hervé, J. L. Leray, R. A. B. Devine, "Evidence of Negative Charge Trapping in High Temperature Annealed Thermal Oxide," *RADECS proceedings*, pp 140-145, 1993.

[18] V. Vasudevan and J. Vasi , "A Simulation of the Multiple Trapping Model for Continuous Time Random Walk Transport," *J. Appl. Phys.*, Vol. 74, pp. 3224-3230, 1993.

TABLE I
MAIN CHARACTERISTICS OF THE CEA/LETI AND SNL SOI TECHNOLOGIES

Origin	CEA/LETI			SNL
type	partially depleted			partially depleted
isolation	LOCOS			shallow trench
silicon film thickness	0.1 µm			0.15 µm
minimum gate length	0.25 µm			0.5 µm
Buried oxide	UNIBOND	Medium dose SIMOX	Low dose SIMOX	Standard dose SIMOX
Buried oxide thickness t_{BOX}	413 nm	140 nm	80 nm	370 nm

TABLE II
BIAS CONDITIONS UNDER IRRADIATION OF THE CEA/LETI AND SNL NMOS/SOI TRANSISTORS. THE SUPPLY VOLTAGE V_{DD} IS 2 V FOR BOTH TECHNOLOGIES. THE TRANSISTORS ARE EITHER EDGELESS FLOATING BODY (WITHOUT BODY TIES), OR WITH EXTERNAL BODY CONTACTS

	source	drain	gate	body	substrate
ON	0V	0V	V_{DD}	0V	0V
OFF	0V	V_{DD}	0V	0V	0V
TG	V_{DD}	V_{DD}	0V	0V	0V
0V-all	0V	0V	0V	0V	0V
2V-all	V_{DD}	V_{DD}	V_{DD}	V_{DD}	0V

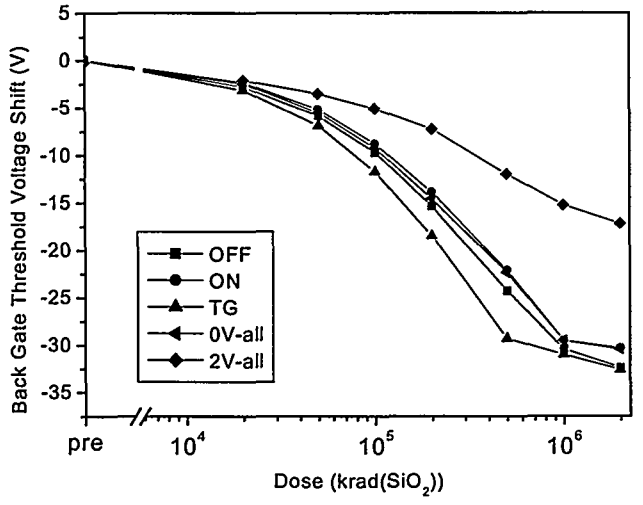

Fig. 1. Back gate threshold voltage shift versus dose of a 0.5µm gate length SNL NMOS/SOI processed on standard SIMOX with external body contacts. The back gate threshold voltage is extracted from Id-Vb characteristics at a drain voltage of Vd=0.1V.

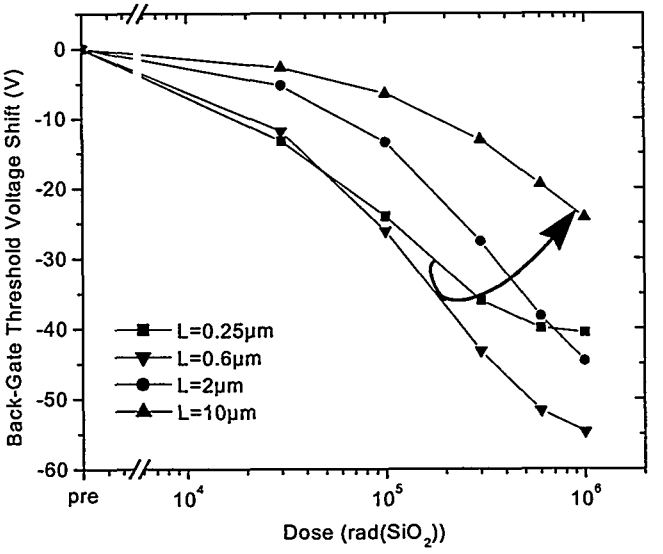

Fig. 2. Back-gate threshold voltage shift versus dose of CEA/LETI NMOS/SOI processed on UNIBOND with external body contacts and different gate length. The transistors are biased according to the TG case during irradiation. The back gate threshold voltage is extracted from Id-Vb characteristics at a drain voltage of Vd=0.1V.

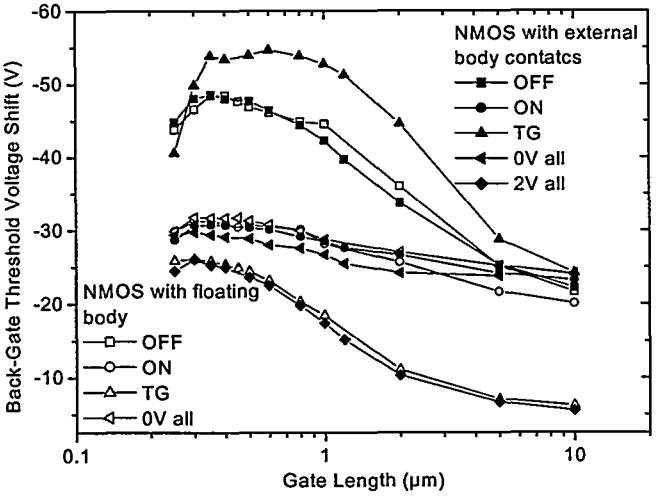

Fig. 3. Back-gate threshold voltage shift versus gate length of NMOS/SOI UNIBOND transistors measured on the Id-Vb characteristics at drain voltage of Vd=0.1V at a dose of 1Mrad(SiO_2).

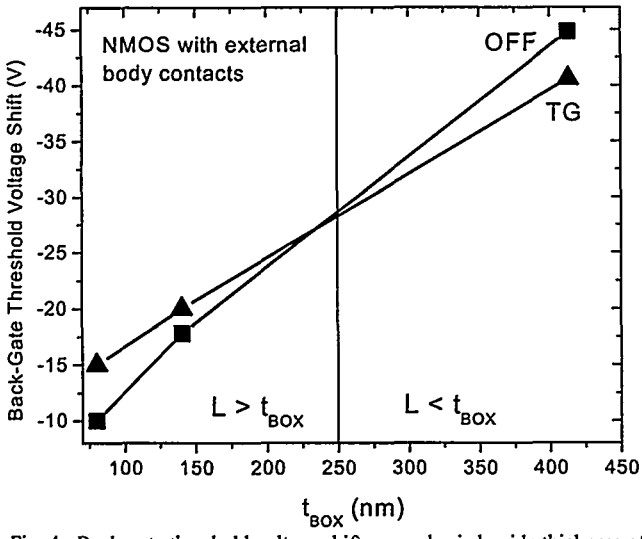

Fig. 4. Back-gate threshold voltage shift versus buried oxide thickness of 0.25µm gate length NMOS/SOI transistors measured on the Id-Vb characteristics at a drain voltage of Vd=0.1V and at a dose of 1Mrad(SiO_2).

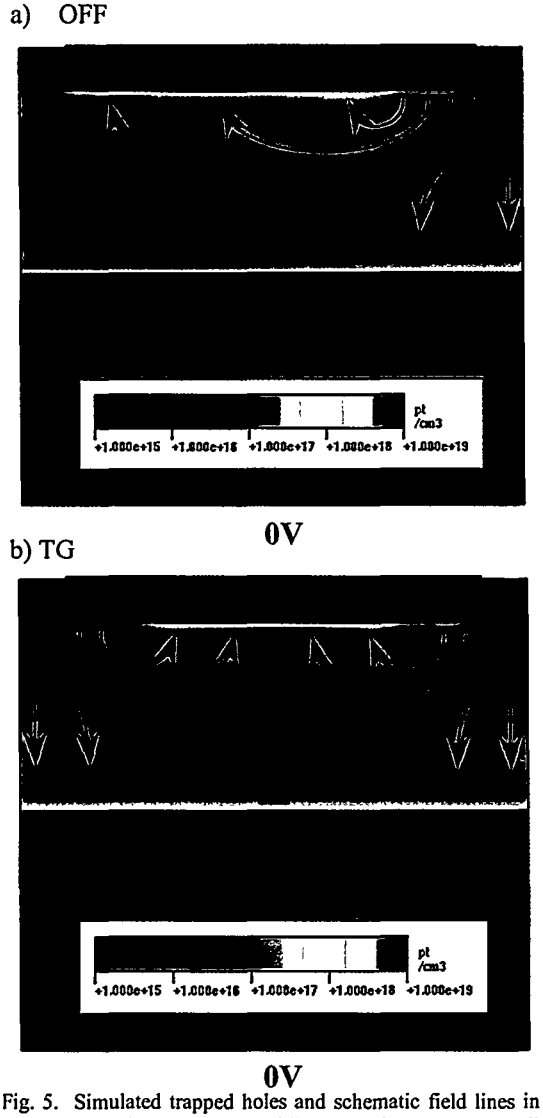

Fig. 5. Simulated trapped holes and schematic field lines in the buried oxide of a floating body NMOS/SOI transistors after irradiating to 1 Mrad(SiO_2). The bias during irradiation is OFF (a) or TG (b).

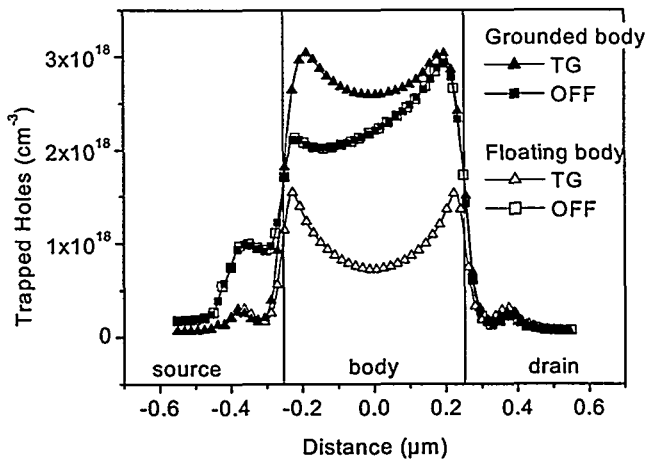

Fig. 6. Simulated trapped hole profiles in the buried oxide, 6 nm under the front interface, for TG and OFF cases, at 1 Mrad(SiO_2). The simulated transistor is either a floating or grounded body NMOS with a gate length of 0.5µm.

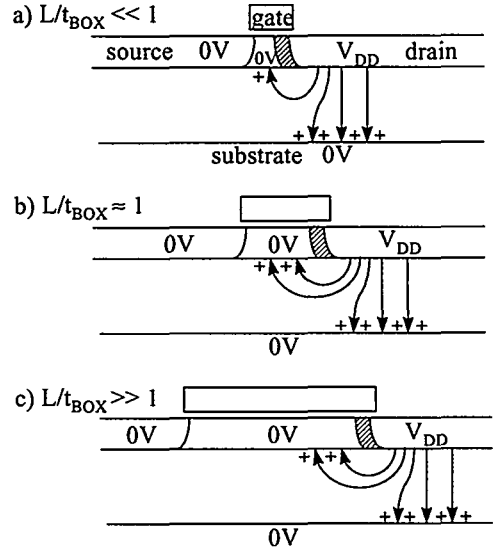

Fig. 7. Schematic representation of field lines and hole trapping in the buried oxide of NMOS/SOI transistors with varying L/t_{BOX} ratio. The grounded body transistors are OFF biased during irradiation.

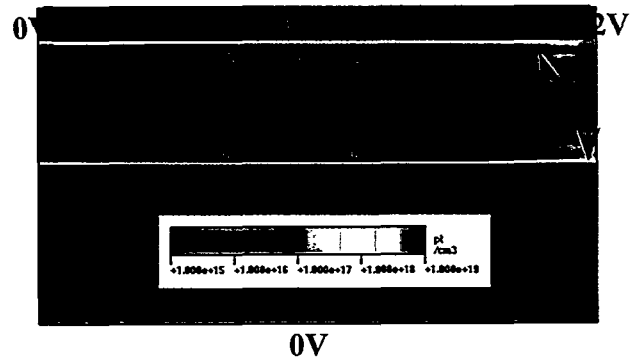

Fig. 8. Simulation of the trapped charge in the buried oxide of a OFF biased 10µm gate length transistor after irradiating to 1 Mrad(SiO_2). For clarity, the vertical dimension of the transistor has been multiplied by 6.

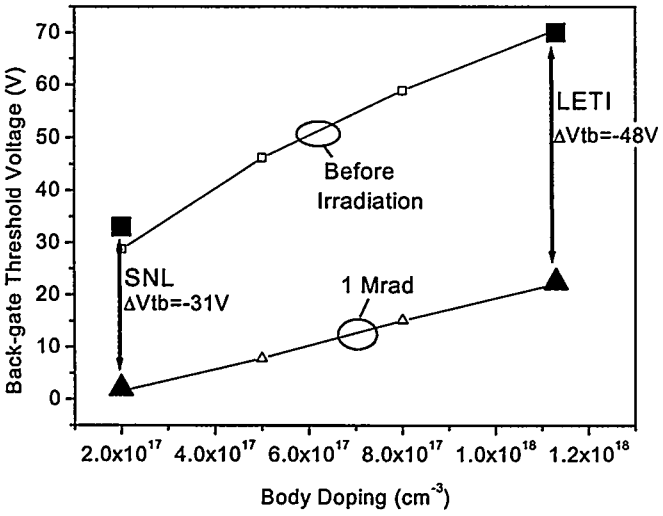

Fig. 9. Simulated threshold voltage of the grounded body back gate transistor versus body doping (open symbols), and comparison with experimental data (closed symbols) on SNL and CEA/LETI transistors. The transistors are OFF biased with a supply voltage of 2V.