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FRONT-END ELECTRONICS FOR IMAGING DETECTORS*

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Abstract

Front-end electronics for imaging detectors with large numbers of pixels (10^5–10^7) is reviewed. The noise limits as a function of detector capacitance and power dissipation are presented for CMOS technology. Active matrix flat panel imagers (AMFPIs) are discussed and their potential noise performance is illustrated

1. Introduction

A key criterion for an imaging detector is the ability to perform "quantum limited imaging", that is to distinguish the signal charge due to a single quantum from any noise generated in the detector and/or the readout system. In addition to obtaining image intensity distribution as a function of position by quantum counting or charge integration, energy and timing measurements on every particle or photon may be performed. While a detailed optimization of an electronic readout may be different for each of the great variety of imaging detectors and their applications, all detectors, with very few exceptions, are capacitive sources of charge. The signal charge is produced either directly by ionization, or indirectly by scintillation and photodetection. The "pair creation energy", i.e., the energy expended to create an ion pair or to emit an electron, covers many orders of magnitude for different detectors ranging from directly converting semiconductors to fast scintillators with appropriate photodetectors. Optimization of imaging detector systems is a multivariable problem, the subject of the vast field of imaging detectors. For signal detection, the key parameters are the signal charge per quantum and the electronic noise. The state of electronics technology determines to a large extent whether an imaging system is practical. Until recently, large numbers of electronics channels have been avoided, and large numbers of resolution elements have been obtained by interpolation. With the increasing availability of monolithic electronics, readout of large numbers of individual (discrete) detector elements has become feasible and has stimulated the development of detectors. The electronic noise, the speed of response and the power dissipation of the front-end are strongly dependent on the detector capacitance, and this is discussed in Section 2. A brief overview of readout configurations of multi-element detectors is given in Section 3. The preamplifier feedback configuration is critical for detector current reset, noise and overall performance, and it is discussed in Section 4. Individual pixel readout becomes impractical on imaging detectors with very large numbers of pixels (~10^6–10^7). Matrix readouts derived from the flat panel display technology have been receiving increasing attention, and are discussed in Section 5.

The emphasis of this review is mostly toward smaller (~10^2 to 10^3 cm^2) high resolution imaging detectors for applications such as x-ray scattering and medical imaging, where the design has to be economical, self-contained and should not require attendance by physicists.

In Section 6, future developments in electronic devices and technology are briefly highlighted and some references provided.

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2. Noise vs detector capacitance and power dissipation

The noise limit to the resolution of a radiation detection system is determined by the performance of the detector and of the field effect transistor (FET) at the input of the front-end, and it is typically expressed in Equivalent Noise Charge (ENC) [1-3]. The ENC depends on the detector (plus parasitic) capacitance C_{DET}, on the input FET gate capacitance C_G and series noise (including both thermal and $1/f$), on the detector leakage current I_{DET} and on the preamplifier reset current I_{RST}. The ENC can be expressed as:

$$\mathrm{ENC}^2 = A_1 \frac{1}{\tau_P} \frac{4kT}{g_m} (C_G + C_{DET})^2 + A_3 \frac{K_F}{C_G} (C_G + C_{DET})^2 + A_2 \tau_P 2q (I_{DET} + I_{RST}) \quad (1)$$

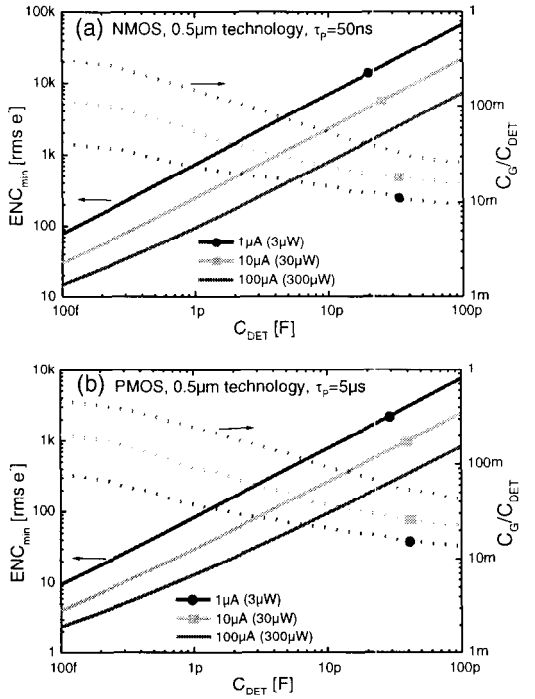

Fig.1. Dependence of the minimum achievable ENC on the detector capacitance C_{DET} for different values of I_D (i.e. power dissipated by the input line) for a commercial 0.5μm CMOS technology and corresponding optimum ratio C_G/C_{DET}. The cases of the NMOS (a) for τ_P=50ns and of the PMOS (b) for τ_P=5μs are compared.

where A_1, A_2 and A_3 are coefficients related to the filter, τ_P is the output pulse peaking time, i.e. a measure of the speed of the detection system, g_m is the input FET transconductance, and K_F is the $1/f$ noise coefficient.

By considering that the peaking time τ_P and the temperature T are set by the application, the minimization of the ENC is the result of the optimization of two components: (i) the detector, through the minimization of its capacitance C_{DET} and leakage current I_{DET}, and (ii) the front-end electronics, through the optimization of the input FET size and the minimization of the reset current I_{RST}. The process of optimization of the front-end electronics starts from the knowledge of C_{DET} and I_{DET}. As a consequence, the former optimization has to be carried out before the latter. In other words, when the design of the front-end electronics begins, it is assumed that the detector optimization has been fully carried out. For this reason, during the design phase of a detector, attention must be paid to the minimization of its capacitance and leakage current.

The continuous impressive increase in the number of front-end channels of a detection system imposes a continuously decreasing limit on the power dissipated by the input FET. This is equivalent to imposing a limit on the FET drain current I_D and on its transconductance g_m. This limit is only partially compensated by the reduction in minimum channel length L (i.e. maximum cutoff frequency ~ g_m/C_G) available through the most recent technologies (see Section 6). To each value of detector capacitance C_{DET} and drain current I_D it corresponds a value of C_G (i.e. of the channel width W) which minimizes the first term of Eq. (1) [4-7]. If no limit is imposed on I_D, the optimum condition leads to C_G=C_{DET} (and then ENC $\propto C_{DET}^{1/2}$). If a limit is imposed on the drain current I_D, the optimum condition leads to C_G=C_{DET}/3 (ENC $\propto C_{DET}^{3/4}$) if the FET operates above threshold (strong inversion for a MOSFET), and to C_G<<C_{DET}/3 (ENC $\propto C_{DET}$) if the FET operates below threshold (weak and moderate inversion for a MOSFET). From Fig. 1 it can be observed the decrease of the optimum ratio C_G/C_{DET}, down to values as low as 0.01, as C_{DET} increases and I_D decreases. Concerning the second term of Eq. (1), the negligible dependence of K_F on the operating point leads to the optimum condition C_G=C_{DET}. The optimum C_G which minimizes both the first and the second term of Eq. (1) is the result of a compromise which takes into account both the thermal and the $1/f$ noise contributions from the input FET for a given peaking time τ_P.

In Fig. 1 the dependence of the minimum achievable ENC on the detector capacitance C_{DET} for different values of I_D is reported for a commercially available 0.5μm CMOS technology. The corresponding optimum ratio C_G/C_{DET} is also shown. The cases of the NMOS for short peaking time applications, characterized by a higher cutoff frequency and of the PMOS for long peaking time applications, characterized by a lower $1/f$ noise, are compared. In the evaluation shown in Fig. 1, which must be assumed as the ultimate limit for this technology, the third term of Eq. (1) was assumed negligible. An overview of the approaches used to minimize I_{RST} will be discussed in Section 4.

3. Readout of Multi-Element Detectors

The four most common readout schemes for very large numbers of pixels (or resolution elements) are shown in Fig. 2. Each scheme is best suited to one or a few detector types. They all have different ulti-

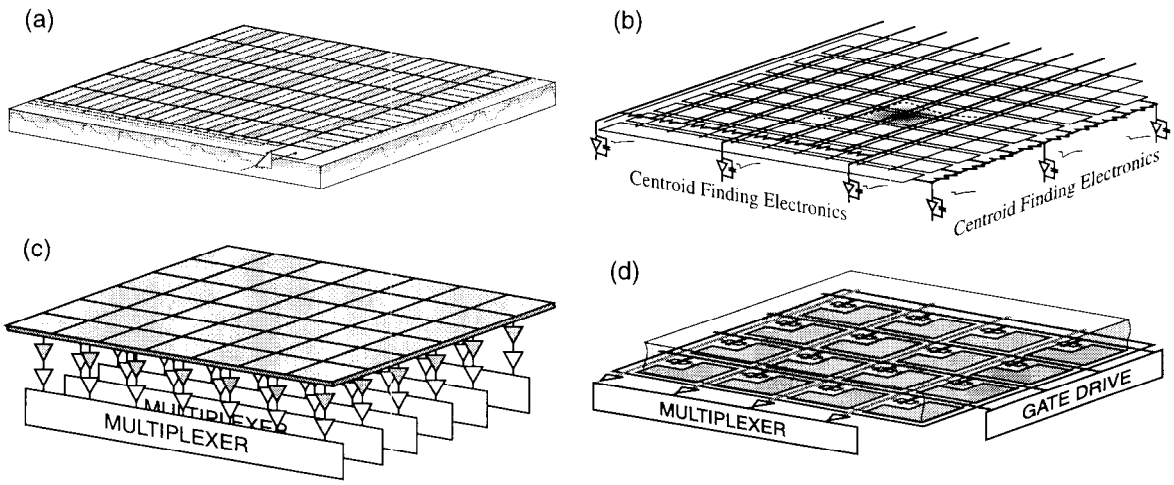

Fig. 2. Readout methods for imaging detectors with very large numbers of pixels: (a) charge coupled device (CCD); (b) projective (interpolating) readout; (c) pixel array with one preamplifier per pixel; (d) active matrix with one switch per pixel.

mate sensitivity, electronic noise, power dissipation and complexity of electronics and interconnections. Imaging by charge integration can be performed by three of the schemes, the charge coupled device (CCD), Fig. 2(a), the pixel array, Fig. 2(c) and the flat panel imagers with matrix readout, Fig. 2(d). Imaging by quantum counting can be performed by the projective readout, Fig. 2(b), and by the pixel array. The number of readout channels (preamplifiers, pulse shapers, amplitude samplers) is *one* for the entire CCD; it equals the number of pixels N_p for the pixel array; and, it is about $N_p^{1/2}$ for the active matrix. In the projective readout, the ratio between the number of pixels (i.e. position resolution elements) and the number of readout channels can be quite large. The number of readout channels is $2N_p^{1/2}/a$, where a is the interpolation factor, which can be typically between 10 and 100.

The lower limit of the electronic noise is uniquely determined by the capacitance of the detector electrode and its interconnections as discussed in Section 2. The lowest electronic noise (~ 1 rms electron) measured on an imager has been on CCDs developed for x-ray astrophysics experiments, and this is due to the very low capacitance (~50 fF) of the readout electrode on which the signal charge is induced, and a long integration time (~64 μs) achieved by repetitive (nondestructive) sampling of the charge produced by a single x-ray photon [8].

The projective readout, which is most suitable for gas proportional chambers of any size from a few cm^2 to 1 – 2 m^2, will have a much larger (cathode strip or wire) capacitance, 10 – 100 pF, and consequently a higher noise. An example of projective readout of detectors for neutron scattering is given in Ref. [9].

The pixel array, applicable to silicon detectors, avalanche photodiodes, gas proportional multi-wire detectors and various gas micro-pattern detectors, may have capacitance in the range from 100 fF to tens of picofarads, with the noise from ~ 50 rms e to 10^3 rms e depending on the peaking (shaping or integration) time.

An imaging detector readout is a result of a complex optimization among many requirements such as the counting rate (global and local), readout time for one detector plane, position, energy and timing resolution. The readout time is a compromise between the parallel and serial flow of information and the length and complexity of interconnections. With respect to signal processing per pixel, the CCD and the pixel array are at opposite ends of the scale. The length and the technology of interconnections in a pixel array, depend on the ratio of the pixel area and the area of the front-end electronics chip per channel. When these areas are matched, bump bonding provides the lowest input capacitance and the lowest noise. Multiplexing after signal processing (pulse shaping and sampling) results in a shorter readout time, since multiplexing speed does not affect the signal to noise ratio as it does in the case of the CCD, where pulse shaping (filtering) is performed for each pixel during the serial readout.

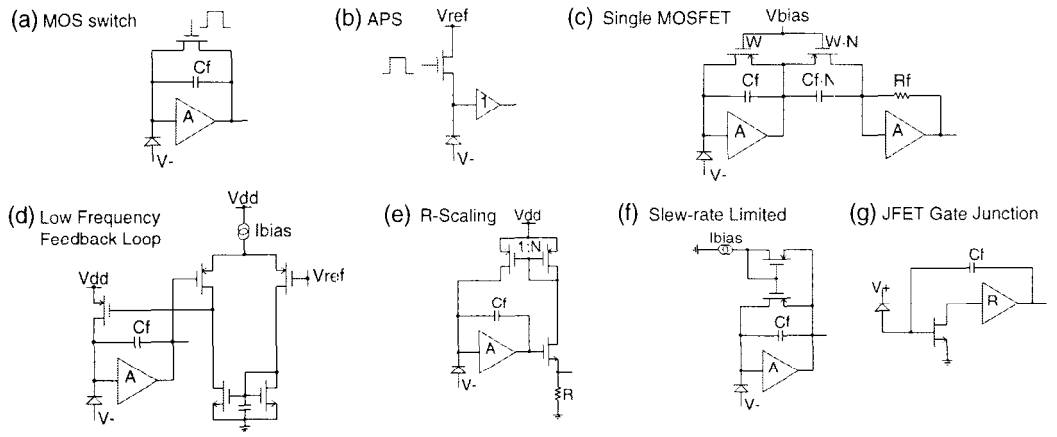

Fig. 3. Most widely used integrated reset configurations for periodic reset (a and b) and continuous reset (c through g).

The pixel array with one-to-one area matching becomes uneconomical beyond certain size (this limit is much higher in detectors for particle physics experiments than for protein crystallography and medical imaging). This is where the active matrix readout discussed in Section 5, provides a simpler solution, which is sufficient since only integrated quantum flux spatial distribution is of interest.

4. Preamplifier feedback and detector current reset technologies

The role of a reset system is to discharge, discretely or continuously, the input node of the detection system from both the charge due to the detector leakage and the signal charge. In the case of charge preamplifiers it also provides stabilization of the operating point. The reset system, being connected to the (most sensitive) input node of the detection system, must be carefully designed as it can generate additional noise. As shown in Eq. (1), its contribution to the ENC can be expressed through an equivalent reset current I_{RST} and it directly compares to the one from the detector leakage current. The difficulties related to the realization of an integrated reset system follow from the difficulties of integrating feedback resistors R_F of large value (noise $4kT/R_F$ to be compared to $2qI_{DET}$). Solutions based on active devices have been consequently developed. In Fig. 3 the most widely used integrated reset configurations are shown.

The *MOS switch* configuration (a) and the *active pixel sensor (APS)* configuration (b), which provide a periodic reset through a MOS switch, are discussed in Section 5.

The *single MOSFET* configuration (c) is based on the use of a MOSFET in feedback and an N times replica of it for the coupling to the next stage [10-12]. The feedback MOSFET is designed to contribute a thermal noise which is always lower than the shot noise from the detector. The sharing of the same gate-to-source voltage of the two MOSFETs provides full and accurate compensation, including the non-linearity unavoidably associated with active devices. This stage, which can be realized in multiple stages, provides an effective current gain equal to N from DC to high frequency and it represents the most effective solution in terms of linearity and resolution.

The *low frequency feedback loop* configuration (d) is the most widely implemented in currently available front-end ASICs [13-16]. It is based on the use of a differential stage along the preamplifier feedback path which sets the output voltage of the preamplifier to a reference value V_{ref}. The feedback loop is filtered in order to be operative only at low frequency. The compensation of the consequent pole/zero and of any non-linearity can be difficult to achieve. The noise contribution from the differential amplifier must be considered.

The *R-scaling* configuration (e) uses a low value resistor to generate the reset current. The current and its noise are scaled down through a suitable network based on current mirrors [17-19]. Due to the use of a resistor, this approach can provide good linearity, though limited by the linearity of the scaling-down network. Compensation is also available in some configurations. The noise contribution from the resistor and from the scaling-down network must be considered. The parasitic feedback capacitance is an issue.

The *slew-rate limited* configuration (f) uses a MOSFET biased in the linear region ($I_{bias}>I_{DET}$). The MOSFET enters the saturation region only when there is signal activity [20,21]. The slew-rate limited reset makes the system suitable for applications employing the time-over-threshold (TOT) processing. In classical pulse processing the non-linearity can be high and its compensation difficult to achieve. The noise contribution from I_{bias} strongly limits the resolution.

The *JFET gate junction* configuration (g) provides the discharge through the gate current generated by the impact ionization at the drain of the input JFET [22-25]. Due to its shot noise origin, the noise contribution from the discharge current can be high. The integrability of the JFET must be available. The compensation is an issue.

5. Active matrix flat panel imagers (AMFPI)

Several important imaging applications (e.g. digital radiology [26,27], protein crystallography at synchrotron sources [28,29]) require large, highly segmented detectors with fast readout. For achieving image quality comparable to older film-based detectors, these applications must have pixel sizes of around 150 μm and active areas up to 40×40 cm^2, making amplifier-per-pixel readout impractical. Instead, matrix detectors based on active switch arrays are used. In such active matrix detectors, each pixel element contains a converter, charge storage node, and switch. The converter may be direct or indirect. Direct converters use photoconductors or photodiodes to convert the incident photons into charge, whereas indirect schemes involve scintillating or phosphorescent films optically coupled to photodetectors. The integrated charge is stored on a pixel capacitance. Switches connect a row of pixels to charge amplifiers located at the bottom of the columns. In this way AMFPIs achieve a multiplexing density intermediate between "active pixels" with one output per cell, and CCDs with only one output for the entire array. They also allow different technologies to be used for the detector and switch fabric. For many applications, the AMFPI approach is the best compromise between interconnect complexity and speed of readout.

Active matrix panels must cover areas nearly 2000 times as large as the typical integrated circuit. Therefore, conventional integrated circuit switch elements like CMOS or BJT cannot be used. Switch elements suitable for large flat panels are polycrystalline or amorphous silicon Thin Film Transistors (TFTs) on glass substrates, the same technology used for active-matrix flat panel displays [30,31]. Other options are photodiodes, poly-CdSe TFTs, or JFETs fabricated directly on detector-grade Si.

For switching matrices, the performance requirements of thin film transistors are modest. On-resistance (R_{on}) in the range of 1 MΩ is adequate to readout the pixel charge with a time constant $R_{on}\cdot C_D$ of the order of 1 μs, which permits 30 frame/s readout of a 1000-line array. The off-resistance R_{off} must be $10^{13}\Omega$ or greater so that the cumulative leakage of 1000 off-transistors in parallel does not degrade the noise. With present fabrication technology, the thermal and flicker noise of TFTs is too high to allow their use as amplifiers.

5.1 AMFPI Readout

The readout electronics of an AMFPI detector is illustrated schematically in Fig. 4. The figure shows the pixel charge accumulation capacitor C_D and TFT switch, the parasitic capacitance C_S of the readout line, the charge integrating amplifier, correlated double sampling (CDS) circuit, and output multiplexer. The readout sequence is shown in the timing diagram at the bottom of the figure. Immediately before reading (at time t_1) the pixel the integrator is reset, bringing the readout line to the integrator reset potential. A "pre-" sample V_1 is then stored on the first sample-and-hold capacitor. The TFT switch is closed and the photoinduced charge held in the pixel is transferred onto the integrator feedback capacitor C_F. When charge transfer is complete (time t_2) a second sample V_2 is stored. The presample V_1 captures the reset noise, i.e. the instantaneous noise sampled on capacitors C_F and C_S, as well as any offset. Sample V_2 also contains the reset noise and offset. The difference signal $V_2 - V_1$ is presented to the output through a column multiplexing switch. Reset noise of C_F and C_S, offset, and any noise whose predominant contribution lies at frequencies less than $(t_2 - t_1)^{-1}$ are canceled by this means.

The acquisition time T_{frame} must be long enough for each row of pixels to transfer its charge completely to the integrator:

$$T_{frame} > N \cdot K \cdot R_{on} \cdot C_D$$

where K is the number of time constants required for complete charge transfer and N is the number of rows in the array.

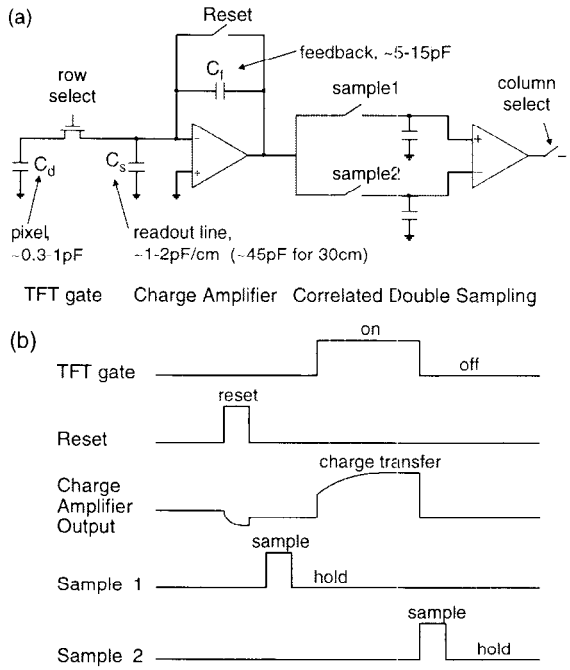

Fig. 4. (a) Schematic illustration of an active matrix flat panel imager (AMFPI) detector; (b) Timing diagram of correlated double sampling (CDS) techinique [27].

The noise bandwidth of the integrator should be limited by a lowpass filter between preamplifier and sampling switch, not shown in the figure.

The output multiplexer must deliver signals from all columns onto an output bus before the next row acquisition can begin.

To reduce demands on the output multiplexer the sampling and multiplexing operations can be pipelined, so that while the charge from a new row is being integrated, the double samples from the previous row can be multiplexed out [32-34]. Also, the output multiplexing can be speeded up by segmenting and precharging the multiplexer outputs.

The maximum charge that the system is required to handle depends on the application. In the brightest Bragg peaks in synchrotron-based crystallography the flux may exceed 10^5 photons/s in a single pixel [35]. Such systems require large, linear capacitors C_D and C_F to store charges as large as 10 pC.

5.2 Noise in AMFPI readouts

The noise of the readout system includes several contributions. It is convenient to group these into two classes: Type R noise which can be reduced by correlated double sampling, and Type NR which cannot. Type R noise sources include:

- Reset noise of C_F
- Reset noise of C_S
- Most low frequency, common mode noise such as external pickup, charge injection, power supply disturbances

Type NR noise:

- Reset noise of C_D
- Shot noise from pixel dark current
- Shot noise from TFT leakage current
- Most amplifier thermal and $1/f$ noise

To achieve quantum limited detection the readout must be designed so that its Type NR noise sources, when referred to the input, are less than the photon statistics noise from the lowest-level signals. The most demanding application is X-ray fluoroscopy, where the limited exposure rate (1 mR per image) requires single-photon detection: an equivalent noise charge < 750 rms electrons at a frame rate of 30 Hz [36].

The Type NR sources referred to the input give:

$$\mathrm{ENC}^2 \approx kTC_D + I_{\mathrm{dark}}T_{\mathrm{frame}} + 4kTR_{\mathrm{on}}BC_D^2 + e_n^2\left(\frac{C_S}{C_F}+1\right)^2 BC_F^2$$

where the first term represents the pixel reset noise, the second term is the dark current shot noise, the third term is the contribution of the TFT on-resistance, and the last term is the integrator noise. B is the effective noise bandwidth, e_n is the voltage noise spectral density of the integrator including thermal and $1/f$ sources.

For a typical AMFPI, $C_D \sim 1$ pF, $I_{\mathrm{dark}} \sim 100$ pA/cm^2, $R_{\mathrm{on}} \sim 1\mathrm{M}\Omega$. The amplifier bandwidth $B \sim 20$ kHz, and $e_n \sim 4$ nV/$\sqrt{\mathrm{Hz}}$. With these parameters the rms noise contributions become approximately

- Pixel kTC noise 400 e
- TFT R_{on} noise 100 e
- Dark current shot noise 100 e
- Amplifier series noise 100 e + 5 e/pF·C_S

For a full-sized AMFPI with 1000×1000 rows and columns C_S is about 100 pF, hence it can be expected that amplifier noise will dominate the readout.

6. Imager readout using scaled CMOS

CMOS is the most widely used technology for readout and control of imagers. It is widely available and well suited to logic, amplification, and switching functions. As CMOS follows the aggressive geometrical scaling dictated by Moore's law into the next decade, feature sizes will approach a limit-

ing value between 50 and 100 nm. At these dimensions digital integration density will reach impressive proportions while analog design will face challenges from low supply voltage, departure from square-law device behavior, off-state switch leakage, high gate tunneling current, and possible increases in device noise from channel hot electrons and gate dielectric damage [37]. Scaled CMOS is expected to remain an attractive choice for charge sensitive amplifiers and associated imager functions for the next 2 – 3 generations. As an example of what can be done today, an 8192 pixel processing chip in 0.25 μm CMOS has been reported [38]. This IC is bump-bonded to an array of Si photodiodes used as a charged particle detector for high energy physics. Each pixel (50 × 425 μm^2) contains amplifier, filter, discriminator, threshold DAC, delay/coincidence logic, FIFO, and control. The 220 mm^2 die holds over 13 million transistors, has less than 300 rms *e* equivalent noise with 25 ns pulse peaking time, and can be read out in 400 μs. Operating off a 1.6V supply it consumes 480 mW of power.

Farther in the future, research laboratories have begun exploring devices based on single-electron effects which are promising as very low-noise electrometers [39,40]. However, there is a fundamental relation between device capacitance and the ability to observe single-electron effects at room temperature that limits their usefulness to devices of a few attofarads (10^{-18} F).

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