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EXTENDING DIII–D NEUTRAL BEAM MODULATED OPERATIONS WITH A CAMAC BASED TOTAL ON TIME INTERLOCK

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Extending DIII–D Neutral Beam Modulated Operations with a CAMAC Based Total On Time Interlock*

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Abstract

A new total-on-time interlock has increased the operational time limits of the Neutral Beam systems at DIII–D. The interlock, called the Neutral Beam On-Time-Limiter (NBOTL), is a custom built CAMAC module utilizing a Xilinx 9572 Complex Programmable Logic Device (CPLD) as its primary circuit. The Neutral Beam Injection Systems are the primary source of auxiliary heating for DIII–D plasma discharges and contain eight sources capable of delivering 20MW of power. The delivered power is typically limited to 3.5 s per source to protect beam-line components, while a DIII–D plasma discharge usually exceeds 5 s. Implemented as a hardware interlock within the neutral beam power supplies, the NBOTL limits the beam injection time. With a continuing emphasis on modulated beam injections, the NBOTL guards against command faults and allows the beam injection to be safely spread over a longer plasma discharge time.

The NBOTL design is an example of incorporating modern circuit design techniques (CPLD) within an established format (CAMAC). The CPLD is the heart of the NBOTL and contains 90% of the circuitry, including a loadable, 1 MHz, 28bit, BCD count down timer, buffers, and CAMAC communication circuitry. This paper discusses the circuit design and implementation. Of particular interest is the melding of flexible modern programmable logic devices with the CAMAC format.

I. INTRODUCTION

The DIII–D tokomak at the DIII–D National Fusion Facility utilizes eight separate neutral beam injection systems for auxiliary heating of plasma discharges. Each system, consists of a neutral beam ion source, high voltage power supply, and a neutral beam control computer interface. The neutral beam control computer provides both the remote timing and command reference control for all eight high voltage power supplies, (subsequently biasing the ion sources to produce the injected beam). Each neutral beam system can operate at pulsed voltage levels approaching 90 kV depending on the physics requirement for a plasma discharge. The pulse duration for which each beam line can deliver energy is limited by the internal components of the beamline. This limit is a function of the beam energy [1]. Figure 1 illustrates the hardware interface between the neutral beam control computer, the DIII–D operations control computer, one of the eight neutral beam power supplies, and the corresponding neutral beam ion souce. The neutral beam control computer processes the requested voltage level along with many other parameters, calculates the time limit the system can safely operate at, and generates the power supply gate and reference command accordingly to produce the injected neutral beam. As shown in Fig. 1, the neutral beam power supply command depends on the neutral beam control computer gate command, the DIII–D pulse command, and the power supply fault control interlocks. The neutral beam control computer controls the shot start and stop time, while the DIII–D pulse command can originate from various sources depending on the plasma discharge requirements.

II. REQUIREMENTS

Due to a non-deterministic response time, the neutral beam control computer is not capable of real-time feedback monitoring and control of the high voltage power supplies. Therefore, it restricts beam operation time lengths under the conservative assumption they will occur with a 100% duty cycle. This assumption does not take advantage of the lower thermal impact beam-line components experience during modulated beam injections and thus unnecessarily limits the performance capability of the neutral beam auxiliary heating system. Yet, this insures against a power supply command error resulting in damaged beam-line components. The recent emphasis on modulated neutral beam operations coupled with the need to safely operate these systems at maximum capability highlighted the need for a stand-alone hardware based real-time interlock capable of eliminating the need for the restrictive computer time limits. The new hardware interlock would have to be capable of monitoring the neutral beam system during injection and stop the injection when the actual "on time" limit was reached. The neutral beam high voltage power supply command circuitry was decided as the best point to monitor and interrupt the injection time of the neutral beam ion source. The new interlock was identified as the Neutral Beam On-Time-Limiter (NBOTL).

III. SPECIFICATIONS

Once the requirement for the NBOTL was identified, initial development progressed by defining some arbitrary performance specifications. The typical neutral beam shot length at DIII–D is less than 4 s in length, while plasma discharges can approach 10 s. However, at lower power levels, the neutral beam systems can operate at time lengths approaching 10 s. In addition, the possibility of future long pulse operations at DIII–D warranted consideration. Therefore, 10 s was defined as both the present and near future expected maximum injection "on time" length. The

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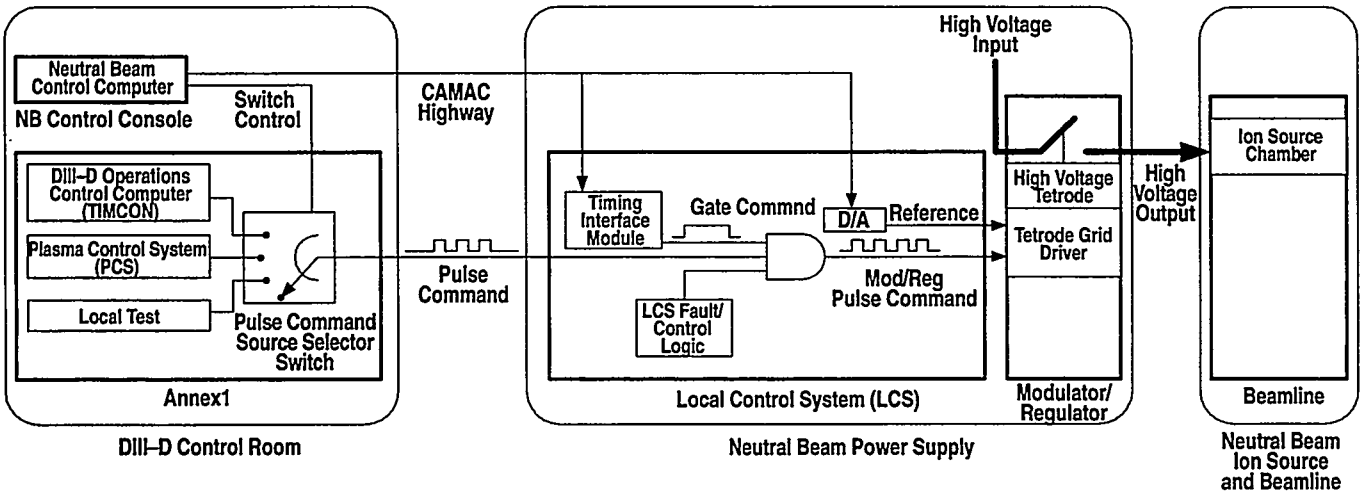

Fig. 1. A diagram of the computer to hardware interface for one of the eight neutral beam injection systems.

maximum modulated frequency was limited to 100 Hz with a duty cycle ranging from near 0% to 100%. The maximum injection time error allowed was to be less than 10 ms. Lastly, the "on time" limit was specified to be readily adjustable and separate for each neutral beam system. Several options were considered and included both analog and digital platforms ranging from analog integrators to small digital micro-controllers. A loadable digital count down counter with count enable control was determined to be the best approach to meet the hardware interlock specifications.

A gated synchronous count down timer was developed from a digital count down counter. A binary coded decimal (BCD) counter format coupled with a divisible by ten clock frequency functions as a timer, and eliminates the need for timer decoding. The gated timer only operates when enabled, i.e. when the neutral beam system is injecting. There are accuracy limitations associated with a synchronous timer utilizing a count enable control input. The limitations are manifested in the timing between the count enable and clock inputs. Depending upon when the count enable arrives in relation to the clock inputs-active state, the counter can miss up to a clocked count on both the rising and falling edge of each count enable pulse. Although this accumulated error is highly unlikely to occur, the timer design had to be conservative enough to accommodate it. Therefore, the timer clock frequency had to be of sufficient speed to minimize the accumulated count/time error. A 10 s shot at 50% duty cycle produces a maximum of 1000 beam "on" pulses. The maximum allowable timer error after a complete beam injection was specified to be less than 10 ms. A clock frequency of 1 MHz reduces the maximum expected accumulated time error to less than 2 ms across a 10 s injection. With the timer clock frequency set at 1 MHz, the 10 s maximum injection time length specification dictated the use of a 28-bit BCD count down counter. This architecture gives the timer a resolution of 1 ms. Seven linked 4-bit BCD counters produce the required 28-bit counter size. Finally, loadable count down counters were used to allow the programming of different time lengths depending on the injection time limit for each system. The loadable 28-bit BCD count down counter with count enable is shown in Fig. 2.

IV. DESIGN DEVELOPEMENT

Once the fundamental counter architecture of the NBOTL was defined, the implementation and interfacing within the neutral beam systems was determined. In evaluating this aspect of the design several considerations were required.

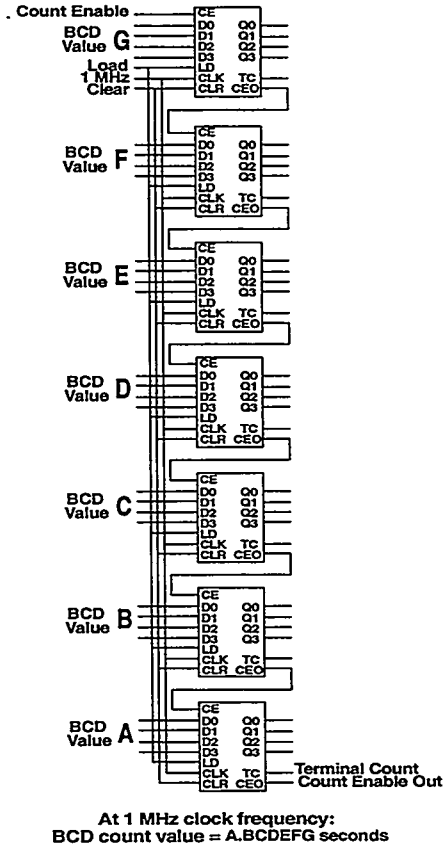

Fig. 2. 28-bit BCD counter design structure.

Since the neutral beam power supplies at DIII–D were produced by two independent manufacturers they shared little similarities in both command signal logic and hardware. However, they did share a common use of a CAMAC highway for computer control and communication. By implementing the NBOTL on a CAMAC platform, a direct interface with the neutral beam control computer was established allowing the counter/timer to be directly loaded with the calculated injection time limit.

A CAMAC highway interface was designed to decode both read and write commands from the neutral beam control computer. The decoded commands included both read and write functions as follows; ID – the NBOTL writes an identification value to the computer to verify its location, READ/STATUS – the NBOTL writes the status and count/timer value to the computer, CLEAR/RESET – the NBOTL resets associated hardware and clears the counter/timer, SET/LOAD – the NBOTL sets associated hardware and leads the counter/timer for count down.

The NBOTL interface to the high voltage power supplies command circuitry did not benefit from the use of the CAMAC platform. In order to make it universal between the two separate high voltage power supply systems, it was designed to be as non-intrusive as possible. By minimizing interface connections, modifications to the existing systems command signal circuitry hardware were painless. The NBOTL layout is shown in Fig. 3.

The NBOTL has three discrete signal connections identified as *Count Enable*, *Interlock In*, and *Interlock Out*. *Count Enable* is the count enable gate control signal for the NBOTL counter/timer. This input utilizes voltage comparators for analog signal conditioning, allowing the count enable signal to range from +0 to +24 V configured as either active high or active low logic. This analog signal conditioning also filters small noise perturbations from triggering a count cycle. *Interlock In* connects to the pole side of two series parallel configured analog switches. *Interlock Out* connects to the contact side of the analog switches. When closed, the switches complete the command signal circuit for the high voltage power supply. Each switch is controlled by a separate counter/timer circuit. This arrangement provides fault tolerance through redundancy. Should any of the separate counter/timer circuits fail in either mode, the remaining circuitry allows the NBOTL to complete its count operation, thereby eliminating any single point failure of the circuitry.

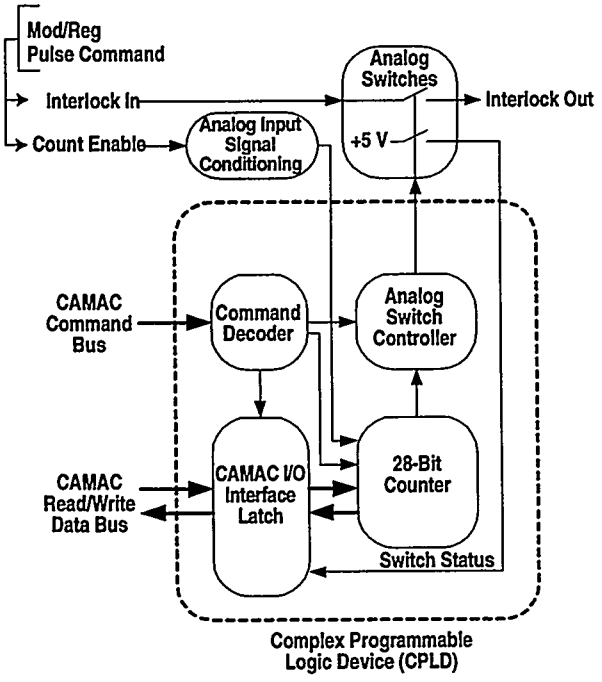

Fig. 3. The layout of one of the NBOTL counter circuits. Four of these circuits are connected in series/parallel.

Since the core of the NBOTL design was digital logic, it was decided that its construction could benefit from the use of Programmable Logic Devices. Both Field Programmable Gate Arrays (FPGA) and CPLDs were considered for this application. Either approach could be expected to produce the large scale integration of the NBOTL digital logic onto a single chip. However, the PLD's architecture is better suited to the programming of state machines utilizing logic functions such as the NBOTL counter circuit. The use of CPLD's provided virtually unlimited flexibility by virtue of their field re-programmability. Modifications to a logic circuit are simply made by reprogramming the CPLD chip, eliminating the need for hardware changes. Additionally, these program changes can be accomplished in situ, eliminating any need to move hardware or remove chip components. By taking advantage of the large scale integration capabilities of the CPLD, each separate counter/timer circuit was able to be programmed onto a separate CPLD chip. This was a major factor towards the NBOTL being laid out on one single width CAMAC printed circuit board.

Although the NBOTL is a custom design, its communication via the CAMAC highway had to meet the required standards [2]. All NBOTL communication across the CAMAC highway was accomplished through decoding logic included within the CPLD programming. A typical NBOTL set-up sequence proceeds as follows: 1) The neutral beam control computer determines the allowable time the neutral beam system can operate predicated by the plasma discharge requirements. 2) The computer resets the NBOTL via the CAMAC highway. 3) The NBOTL is read to verify the analog switches are open and the count is equal to zero. 4) The computer loads the count into the NBOTL. 5) The NBOTL is read to verify the analog switches are closed and the proper count has been loaded. 6) The command is sent to the neutral beam high voltage power supplies. The power supply output drives the ion source to produce the beam injection. During this time, the counter/timer within the NBOTL monitors the neutral beam power supplies' mod/reg command signal. If the command signal active state reaches the loaded time limit, the NBOTL analog switches are tripped and the power supply

command is interrupted. 7) After an injection, the NBOTL is read to verify the state of all four counter/timer circuits. If the injection was terminated for any other reason, the remaining count time of each counter/timer will be read and verified as a hardware cross check.

Figure 4 is a picture of the NBOTL. The four separate CPLD chips are visible along with the surrounding analog signal conditioning circuitry. By placing all the logic functionality within the CPLD programming, the circuit board layout was simplified.

V. PERFORMANCE

Utilization of the neutral beam systems at DIII–D has become more creative over the years, including the capability to modulate injections with "on times" ranging from 5 ms to full duty. In addition the plasma control computer (PCS) has the capability of holding certain DIII–D plasma parameters constant by varying the injected neutral beam power in real-time. Further, the PCS has recently introduced the real-time capability of substituting one neutral beam system for another which was requested for injection but failed to operate [3]. In order for beam substitution to work, the requested substitute neutral beam system must be scheduled to operate across the entire plasma discharge. However, the requested substitute may or may not be used depending on the real-time requirements during the plasma discharge. The substitute neutral beam source must therefore stand by in an armed and ready status. With several different systems possibly demanding the pulsing of the substitute beam, consequences of such a pulse can be serious. The requirement for an independent means of enforcing the neutral beam safe operating time limits drove the development of the NBOTL. The NBOTL has enhanced the performance of the neutral beam systems by increasing their flexibility in supporting plasma discharges.

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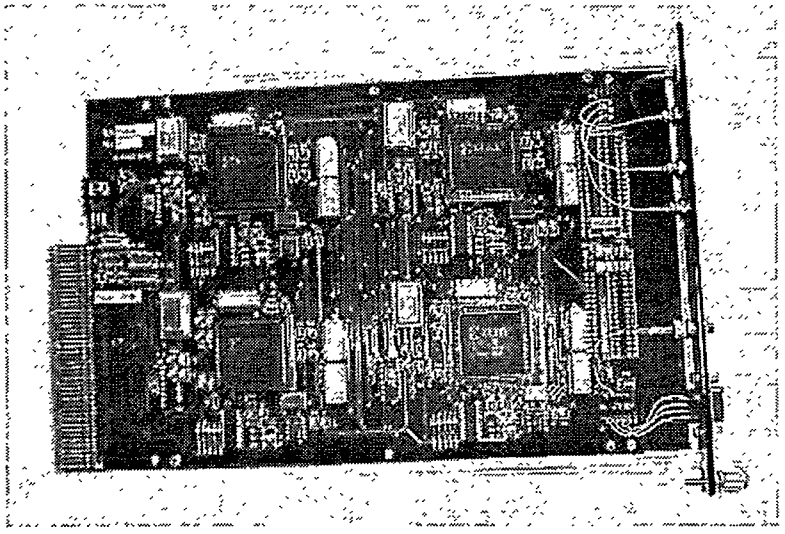

Fig. 4. Picture of the NBOTL final assembly (CAMAC single board width).