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LABORATORY

LLNL-TR-747185

3D Stacked Memory Final Report CRADA No. TC-0494-93

A. Bernhardt, G. Beene

March 2, 2018

Disclaimer

This work performed under the auspices of the U.S. Department of Energy by Lawrence Livermore National Laboratory under Contract DE-AC52-07NA27344.

3D Stacked Memory

Final Report
CRADA No. TC-0494-93

Date: April 23, 1998 Revision: 1

A. Parties

The project was a relationship between the Lawrence Livermore National Laboratory (LLNL) and Texas Instruments.

University of California
Lawrence Livermore National Laboratory
7000 East Avenue, L-795
Livermore, CA 94550

Texas Instruments
13532 N. Central Expwy
Dallas, TX 75265

B. Project Scope

TI and LLNL demonstrated: (1) a process for the fabrication of 3-D memory using stacked DRAM chips, and (2) a fast prototyping process for 3-D stacks and MCMs.

The metallization to route the chip pads to the sides of the die was carried out in a single high-speed masking step. The mask was not the usual physical one in glass and chrome, but was simply a computer file used to control the laser patterning process. Changes in either chip or customer circuit-board pad layout were easily and inexpensively accommodated, so that prototyping was a natural consequence of the laser patterning process. As in the current TI process, a dielectric layer was added to the wafer, and vias to the chip I/O pads were formed. All of the steps in Texas Instruments earlier process that were required to gold bump the pads were eliminated, significantly reducing fabrication cost and complexity. Pads were created on the sides of the die, which became pads on the side of the stack. In order to extend the process to accommodate non-memory devices with substantially greater I/O than is required for DRAMs, pads were patterned on two sides of the memory stacks as a proof of principle.

Stacking and bonding were done using modifications of the current TI process. After stacking and bonding, the pads on the sides of the dice were connected by application of a polyimide insulator film with laser ablation of the polyimide to form contacts to the pads. Then metallization was accomplished in the same manner as on the individual die.

	Deliverables /Milestones
1	Deliver first 10 laser-metallized DRAMs for stacking.
2	Metallize and bond stacks
3	Test stacks
4	Evaluate data on vapor deposited polyimide
5	Evaluate full process sequence
6	Deliver non-memory stack for testing

Project Changes

The project began in early 1995 after extensive negotiations over CRADA terms. The 2-year project terminated as scheduled in early 1997. The process milestones were met and certain process improvements were incorporated. Deliverables associated with stacked DRAM were also accomplished. The final deliverable (see Table above) was not attempted as the project had become closely tied to programmatic goals associated with the solid state memory required for the Flight Test program in Enhanced Surveillance and non-memory applications were not deemed to be of sufficient importance. Testing software was transferred from TI to Allied Signal Kansas City Plant where DRAMs and DRAM stacks produced by LLNL for the Flight Test program are currently being tested.

C. Technical

The process for fabrication of stacked DRAM memories has been significantly simplified and improved. The introduction of the 16Mb generation of DRAM permitted deposition of die side-wall passivation using a physical mask to protect I/O pads which are located along the center line of the die instead of around the perimeter of the die.

D. Partner Contribution

A process for the fabrication of stacked Dynamic Random Access Memory (DRAM) devices for high density packaging was pioneered by Texas Instruments. The purpose of this project was to reduce the total cost of stacked memory production, to enable the technology to be applied to non-memory dice, and to provide a method for quick prototyping of stacked dice modules and multichip modules (MCM). TI contributed expertise in die processing, bonding and testing to the project. In addition, TI provided cost modeling so that the full process sequence could be compared to alternatives and so that the absolute numbers could be compared to market price demands.

E. Documents/Reference List

1) Reports: None

2) Intellectual Property

i) Subject Inventions

Art. I: "Subject Invention" means any invention of The Regents or Participant conceived or first actually reduced to practice in the performance of work under this CRADA.

Art. XIV: The Parties agree to disclose to each other each and every Subject Invention that may be patentable or otherwise protectable under the Patent Act.

Art. XV: Each Party has the option to retain title to any invention made by its employees. If a Party elects not to retain title to any invention made by its employees, then the other Party has an option to elect to retain title to such invention under the CRADA.

LLNL Sole Subject Invention:

IL-9884, "A New Outside Gaseous Source of Organic Monomer for High Vapor Pressure Delivery Into A Vacuum Chamber," Vincent Malba, Vladimir Liberman.

LLNL declined to elect title to this Subject Invention. Participant has not indicated an interest in electing title to this Subject Invention.

Participant Sole Subject Inventions disclosed: None

Joint Subject Inventions: None

ii) Copyrighted Computer Software:

No copyrighted computer software was developed by LLNL or Participant under this CRADA.

iii) Licensing Activity:

Appendix C provides that to the extent that LLNL obtains title or authority to license solely developed CRADA Intellectual Property first arising or produced under the Statement of Work, LLNL shall negotiate and grant to Texas Instruments, Defense Systems and Electronics Group at its request, by separate agreement, a five year, royalty-free, nonexclusive license to use such intellectual property to make, have made, use and sell products based thereon.

Appendix C further provides that if there are other intellectual properties owned or controlled by either Party that are needed by either side for the effective and timely commercialization of Project technology, the Party or Parties, subject to internal policy and prior commitments, shall made such intellectual properties available under appropriate commercial licenses or other use arrangements.

Participant has not requested to license any LLNL technology arising out of the work conducted under this CRADA.

E. Acknowledgement

Participant's signature of the final report indicates the following:

1) The Participant has reviewed the final report and concurs with the statements made therein.
2) The Participant agrees that any modifications or changes from the initial proposal were discussed and agreed to during the term of the project.
3) The Participant certifies that:
   a) all reports either completed or in process are listed;
   b) all subject inventions attributable to the project have been disclosed or are included on a list attached to this report; and
   c) appropriate measures have been taken to protect intellectual property attributable to this project.
4) The Participant certifies that if tangible personal property was exchanged during the agreement, all has either been returned to the initial custodian or transferred permanently.
5) The Participant certifies that proprietary information has been returned or destroyed by LLNL.

Gary Beene Date	Anthony Bernhardt Date
Texas Instruments	Lawrence Livermore National Laboratory
Raytheon TI Systems Division	
(formerly Defense Systems Group of TI)	

Attachment I – Final Abstract
Attachment II – Project Accomplishments Summary
Attachment III – Final Quarterly Report

3D Stacked Memory

Final Abstract
Attachment I
CRADA No. TC-0494-93

TI and LLNL demonstrated: (1) a process for the fabrication of 3-D memory using stacked DRAM chips, and (2) a fast prototyping process for 3-D stacks and MCMs.

The metallization to route the chip pads to the sides of the die was carried out in a single high-speed masking step. The mask was not the usual physical one in glass and chrome, but was simply a computer file used to control the laser patterning process. Changes in either chip or customer circuit-board pad layout were easily and inexpensively accommodated, so that prototyping was a natural consequence of the laser patterning process. As in the current TI process, a dielectric layer was added to the wafer, and vias to the chip I/O pads were formed. All of the steps in Texas Instruments earlier process that were required to gold bump the pads were eliminated, significantly reducing fabrication cost and complexity. Pads were created on the sides of the die, which became pads on the side of the stack. In order to extend the process to accommodate non-memory devices with substantially greater I/O than is required for DRAMs, pads were patterned on two sides of the memory stacks as a proof of principle.

Stacking and bonding were done using modifications of the current TI process. After stacking and bonding, the pads on the sides of the dice were connected by application of a polyimide insulator film with laser ablation of the polyimide to form contacts to the pads. Then metallization was accomplished in the same manner as on the individual die.

3D Stacked Memory

Project Accomplishments Summary (Attachment II)
CRADA No. TC-0494-94

Date: April 23, 1998 Revision:

A. Parties

The project was a relationship between the Lawrence Livermore National Laboratory (LLNL) and Texas Instruments.

University of California
Lawrence Livermore National Laboratory
7000 East Avenue, L-795
Livermore, CA 94550

Texas Instruments
13532 N. Central Expwy
Dallas, TX 75265

B. Background

A process for the fabrication of stacked Dynamic Random Access Memory (DRAM) devices for high density packaging had been demonstrated by Texas Instruments (TI) under DARPA support. Texas Instruments wished to improve the processes for making these stacked memory modules. The purpose of the improvements was to reduce the total cost of stacked memory production, to enable the technology to be applied to non-memory dice, and to provide a method for quick prototyping of stacked dice modules and multichip modules (MCM).

Lawrence Livermore National Laboratory (LLNL) had developed a laser patterning process for interconnecting dice to MCM substrates. This process is capable of patterning metal interconnect lines on three dimensional (3-D) surfaces, which means that the process could be used to "write around the corner" of a die or substrate. In fact, LLNL had patterned metal lines that run along the top, sidewall, and bottom of substrates. The laser process is computer controlled, so that masks, screens, or TAB tape are not required, greatly reducing lithography costs and turnaround time.

The LLNL 3-D laser patterning process (and other technology developed at LLNL) may substantially reduce the per-chip packaging cost for TI. The current TI process costs about $75 per chip compared to the roughly $2/chip it costs to package multiple memory die by conventional methods (e.g., SIMMs). Customers will pay a premium for the high density of stacked memories but not more than a fraction of the cost of the memory die themselves. TI estimates that its present process cost could not be reduced below $10 per die in high volume production. Using the LLNL technology, 3-D packaging costs per die might be reduced to the $3–5 per die target range.

TI was limited to stacking only DRAMs, because their process could not interconnect dice on more than one side of the stack. LLNL's technology is capable of patterning interconnects on four sides of the stack, which means that chips with a high density of I/O pads on all four sides can be stacked. A technology capable of stacking microprocessors, memory, and other logic devices would create new markets, particularly in the military and space arenas, but also in the commercial arena, where hand-held instruments, laptops, automotive controls, and robotics would benefit greatly from the increase in processing power per unit volume.

The 3-D laser patterning technology developed by LLNL would also be beneficial for prototyping new stack configurations and new MCM designs. Since the LLNL process requires no masks or TAB tape, different combinations of chips can be tried with considerably lower cost and faster turnaround time than is currently possible. The advantage of such a prototyping process is that products can be developed much quicker, so that the design-to-market time is reduced, improving TI's competitiveness. LLNL intends to develop a prototyping system with TI that will have applicability to both stacked dice modules and conventional multichip modules.

C. Description

TI and LLNL demonstrated: (1) a process for the fabrication of 3-D memory using stacked DRAM chips, and (2) a fast prototyping process for 3-D stacks and MCMs.

The metallization to route the chip pads to the sides of the die was carried out in a single high-speed masking step. The mask was not the usual physical one in glass and chrome, but was simply a computer file used to control the laser patterning process. Changes in either chip or customer circuit-board pad layout were easily and inexpensively accommodated, so that prototyping was a natural consequence of the laser patterning process. As in the current TI process, a dielectric layer was added to the wafer, and vias to the chip I/O pads were formed. All of the steps in Texas Instruments earlier process that were required to gold bump the pads were eliminated, significantly reducing fabrication cost and complexity. Pads were created on the sides of the die, which became pads on the side of the stack. In order to extend the process to accommodate non-memory devices with substantially greater I/O than is required for DRAMs, pads were patterned on two sides of the memory stacks as a proof of principle.

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D. Expected Economic Impact

A mass market needs to develop in order for the technology to be commercialized. Potential mass markets include memories for laptop computers, cellular telephone baseband memory and logic, and digital cameras. But manufacturers of such mass market products need to be assured that the technology will be cost effective. We are working with potential vendors for the technology and big potential customers on resolving the problem of distributing the risk associated with the commercialization of the technology.

E. Benefits to DOE

The original development work for stacked memories was supported by DARPA because of numerous applications in defense systems. The DOE Space Initiative with NASA, as well as related DOE-executed Department of Defense (DOD) satellite programs, need densely packaged memories. Smarter satellites will be important for

treaty verification. Supercomputer systems used by the DOE for weapons development, Grand Challenge problems, and numerous physics and engineering simulations all benefit from higher clock rates, larger high-speed storage, lower system power, and lower cost provided by stacked memories. Hand-held electronics are significant in military markets (for example GPS location designation systems with stored maps). Furthermore, a US-based supply of such memory systems to domestic computer suppliers will help the DOE retain first-access to the latest supercomputer technology.

The TI collaboration is essential to LLNL's success in building a solid state memory for the telemeter for the Flight Test application. First of all, this collaboration paid for LLNL's process development for vapor deposited polyimide and laser metallization. In addition, TI supplied LLNL with know-how on chip bonding and stacking and will be doing environmental testing on our memory cubes. Such testing validates the LLNL 3-D stacked memory technology for military applications as well as for DOE applications. TI will do the electrical tests of the LLNL memory module for the telemetry package and has agreed to supply its electrical test programs to Allied Signal Kansas City Plant for future telemetry modules.

On our end of the collaboration LLNL has supplied prototype parts and know-how on our vapor deposited polyimide and Laser Pantography processes to TI who will be fabricating memory stacks for Cray Research. The Cray deal bolsters the ASCI Program with higher performance, lower cost, and denser memories.

This advanced electronic packaging technology is also important to micro-electromagnetic strong links for the fabrication of a miniature integrated protection and initiation device. In this application, a discrete magnetic core replaces the DRAM in the TI collaboration but our 3D metallization process is the same. In one type of strong link, a magnetic core forms the actuator of a micro-relay. Using this process we have bridged the gap between wires mechanically wrapped around magnetic cores (too big) and thin film deposited magnetic structures (no inductance or power handing).

F. Industry Area

Consumer electronics, semiconductor packaging, communication.

G. Project Status

This project is completed.

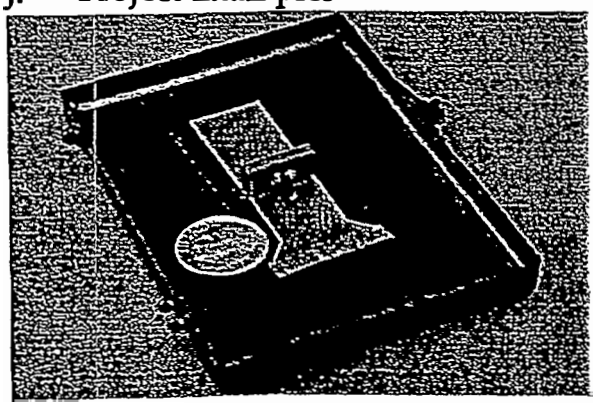
H. LLNL Point of Contact for Project Information

Anthony Bernhardt
LLNL
L-271
Ph: (925) 423-7801

I. Company Size and Point(s) of Contact

The industrial partner was the Defense Systems Group of Texas Instruments which has since become Raytheon TI Systems Division of Raytheon, Inc. The technical contact was Gary Beene, (972) 995-1295; fax (972) 995-0064.

J. Project Examples



This is a stack of nine 16 Mb DRAM chips plus a decoupling capacitor substrate, mounted on flex tape prior to attachment to a circuit board. The total capacity of this stack is 144 Mb in a volume of 15X7X4 mm. Note that funding from the Enhanced Surveillance Program also contributed to this module.

K. Intellectual Property

i) Subject Inventions

Art. I: "Subject Invention" means any invention of The Regents or Participant conceived or first actually reduced to practice in the performance of work under this CRADA.

Art. XIV: The Parties agree to disclose to each other each and every Subject Invention that may be patentable or otherwise protectable under the Patent Act.

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LLNL Sole Subject Invention:

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Participant Sole Subject Inventions disclosed: None

Joint Subject Inventions: None

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iii) Licensing Activity:

Appendix C provides that to the extent that LLNL obtains title or authority to license solely developed CRADA Intellectual Property first arising or produced under the Statement of Work, LLNL shall negotiate and grant to Texas Instruments, Defense Systems and Electronics Group at its request, by separate agreement, a five year, royalty-free, nonexclusive license to use such intellectual property to make, have made, use and sell products based thereon.

Appendix C further provides that if there are other intellectual properties owned or controlled by either Party that are needed by either side for the effective and timely commercialization of Project technology, the Party or Parties, subject to internal policy and prior commitments, shall made such intellectual properties available under appropriate commercial licenses or other use arrangements.

Participant has not requested to license any LLNL technology arising out of the work conducted under this CRADA.

L. Release of Information

I certify that all information contained in this report is accurate and releasable to the best of my knowledge.

Karena McKinley, Director
Industrial Partnerships
and Commercialization

9/12/00
Date

RELEASE OF INFORMATION

I have reviewed the attached Project Accomplishment Summary prepared by Lawrence Livermore National Laboratory and agree that the information about our CRADA may be released for external distribution.

Gary Beene
Texas Instruments
Raytheon TI Systems Division
(formerly Defense Systems Group of TI)

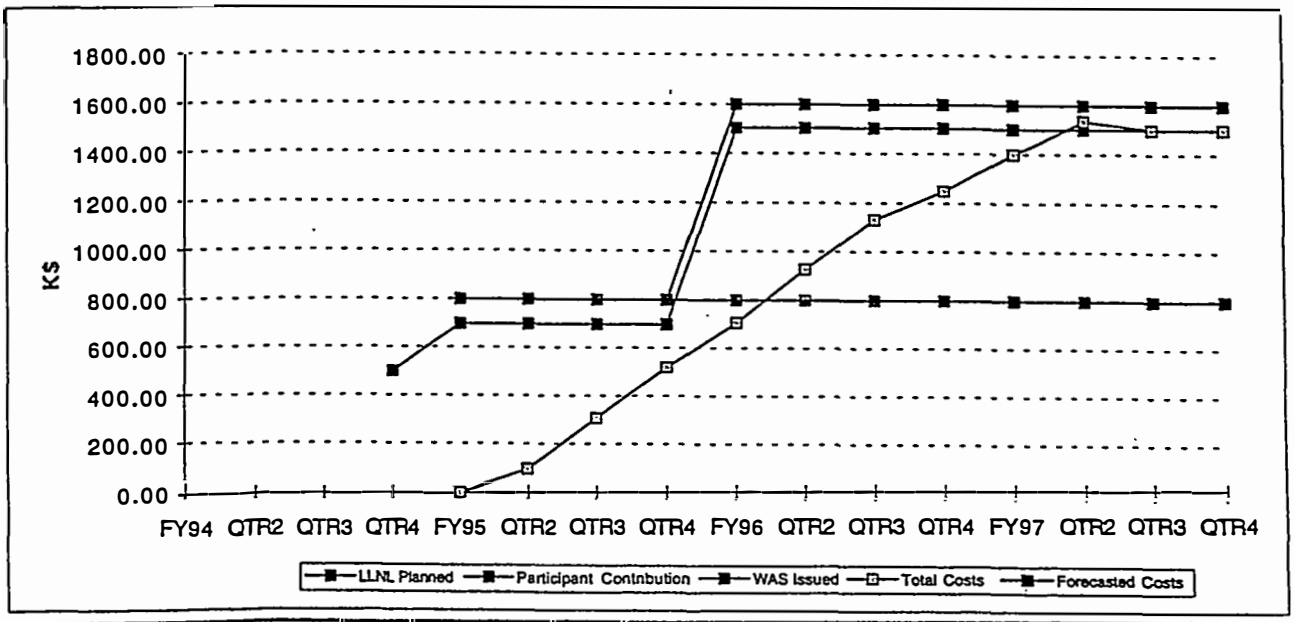
8/9/00
Date

Lawrence Livermore National Laboratory

Title:	3D Stacked Memory	Reporting Period:	06/30/95 - 9/30/97
Participant:	Texas Instruments	Date CRADA Executed:	1/9/95
DOE TTI No.:	93-LLNL-045-D1	DOE Approval Date:	12/19/93
CRADA No.:	TC-0494-93	Scheduled Ending Date:	1/8/97
TACT:	Microelectronics	B & R Code (S):	GB010601
Account Numbers	4775-24/25		35GB0106

Approved Funding Profile ($K)

	FY94	FY95	FY96	FY97	FYOUT	Total
LLNL Planned	0	800	800	0	0	1600
Participant In-Kind	0	800	0	0	0	800
Participant Funds-In	0	0	0	0	0	0
WAS Operating	500	200	803	-2	0	1501
WAS Capital	0	0	0	0	0	0
Total Costs	0	518	732	250	0	1500



GB010601	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	July	Aug	Sep	FYTD
FY94	0	0	0	0	0	0	0	0	0	0	0	0	0
FY95	0	0	0	0	43	54	57	76	78	157	-13	66	518
FY96	35	67	87	62	81	77	59	66	81	10	55	54	732
FY97	41	55	53	45	45	47	-36	0	2	-2	0	0	250
FYOUT	0	0	0	0	0	0	0	0	0	0	0	0	0

1500

35GB0106	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	July	Aug	Sep	FYTD
FY94	0	0	0	0	0	0	0	0	0	0	0	0	0
FY95	0	0	0	0	0	0	0	0	0	0	0	0	0
FY96	0	0	0	0	0	0	0	0	0	0	0	0	0
FY97	0	0	0	0	0	0	0	0	0	0	0	0	0
FYOUT	0	0	0	0	0	0	0	0	0	0	0	0	0

0

STAFF w/phone:

Lab PI: Tony Bernhardt (510) 423-7801 — Participant: Gary Beene (214) 995-1295

Resource Manager: Dana Richards (510) 422-4366

DOE OAK: Jerry Scheinberg (510) 637-1653 — DOE HQ: Diane Bird (202) 586-0499

Reporting Period: 06/30/95 - 9/30/97
DOE TTI No.: 93-LLNL-045-D1
CRADA No.: TC-0494-93

Milestones and Deliverables:

List the complete set of milestones for all phases of the CRADA. Continue on separate pages if necessary.
Report any changes from the original CRADA or previous quarterly report on the CRADA Change Form.

	Completion Date: Scheduled	Actual
Deliver first 10 laser-metallized DRAMs for stacking.	09/95	09/95
Metallize and bond stacks	10/96	10/96
Test stacks	10/96	10/96
Evaluate data on vapor deposited polyimide	07/96	07/96
Evaluate full process sequence	12/96	12/96

Verification of participants' in-kind contribution was made in accordance with LLNL policy. Explain basis of verification: Please initial: YES X NO ____

TI contributed expertise in die processing, bonding and testing to the project and provided cost modeling so that the full process sequence could be compared to alternatives and so that the absolute numbers could be compared to market price demands. TI will do the electrical tests of te LLNL memory module for the telemetry package and has agreed to supply its electrical test programs to Allied Signal Kansas City Plant for future telemetry modules.

List any copyrights, awards, patents, invention disclosures, additional background intellectual property, or reportable economic impacts during the quarter

Accomplishments this quarter (address and be specific about milestones, problems, participant contributions)
Continue on a separate page if necessary.

See attached.

Reviewed by CRADA project Program Manager: _____ Date: _____

Reviewed by Karena McKinley, Director, IP&C: Norma E Dunagan Date: 9/12/00

Direct questions regarding this Quarterly Report to IP&C Resource Manager, Carol Asher, at (510) 422-7618