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GaAs Integrated Circuit Process Characterization and Non-Destructive Process Monitoring by Atomic Force Microscopy

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We report a new application of atomic force microscopy (AFM) for process characterization of GaAs integrated circuit fabrication. By using the near atomic-level z-resolution of AFM, we are able to gain information not available by other imaging techniques in a number of steps in the sequence for GaAs IC fabrication. A non-destructive method of determining whether micron-sized vias have been etched to completion is presented. In addition, the AFM has been used to evaluate material removal following several of fabrication steps. Shallow trench formation occurs as a result of GaAs removal during the sidewall etch for a commonly used sidewall spacer process. This effect has been not been observed previously by other techniques. Other examples of unintentional removal of small amounts of GaAs during shallow wet and dry etches are presented. These examples show the utility of AFM as an in-line process characterization tool.

INTRODUCTION

As microelectronic device dimensions get smaller and smaller, the need for higher resolution imaging and novel methods of microcircuit process characterization increases. Some features become too small to image effectively with commonly used tools. In other cases small defects not adversely affecting current generation technologies can be very significant for emerging technologies. Atomic force microscopy (AFM) is a relatively new technique, which in many cases provides superior imaging capabilities to conventional techniques such as scanning electron microscopy (SEM), while in other cases offers novel ways of examining device structures. Because of its superior imaging capabilities and the ability to image non-conductive samples as easily as conductive samples, AFM is rapidly becoming a widely used characterization tool for examining the growth and deposition of thin film semiconductor materials. However, the use of AFM as an integrated-circuit (IC) process characterization tool is just beginning [1,2].

In this paper we present three novel applications of AFM to GaAs IC process characterization and process monitoring. First the high resolution imaging capabilities of AFM are exploited to provide a non-destructive, in-line tool for monitoring micron-sized vias in a 2-level metal interconnect process. Second, a subtle defect associated with the sidewall formation in self-aligned field effect transistors (FET) is reported. This defect, a shallow trench at the sidewall edge, has escaped detection by conventional process characterization tools. Finally, AFM is used to characterize the unintentional removal of small amounts of GaAs during shallow wet and dry etches. In all of these examples, the use of AFM extends the process characterization capabilities beyond that available by other techniques.

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GaAs IC PROCESS CHARACTERIZATION AND MONITORING

IC fabrication relies heavily on process characterization and monitoring tools first to define a process for a given fabrication step and then to ensure that the process operates repeatably. In general, process characterization refers to the use of both destructive and non-destructive techniques that may not be suitable for production to optimize the process conditions and learn as much as possible about the process. The end goal of this process characterization is the determination of a range of process parameters within which the process is robust, i.e. operates with limits (called the process window) which are larger than random variations typically encountered. Process monitoring refers to techniques that verify that the process window is not exceeded and these should be non-destructive, or possibly used on an infrequent sampling basis. Often the techniques used for process characterization are higher in resolution or otherwise offer more information than techniques used in process monitoring. However, the examples presented in this paper show that the AFM is a versatile tool with capabilities for both process characterization and in-line process monitoring.

The examples chosen for this paper come from a GaAs IC process whose performance and fabrication details have been presented previously [3,4]. However, these examples with slight changes should be applicable to any IC process. All AFM imaging was performed using a Digital Instruments Dimension 3000 system operating in tapping mode with Si tips in a class 100 clean room.

IN-LINE PROCESS MONITORING OF MICRON-SIZED VIAS

The via hole is an opening in a dielectric insulator for a contact between different interconnect metal layers. The via is patterned with photoresist and formed by reactive ion etching (RIE). Micron-sized vias can be inspected non-destructively with optical microscopy or by low voltage SEM, but these techniques do not conclusively determine successful etch completion because a small amount of residual dielectric film in the via bottom cannot be detected. Under-etched via holes lead to "opens" when a subsequent electrical test is performed. By the time an electrical test determines a via failure, many more lots may have been ruined, so more immediate feedback of process failures is desirable. Using surface profilometry measurements on larger area etched features for process monitoring is an option, but the results can be misleading due to microloading effects (differing etch rates for small and large area features) and etchant transport effects (etchant is less efficient getting into small

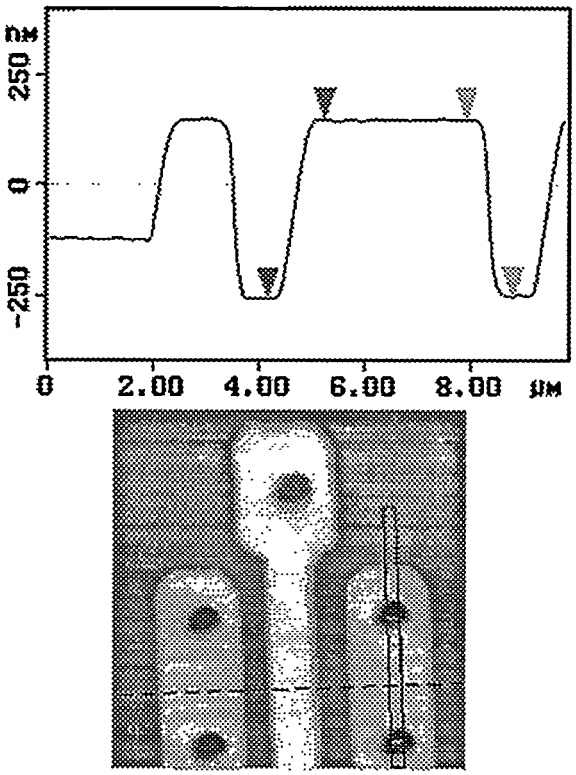

Figure 1. Cross-sectional analysis method for determining via etch depth. The rectangular area in the AFM image averages data for the AFM cross section. Cursor placement yields via depths of 402 nm and 399 nm.

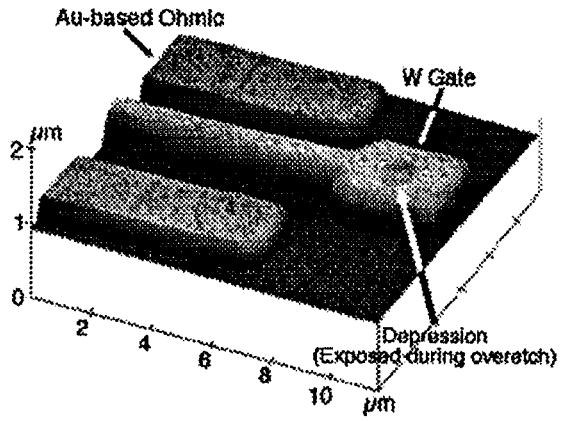

Figure 2. AFM image of the 150% etched sample after the Si_3N_4 was chemically removed. Note the depression in the W gate and lack thereof in the ohmics.

diameter deep features) which are common in RIE.

The GaAs-based FET fabrication steps relevant to this section are as follows: (1) Refractory gate definition with a 300 nm thick W film and RIE; (2) Ohmic metal definition with approximately 300 nm of GeAuNiAu; (3) Interlevel dielectric deposition using approximately 400 nm of Si_3N_4; and (4) Fabrication of 1.25 μm via holes defined by optical lithography and etched in a RIE SF_6/O_2 plasma. Endpoint is determined during the RIE using in-situ optical interferometry on large open areas. If the via hole resist mask is even slightly underexposed or underdeveloped, resist may remain in the via resulting in an incomplete etch.

An AFM image of five etched Si_3N_4 via holes to the gate and ohmic metal pads are shown in Figure 1. SEM images similar to this AFM image can be obtained non-destructively, but 3-D digital height data is not available with SEM. Using the measured 3-D AFM data, the images are analyzed in cross section by taking line traces through the vias over one ohmic metal pad. Etch depths of 402 nm and 399 nm are measured for these vias. These measurements illustrate the manner in which all of the via etches were imaged and analyzed. Although the measured via depth is close to the measured thickness of the Si_3N_4 dielectric, thickness variations as well as measurement uncertainties do not rule out the possibility that a small amount of dielectric remains at the via bottom. In order to identify a more highly controlled process control monitor using the AFM, via depth was compared for both gate and ohmic vias from the same FET. Because the W-based gate via should continue to etch in the F-based chemistry but the Au-based ohmic via should not, we investigated a via etch difference as a specific endpoint marker. Fig. 2 shows an AFM image of a GaAs FET with a via etch 50 % beyond endpoint and with the Si_3N_4 subsequently removed by buffered oxide etchant (BOE). The circular depression in the W gate and the lack of these features in the adjacent Au-based ohmics verifies that the etch difference is evident in the GaAs IC process. This depression was measured by AFM to be 45 ± 5 nm, which equates to an etch rate of W in the SF_6/O_2 RIE of 69 nm/min (the Si_3N_4 etch rate is 300 nm/min).

Vias were also etched from 20 to 150% of the optically determined endpoint. In Figure 3 the AFM measured etch depth for the vias over the gate and ohmic metals are plotted as a function of etch time. The difference in measured etch depth between the gate and ohmic vias is also plotted in Figure 3. The via depth over the Au-based ohmic metal reaches a maximum value, whereas, the via depth over the W metallization continues to increase. Fig. 4 shows the etch difference between gate and ohmic vias plotted against the measured gate via depression after nitride removal. As expected, there is good agreement between these independently measured results. The via process typically includes a 20 % over etch to account for uncertainties in endpoint, microloading effects, Si_3N_4 thickness non-uniformities, and etch non-uniformity. With this specific process marker, we conclude that the vias are etched to completion as long as at least a 10 nm via etch depth difference is measured on adjacent gate- and ohmic-based vias. The 10 nm etch difference

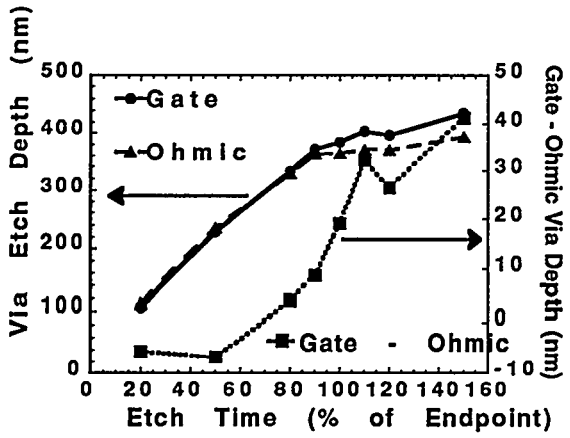

Figure 3. Plot showing the AFM measured via etch depth over ohmic and gate metallizations as a function of etch time. The second plot is of the measured via depth over gate minus the via depth over ohmic; the difference increases due to W plasma attack during overetch.

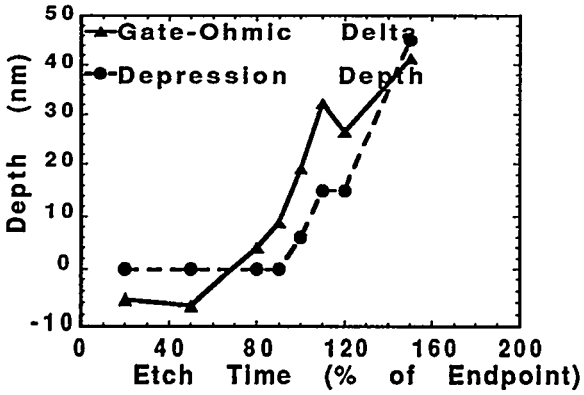

Figure 4. A comparison between the AFM measured via depth over gate minus via depth over ohmic difference and the measured etched depth into the W gate metal (after Si_3N_4 removal) as a function of etch time.

is achieved well within the 20 % over etch time. Therefore, the use of AFM-derived via etch differences between the gate and ohmic vias as a marker for etch completion was verified and implemented in our laboratory. A process failure is now detectable at a point in the process where rework is a feasible option. We are now also expanding this technique into other material systems to make it useful to a sider range of applications, i.e. Si-based via imaging.

TRENCH FORMATION DURING GaAs FET SIDEWALL ETCH

Refractory gates are used for self-aligning the source and drain implants in GaAs FETs in order to produce low source resistances. As the gate length is reduced into the sub-micron regime, severe short channel effects are encountered unless the implant is spaced from the edge of the gate. Dielectric sidewalls are a commonly used means to space the implants. In the GaAs FET sidewall process, sidewalls are formed at the edge of a refractory gate by the following process: (1) An approximately 400 nm SiO_2 film is deposited over the W-gate by plasma enhanced chemical vapor deposition; (2) The SiO_2 is then etched back with reactive ion etching (RIE) in a CHF_3/O_2 chemistry. Because of the predominance of vertical etching in RIE, a sidewall is formed next to the gate in the region where the vertical thickness of the deposited film is the greatest.

AFM was used to analyze the GaAs surface at the gate region after removing the sidewalls in buffered oxide etch and then removing the gates with micro-mechanical probes. This technique is useful because only part of the gate is removed with the remaining gate serving as a location guide to image the region of interest. The resulting 3-D AFM image is shown in Fig. 5. The previously uncovered GaAs surface "field" was apparently etched, resulting in a step where the GaAs was protected by W. Note the trenches which appear on both sides of the GaAs that was

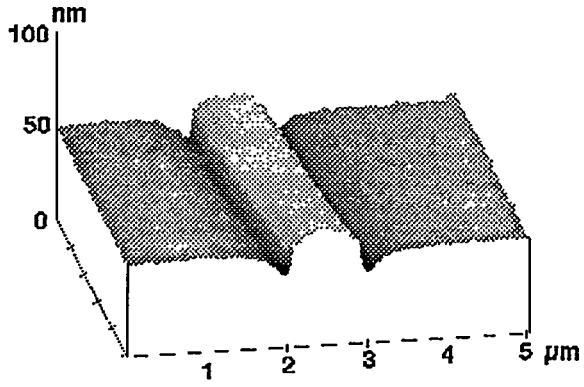

Figure 5. 3-D AFM image of a GaAs surface where a patterned W gate with SiO_2 sidewalls was chemically removed. Note the trenches at the edges of where the gate was before removal.

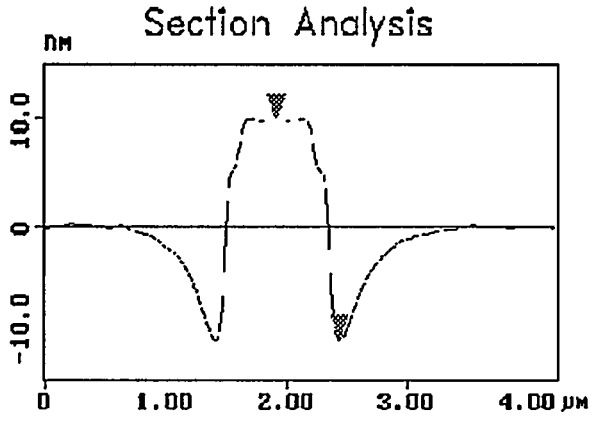

Figure 6. AFM cross-sectional analysis on the image shown in Figure 5. The cursor placement indicates that the trenches are etched 21 nm deep into the GaAs surface.

under the gate metal. The "GaAs gate" was visible only as a shadow when viewed under an optical microscope and only as a shadow at the edge of the gate when viewed by SEM. The etched depth was not quantifiable when viewed by cross-sectional SEM. These AFM images were further analyzed by averaging several line scans through the 0.8 μm gate. An averaged line scan trace for the device region shown in Figure 5 is displayed in Figure 6. Cursors mark the region of greatest interest (and concern) showing a height difference of 21 nm in a region where the GaAs field ideally would not be noticeably attacked during the refractory or sidewall etch.

In order to verify this interpretation of the AFM data and uncover the cause of the trenching, cross-sectional SEM analysis was performed on un-etched and partially etched dielectric sidewall samples. Fig. 7 shows a SEM cross section of the gate region after SiO_2 deposition. It is seen that a cusp forms at the intersection of the film covering the GaAs and the side of the gate. In Fig. 8 it is seen that the region of the cusp forms a trench in the dielectric prior to completion of the sidewall etch. This trench then exposes the GaAs surface at the edge of the sidewall to sputtering from the RIE prior to dielectric etch completion. The trench is then transferred to the GaAs under conditions where the GaAs sputter rate is significant in comparison to the SiO_2 etch rate. For our GaAs IC process, the SiO_2 etch rate is 19 nm/min compared to a GaAs sputter rate of 2 nm/min in the RIE. Thus, it is apparent that unintentional removal of small amounts of GaAs must also be quantified, a subject treated in the next section. This example also illustrates that AFM in no way precludes the use of conventional imaging techniques, but rather can complement them very well.

Based on this information, a solution to the problem was found by changing dielectrics to a Si_3N_4 PECVD film and using a SF_6/CHF_3 chemistry, thus increasing the Si_3N_4 etch rate to 160 nm/min. As this chemistry also increased the GaAs sputter rate, a 2-step etch was employed to use the CHF_3/O_2 chemistry during the over etch period to maintain the GaAs sputter rate at 2 nm/min [5].

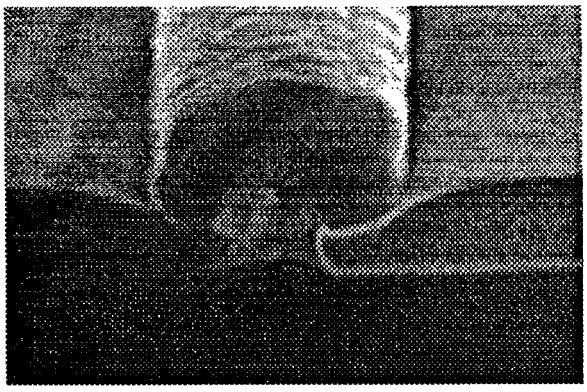

Figure 7. SEM cross-section of SiO_2 over gate prior to sidewall etch.

Figure 8. SEM cross-section of a SiO_2 sidewall etch stopped at 60 % of end point.

UNINTENTIONAL GaAs REMOVAL

Material removal rate information is useful to the process engineer to better control various processing steps. Surface profilometry is the technique of choice for quantifying material removal in IC fabrication facilities because of its ease of use, low cost, and accuracy of approximately ± 5-10 nm. In a number of processing steps, it is useful to quantify total material removal of less than 5-10 nm and surface profilometry is not suitable unless longer than typical process times are used, and then subtle effects such as latency of etch initiation must be taken into consideration. To determine whether that is the case and to better characterize small amounts of material removal, AFM is a useful tool.

An example of shallow wet etches in a GaAs FET process is the p^+-GaAs removal after gate formation for a GaAs JFET [6]. The GaAs active region of the FET was implanted prior to the etch, while the non-FET region outside the active area remained unimplanted. When the FET was imaged by AFM, a 1 nm etch difference in a total etch of 30 nm was observed between implanted and unimplanted areas at the edge of the FET active region while using a H_3PO_4:H_2O_2:H_2O etch chemistry. Further work may determine whether this difference is due to etch latency in the implanted region or whether there is a small constant etch rate difference. However, for the GaAs JFET process this effect was not determined to significantly affect the devices.

Another example is the GaAs sputter rate responsible for the trench formation discussed previously and GaAs sputtering during gate metal etching. Prior to this work, this sputter rate was assumed to be negligibly small and no attempt was made to measure it with other techniques. Using photoresist as a mask on GaAs, the effects of SiO_2 sidewall etching in a CHF_3/O_2 chemistry and W gate etching in a SF_6/Ar chemistry on GaAs were examined for times ranging from 0.5 to 5 min. After removing the photoresist in acetone and isopropyl alcohol, the samples were imaged using AFM. As seen from the results plotted in Fig. 9, the sputter rate is linear in time with as little as 1 nm material removal being measured. No etch latency is observed. This result is consistent with the assumed sputter mechanism of GaAs. These data can be used to determine acceptable RIE exposures of GaAs based on tolerable limits of material removal. The similar sputter rates of the sidewall and gate etch chemistries is probably coincidental because of the different ion masses, pressure, and dc bias in the two etch chemistries.

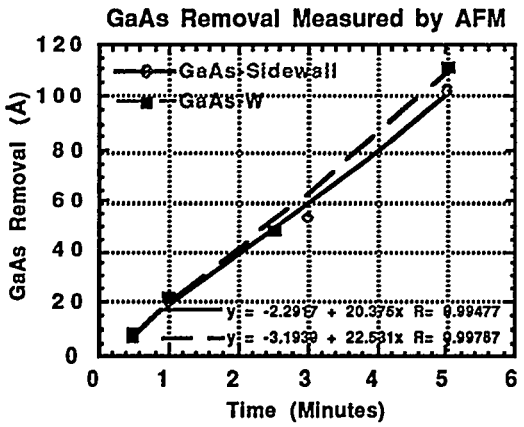

Figure 9. GaAs sputter rate for the over etch period of a W gate etch and a SiO_2 sidewall etch.

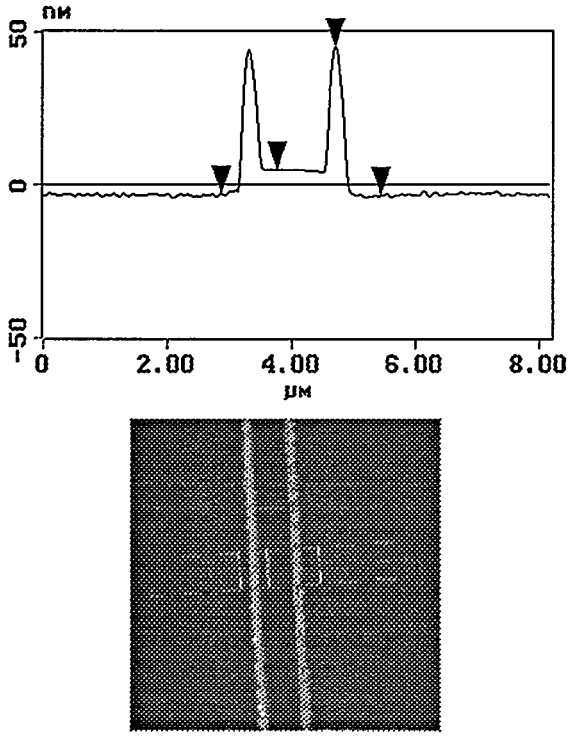

Figure 10. Cross section analysis and top view AFM image of a photoresist gate pattern on GaAs after resist removal. Etch chemistry is CHF3/O2 used in SiO2 sidewall etch and etch time is 5 minutes.

An AFM image for a photoresist-masked GaAs sample described above and exposed to the W gate etch chemistry for 5 min is shown in Fig. 10 after photoresist removal. This image illustrates two features not observable by other techniques. First, the image has been analyzed for surface roughness both within the 1 µm line originally protected by the photoresist and outside of this area. The 0.5 nm rms roughness of the GaAs in the protected area is characteristic of virgin GaAs, while the 2.4 nm rms roughness in the etched area is due to the RIE exposure. It should be noted that quantitative step-height measurements are affected by differences in actual roughness of the sample as well as sampling area of the tip, making spatial analysis of the roughness very useful. Averaging the roughness yields an 8 nm step for this sample. Second, the cross-sectional trace from data averaged in the rectangular area of the AFM image shows approximately 45 nm "wings" at the edges of the photoresist defined region that are not removed by the acetone/isopropyl alcohol treatment. We interpret these features to be a polymer build-up that is sometimes observed during F-based etching in the presence of photoresist. The ability to quantify this effect is a valuable byproduct of the AFM study of material removal.

CONCLUSION

Several GaAs IC fabrication steps have been analyzed by AFM in ways not available using other techniques. Unique capabilities of the AFM provide a non-destructive method of in-line process monitoring of an interconnect via process. Process characterization of a self-aligned-gate sidewall process has revealed previously unobserved trenches created during the sidewall etch. These and other examples of small unintentional material removal establish the AFM as a useful new tool for integrated circuit processing.

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