

**Ion Beam Induced Charge Collection (IBICC) Studies  
Of Integrated Circuits Using a 10 MeV Carbon Microbeam**

F.D. McDaniel, B.N. Guo, S.N. Renfrow, M. El Bouanani, J.L. Duggan  
Ion Beam Modification and Analysis Laboratory, Department of Physics,

University of North Texas, Denton, TX 76203, USA

B.L. Doyle, D.S. Walsh

Sandia National Laboratories, MS 1056, PO Box 5800, Albuquerque, NM 87185, USA

T. J. Aton

Silicon Technology Development, Texas Instruments Incorporated,  
PO Box 650311, MS 3704, Dallas, TX 75265, USA

**Abstract**

As feature sizes of Integrated Circuits (ICs) continue to shrink, the sensitivity of these devices, particularly SRAMs and DRAMs, to natural radiation is increasing. The radiation can lead to the uncontrolled deposition of charge within an IC, which can alter, for example, the memory state of a bit, and thereby produce what is called a "soft" error, or Single Event Upset (SEU). The response of ICs to natural background radiation is therefore of great concern regarding the reliability of future devices.

In this paper, we present results where Ion Beam Induced Charge Collection (IBICC) technique was used to simulate neutron-induced Si recoil effects in IC test structures. The present work, conducted at the Sandia National Laboratories, uses a 10 MeV Carbon microbeam with 1  $\mu\text{m}$  spot to scan test structures on specifically designed ICs. The test structure contains junctions typical of SRAMs and DRAMs. Charge is collected from different areas of the IC under various conditions of junction back bias. The data are digitized and displayed as 3D images combined with (X,Y) coordination. With the aid of IC layout information, the 3D images are separated into different layers to allow the identification of charge collection efficiency in the test structures. An analysis of the charge collection efficiency from different test areas is given.

**1. Introduction**

For a decade, feature sizes of Integrated Circuits (ICs) continue to shrink. ICs work with lower voltages and fewer electrons in a charge packet indicating a zero or one. The sensitivity of ICs, particularly SRAMs and DRAMs, to natural radiation is increasing. There are two ionization radiation sources had been identified: 1) The ionizing decay products (such as several MeV alpha particles) of radioactive atoms, which exist in trace amounts in the memory packaging materials [1]. 2) The cascade products of extraterrestrial cosmic ray particles, which undergo nuclear reactions or scattering events with the atoms in ICs [2, 3].

Ionization radiation can deposit energy along the penetrating track, and generate the excess electron-hole pairs. Device junctions may collect induced charge before electron-hole recombination occurs. High electric field gradients present nearby the junction can enhance the charge separation and collection. Induced charge along the

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penetrating track can distort local electrical fields so that the charge can sometimes be pulled backed up the track toward the silicon surface rather than diffusing into the silicon bulk (funneling) [4]. If the induced charged collection by the IC exceeds a critical threshold charge, the state of the IC can be altered and thereby produce what is called a soft error or Single Event Upset (SEU).

The response of ICs to natural radiation is therefore of great concern regarding the reliability of future devices, and immunity to soft errors is called out as a requirement in the 1997 National Technology Roadmap for Semiconductors prepared by the Semiconductor Industry Association in the US [5]. An extensive design effort has been spending to make electronics immune to such ionization radiation.

To design robust ICs, it is essential to create and test accurate models of the charge collection process. Computer simulation based on theoretical model is an important tool to understand the process. But the model need be experimental validated and tested. Such model based testing requires energetic heavy ions whose number, arrival time, spatial location, energy, and angle can be controlled when they strike the ICs. Ion microbeam from accelerator is ideal for such testing. Ion beam can be focused to a spot size of sub-micron through complicated focus lens system. The microbeam can be used to study charge collection process in the ICs and to locate the weak nodes and structures for improvement through hardening design.

In this paper, we present results where Ion Beam Induced Charge Collection (IBICC) technique was used to simulate neutron-induced Si recoil effects in IC test structure.

## 2. Experimental Details

### 2.1. The ion microbeam and data acquisition system

The present work, conducted at the Sandia National Laboratories, uses a 10 MeV Carbon beam with a beam spot size of 1  $\mu\text{m}$  to scan test structures on specifically designed ICs. The microbeam is scanned across the various test structures by applying scanning signals on the focus lenses. The beam spot size is determined from STIM (Scanning Transmission Ion Microscopy) images of a 1000 mesh TEM grid (bar 9  $\mu\text{m}$ , hole 16  $\mu\text{m}$ ). The TEM grid is adhered on the top of a pin diode (S1223) using conducting silver paint. The area of the beam scan is calibrated using the pitch of the grid in the STIM image or known feature sizes of scanning test structures. Also the STIM image can be used as the standard to calibrate the value of collected charge by the test structures.

Charge is collected by junctions on the test structure under various conditions of junction back bias. The collected charge is converted as charge pulse heights after passing a charge-sensitive preamplifier and an amplifier. The pulse heights are digitized by an Analog-to-Digital Converter (ADC) and recorded along with the scanning beam (X,Y) coordination in list mode by a computer for off-line analysis. The data can be contained within a 3 dimensional data cube (512x512x4096). For the statistical purpose, the data are binned as 3 dimensional (64x64x64) images. In order to minimize damage effects, the test structure were optically targeted using a front view microscope and then scanned by the beam [6].

The induced charge profile, Linear Energy Transfer (LET) versus depth of the normally incident 10 MeV carbon ion strikes was computed using TRIM-96 [7]. The range of 10 MeV carbon in silicon is 8.9  $\mu\text{m}$ , with an LET of 4.9 MeV/mg/cm<sup>2</sup> at the surface, a maximum LET of 5.4 MeV/mg/cm<sup>2</sup> at a depth of 6.8  $\mu\text{m}$ , and dropping

below 4.9 MeV/mg/cm<sup>2</sup> at a depth of 7.4  $\mu\text{m}$ . With 15 V reverse bias, the depletion depth of pin diode is beyond the ion range. The total charge (445 fC) collected by the pin diode is used to calibrate the measurements.

## 2.2. Test structures

On a specifically designed IC, there are various kind test structures. We present the charge collection measurements on two kind test structures: large diode, and ring-gate-inner diodes. The diodes are formed from the diffusions in a p-substrate. There is a window cover on the packaged IC, which can be removed to expose the IC to optical microscope for examination or microbeam for measurements. Test structures are separately connected through different metal pads for outside packaging wire to allow the operating voltage of test structures to be controlled independently.

Charge induced by an incident ion in a junction diode is generally collected by two processes: by a drift process under the influence of a high electric field in the depletion region of junction and by a diffusion process from the outer region of junction. Because of the different charge collection efficiency for different regions, the 3D image shows the differential charge collection ability. With the aid of the IC layout information, images are created by grouping similar layers of the 3D image, which demonstrate the charge collection efficiency. In general, the charge collected due to the diffusion process is less than that collected due to the drift process. Based on image information and correlation with the geometry of the test structures, we can infer which charge collection process dominated.

The large diode is separated as 4 divisions (division area: 135x120  $\mu\text{m}$ ) by metal lines (width: 15 $\mu\text{m}$ ). It also includes 3 metal pads (area: 100x100  $\mu\text{m}^2$ ) within the n-doped region. Only one pad is used to connect with metal lines for outside packaging wire. The rest two are not connected to anything and used as a reference. The metal lines are separated from the edges of the n-doped region with distances of 5 and 6  $\mu\text{m}$ , respectively (Figure 1).

Ring-gate-inner test structure is specifically designed to measure the charge collection from junctions typical of SRAMs and DRAMs [8]. Figure 2 is the 6T-CMOS design layout of the test structure. The equivalent circuit diagram had been present in Ref. [9]. The charge collection nodes are the diodes formed from the contact diffusions of an n-channel MOSFET transistor in a p-substrate. The gate (G3) of this transistor is a square ring, completely enclosing one of the diffusions. We refer to the enclosed diode as the "inner" node and the ring-shaped diode surrounding the gate as the "ring" diode. The gate widths were chosen to approximate node-to-node spacing of memories and are not typical of the pass gate widths of DRAMs. We measured one of these 6T CMOS test structures. The structure has a 10x10  $\mu\text{m}^2$  inner diode and a 25x25  $\mu\text{m}^2$  ring diode separated by a 2  $\mu\text{m}$  width ring gate.

## 3. Results

### 3.1. IBICC measurements on large diode

Figure 3 shows IBICC measurement on the large diode. The scanned region includes one division of the large diode, portions of two metal pads (one for outside packaging wire, and one for reference, Figure 1-A). A 3 V back

bias voltage was applied through a preamplifier. The p-substrate was grounded. The microbeam was scanned over  $240 \times 240 \mu\text{m}^2$  area. The counting rate of charge collection was about  $2 \times 10^3$  count per second (cps).

Figure 3-A is the 3D image with color scale. B, C, D, and E are images by grouping layers of the 3D image with reference of the scanning area, and also the images have been re-scaled and recolor-coded. Charge collected in B is from the area outside of the n-doped area. In C, charge collected is from the metallization lines and the edge of the metal pads. In D and E, charge is collected mainly from the n-doped region. The difference between D and E is that the charge collected from the n-doped areas is more than that collected from the metal pad areas.

When ions strike the inside division of large diode defined by the metal lines, the charge is localized and totally collected (Figure 3-E). Because of energy loss when the ions penetrated the metal lines and metal contact pads, charge generated under the metal lines and pads are less than that from the inside the division (Figure 3-C, D, and E). Collected charge from the metal lines is higher than that from the metal pads. It is also noticeable that charge collection from the metal pads is different between the edges of the pads and inside portion of the pads. The reason for this is that formation of the pads. There is a passivation layer on the top of the test structure except that metal pad has a  $100 \times 100 \mu\text{m}^2$  window cut for the wiring. The energy loss when the ions pass through the passivation layer have to be take account for the computer simulation.

When the ions strike the outside divisions of the large diode, the charge collection are not as efficient as inside of the division (Figure 3-D, and E). At the edges of the n-doped edges, generated charge is diffused and less collected than that inside of the n-doped region. Charge diffusion process around the metal line can be observed with reference of width of the metal lines. By setting a series of the low threshold values of the images, we have observed the collected charge decreases with the distance from the edge of the n-doped region. (Figure 3-A, B, and C).

With various conditions of back bias, the charge collection images have similar behavior described above. Figure 4 shows trends of charge collection from the same scanning area as shown in Figure 3 under different back biases. The error bars are extracted around most frequently charge amplitude, there are not the lower and upper limits of groped layers. Due to the higher back bias corresponding to stronger/thicker depletion layer, more charge can be collected by the diode with better charge collection efficiency. Charge is collected under the metal lines and metal pads following the same ascending trends versus back bias as the large diode. The similar difference between two trends of induced charge indicates that the energy loss through the metal line and metal lines is the main reason. Also with higher back bias, charge collection deviates from the trend indicated by the lower back bias.

### 3.2. IBICC measurement on ring-gate-inner diodes

The beam scanning area for the ring-gate-inner structure is about  $60 \times 60 \mu\text{m}^2$  (Figure 2).

Figure 5 and Figure 6 are IBICC measurements on ring-gate-inner diodes with Gate 3 off (0V) and gate on (4V), respectively. The  $V_{in}$  and  $V_{dd}$  were tied together to feed into the preamplifier. The Gate 1 and Gate 2 were set on with 4V bias. Also the source followers were biased at  $-1.4$  V. Reference figures are shown in [9].

Figure 5-A and 6-A are the images based on the median values of collected charge. The center of Figure 5-A is a flat mesa. B, C, and D in Figure 5 and 6 are images by grouping the layers based on the design layout with label

of layers number and corresponding collected charge range. The maximum collected charge is in consistency with values given in Ref. [9]. In Figure 5-B and 6-B, charge is collected from the outside of ring diode. The charge can only be collected by the outer ring diode no matter what state the Gate 3 is. And the collected charge is decreased as the ions strikes spot further away from the diodes. In Figure 5-C, charge is collected from inner diode and ring diode. It forms a target shape. With the Gate 3 off, the collected charge is localized to the diode where ions directly strike. In Figure 5-D, it forms a hollow square region. The hollow area is corresponding to a little smaller area than that enclosed by Gate 3. Collected charge is from charge sharing between the inner and outer diodes. Because there are have two channels for charge collection, it is expected that there is more charge collected. From Figure 6-C, and D, charge is collected more efficiency due to the gate on. With the same reason as Figure 5-D, charge is collected through inner and outer junctions. From Figure 5-A and 6-A, the median value pictures directly confirm the above explanation.

#### 4. Conclusion

This work uses a 10 MeV Carbon microbeam with a beam spot size of  $1\ \mu\text{m}$  to scan different test areas, including large diode, and ring-gate-inner FET structures. These test structures are incorporated in a specifically designed IC to measure the charge collection from ion strikes on junctions. The IBICC measurements are calibrated with pin diode for absolute charge collection. The measurements demonstrate the differential charge collection efficiency with aid of the IC design information.

A previous IBICC study on 6T CMOS test structures used a moderate resolution pin-hole external system at the University of North Texas [9]. These earlier experiments did not rely on resolving the charge collection from individual circuit elements, but instead, required coincidence between charge collected in both the inner and outer diodes.

The measured maximum collected charge from 6T CMOS ring-gate-inner structures is about  $90\text{fC}$ , which is consistent with the values in Ref. [9]. Also the current high-resolution microbeam measurements directly confirmed the interpretations made in the earlier work. 1) When ions directly strike the inner and outer diodes, collected charge are localized to these diodes. 2) Charge collection for ions striking the gate region was shared between the inner and outer diodes. 3) When ions strike outside the FET, charge was only measured on the outer ring, and decreased with strike distance from this diode.

In the future works, it is also interesting to observe that the charge collection variation with time as the ion striking the test structures. Also simultaneous charge collection measurements from the different areas will greatly increase the knowledge about the charge sharing among different areas. For example, we can measure the charge collection from the inner-gate-outer diodes at the same time and acquire multiple IBICC spectra. Then above conclusion can be further confirmed. Also radiation damage is an important issue during the measurement. With multiple data acquisition system, it will minimize the possibility of the IC degradation.

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## Captions

Figure 1. Picture of the large diode along with design layout. A and B are same beam scanning area ( $240 \times 240 \mu\text{m}^2$ ). In the design layout, pink color areas are n-doped on the p-substrate, the light green areas are metal lines, and the dark green areas are contact pads.

Figure 2. The design layout the 6T CMOS test structure. (The equivalent circuit diagram and structure cross section had been present in Ref. [9].) The 3 source followers, 3 gates,  $V_{in}$ ,  $V_{dd}$ , and reference capacitor are labeled. The yellow color areas correspond to the gate areas. The box area ( $60 \times 60 \mu\text{m}^2$ ) is the beam scanning area. The area of the out ring diode is  $25 \times 25 \mu\text{m}^2$ , the inner diode is  $10 \times 10 \mu\text{m}^2$ , and the gate width is  $2 \mu\text{m}$ .

Figure 3. IBICC measurements on large diode and metal contact pads. A is the 3D image with color scale. B, C, D, and E are images by grouping layers of the 3D image with reference of the scanning area, and also the images have been re-scaled.

Figure 4. Charge collection from the large diode, metal lines, and metal pads under various back biases.

Figure 5. IBICC measurement on ring-gate-inner diodes of 6T CMOS test structure with Gate 3 off. Each layer is corresponding to collected charge  $6.9 \text{ fC}$ . A is the median values of the collected data. B, C, and D are images by grouping the layers of the 3D image based on the design layout.

Figure 6. IBICC measurement on ring-gate-inner diodes, same as Figure 5 except with Gate 3 on.

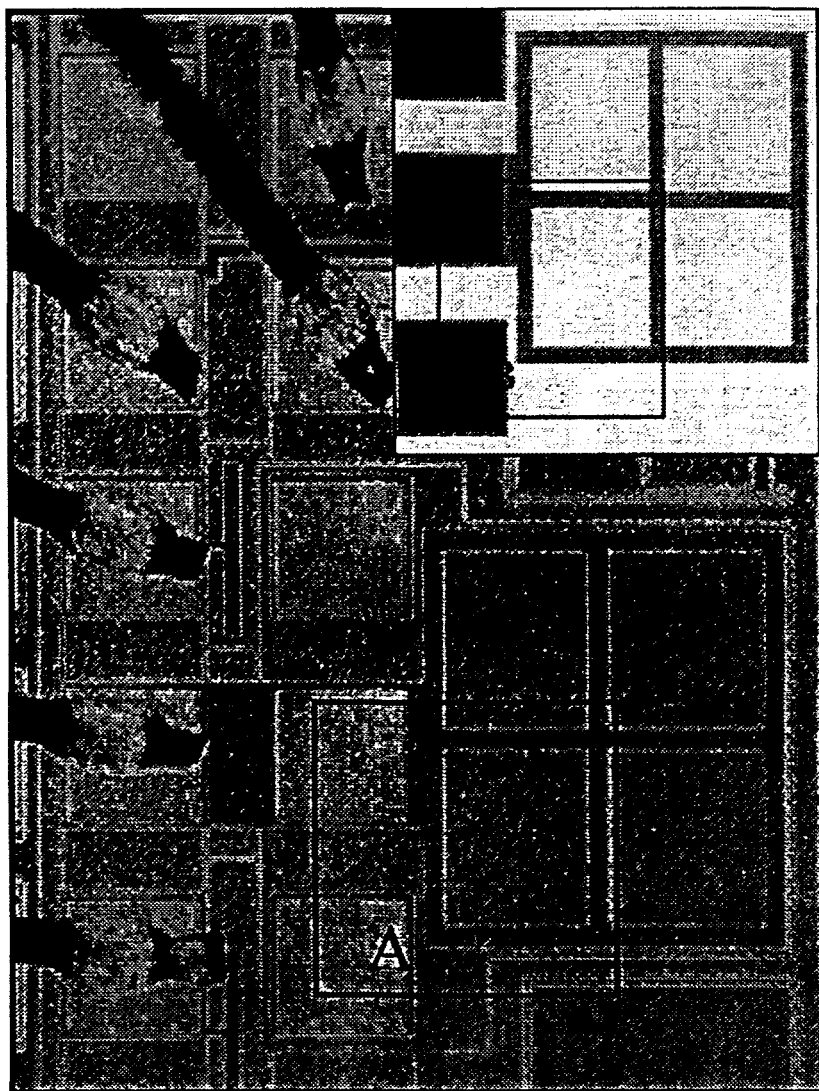


Figure 1-A, B

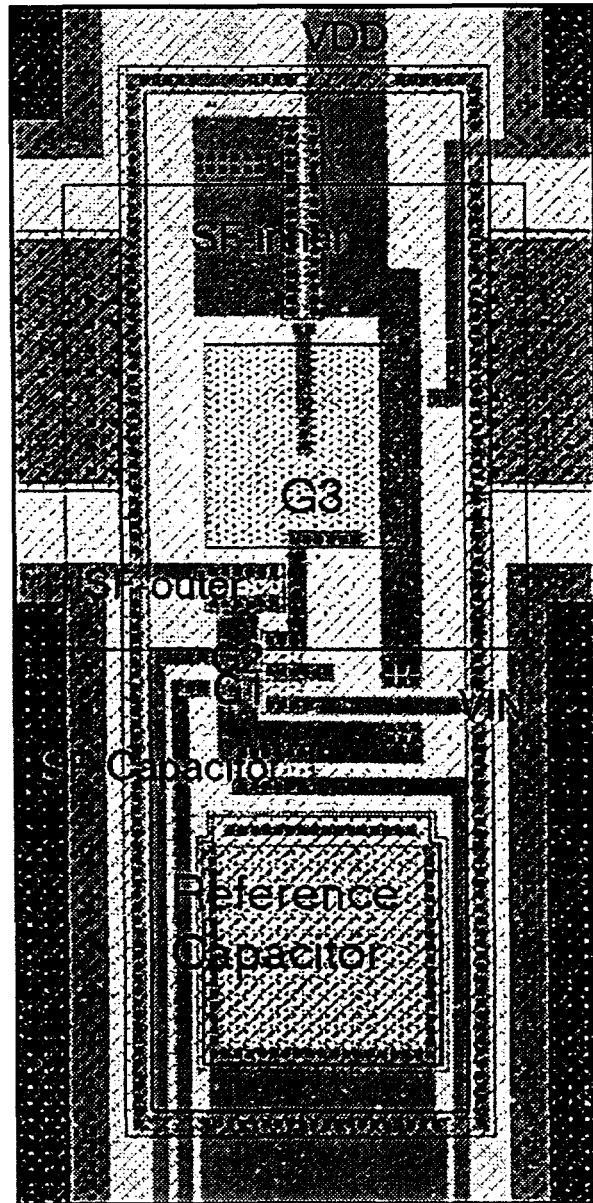
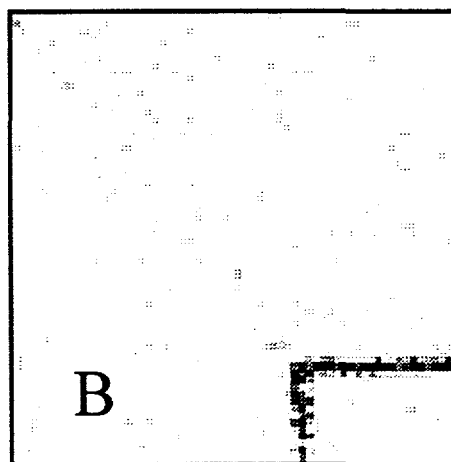
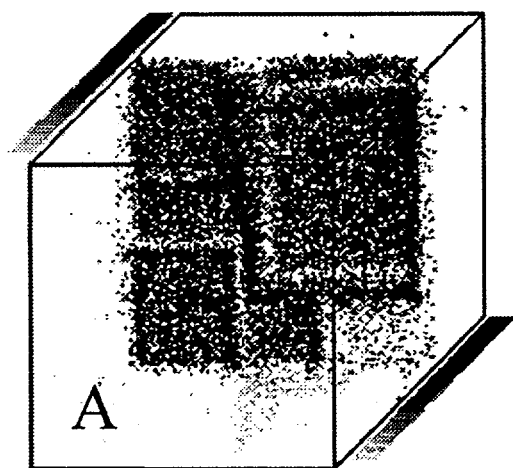
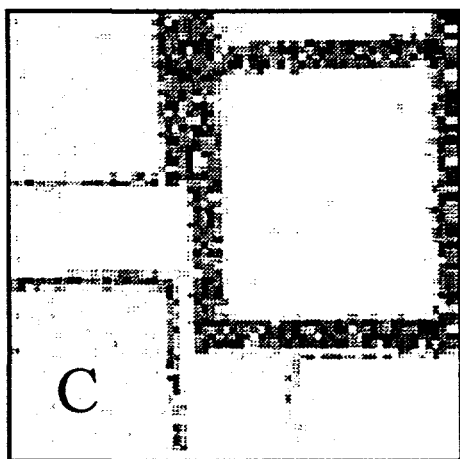


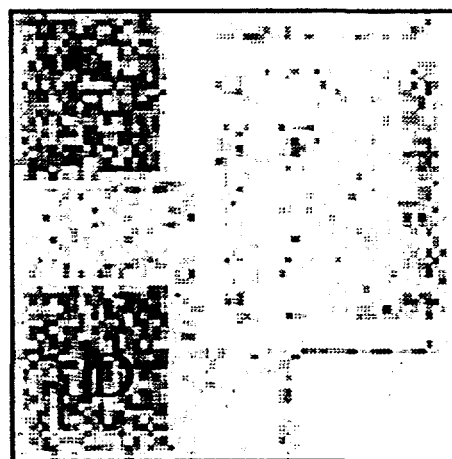
Figure 2



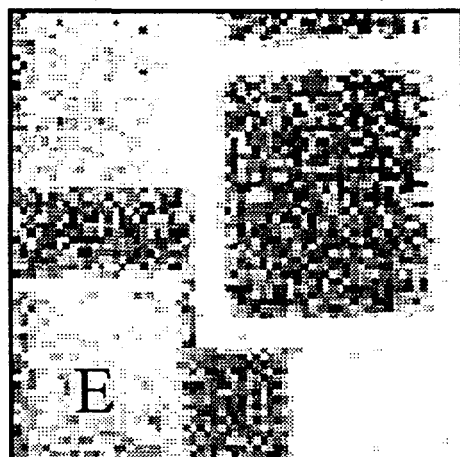
(0-192fC)



(192-274fC)



(274-295fC)



(274-295fC)

Figure 3-A, B, C, D, E

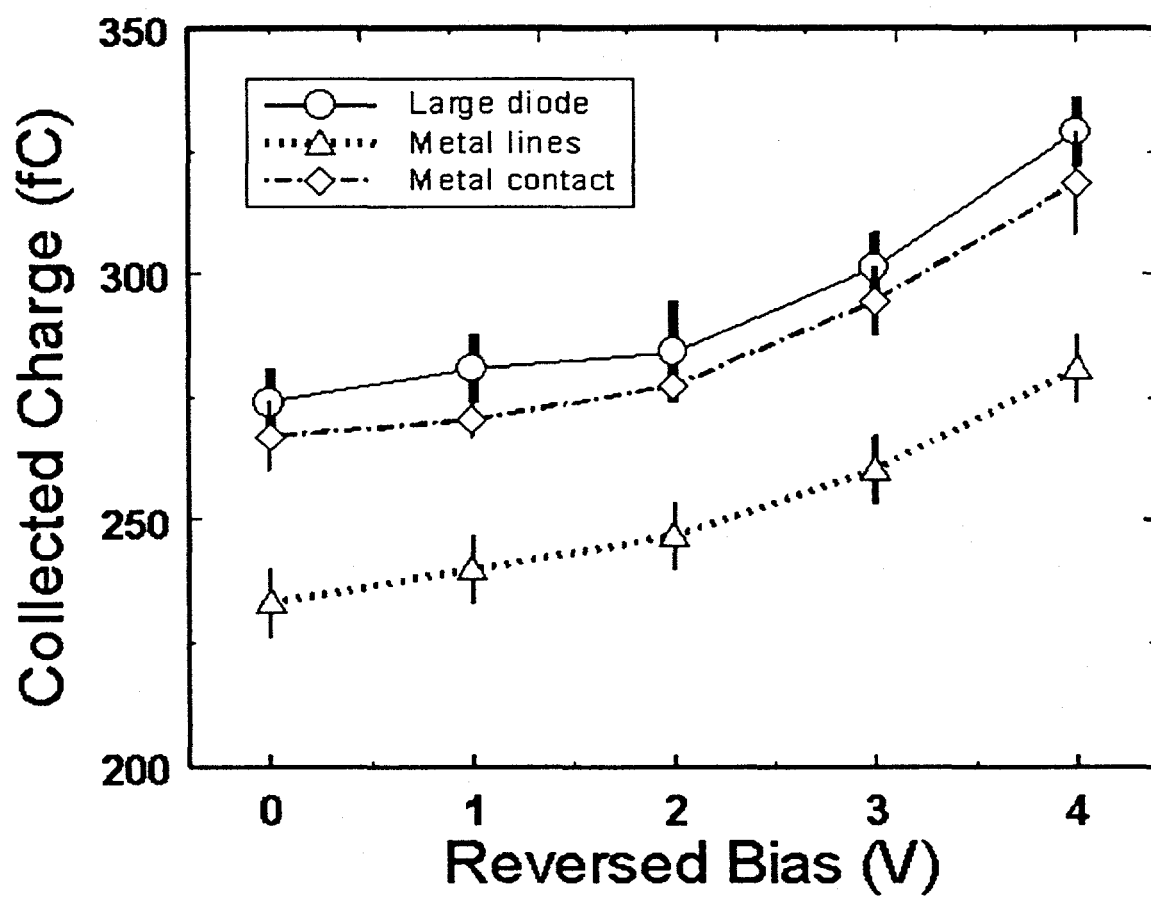
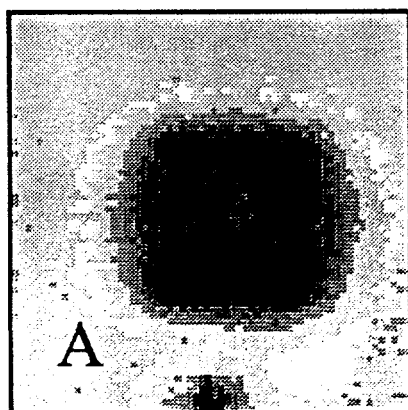
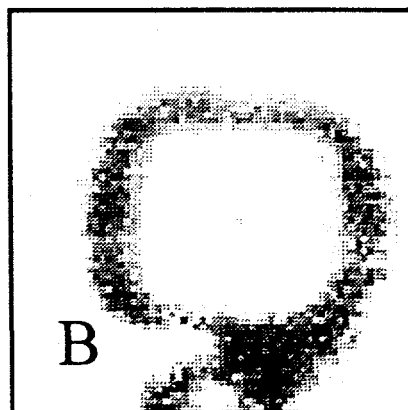


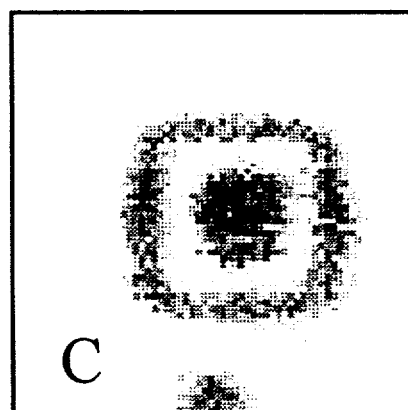
Figure 4



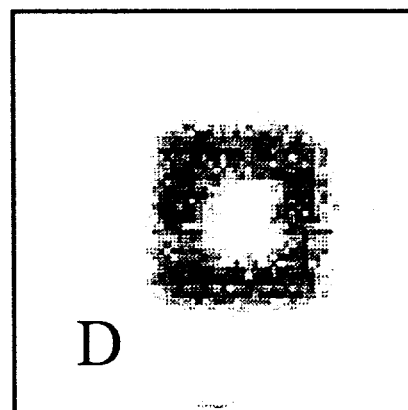
(Median)



(0-27fC)

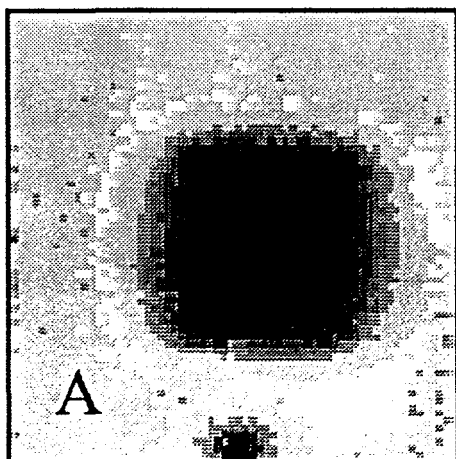


(27-55fC)

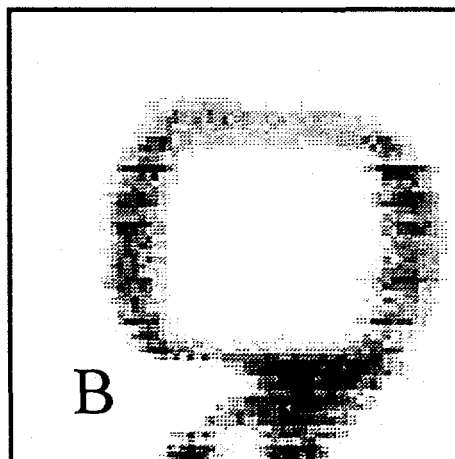


(55-89fC)

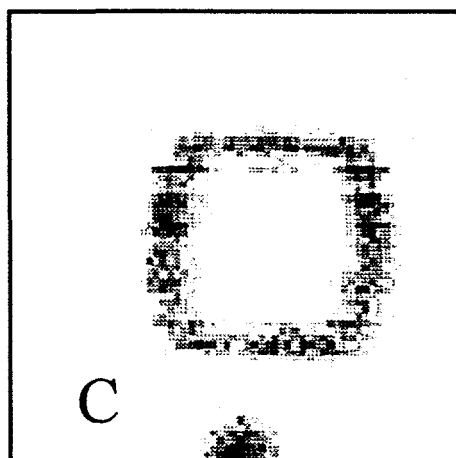
Figure 5-A, B, C, D



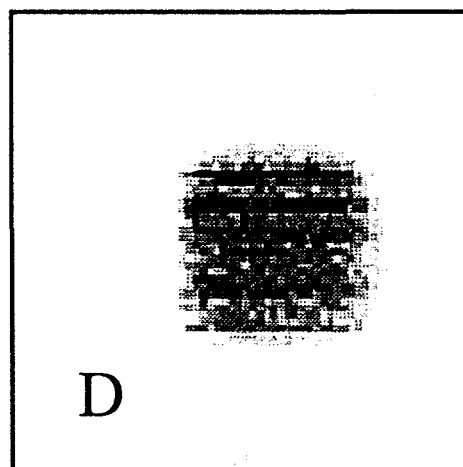
(Median)



(0-27fC)



(27-55fC)



(55-89fC)

Figure 6-A, B, C, D