Single-Event Upset and Snapback in Silicon-on-Insulator Devices and Integrated Circuits

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***Abstract*—The characteristics of ion-induced charge collection and single-event upset are studied in SOI transistors and circuits with various body tie structures. Impact ionization effects, including single-event snapback, are shown to be very important. Focused ion microbeam experiments are used to find single-event snapback drain voltage thresholds in n-channel SOI transistors as a function of device width. Three-dimensional device simulations are used to determine single-event upset and snapback thresholds in SOI SRAMs, and to study design tradeoffs for various body-tie structures. A window of vulnerability to single-event snapback is shown to exist below the single-event upset threshold. The presence of single-event snapback in commercial SOI SRAMs is confirmed through broadbeam ion testing, and implications for hardness assurance testing of SOI integrated circuits are discussed.**

I. Introduction

Single-event upsets (SEUs) are caused by charge collection at sensitive circuit nodes following an incident energetic particle strike (e.g., a heavy ion). One method for hardening against SEU is to reduce the amount of ion-induced charge collection, for instance through the use of silicon-on-insulator (SOI) substrates [1]-[3]. SOI technologies also have advantages for dose-rate environments and have been total-dose hardened to > 1 Mrad(SiO_2) [4]. In SOI devices the charge collection volume is greatly reduced because the device is fabricated in a thin top silicon layer that is dielectrically isolated from the substrate by a buried oxide, as illustrated in Fig. 1. In this figure, we see a diagram of a typical partially-depleted n-channel SOI transistor. The top silicon layer thickness is on the order of 100-300 nm, and the heavily-doped source and drain regions extend to the top silicon/buried oxide interface. The active silicon region underneath the gate is known as the body region. Following an ion strike, charge deposited in the silicon substrate underneath the buried oxide cannot be collected at the drain due to the dielectric isolation afforded by the buried oxide. Because of the reduction in charge collection depth from as much as a few microns in bulk-Si devices to 100-300 nm in SOI devices, SOI integrated circuits (ICs) may have increased SEU thresholds compared to bulk-Si ICs [2], [5]-[8].

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In addition to reduced charge-collection depths, the lateral dimensions of the SEU-sensitive volume are also typically smaller in SOI devices due to reduced p/n junction area. For example, because the source and drain regions extend through the top silicon layer to the buried oxide interface, there is no junction depletion region underneath the source and drain. Instead, only small lateral depletion regions exist between the body and the heavily doped source and drain regions (indicated by the dashed lines in Figure 1). This reduced p/n junction area can lead to significant reductions in the SEU cross-section for SOI ICs compared to their bulk counterparts [5], [8], [9].

Unfortunately, charge deposited in the body region of SOI transistors can trigger a bipolar mechanism that limits the SEU hardness of SOI circuits [1], [2], [10]. Following a heavy ion strike, electrons generated in the body region are quickly collected at the source and drain, but holes are confined to the body region by the buried oxide. In bulk-Si devices, these residual holes can diffuse freely into the substrate beneath the device. In n-channel SOI transistors, however, holes left in the body following an ion strike can raise the body potential (known as a floating body effect, or FBE), forward biasing the lateral parasitic bipolar transistor (n-source/p-body/n-drain) inherent to MOS transistors. This bipolar effect can amplify charge collection in SOI transistors, leading to larger amounts of charge being collected than was initially deposited in the top silicon layer [2], [11]. In extreme cases, FBEs can also trigger a high-current state referred to as single-event snapback (SES, also known as single-transistor latch) if channel conduction is sustained through regenerative impact ionization effects [12]-[14]. To reduce FBEs, SOI transistors are often designed with body ties to hold the body region at a fixed potential (usually the source potential) [3], [6].

Proper body tie design to prevent FBEs is a key element for achieving SEU-hard circuits in SOI. In this paper, we use focused ion microbeam experiments, 3D numerical simulations, and broadbeam accelerator testing to study charge collection, snapback, and SEU in SOI transistors and simple memory circuits with various body tie structures. Impact ionization effects such as single-event snapback are shown to be extremely important for deep submicron devices. SES drain voltage thresholds are measured as a function of device width for 0.6-μm n-channel SOI transistors, and

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compared to electrically-induced snapback thresholds. 3D device simulations are used to determine SES and SEU linear energy transfer (LET) thresholds in SOI SRAMs, and to study design tradeoffs for various body-tie structures. A window of vulnerability to single-event snapback is shown to exist for some SOI SRAMs below the threshold for single-event upset. The presence of SES in a commercial SOI SRAM is confirmed through broadbeam ion testing. The results have implications for hardness assurance testing of SOI integrated circuits.

II. Experimental and Simulation Details

A. Devices

Body-tied n-channel transistors were fabricated in Sandia's Microelectronic Development Laboratory using a 5-V partially-depleted (PD) SOI technology known as CMOS6rs. The CMOS6rs technology is similar to Sandia's bulk-silicon CMOS6r technology described previously [15], except that it is fabricated on SOI substrates. The technology has a drawn gate length of 0.6 µm, a gate-oxide thickness of 12.5 nm, and uses a hardened shallow trench isolation (STI). The CMOS6rs transistors studied in this paper were fabricated using 6" IBIS standard-dose SIMOX wafers with a buried oxide thickness of ~370 nm and a top silicon thickness of 170 nm.

4-Kbit commercial SOI SRAMs from AlliedSignal were also evaluated in this study. These SRAMs operate at 5 V and were fabricated in a partially-depleted 1.2-µm SOI process on SIMOX wafers.

B. Experimental Measurements

Electrical characterization of impact ionization effects and snapback in the Sandia n-channel SOI transistors was performed using a computer-controlled Hewlett-Packard 4062 parametric analyzer. These transistors were also studied in a heavy ion environment using the focused ion microbeam facility on the EN tandem Van de Graaff at Sandia [16]. Transistors were biased in the OFF condition (variable V_{DS}, all other pins grounded), and current was simply monitored using a programmable multimeter. To verify that devices had not been significantly damaged by heavy ion fluence, additional transistor electrical characterization was performed between irradiations at the microbeam facility using an HP 4145B semiconductor parameter analyzer. Broadbeam heavy ion characterization of AlliedSignal 4-Kbit SRAMs was performed at the Brookhaven National Laboratory tandem Van de Graaff accelerator using a JD Instruments ATV test system. Power supply current levels were monitored and recorded using a programmable multimeter.

C. Simulation Methodology

Simulations were performed using the three-dimensional device/circuit simulator Davinci [17]. 3D simulations are necessary both to accurately describe the ion strike and to define realistic three-dimensional body tie structures. We have performed charge-collection simulations of single transistor structures, and SEU threshold calculations for CMOS SRAMs using Davinci's mixed-level device/circuit capabilities [18]. Physical models used in the simulations included carrier concentration-dependent minority carrier lifetimes, Auger recombination, and mobility models which included doping, electric field, and carrier-carrier scattering dependence. To determine its impact on the results, simulations were performed both with and without Davinci's impact ionization model active.

Simulations were performed for both the CMOS6rs n-channel SOI transistors, and for transistors and SRAMs based on Sandia's CMOS7 process technology. The CMOS7 partially-depleted SOI technology is similar to CMOS6rs, but has a drawn gate length of 0.35 µm, a gate oxide thickness of 8 nm, and is designed for 3.3-V operation. CMOS6rs device simulations were based on doping profiles and structural information (oxide thicknesses and topography) obtained from TSUPREM4 process simulations of the actual wafer lots that were tested. As detailed later, various device widths were simulated. Because the CMOS7 technology is still under development, not all parameters have been finalized. For the simulations in this work, the gate width was 0.75 µm, the simulated top silicon thickness was 180 nm, and the buried oxide thickness was 370 nm. For the modeled n-channel transistors a retrograde well profile was used with a surface concentration of $\sim 1.5 \times 10^{17}$ cm^{-3} and a back-channel concentration at the silicon/buried oxide interface of $\sim 1 \times 10^{18}$ cm^{-3}. For circuit simulation parameters, the p-channel transistors were assumed to be the same size as the n-channels. A worst-case strike location at the center of the "off" n-channel gate was used for all simulations [19].

D. Body Tie Structures

N-channel transistors were fabricated and simulated with two basic types of body ties: a conventional Body-Tied-to-Source (BTS) configuration [6], and structures based on combining BTS body ties with the previously proposed Body-Under-Source FET (BUSFET, [20]). The BTS body ties are illustrated in Fig. 2. For conventional BTS body ties, the body is tied at both ends of the channel by p-type regions. These regions are typically shorted directly to the source by silicidation, as shown in Fig. 2a [6]. For structures combining the BUSFET with the BTS body tie, the layout is identical to Fig. 2a, except that in the BUSFET the source junction is shallow; in the conventional BTS structure the source doping extends to the silicon/buried oxide interface. The shallow source gives the BUSFET a body tie underneath the source along the entire width of the channel. This body tie is never more than the source length (which can be made quite small) away from the channel [20].

For each style of body tie (BTS and BTS+BUSFET), a less ideal version was also simulated, as shown in Fig. 2b. In circuit applications, several transistors must sometimes be connected in series (for example, in a multiple-input NAND gate). In such cases, several transistors may be connected to a

single body tie, with the furthest transistor lying at some distance from the body tie contact†. This is reflected in the non-ideal structure of Fig. 2b, where the body contact and the body region are separated by a silicon body tie region of width 0.25 μm whose length Δ was varied in the simulations. For CMOS7 simulations in this work, the body tie region was assumed to have a doping level equal to the channel region. The CMOS6rs transistors fabricated and studied in this work had an independent body tie contact at both ends of the channel, with a distance between the p+ body tie and the channel of about 0.5 μm.

III. Charge Collection and Snapback in SOI Transistors

A. Electrical Characterization and Model Validation

It is well-known that impact ionization and floating-body effects in SOI transistors can lead to threshold voltage hysteresis, kinks and discontinuities in drain current characteristics, and in extreme cases to electrically-induced snapback [3], [13], [21]-[23]. These effects can make circuit design in SOI very challenging, although in some cases designers have learned to use them to their advantage [24].

Figure 3 shows typical subthreshold drain current-voltage (I-V) characteristics of body-tied CMOS6rs n-channel SOI transistors for three different device widths: 20 μm, 10 μm, and 2.3 μm. The drain current (I_{DS}) was measured as the gate voltage (V_{GS}) was swept from accumulation to depletion (negative to positive voltages for n-channel transistors). The drain bias (V_{DS}) was held at 5.1 V. For the smallest transistor width (2.3 μm), the drain current characteristic looks normal, with no evidence of impact ionization. As the transistor width increases, the body ties (located at the two ends of the channel) become less effective and charge multiplication due to impact ionization in the center of the channel leads to discontinuities in the drain current for the two larger devices. This mechanism limits the maximum single transistor width that can be used in most SOI technologies. Also shown in Fig. 3 are corresponding Davinci simulations of the subthreshold drain current characteristics. We find excellent agreement between the simulations and data, with the accurate prediction of the point of I_{DS} discontinuity being particularly striking (the simulations were not continued past the point of the I_{DS} discontinuity). To achieve this agreement, only a minor adjustment to the Chynoweth law impact ionization model parameters was needed. The critical electric field parameter [17] for impact ionization by electrons was raised slightly from ~1.3 MV/cm to a value of 1.7 MV/cm. Previous researchers have on occasion used much larger increases in this parameter (up to ~2.8 MV/cm) to match SOI transistor characteristics [25], [26].

† Devices such as pass transistors may also require independent body contacts that lie at some distance from the body region [6].

At sufficient drain voltages and for poor enough body ties, the impact ionization effects evidenced in Fig. 3 become self-sustaining and lead to a high current state in which the gate voltage no longer controls the drain current in the transistor. At this point the transistor has entered snapback. Figure 4 shows subthreshold drain I-V characteristics for transistors of varying widths with either BTS (Fig. 4a) or BTS+BUSFET (Fig. 4b) body ties. For these curves the gate voltage was swept from depletion to accumulation as the drain bias was held at 5.1 V. The direction of the gate sweep is important because once the transistor has been induced into the snapback state (for example, by turning the channel on with a positive gate bias), the transistor will respond differently as the measurement continues. As an example, when the 20 μm devices are swept from accumulation to depletion (previous figure, Fig. 3), we see a discontinuity in the drain current, but no significant current flow at negative gate biases. However, when the same devices are swept back in the opposite direction (Fig. 4a), we find that even 8 μm-wide devices have entered snapback and the current remains high for all applied gate voltages. This hysteresis in I-V characteristics is a typical result of impact ionization effects in n-channel SOI transistors [3]. By examining the data in Fig. 4a we see that the maximum transistor width before observing snapback in the devices with BTS body ties is about 6 μm (for V_{DS} = 5.1 V). In contrast, we see no snapback in the BTS+BUSFET devices for widths up to 20 μm (the largest width tested). As expected, BUSFETs have no fundamental width limitation from the standpoint of body tie effectiveness [20].

Before continuing, it should be noted that two conditions are necessary for snapback to occur (electrically or following an ion impact). First, the drain voltage must be high enough to produce significant impact ionization near the drain junction. Second, a source of carriers in the body is required to initiate the impact ionization process. For electrically-induced snapback, these carriers are provided by increasing the gate voltage to produce inversion-channel electrons, and for ion-induced snapback they are provided by the electron-hole pair production of the ion strike. The ion LET in SES is therefore somewhat akin to the gate voltage in electrical snapback.

B. Charge-Collection Simulations

To understand the importance of impact ionization effects and body tie design on the SEU response of SOI integrated circuits, we started by studying charge collection in single n-channel CMOS7 (0.75 μm × 0.35 μm) transistors. Figure 5 shows the simulated total charge collection in conventional BTS n-channel transistors for a drain bias of 3 V with and without including the effects of impact ionization (II). The simulated ion strike deposits about 11 fC of charge in the active silicon layer (equivalent to an LET of about 6 MeV-cm^2/mg). In these simulations, the device width was held constant, and the distance between the channel and the body contact (parameter Δ in Fig. 2b) was varied. With impact ionization "turned off" in Davinci (blue circles), we see gradually increasing charge collection as the distance from

the p+ body contact to the body region is increased (the idealized case of Fig. 2a is plotted as a distance to body contact of 0, and for the non-ideal case the distance to body contact corresponds to the parameter Δ in Fig. 2b). This increase in charge collection is due entirely to the bipolar mechanism [10], which increases in importance as body tie effectiveness falls off with distance [11], [19]. Note that even for the ideal case, the bipolar effect causes charge multiplication and more than twice the charge that was initially deposited in the top silicon is collected. As the distance to the body contact increases we approach the case for non-body-tied (i.e., floating body) transistors. This is a useful result because we can't in general simulate SOI transistors without body ties directly due to convergence problems with numerical simulators for floating body devices [26].

For simulations including impact ionization (red squares in Fig. 5), the results are dramatically different. At body contact distances of 1.75 μm and above the transistor enters snapback for the ion strike simulated here. This snapback mode occurs within 1 ns after the strike, when the drain current rises to about 0.2 mA and is sustained through impact ionization at the drain junction. The transistor becomes latched in this high-current condition, resulting in continually increasing charge collection at the drain. In Fig. 5, the charge collection in cases where snapback occurs has been arbitrarily plotted as 320 fC, with arrows indicating that the collection is actually much higher. It is important to note that in these simulations, the drain bias is artificially maintained at 3 V, which helps sustain impact ionization due to the large drain electric field. Whether this snapback mode would actually be observed in circuit operation will be discussed in the Section IV.

Simulations of drain charge collection were also performed for n-channel BUSFETs with BTS body ties. The characteristics are similar to those of the BTS alone, but due to the considerably more effective BUSFET body tie, snapback is not observed until the body contact is 7.75 μm from the body. This represents a more than fourfold increase in the maximum body contact spacing before the onset of snapback.

C. *Focused Ion Microbeam Experiments*

To investigate ion-induced snapback at the transistor level, we performed focused ion microbeam experiments on CMOS6rs n-channel SOI transistors of varying widths. The channel length of all the transistors was 0.6 μm, and the channel width ranged from 0.75 μm to 20 μm. The parts were mounted in a test fixture inside the microbeam vacuum chamber that allowed independent control of each transistor's gate and drain voltage, and the source, body, and substrate pins were grounded. During ion exposures the transistor gate was grounded and the ion beam was scanned across the active device over an area of approximately 30 μm × 30 μm. Starting at a drain voltage below snapback, V_{DS} was progressively stepped higher between ion exposures until ion-induced snapback was observed as a large increase in the drain current (typically from a few nA or less to 0.5-1.5 mA). The lowest V_{DS} for which snapback was observed was recorded as the ion-induced snapback threshold drain voltage, V_{DS} *(SES)*. Following snapback, the drain voltage was reduced to terminate the impact ionization process and reduce subsequent damage to the transistor. In general, for each transistor width at least two parts were tested and the average values are reported here, with the standard deviation shown as error bars.

Figure 6 shows the snapback threshold drain voltage V_{DS} *(SES)* as a function of transistor width for incident 35 MeV chlorine ions. These ions have an LET at the silicon surface of about 18 MeV-cm^2/mg, and a range of about 10 μm. As can be seen in Fig. 6, as the device width decreases, the drain voltage necessary to induce snapback rises rapidly. For devices narrower than 2 μm, very high drain voltages are required to induce snapback. On the other hand, for the 20-μm wide transistors, snapback occurs at $V_{DS} = 5.3$ V, well within the nominal $V_{DD} \pm 10\%$. Also shown in Fig. 6 are the results of 3D simulations to predict V_{DS} *(SES)* for four of the intermediate-width devices. The simulations agree well with the measured thresholds, but appear to have a smaller dependence on device width than the microbeam data.

Given that we can induce snapback in these devices electrically, it would be very interesting and useful to know if there were a correlation between the electrically-induced and the ion-induced snapback threshold drain voltages. One might also ask if using an ion with a higher LET reduces the drain voltage required to induce snapback. In Fig. 7 we show the original data taken using chlorine ions (blue circles), a new set of data using 40 MeV copper ions with an incident LET of about 29 MeV-cm^2/mg (green squares), and snapback threshold drain voltages from electrical measurements. The electrically-induced thresholds were determined by sweeping the gate from depletion to accumulation and determining the lowest V_{DS} for which the drain current remained high at zero gate voltage. We can see from this figure that the electrically-induced snapback thresholds agree very well with the ion-induced thresholds, and that there is little difference between the data for the two ions. The fact that the ion species doesn't affect the results suggests that the snapback process has a saturation behavior; once the ion strike can supply enough charge to the body region to initiate the snapback process, a higher LET particle doesn't significantly alter the voltage threshold. This is consistent with the electrical data in that once the gate voltage is high enough to initiate snapback, further increases in gate voltage don't lower the snapback drain voltage threshold. The fact that both electrical and ion-induced production of carriers in the body lead to equivalent snapback drain voltage thresholds is very useful, because it suggests that electrical testing at the transistor level could be used to screen for ion-induced snapback. In other words, if a transistor has a potential snapback problem in a heavy ion environment, we would expect that it could be detected electrically as well.

D. Light Emission from SES

Light emission from silicon transistors during latchup and snapback is a well-known effect, and is often used in IC failure analysis to diagnose latchup sensitivities [27], [28]. During ion microbeam testing of the CMOS6rs transistors, we observed light emission from the active region of the transistors when they entered SES. A front-viewing optical microscope attached to a CCD camera is used in the microbeam chamber to target the beam on the device under test. During exposures, the chamber was dark, but when snapback occurred we observed a brightly glowing spot precisely located under the transistor gate. An image of light emission from a 10-μm wide CMOS6rs transistor taken during a snapback event at $V_{DS} = 6.1$ V is shown in Fig. 8. This figure overlays the snapback image taken without external light (circled region) on top of an image of the die taken following the ion exposure. A photon intensifier was used on the CCD camera to increase the light intensity of the snapback image. These light emission characteristics were a very repeatable indicator of the presence of snapback in these devices, occurring during every SES event. As mentioned above, the transistor current levels during snapback (and light emission) were on the order of 500 μA to 1.5 mA, well within the range of normal current drives for these transistors. Interestingly, if we electrically induced snapback in the transistors while in the chamber (by raising the gate voltage), we saw no evidence of light emission, although the same current levels were reached. At the present time we have no explanation for this observed difference between electrically-induced snapback and SES.

IV. Single-Event Upset and Snapback in SOI Integrated Circuits

As mentioned previously, it is important to note that in the single-transistor test structures discussed so far, the drain bias is artificially maintained at the power supply voltage. This helps promote impact ionization due to the large drain electric field, but in actual circuit operation the bias on nodes may change in response to a single-event transient. In this section, we explore the likelihood of observing snapback in SOI integrated circuits.

A. SRAM Simulations

SRAM cells incorporating the same n-channel body-tied 0.75 μm × 0.35 μm transistors discussed previously (Fig. 2) were simulated in Davinci. Gate strikes to the center of the "off" biased n-channel transistor in a six-transistor SRAM cell were simulated, with the other transistors modeled in the circuit domain (the two access transistors were not modeled because they don't usually participate in the upset process). Impact ionization was included in all SRAM simulations.

The calculated SES and SEU thresholds as a function of distance to the body contact for BTS structures are shown in Fig. 9 for SRAMs with no feedback resistors and with 100 kΩ resistors. As expected, the upset threshold drops as the distance between the body and the body contact increases, because the body tie becomes less effective at preventing the body potential from floating. Again, the results at long distances are indicative of the expected behavior of non-body-tied transistors. For body contacts farther than 5.75 μm from the body, simulations predict that single-event snapback will indeed occur in these SRAM circuits.

For SES to occur, the SES threshold must be below the SEU threshold, creating a window of SES vulnerability. Once the SEU threshold is passed, snapback no longer occurs because the drain bias switches from V_{DD} to 0 V following an ion strike and is unable to sustain impact ionization. Our simulations predict that the onset of SES occurs at the same LET for both cells with and without feedback resistors. The window of SES vulnerability therefore increases with increasing feedback resistance because the upset threshold increases. For example, without feedback resistors the SES-susceptible window is predicted to occur for LETs between 2.5 and 6 MeV-cm^2/mg in the SRAM with body contacts 5.75 μm from the body, but with 100 kΩ resistors, the window opens to LETs between 2.5 and 20 MeV-cm^2/mg.

The window of SES vulnerability is illustrated more clearly in Fig. 10 for the SRAM with body contacts 5.75 μm from the body. In this figure, we plot the SES and SEU thresholds for the SRAM with 100 kΩ resistors as a function of V_{DD}. Note that the worst-case power supply for SEU is V_{DD} – 10% (3 V), but for SES it is V_{DD} + 10% (3.6 V). In fact, at 3.6 V the SES window has opened even further because at higher voltages not only does the SES threshold decrease, the SEU threshold increases.

Figure 11 shows the results of similar SEU threshold simulations for SRAMs using the BUSFET structure in combination with BTS body ties. The calculated SEU thresholds are similar to the results for the BTS body-tied structures. For body contact distances up to 10.75 μm (the largest simulated here), we predict that SES will not occur in the BUSFET SRAMs, but at larger body contact distances it is expected that SES would eventually occur.

B. Commercial SOI SRAM Heavy Ion Tests

To determine to what extent SES might be present in commercially-available SOI ICs, we performed broadbeam heavy ion tests on 4 K-bit SRAMs manufactured by AlliedSignal. These ICs were fabricated in a 1.2-μm partially-depleted SOI technology designed for 5-V operation. We do not presently know whether these ICs use body ties. Heavy ion exposures were performed using 285-MeV bromine ions and 340-MeV iodine ions. During exposures the power supply current was recorded and after each exposure the SRAMs were tested for errors, giving both SEU and SES characteristics for the ICs as a function of LET.

At $V_{DD} = 4.5$ V (nominal – 10%, worst case for SEU) no SES was observed for either Br or I exposures, and the SEU threshold was found to be about 60 MeV-cm^2/mg, consistent with the manufacturer's specification. At $V_{DD} = 5.5$ V (worst case for SES) no SES was observed and the measured SEU

threshold increased to 70 MeV-cm^2/mg. When the power supply was raised still further to 6.0 V (outside the manufacturer's specification), we found that SES did indeed occur, at a threshold LET of about 50 MeV-cm^2/mg. For this bias, the SEU threshold was near 75 MeV-cm^2/mg. At the highest LETs that we tested (84 MeV-cm^2/mg), we saw both SES and SEU, indicating that near the edge of the SES window, both events can occur. This is a natural consequence of the fact that the SEU threshold is not exactly the same for all memory cells. Unfortunately, due to ion facility problems we were unable to complete tests at higher LET to determine if SES disappears as SEU becomes dominant, as expected from the simulation results.

Figure 12 shows a typical current log for a 340-MeV iodine exposure with an effective LET of ~75 MeV-cm^2/mg. Three distinct steps in the power supply current are recorded, indicating 3 separate SES events occurred (in 3 different transistors). After exposure, the current remains high until the part is rewritten, at which point the current drops to its original (low) value. Note that the current steps for the first two SES events are both about 2 mA, while the third SES increases the current by only an additional 1 mA; this may be an indication that different sizes of transistors experienced SES during the exposure.

V. Discussion

A. Radiation Hardness Assurance Implications

The experiments and simulations clearly show the dramatic effects of various transistor widths and body tie configurations on the single-event snapback susceptibility of SOI transistors. Not surprisingly, it is very important to consider impact ionization effects in deep submicron SOI transistors, with the simulations predicting the occurrence of SES for cases where the body contacts are too far away from the body region or the device width is too large. This result has implications for commercial SOI circuits that may not use body ties at all, or that use them selectively in the circuit design [24]. Transistor-level ion microbeam experiments confirm the presence of SES, and more importantly, show that electrically-induced snapback occurs at the same threshold drain voltage as SES. Because electrically-induced snapback occurs under similar conditions to SES, it is likely that most commercial SOI circuits not specifically designed for space environments will not exhibit SES because they must be designed to operate reliably during electrical stimulation. We caution the reader, however, that this conclusion is based on transistor-level testing of a single technology. In a complex integrated circuit, direct external control over the state of individual circuit nodes is not possible. It is not too difficult to imagine that there could be logic states where electrical excitation into snapback is precluded by circuit design and timing, but where a well-placed and well-timed ion strike could nevertheless initiate snapback.

The results also have implications for present hardness assurance screens, where current-monitoring latchup tests (which might also be capable of detecting snapback) may not even be performed on SOI devices because they are assumed to be latchup immune. Even if latchup tests are performed, they may not probe the window of SES vulnerability, which exists only below the SEU threshold. For the user of commercial SOI ICs where the manufacturer has made no guarantee of SES-free operation, we recommend performing the following SES screen during the single-event effects test campaign: Perform the usual heavy-ion tests to find the SEU cross-section and threshold at V_{DD} – 10%. *At or just below the SEU threshold*, increase the power supply bias to V_{DD} + 10% and monitor power supply current during ion exposure to detect SES.

In cases where SES occurs, our simulations predict degraded logic levels within the IC. In the simulations shown in Figs. 9 through 11, the drain voltage drops from 3 V to a level when in snapback of 2.4 V. In this case, the memory cell contents would still be read correctly, but power consumption would increase as the SRAM cell draws a static current after a single SES of about 0.2 mA. We saw power supply current increases larger than these (~0.5-1.5 mA) in the experiments, probably due to larger device sizes. In SRAMs, a write of the memory to the opposite state clears the snapback condition [12]. Whether the increase in static power consumption would be a serious problem depends on the individual application, and how many SES events might accumulate before being cleared. However, continued operation in this impact ionization regime is not desirable as it is known to lead to hot-carrier induced degradation of the gate oxide [29], and possible charging of the buried oxide. In addition to the light emission noted previously for the CMOS6rs transistors, we found significant positive top gate threshold voltage shifts following multiple snapback events, a probable indication of hot electron injection into the gate oxide. Allowed to continue unabated in the SES mode, transistors were eventually destroyed in some cases and light emission was noted over large areas surrounding the device. As noted by Koga [12], some local heating of the device is probably inevitable during SES and may lead to burnout if unchecked.

B. Body Tie Design Implications

In this paper, we have separately simulated the effects of varying device width and body contact spacing on the SEU and SES characteristics of SOI SRAMs. In conventional BTS structures that are tied only at the ends of the channel, body tie effectiveness depends on both of these parameters. An inherent tradeoff thus exists between device width and body tie proximity. For the results shown in Fig. 9, the maximum total distance from the body tie contact to the center of the gate (Δ + W/2) before SES is observed is about 6 µm. For wider transistors, Δ must be reduced to prevent SES. This "design window" is presented graphically as the triangular shaded region in the lower left corner of Fig. 13. The design window to prevent SES for the parameters simulated here is small, and places relatively severe restrictions on both the device width and body tie spacing. These restrictions can

make circuit design challenging and may also require increased die area to accommodate more frequent body contacts. Also shown in Fig. 13 is the design window for BUSFETs, based on the simulations of Fig. 11. For the BUSFET, width is not really an issue since the transistor is tied underneath the source at a distance Δ no matter the transistor width (recall also Fig. 4b). No SES was observed for body tie spacings in excess of 10 μm, so the upper boundary is given as a minimum value. This gives the BUSFET a much wider design space, as depicted by the rectangular region in Fig. 13. Depending on design rules, use of the BUSFET may reduce die area, at the cost of additional process complexity [20].

VI. Summary

Body tie layout and transistor width greatly affect the single-event upset and snapback characteristics of SOI transistors and ICs. Impact ionization effects in SOI transistors are important even in the absence of radiation environments, where they can produce discontinuities in drain current and electrically-induced snapback. 3D charge-collection simulations showed the importance of bipolar amplification and predicted that body ties must be kept very close to the transistor channel to prevent SES in single transistors held at a constant bias. Focused ion microbeam experiments confirmed the presence of SES in single-transistor test structures, with the drain voltage required to produce snapback decreasing with increasing transistor width. The applied drain voltage required for snapback to occur was found to be the same whether snapback was initiated electrically or using heavy ions, implying that electrical testing may be an accurate screen for SES. Visible light emission from the gate region was observed for transistors in a state of SES.

SRAM simulations indicate that a sensitive window for SES exists below the SEU threshold. Above the SEU threshold, the SES process is self-terminated by loss of drain bias. Feedback resistors were found to have no effect on the SES threshold, but because they raise the SEU threshold they open the SES-sensitive window. BUSFET body-tie structures were found to be SES immune over the range of devices simulated in the present work. SES was observed in a commercially-available SOI SRAM, but only when the manufacturer's rated maximum power supply voltage was exceeded.

Because electrically-induced snapback occurs under similar conditions to SES, it is possible that commercial SOI circuits not specifically designed for space environments will not exhibit SES because they must be designed to operate reliably during electrical stimulation. Nevertheless, we recommend performing an SES screen before using SOI ICs in a heavy ion environment. The hardness assurance screen consists of simply monitoring power supply current for ion exposures just below the SEU threshold to ensure no SES occurs.

VII. References

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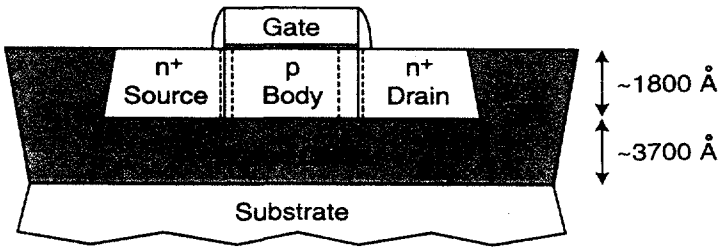

Figure 1. Cross-sectional diagram of a typical partially-depleted n-channel SOI transistor.

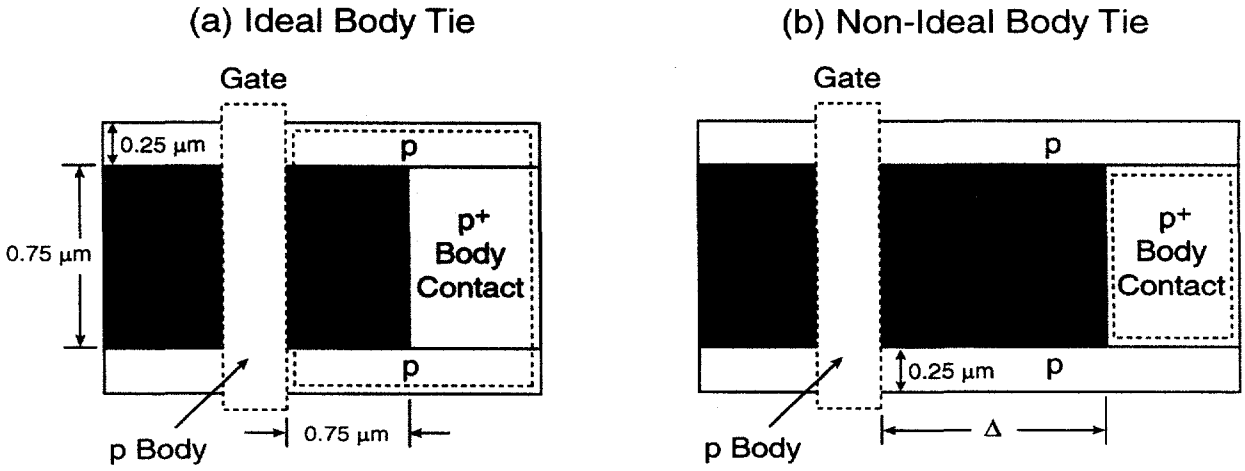

Figure 2. Plan views of simulated body tie structures, with dotted outlines denoting contact regions. (a) Ideal structure with a single silicided region forming both source and body contacts. (b) Non-ideal structure with separate source and body contacts and a distance Δ separating the body contact and the active device channel. For BUSFETs, the layout is the same, but the source doping does not extend all the way to the top silicon/buried oxide interface [19].

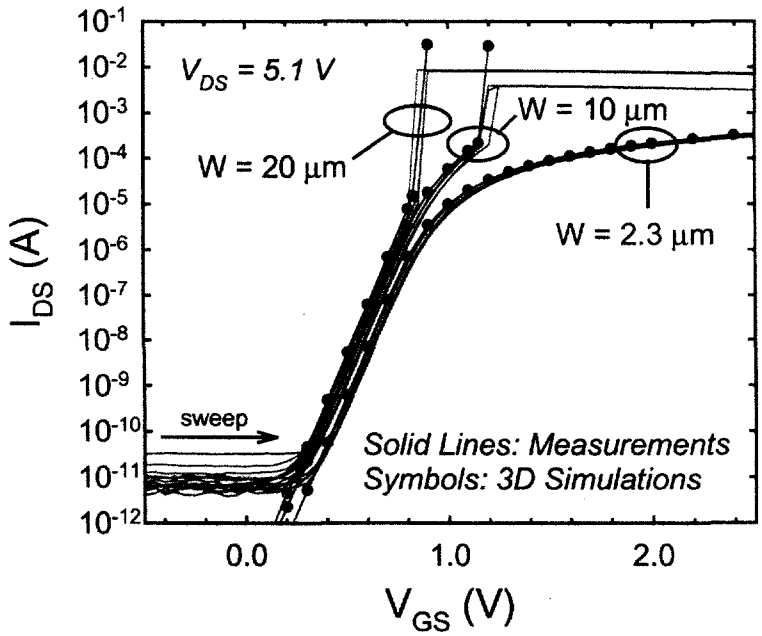

Figure 3. Measured and simulated subthreshold drain current characteristics for CMOS6rs n-channel transistors with BTS body ties. Discontinuities due to impact ionization effects are observed for larger transistors.

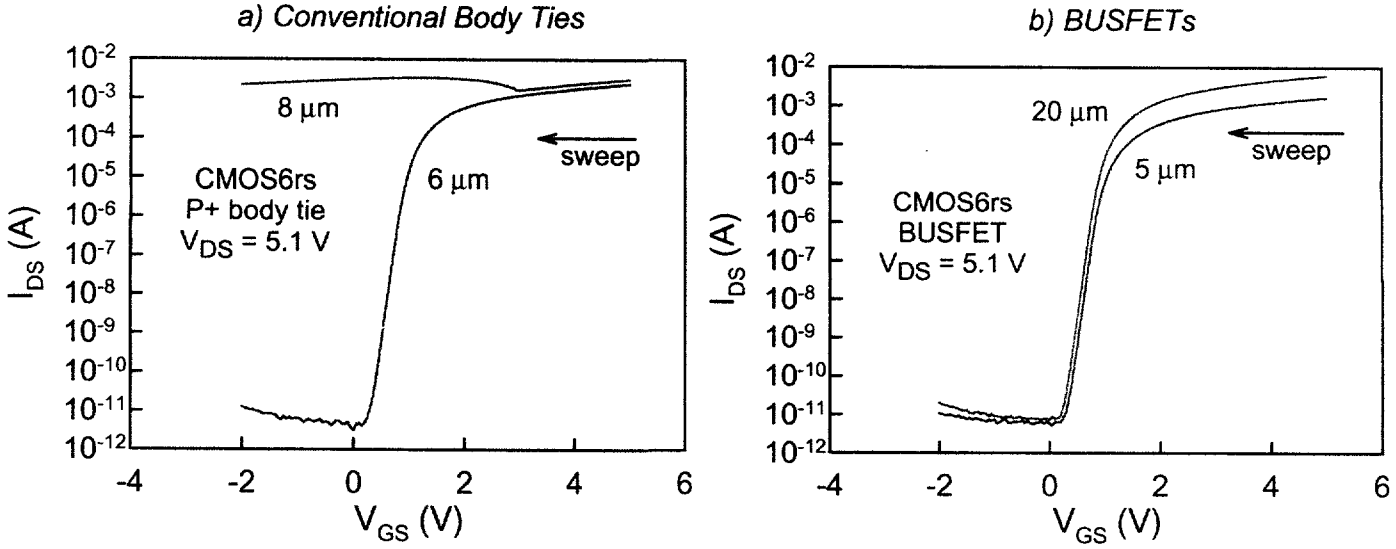

Figure 4. Subthreshold drain current characteristics for n-channel transistors with a) conventional BTS body ties, and b) BUSFETs with BTS body ties. For conventional body ties, the maximum device width before snapback is observed is about 6 µm, but the BUSFET structures have no inherent width limitation.

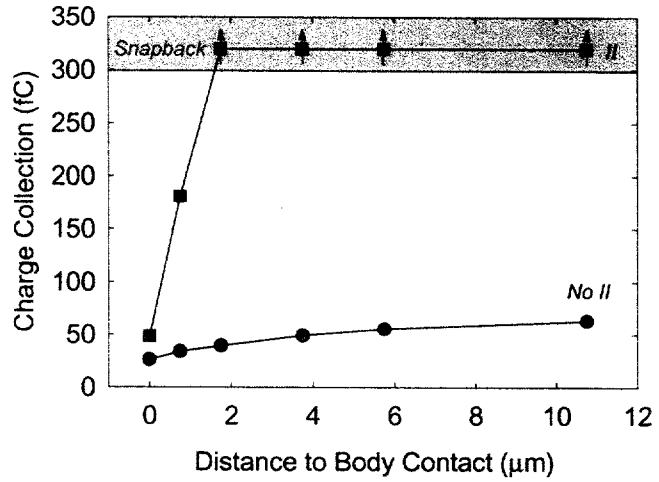

Figure 5. Simulated total drain charge collection in n-channel transistors with BTS body ties. Results are shown for simulations with and without including the effects of impact ionization.

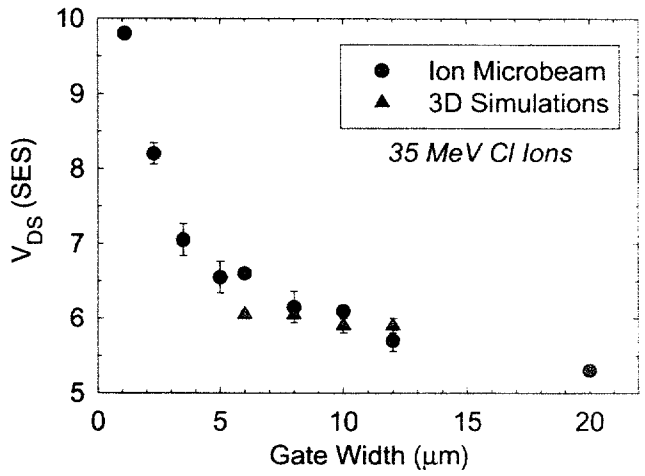

Figure 6. Measured and simulated threshold drain voltage required to produce SES as a function of gate width for CMOS6rs n-channel transistors exposed to 35 MeV chlorine ions (LET ≈ 18 MeV-cm^2/mg).

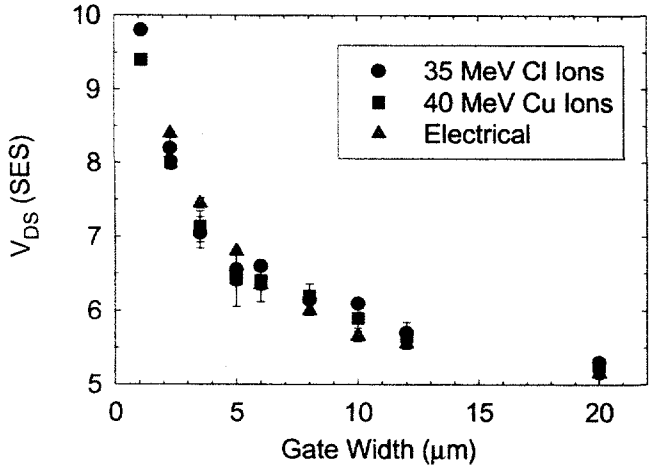

Figure 7. Threshold drain voltages required to produce SES for 35 MeV chlorine ions and 40 MeV copper ions (LET ≈ 29 MeV-cm^2/mg). Also shown are threshold drain voltages for electrically-induced snapback.

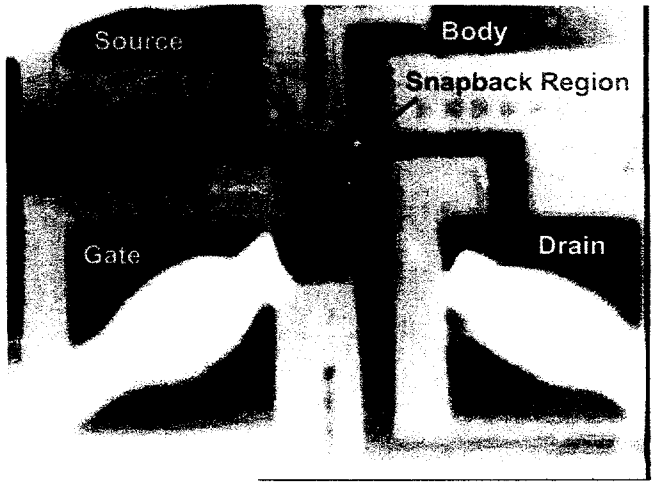

Figure 8. Light emission from chlorine-induced SES in a 10 µm-wide n-channel SOI transistor. The light emission spot has been overlaid on top of a die image taken immediately following the ion irradiation.

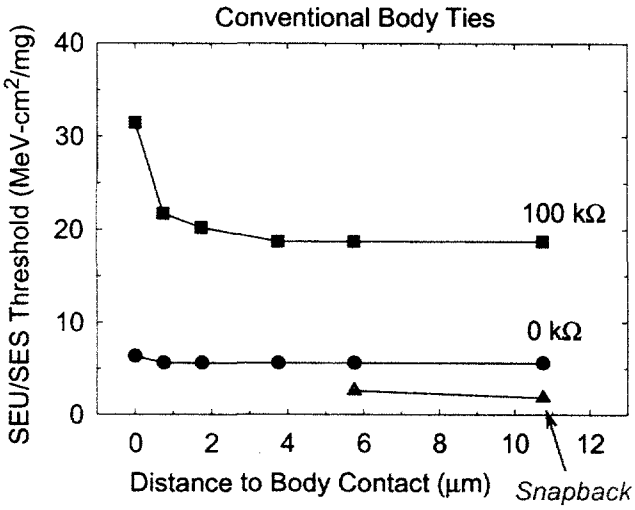

Figure 9. Simulated SEU and SES thresholds for SOI SRAMs using BTS body ties as a function of body contact distance from body. The threshold for SES (red triangles) is the same for SRAMs without feedback resistors or with 100 kΩ resistors.

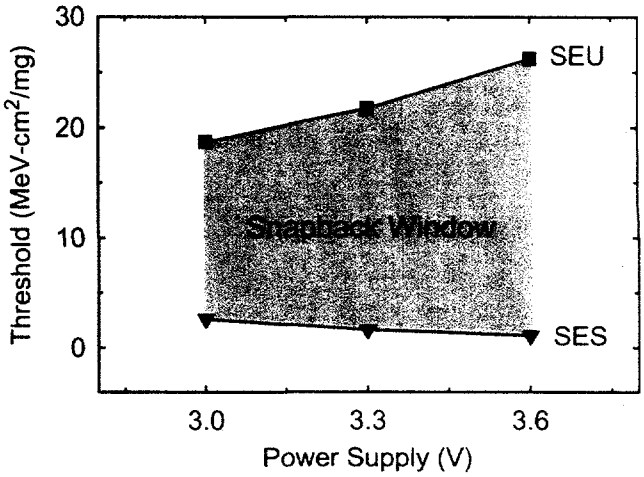

Figure 10. Simulated SES and SEU thresholds for an SRAM with 100 kΩ feedback resistors as a function of V_{DD}. The SRAM has conventional BTS body ties at a distance of 5.75 μm from the transistor channels. Note opening of snapback window as V_{DD} increases.

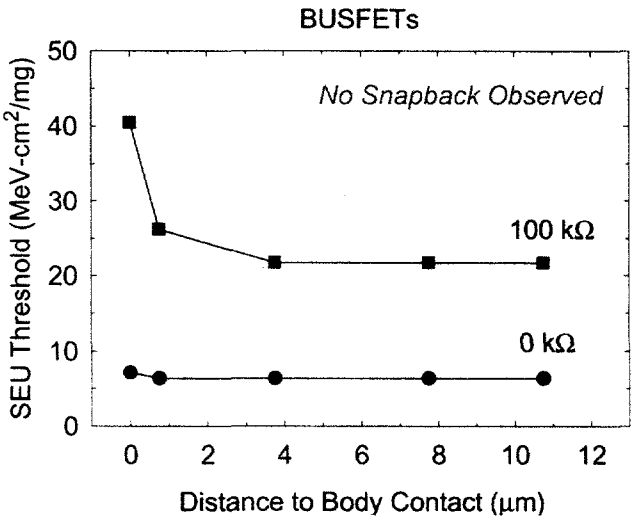

Figure 11. Simulated SEU thresholds for SOI SRAMs using BUSFETs in combination with BTS body ties.

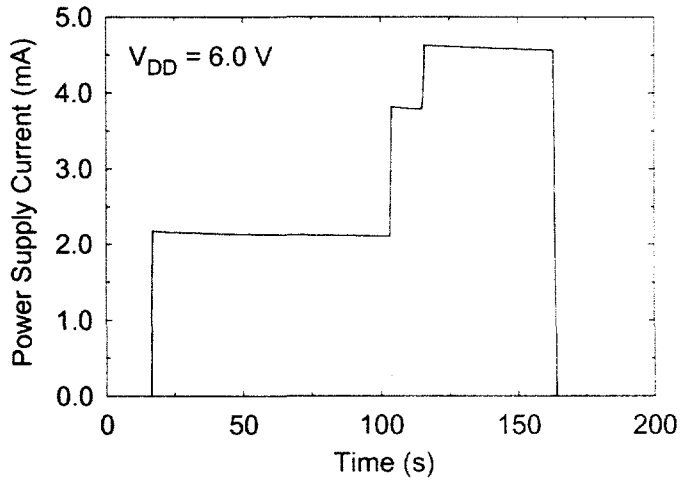

Figure 12. Power supply current in AlliedSignal 4-Kbit SOI SRAM during a broadbeam exposure to 340 MeV iodine ions (LET ≈ 75 MeV-cm²/mg). Three separate snapback events were recorded before the part was cleared by rewriting the contents of the memory.

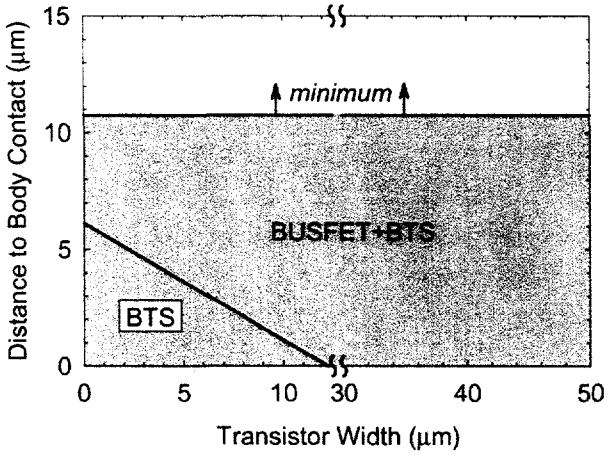

Figure 13. Design tradeoff between transistor width and distance to body contact for BTS and BUSFET structures.