Electrical Breakdown of Thin Oxides During Ramped Current-Temperature Stress

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***Abstract*--Electrical breakdown in thin gate oxides is studied with a new bias-temperature ramp technique. Research grade 6.5 nm oxides with Al gates show erratic current-temperature (*I-T*) response with increasing electric field, consistent with a wide breakdown distribution at room temperature. Industrial grade 7.0 nm thermal and N_2O-nitrided oxides show well-behaved *I-T* plots, consistent with tight breakdown distributions at room temperature. In all cases, temperature-to-breakdown decreases with increasing electric field. Charge-to-breakdown Q_{BD} levels at elevated temperatures exceed values observed in previous work, despite similar Q_{BD} values at room temperature, especially for the 7 nm nitrided oxides. No significant effect of radiation exposure on high-field oxide conduction or breakdown is observed under positive, zero, or negative radiation bias for the thermal and nitrided oxides, up to 20 Mrad(SiO_2). These results demonstrate the utility of the ramped current-temperature stress measurements, and suggest that the long-term reliability of high quality gate oxides may not be significantly degraded by radiation exposure at levels typical of system operation.**

I. INTRODUCTION

As MOS integrated circuit (IC) gate oxides have become thinner than ~ 10 nm, historical concerns about threshold voltage shifts and mobility degradation in a radiation environment are being replaced by the concern that radiation exposure may reduce the long-term reliability of the dielectric layer. For example, recent work at the University of Padova [1-5] has shown that high doses of ionizing radiation can lead to Radiation Induced Leakage Current (RILC) in oxides thinner than ~ 7 nm. RILC is enhanced leakage current through the gate oxide caused by defects in the insulator, and is analogous to the Stress Induced Leakage Current (SILC) [5-10] that is commonly observed in thin oxides exposed to high current electrical stress. Doses at which significant RILC is observed typically exceed 10 Mrad(SiO_2) [1,3]. It is not known whether RILC or other types of oxide degradation lead to decreased device or IC reliability at lower radiation doses more typical of system applications. However, the mutual sensitivities of radiation and long-term reliability effects to defects in the oxide and hydrogen species [2,5,8-12] mean that one cannot safely assume the effects are independent.

We have developed a new test technique to help assess the high-field electrical breakdown of thin oxides. This method is based on monitoring the current at fixed, high voltage during a ramped temperature stress. The technique takes advantage of the high-precision current measurements possible using a thermally stimulated current test system [12-15] in a different mode of operation. In this paper, we briefly describe the measurements, show results for thin Al and Si gate capacitors from research and development (R&D) and industrial-class fabrication facilities, and use the method to study the effects of radiation exposure on the breakdown of thermal and N_2O-nitrided oxides. Comparison is made to previous work on the temperature dependence of oxide breakdown, and to measurements of RILC in a heavy ion environment. The implications of these results are discussed for MOS long-term reliability and radiation response.

II. EXPERIMENTAL RESULTS

A. Temperature Ramp Technique.

Measurements of dielectric breakdown during high-field electrical stress are typically performed at or near room temperature via constant voltage or current stress methods [8,10,16]. We have found that useful information can also be obtained by performing current measurements during a temperature ramp at a constant, high electric field. For example, in Fig. 1 Al-gate capacitors with 6.5 nm thermal oxides from a R&D class fabrication facility [17] are ramped from 20 °C to ~ 300 °C at ~ 0.11 °C/s [14] at 5.5–6.5 V biases. These voltages correspond to 9.4–10.9 MV/cm electric fields, including gate-to-Si work function differences. The curves shown in Fig. 1 are representative of more than 20 devices measured from this wafer. At the two lowest voltages, the current I increases monotonically until the temperature T is high enough and/or enough charge has passed through the oxide that it breaks down. At higher voltages and lower values of T, there can be a competition between breakdown and recovery at high currents and temperatures, leading to erratic *I-T* curves. For the 6.5 V stress in Fig. 1, an early apparent breakdown recovers before the oxide truly breaks down above 150 °C. Although there is increasing current with increasing T, there is not always a monotonic relationship between the applied voltage and the temperature at which

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DISCLAIMER

breakdown occurs for these devices. It is likely that this erratic and irreproducible response is due to differences in as-processed defect densities, although some role for oxide degradation at high temperature due to electrochemical reactions between the Al and the SiO_2 is also possible. In previous work on these devices at room temperature, a wide spread in breakdown voltages was also reported [17]. Hence, the variability observed in the current-temperature ramp response in Fig. 1 is consistent with trends in the room-temperature breakdown distributions.

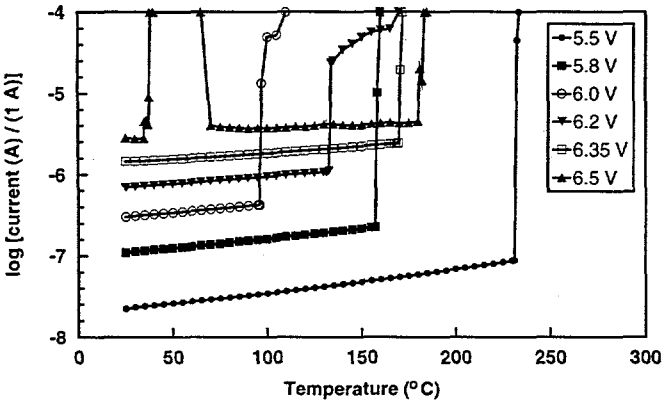

Fig. 1. Log_{10} (current) vs. temperature and applied gate bias for 0.00024 cm^2 *n* substrate capacitors with Al gates and 6.5 nm thermal oxides.

Industrial grade thermal and N_2O-nitrided 7.0 nm oxides [18] with poly-Si gates show strikingly more uniform *I-T* curves in Figs. 2 and 3, respectively. This is consistent with the fairly tight breakdown distributions reported for these devices during room temperature tests [18]. The curves in Figs. 2 and 3 are representative of the response of more than 20 devices measured from each of these two wafers. In all cases, the current increases monotonically with increasing voltage and temperature, and the breakdown temperature T_{BD} decreases monotonically with increasing electric field. Comparing the two device types, there is less current in the N_2O oxides than the thermal oxides at a given temperature.

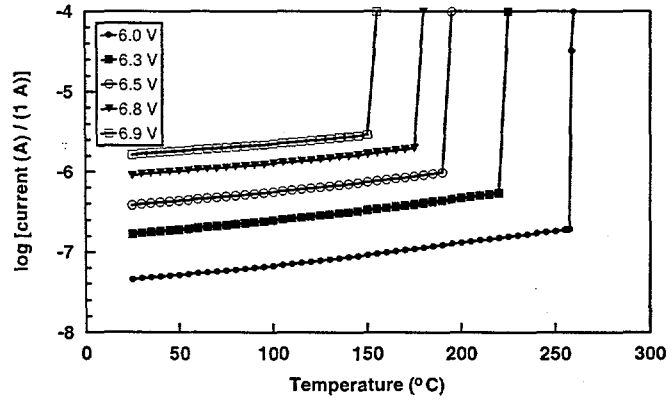

Fig. 2. Log_{10} (current) vs. temperature and applied gate bias for 0.00035 cm^2 *n* substrate capacitors with poly-Si gates and 7.0 nm thermal oxides.

The strong dependence of the current through the insulator on electric field is highlighted in Fig. 4, where data at three temperatures are plotted for the thermal oxides of Fig. 2 as a function of electric field *E*. The data at the lowest electric fields reflect the leakage floor of the TSC test system [14,15]. At higher fields, the current increases exponentially with increasing *E*. Similar results are observed for the N_2O-nitrided oxides. The strong increase in current with increasing electric field and the weaker dependence on temperature are consistent with Fowler-Nordheim tunneling [10,11,16], but Schottky and/or Poole-Frenkel barrier lowering can also affect the conduction under these conditions [19,20].

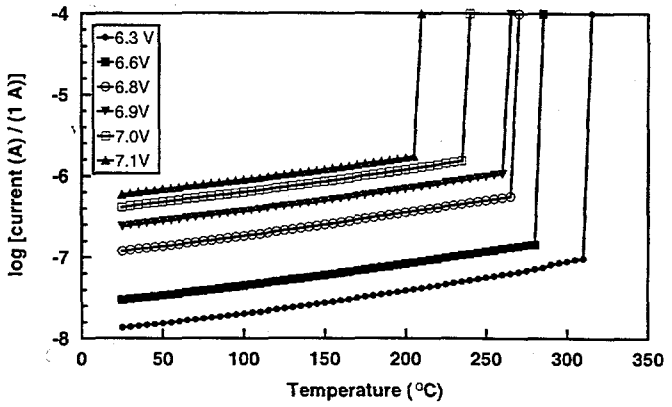

Fig. 3. Log_{10} (current) vs. temperature and applied gate bias for 0.00035 cm^2 *n* substrate capacitors with poly-Si gates and 7.0 nm nitrided oxides.

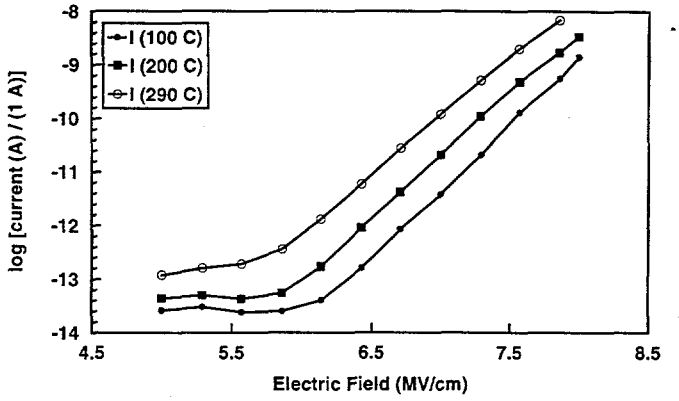

Fig. 4. Log_{10} (current) vs. applied electric field (well below breakdown) and temperature for the thermal oxides of Fig. 2.

In Fig. 5, we compare the values of temperature-to-breakdown T_{BD} for the thermal and N_2O-nitrided oxides of Figs. 2 and 3, where T_{BD} is the temperature at which one observes the initial, sharp up-tick in current in each curve. In Fig. 5, for each type of insulator, the value of T_{BD} decreases approximately linearly with increasing applied voltage. In addition, for the range in which comparison is possible (6.3 to 6.9 V, corresponding to electric fields of 9.4 to 10.3 MV/cm), values of T_{BD} are 97 ± 8 °C higher for the nitrided oxides than for the thermal oxides.

To understand the reasons for the differences in responses of the various oxides, it is useful to consider the effective values of charge-to-breakdown Q_{BD}. Fig. 6 is a plot of Q_{BD} as a function of applied gate bias for the devices of Figs. 1-3. To obtain an estimate of Q_{BD}, charge is integrated over time only to the first breakdown-like event, as beyond that point the oxide conduction changes its character, and Q_{BD} loses its

usefulness as a figure of merit. Note that, with the exceptions of two "early" breakdowns for the Al gate oxides of Fig. 1, Q_{BD} generally increases at higher fields (corresponding to lower values of T_{BD}). When Q_{BD} becomes comparable to breakdown levels at room temperature for these oxides (e.g., 5-10 C/cm^2 for the Si gate devices of Figs. 2 and 3 [18], which is a typical breakdown level for a high-quality 7 nm oxide at ~ 300 K [10,16]), the device breaks down. Thus, for these devices, the high-T Q_{BD} is less than or equal to the room temperature Q_{BD}. Ultimately, it is the amount of charge that transports through the oxide (or, more precisely, the concomitant number of defects created) that causes electrical breakdown. Thus, the value of T_{BD} will decrease with decreasing ramp rate used for the ramped current-temperature stress. The particular ramp rate used here was the fastest rate that we can use in this particular system, while still preserving accurate thermometry [14,21]. A more detailed comparison of the temperature dependence of Q_{BD} with that observed in previous work is presented in Section III below.

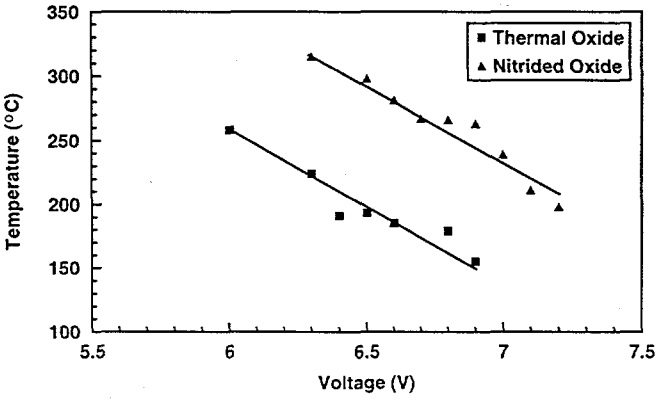

Fig. 5. Temperature-to-breakdown vs. applied gate voltage for the devices of Figs. 2 and 3.

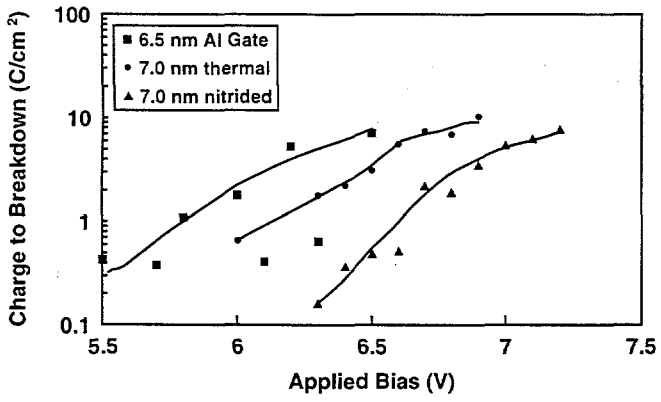

Fig. 6. Charge to breakdown vs. applied gate bias for the devices of Figs. 1-3. Two "premature" breakdowns occur in the Al gate data (squares).

B. Breakdown of Irradiated Capacitors.

Now that the utility of the temperature-ramp technique has been illustrated, it is interesting to see whether radiation exposure alters the observed response. Fig. 7 shows the effects of ionizing radiation exposure on the breakdown response of the thermal oxides of Fig. 2. Devices were irradiated with 10-keV x rays at a dose rate of ~ 3000 rad(SiO_2)/s to doses as high as 20 Mrad(SiO_2) at 3 V bias. Threshold voltage shifts due to oxide and interface trap charge were less than ~ 100 mV, even at the highest doses, showing that, as expected, there is little net charge trapping in these thin oxides [22,23], although the presence of higher densities of neutral defects [9] and/or dipole charge is likely [24]. Fig. 7 shows that there are no significant effects of radiation exposure on T_{BD} or Q_{BD}.

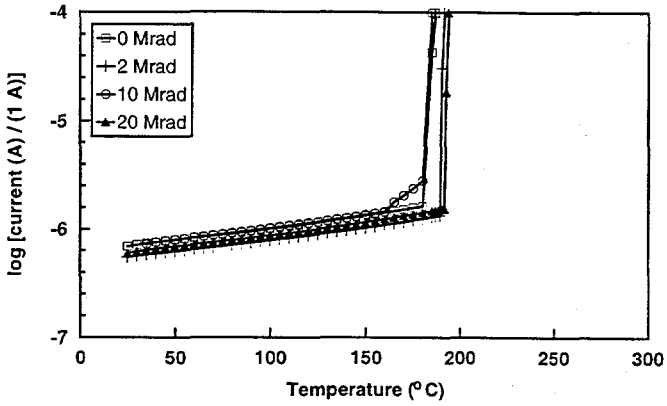

Fig. 7. Log_{10} (current) vs. temperature and x-ray dose for the thermal oxides of Fig. 2. The applied gate bias was 3 V during irradiation and 6.6 V during postirradiation I-T stress. Estimated values of Q_{BD} were ~ 5.6, 4.7, 5.7, and 5.1 C/cm^2 for capacitors irradiated to 0, 2, 10, and 20 Mrad(SiO_2).

Similar results were observed for more than 15 other thermal or N_2O-nitrided oxides irradiated at positive, negative, or zero bias. Representative I-T ramps are compared in Fig. 8 for (a) nitrided oxides, and (b) thermal oxides, where devices are either unirradiated, irradiated to 20 Mrad(SiO_2) at ± 3 V at a rate of ~ 3000 rad(SiO_2)/s with 10-keV x rays, and/or (for one of the nitrided oxides) given a 1-week room-temperature anneal at 3 V between x-ray irradiation and breakdown testing. In none of these or other examples we have examined have the current levels or the values of Q_{BD} or T_{BD} been affected significantly by radiation exposure.

If, as one suspects, ionizing radiation exposure breaks weak bonds in SiO_2 and/or releases hydrogen species in the gate oxide, it is clear these defects are not significantly affecting the I-T curves here. This may occur because radiation induced defects tend to be point defects, while defects contributing to electrical breakdown tend to be extended clusters of defects that are physically linked into a conducting path [10,18]. Moreover, 1 C/cm^2 corresponds to 1.6 x 10^{19} charges/cm^2, while 20 Mrad(SiO_2) is only ~ 1.1 x 10^{15} electron-hole pairs/cm^2 in these 7 nm oxides. Thus, the total charge density created by ionizing radiation exposure is much smaller than that in the electrical stress, which also may help to mitigate the effects of radiation exposure on oxide reliability. Finally, the passage of high current through an oxide will lead to the annealing of some radiation damage, either at room or elevated temperature, which may further reduce the effects of radiation exposure on long-term MOS oxide reliability. Of course, Figs. 7 and 8 are by no means comprehensive, so the results for other devices with different processing may vary from those shown here.

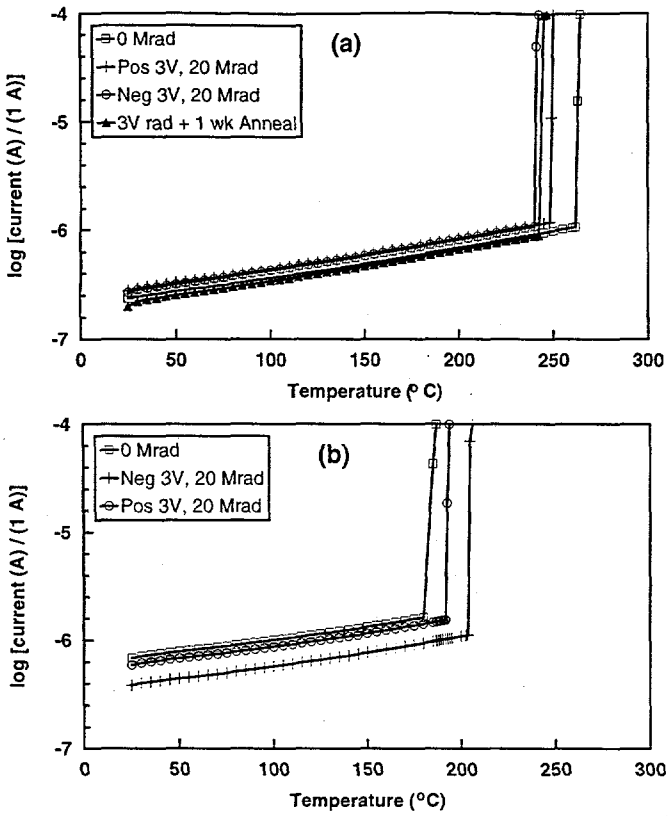

Fig. 8. *I-T* plots vs. radiation dose, bias, and/or postirradiation room-temperature annealing for (a) the N_2O nitrided oxides of Fig. 3, and (b) the thermal oxides of Fig. 2. The applied gate bias was ± 3 V during irradiation, and the dose was 20 Mrad(SiO_2) for these exposures. The postirradiation *I-T* stress voltage was 6.9 V for the nitrided oxides, and 6.6 V for the thermal oxides. Values of Q_{BD} were ~ 3.5, 4.0, 3.7, and 3.1 C/cm^2 for the N_2O oxides of (a), in order of appearance in the caption, and ~ 5.6, 5.1, and 3.8 C/cm^2 for the corresponding thermal oxides in (b).

III. Discussion

A. Temperature Dependence of Q_{BD}

The above results clearly demonstrate that the breakdown mechanisms at room and elevated temperatures are similar in these devices. Hence, the current-temperature ramp technique can provide a useful measure of oxide reliability in these cases. During some of the *I-T* ramps at lower electric fields, breakdown occurs "prematurely" (i.e., at values of Q_{BD} well below room temperature levels) at high temperatures. To first order, the trend that we observe toward a reduction in values of Q_{BD} with increasing measurement temperature is consistent with previous work at constant field and temperature [7,16,19,25,26]. The decrease in Q_{BD} with increasing temperature in thin oxides has been attributed to the strong increase in trap creation with increasing temperature [16,26].

It is not easy to perform a quantitative comparison of the dependence of Q_{BD} on temperature for ramped current-temperature and constant temperature stress measurements, since the thermal histories are significantly different in the two cases. For example, Fig. 9 shows a simple comparison of the values of T_{BD} in this work to the temperature dependence of Q_{BD} in previous work on 7 nm oxides performed by Apte et al. [25], and discussed in the context of trap generation models by DiMaria et al. [16] Note that breakdown occurs at much higher temperatures for the ramped parts than for parts stressed at a constant temperature. However, much of this difference occurs simply because there is a range of temperatures in the ramped measurements, and presumably a different characteristic value of Q_{BD} (decreasing with increasing T) that corresponds to each of these temperatures. Hence, one must correct for this factor in such a comparison.

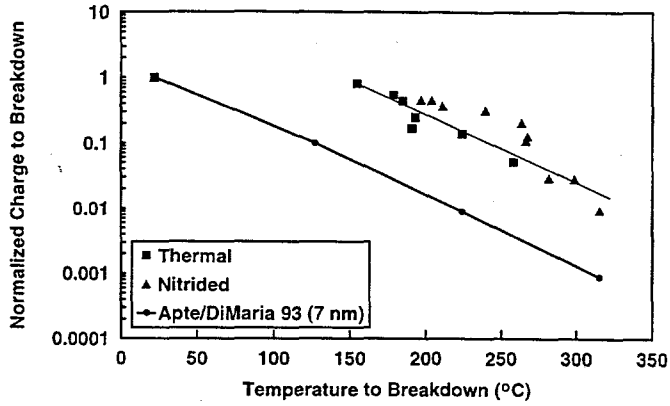

Fig. 9. $Q_{BD}(T)/Q_{BD}(22\ °C)$ vs. T_{BD} for the bias-temperature ramp testing of the thermal oxides of Fig. 2 and the nitrided oxides of Fig. 3. For comparison, charge-to-breakdown data for 7 nm thermal oxides under constant-temperature electrical stress is shown from Fig. 27 of Ref. [16].

One way to at least qualitatively compare ramped and constant temperature stress data is illustrated in Fig. 10. Here the ramped temperature results are replotted in terms of the cumulative charge per unit area that has passed through the oxide. The curvature in the plots at low temperatures is due to the nonlinear heating rates during the *I-T* measurements below ~ 60 °C [14]. By comparing the amount of charge that passes through the thermal and nitrided oxides with the values of Q_{BD} in previous work, a better comparison is possible.

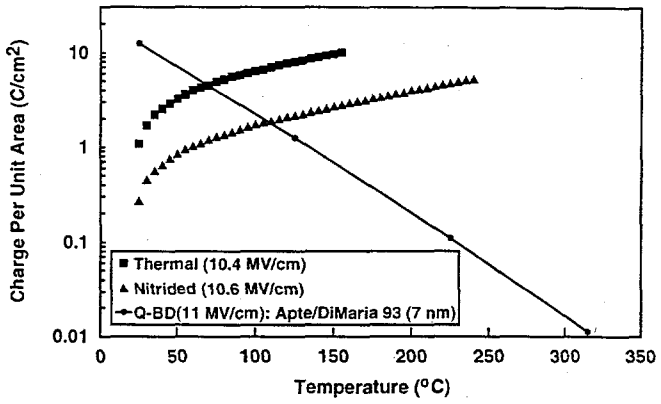

Fig. 10. Cumulative charge per unit area as a function of temperature for the thermal oxides of Fig. 2 at 10.4 MV/cm, the nitrided oxides of Fig. 3 at 10.6 MV/cm, and normalized 7 nm thermal oxide data from Ref. [16]. The data of Ref. [16] have been scaled to a room temperature Q_{BD} value of 12.5 C/cm^2, equal to the room temperature Q_{BD} for the 7 nm thermal oxides used in this work, to facilitate the comparison.

For example, consider first the 7 nm thermal oxides from Fig. 2. Between temperatures of 100 and 150 °C, ~ 3.7 C/cm^2 flows through this oxide just before breakdown. Even if one

completely ignores the previous ~ 6.4 C/cm^2 that passed through the oxide below 100 °C, this amount of charge is roughly 3 times the (relative) amount of charge that the oxides in Refs. [16] can sustain at a comparable temperature of 125 °C. The nitrided oxides provide an even more dramatic example. Between 210 and 240 °C, ~ 1 C/cm^2 flows through the 7 nm nitrided oxides. In contrast, relative to their room temperature response, the thermal oxides of Ref. [16] can sustain only about 1/10 this amount of charge before breaking down. Thus, while the first order dependence of breakdown on temperature is similar, it seems that these devices can withstand the passage of more charge before breakdown at higher temperatures than can oxides of similar thickness in constant temperature measurements in prior work.

Some differences in the temperature dependence of Q_{BD} between this and prior work may be due simply to differences in as-processed defect densities among the devices. However, the increased Q_{BD} at elevated temperature seen here may also occur because the ramp technique allows the oxide to relax as the device is heated under bias, in contrast to cases in which high fields are first applied at high temperature. In the latter case, the electrons will have a more difficult time coming into equilibrium with the lattice than in the ramped temperature case where the device has been "pre-conditioned" by current flow at room temperature, and then the temperature is slowly raised into a regime in which the breakdown process is accelerated significantly. The further improvement in Q_{BD} for the nitrided oxides at high temperature is likely a result of the nitride-inhibited motion of hydrogen-related species that can degrade the reliability of the oxide [16], although a change in barrier height may also contribute to the difference.

B. RILC due to Ion Exposure.

It is interesting to compare the results of Figs. 7 and 8 for electrical breakdown to previous studies of these devices in a heavy ion environment. The dependence of heavy ion-induced gate rupture was discussed in detail in Ref. [18]. In that work, damage due to heavy ion exposure was reported, which is analogous to the RILC in gamma and electron irradiations in Ref. [1-5]. Fig. 11 recapitulates some of the results of this study. Interestingly, in Fig. 11(a) no measurable RILC (i.e., less than 10 pA) is observed at 4 V for 7 nm thermal oxides exposed to a fluence of 7 x 10^8 cm^{-2} 283-MeV Br ions at 5 V exposure bias, but in Fig. 11(b) significant RILC was observed for 5.2 V exposures of a nitrided oxide for fluences above 5 x 10^7 cm^{-2} of 283-MeV Br ions.

The linear energy transfer (LET) of 283-MeV Br ions is ~ 60 MeV-cm^2/mg. A first order approximation of the total ionizing dose in SiO_2 for a fluence of ~ 10^8 283-MeV Br ions is ~ 40 Mrad(SiO_2), assuming (1) a charge generation rate of ~ 8 x 10^{12} electron-hole pairs per rad(SiO_2) per cm^3, (2) an average energy of ~ 17 eV per electron-hole pair [27], and (3) that most of the energy loss in the oxide is due to ionization processes. Hence, for Br ion bombardment, the threshold for observation of RILC in the nitrided oxides is comparable to that observed at comparable electric fields in previous RILC studies at the University of Padua [1-5]. However, the thermal oxides seem more resistant to RILC, with no measurable excess leakage current even at Br ion-equivalent doses greater than 100 Mrad(SiO_2). This result is especially significant in view of the fact that the heavy ions will cause significant displacement damage, in addition to ionization effects. Further, these exposures should also tend to produce oxide defects in a pipe through the oxide [18], which one might expect to enhance the leakage current [10,18]. Still, the observed RILC was comparable to, or less than, that for cases in which significant displacement damage is not expected.

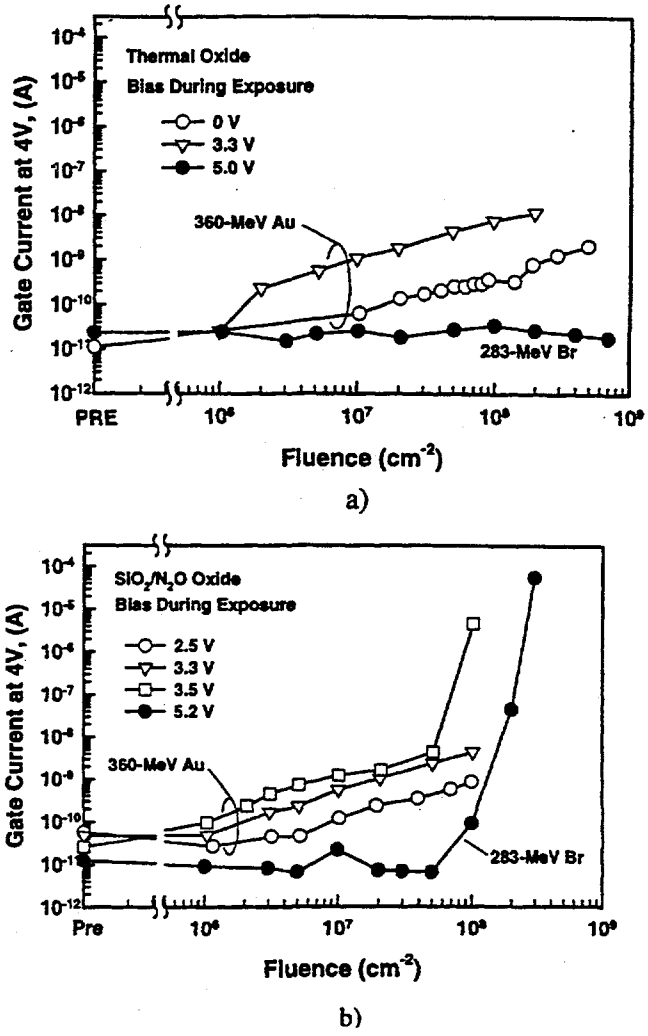

Fig. 11. Leakage current at 4 V as a function of heavy ion fluence and bias during exposure at Brookhaven National Lab for the 7 nm (a) thermal oxides of Fig. 2, and (b) N_2O-nitrided oxides of Fig. 3. (After Ref. [18].)

When the oxides of Fig. 11 were bombarded by ~ 360-MeV Au ions (LET ~ 80 MeV-cm^2/mg), the threshold for the observation of detectable RILC (0.1 to 1.0 nA) was ~ 3 x 10^6 ions/cm^2 for both the 7 nm thermal and nitrided oxides. This fluence level of Au ions corresponds to an equivalent dose of ~ 16 Mrad(SiO_2). These results confirm that very high radiation exposure can lead to RILC in these oxides. However, whether this degradation is observable or relevant to the reliability of these or other oxides in a system of practical interest likely depends on the details of the exposure conditions and the quality of the oxide. Most notably, neither in Ref. [18] nor in this work does prior irradiation exposure cause a significant reduction in the electrical breakdown or ion-induced rupture of high quality oxides.

IV. SUMMARY AND CONCLUSIONS

We have found that *I-T* measurements can provide useful information about electrical breakdown in thin oxides. High-quality MOS gate oxides can show exceptionally well-behaved characteristics with high reproducibility from device to device. Other oxides like the Al gate capacitors in Fig. 1 can show a more erratic response. Hence, *I-T* measurements can potentially be used as a figure-of-merit to evaluate the intrinsic reliability of MOS gate insulators. Moreover, we have also found that these measurements can provide a useful test for the effects of radiation exposure on the intrinsic reliability of high quality gate dielectrics

The decreases in measured values of charge to breakdown with increasing temperature are qualitatively similar between this and previous [16,25,26] work. Moreover, the ramped temperature stress technique evidently allows the oxide to remain in thermal equilibrium longer and/or relax more efficiently than constant temperature, high-field-stress measurements. This suggests that ramped current-temperature stress may provide a more faithful simulation of the response of a device over long times at lower electric fields and lower temperatures than do accelerated test methods in which high fields are directly applied at elevated temperature. If this is the case, these measurements could become a key element in future efforts to predict the long-term reliability of MOS gate oxides. However, additional comparative studies are required to determine whether this is indeed the case.

Differences are observed between the high-temperature conduction and the temperature dependence of oxide breakdown at high fields between N_2O-nitrided and thermal oxides. These differences are evidently due to differences in effective barrier heights, conductivity, and/or material quality. No significant decrease in thin MOS dielectric reliability was observed for radiation doses up to 20 Mrad(SiO_2) for high-quality 7 nm nitrided or thermal oxides. However, more defective oxides may be more sensitive to reliability degradation with radiation exposure. Hence, while these results show that there is no fundamental reduction in the reliability of high-quality oxides due to radiation exposure, they do not prove that the reliability of other types of oxides will be similarly unaffected. In the future, it would be very interesting to perform these kinds of measurements on alternative gate dielectrics to SiO_2, both before and after radiation exposure.

V. ACKNOWLEDGMENTS

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