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Double barrier resonant tunneling transistor with a fully two dimensional emitter

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A novel planar resonant tunneling transistor is demonstrated. The growth structure is similar to that of a double-barrier resonant tunneling diode (RTD), except for a fully two-dimensional (2D) emitter formed by a quantum well. Current is fed laterally into the emitter, and the 2D – 2D resonant tunneling current is controlled by a surface gate. This unique device structure achieves figures-of-merit, i.e. peak current densities and peak voltages, approaching that of state-of-the-art RTDs. Most importantly, sensitive control of the peak current and voltage is achieved by gating of the emitter quantum well subband energy. This quantum tunneling transistor shows exceptional promise for ultra-high speed and multifunctional operation at room temperature.

DISCLAIMER

For well over two decades, electronic devices based on quantum effects have offered the promise of increased functionality and greatly enhanced switching speeds. Although various different devices have been proposed and demonstrated (*1-3*), to date the double barrier resonant tunneling diode (RTD) (*4,5*) based on tunneling from a three-dimensional (3D) emitter to a two-dimensional (2D) resonant layer, has been by far the most successful. RTDs have been demonstrated with resonant current peak-to-valley ratios (PVRs) of 30:1 at 300 K (*6*), picosecond switching times (*7*), and are now finding circuit applications in memories (*8,9*). RTD-like structures have also been shown to detect THz frequency photons (*10*).

There have also been numerous attempts to develop a practical resonant tunneling transistor (RTT) by controlling the resonant tunneling current in RTDs via a base current (*11,12*) or a gate voltage (*13*). Such a three-terminal device would have many more applications than a conventional, two-terminal, RTD. By contrast, however, these efforts have met with much less success. (*14*) For instance, RTT's based on the side-wall gating of narrow RTD post-like structures (*13*) have suffered from relatively small transconductances, as well as severe fabrication problems due to the required submicron resolution and non-planarity of the geometry. The majority of these schemes to realize RTTs have involved slight modifications of the fundamental RTD design, which is based on 3D-2D tunneling. One early exception to this basic design was a planar structure involving the gate control of tunneling between a 3D and a 2D region through a single barrier. (*15,16*) Unfortunately, this device exhibited a very poor PVR, even at the low temperature of 7 K.

In the past few years, however, several techniques for making independent electrical contact to the two closely spaced (~200 Å) 2D electron layers in double quantum well (DQW) structures have been developed. (*17–19*) This has made possible the development of a new type of RTT, the double electron layer tunneling transistor (DELTT). In this device, resonant tunneling occurs between *two independently contacted 2D electron layers* separated by *a single barrier*, and is controlled by a surface gate. (*20-22*) The DELTT represented a significant advance over other RTTs, as it exhibited PVRs of order 10:1 at 77 K, was sufficiently stable to act as a single transistor static memory, and enabled the demonstration of unipolar complementary circuits for the first time. (*23*) Most importantly, the DELTT geometry is entirely planar and scalable, meaning that in principle it could be used in large numbers in integrated circuits. Despite these advances, the original DELTT design suffered from a number of performance shortcomings that would need to be overcome for practical applications. These included (i) a peak voltage too low (~20 mV) to interface with conventional electronics and to be robust against enviromental noise, (ii) a low peak current density, (iii) a relatively weak dependence of the peak voltage on applied gate voltage, and (iv) an operating temperature that, while fairly high, remained below room temperature.

In this letter, we report an advanced resonant tunneling transistor that incorporates structural elements both of the DELTT and of conventional double barrier RTDs. Specifically, the device is similar to the DELTT in that it is based on 2D-2D tunneling and is controlled by a surface gate, yet is also similar to the RTD in that it has a double barrier structure and a third collector region. Indeed, the device may be thought of either as an RTD with a gate-controlled, fully 2D emitter, or alternatively, as a "3-layer

DELTT," the name we have tentatively chosen for the device. As we demonstrate here, this new RTT retains the original DELTT advantages of a planar geometry and sharp 2D-2D tunneling characteristics, yet also overcomes the performance shortcomings of the original DELTT design. In particular, it exhibits the *high peak voltages and current densities* associated with conventional RTDs, allows *sensitive control of the peak voltage* by the control gate, and operates nearly at *room temperature.*

We now turn to the basic design and operation of the new 3-layer DELTT. Fig. 1(a) shows a sketch of the band structure, and Fig. 1(b) a cross sectional view of the device geometry. Current flows from the emitter to the collector as follows: First, electrons are fed laterally from the emitter contact into the lowest 2D subband of the emitter QW. If the gate is biased appropriately, the electrons then tunnel vertically through the emitter barrier into the lowest 2D subband of the resonant layer QW. Once electrons are in the resonant layer QW, they will then continue onwards through the much thinner collector barrier, into the broad continuum of electron states existing in the third bulk-like collector layer. (*24*) The electrons then flow laterally through the collector layer into the collector contact, exiting the device. (*25*) A significant impediment to current flow can exist only when electrons tunnel from the emitter subband to the resonant layer subband. As in the case of the original double quantum well DELTT, this 2D-2D tunneling step can only occur when these two subbands are precisely aligned in energy, due to the simultaneous conservation of energy and momentum. (*20*) The subbands can be brought into alignment by either (i) applying sufficient emitter-collector bias, or (ii) biasing the control gate to raise or lower the emitter subband energy, or (iii) both.

The 3-layer DELTT devices described in this work were processed from several different molecular beam epitaxy (MBE) grown GaAs/$Al_{0.3}Ga_{0.7}As$ heterostructures, whose parameters are given in Table 1. For all devices, the emitter QW was 220 Å thick and the resonant QW 120 Å thick. The GaAs collector layer was 3000 Å thick for all structures except EA338, for which it was 2000 Å. The emitter and collector barrier thicknesses (L_{EB} and L_{CB}) were varied over a wide range, subject to the constraint $L_{CB} \leq L_{EB}$. Independent contacts to the emitter and collector layers were formed by biasing (typically at a few volts) front and back depletion gates to deplete electrons from all layers except the contacted one. (*17*) The close proximity backgates were only ~0.5 μm from the collector layer, and were fabricated using the epoxy-bond-and-stop-etch (EBASE) process. (*19*) The typical lateral dimensions of the gates and their spacings are similar to those of the original DELTT structures, described earlier. (*20*) All measurements exhibited excellent reproducibility over thermal cycling.

In Fig. 2 we show the 77 K emitter-collector current-voltage (I-V) characteristics of 3-layer DELTT EA339, for several top control gate voltages V_{TC}. The I-V is highly non-linear, with sharp resonant tunneling peaks whose current and voltage positions are clearly controlled by V_{TC}. Strikingly, at $V_{TC} = 0$ the main resonant peak voltage V_P is at $V_{EC} \approx 0.36$ V, over an order of magnitude larger than typically observed in 2-layer DELTTs. (*21*) In addition, the peak-to-valley ratio at $V_{TC} = 0$ is 32:1, which is also considerably higher than observed in 2-layer DELTTs at this temperature. As V_{TC} increases (i.e. as the Fermi energy in the emitter QW increases), both the peak current density J_p and the peak voltage V_P increase monotonically.

A quantitative understanding of this high V_P can be gained with the following simple model. If the applied emitter-collector bias V_{EC} is assumed to drop uniformly across the distance L_{EC} between the electron wavefunctions of the emitter and collector [see Fig. 1(a)], then we expect that:

$$V_P = (L_{EC}/L_{ER})\Delta E_{ER}/e \qquad (1)$$

where L_{ER} is the distance between the electron wavefunctions of the emitter and resonant layer subbands, and $\Delta E_{ER} = E_{R0}-E_{E0}$ is the difference in energy between the emitter and resonant layer ground subbands at zero bias. Fig. 3(a) shows the results of a 4.2 K self-consistent Hartree calculation of the bandstructure of EA339 at $V_{TC} = V_{EC} = 0$. From this we obtain $\Delta E_{ER} = 28.7$ meV, $L_{EC} = 3394$ Å, and $L_{ER} = 330$ Å. This yields an estimate of $V_P = 0.30$ V, in fair agreement with the observed value. This calculated value for ΔE_{ER} is further supported by photoluminescence (PL) measurements on wafer EA339, shown in Fig. 3(b). The emitter and resonant QW peaks are clearly visible in the PL data, and their energy difference of 27.6 meV is close to our calculated value. (*26,27*)

The increase in V_P with increasing V_{TC} is further illustrated in the inset to Fig. 2. We define the resonant peak voltage gain G_{RPV} as $\Delta V_P/\Delta V_{TC}$, which provides a useful measure of the effectiveness of the gate. A value for G_{RPV} can be estimated from our model by assuming that the gate acts only to change the electron density in the emitter, and that any electric field penetration from the gate to the collector layer is negligible. (23) Thus we obtain:

$$G_{RPV} = \Delta V_P / \Delta V_{TC} \approx \frac{\varepsilon}{d_{GE}} \frac{\pi\hbar^2}{m^* e^2} \frac{L_{EC}}{L_{ER}} \qquad (2)$$

where ε is the dielectric constant, d_{GE} is the gate to emitter wavefunction distance, and m* is the effective mass. Using m* = 0.067 m_e, d_{GE} = 6000 Å, and the L_{EC} and L_{ER} values obtained from the Hartree simulation for V_{TC} = 0, we obtain $\Delta V_P / \Delta V_{TC}$ = 0.044, quite close to the experimental value of ~ 0.048 at V_{TC} = 0. This measured value for G_{RPV} is rather small because of the unusually large gate-emitter distance d_{GE} of 6000 Å for this test structure, which contained a silicon oxide layer beneath the gate. We expect that 3-layer DELTT structures with d_{GE}'s approaching the 500 Å typically found in commercial HEMTs should readily exhibit a G_{RPV} of unity or above. Nonetheless, the data amply illustrate that the G_{RPV} is increased by the geometric leverage factor L_{EC}/L_{ER} (> 10) over that observed in the previous DQW DELTT. Thus, unity G_{RPV} operation, which is extremely difficult to obtain from a single barrier tunneling device (*15,16,20*) can be readily achieved in these new 3-layer DELTT structures.

We now turn to the subject of current density J_P in the 3-layer DELTT. Although the intrinsic speed of electron tunneling is extremely fast, in an actual device parasitic effects often limit the operating frequency long before the intrinsic switching speed is reached. Typically these take the form of an RC-like charging time $1/\tau = J_P/C_{EC}$, where C_{EC} is the capacitance between the emitter and collector. (*28*) Thus, in order to realize extremely high speeds in the 3-layer DELTT, it is highly desirable to increase the peak current density, J_P.

The factors determining the current density in the new 3-layer DELTTs are similar to those in RTDs. The first factor determining J_P is the emitter barrier thickness. The relatively low J_P in EA339 is due to its extremely thick (d_{EB} = 120 Å) emitter barrier. The

other structures, with thinner emitter barriers, have substantially larger J_P. Fig. 4 shows the J_P values measured at $V_{TC} = 0$ V from the five devices of Table 1, plotted as a function of d_{EB}. (These structures all have nominally the same emitter density of ~2.5 x 10^{11} cm^{-2}.) The peak current density J_P is seen to increase by a factor of ~1.52 for each monolayer (2.826 Å) reduction in d_{EB}. (*29*) If the curve is extrapolated to a d_{EB} of only 10 monolayers (28.3 Å), then we would expect J_P to approach 8.2 x 10^3 A/cm^2.

The second factor influencing J_P is the supply function, or the number of emitter electrons available to participate in tunneling. The number of available emitter electrons per unit area is given by DOS(2D)*E_F^{2D}(emitter) = n_E^{2D}, the electron density in the emitter QW. Here DOS(2D) is the 2D electronic density of states, and E_F^{2D} (emitter) is the Fermi energy in the emitter. This is consistent with the increase in J_P with increasing V_{TC} observed in Fig. 2. [We note that in RTDs, a much weaker dependence on emitter density is found, $DOS(2D) \cdot E_F^{3D}(emitter) = \frac{\pi}{2}\left(\frac{3n_E^{3D}}{\pi}\right)^{2/3}$.] As a result, the current density of 3-layer DELTTs can also be substantially increased by raising the $V_{TC} = 0$ value of the emitter density. As indicated by the dashed line in Fig. 4, a 3-layer DELTT with a 1 x 10^{12} cm^{-2} emitter electron density and a d_{EB} = 10 monolayers can be expected to have J_P = 3.2 x 10^4 A/cm^2, comparable to some of the higher values reported for conventional RTDs. Because the emitter-collector capacitance per unit area C_{EC} of 3-layer DELTTs is also comparable to that found in RTDs, this new RTT device shows considerable promise for operating at comparable speeds of several hundred GHz.

Finally, we discuss the temperature behavior of 3-layer DELTTs. Fig. 5(a) shows the emitter-collector I-V curve of DELTT EA339 at $V_{TC} = 0$ V, for several temperatures.

While below 200 K the valley current increases relatively slowly with, a sudden increase in valley current above ~200 K results in a diminished PVR. Nonetheless, regions of NDR persist to ~250 K. Similar behavior is also observed for DELTT EA338, which is shown in Fig. 5(b) for several different V_{TC} at 273 K, or 0 °C. Clear gate control of the resonant current peak is observed. We note that these 3-layer DELTTs operate at temperatures considerably higher than the original DQW DELTTs. We attribute this to the double barrier structure of the new design, which serves to reduce the off-resonant valley current. Because the new 3-layer DELTT structure shares the double-barrier design of RTDs, we expect that room temperature operation can be achieved via the use of different material systems with higher conduction band offsets, much as has been observed in RTDs. Such material systems would include, for instance, $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ lattice matched to InP (*6,30*), or InAs/AlSb/GaSb (*31*).

In summary, we have demonstrated a new resonant tunneling transistor which combines the novel gate-controlled 2D-2D tunneling mechanism of the original DELTT transistor with the resonant double-barrier structure found in conventional RTDs. The resulting RTT is fully planar, and exhibits operation at high temperatures, high peak voltages, and high current densities, holding excellent promise for further development as a practical high-speed electronic device.

TABLE 1. Device parameters.

L_{EB}: Emitter barrier thickness, L_{CB}: Collector barrier thickness, V_p : voltage at I-V peak, PVR: peak-to-valley current ratio.

Device	L_{EB} (nm)	L_{CB} (nm)	V_p (V)	PVR (77 K)
EA339	12	8	0.36	32:1
EA338	10	8	0.5	20:1
EA491	8	8	0.65	15:1
EA492	7	7	1.4	3:1
EA493	6	6	1.63	1.1:1

References

1. A. O. Orlov, I. Amlani, G. H. Berstein, C. S. Lent, G. L. Snider, Science **277**, 928 (1997).

2. L. J. Guo, E. Leobandung, S. Y. Chou, Science **277**, 21 (1997).

3. S. J. Tans, A. R. M. Verschueren, C. Dekker, Nature **393**, 49 (1998).

4. R. Tsu, L. Esaki, Appl. Phys. Lett. **22**, 562 (1973).

5. L. L. Chang, L. Esaki, R. Tsu, Appl. Phys. Lett. **24**, 593 (1974).

6. T. P. E. Broekaert, W. Lee, C. G. Fonstad, Appl. Phys. Lett. **53**, 1545 (1988).

7. J. F. Whitaker, G. A. Mourou, T. C. L. G. Sollner, W. D. Goodhue, Appl. Phys. Lett. **53**, 385 (1988).

8. P. Mazumder, S. Kulkarni, M. Bhattacharya, J. P. Sun, G. Haddad, Proceedings of the IEEE. **86**, 664 (1998).

9. J. P. A. Vanderwagt, A. C. Seabaugh, E. A. Beam, IEEE Electron Dev. Lett. **19**, 7 (1998).

10. H. Drexler, J. S. Scott, S. J. Allen, K. L. Campman, A. C. Gossard, Appl. Phys. Lett. **67**, 2816 (1995).

11. F. Capasso, R. A. Kiehl, J. of Appl. Phys. **58**, 1366 (1985).

12. M. A. Reed, W. R. Frensley, R. J. Matyi, J. N. Randall, A. C. Seabaugh, Appl. Phys. Lett. **54** , 1034 (1989).

13. W. B. Kinard, M. H. Weichold, W. P. Kirk, J. Vac. Sci. Tech. B **8**, 393 (1990).

14. S. Luryi, A. Zaslavsky in *Modern Semiconductor Device Physics*, S. M. Sze, Ed (Wiley-Interscience, New York, 1998), pp 253-341.

15. A. R. Bennofoi, D. H. Chow, T. C. McGill, Appl. Phys. Lett. **47**, 888 (1985).

16. F. Beltram, F. Capasso, S. Luryi, S. N. G. Chu, A. Y. Cho, Appl. Phys. Lett. **53**, 219 (1988).

17. J. P. Eisenstein, L. N. Pfeiffer, K. W. West, Appl. Phys. Lett. **57**, 2324 (1990).

18. K. M.Brown et al., Appl. Phys. Lett. **64**, 1827 (1994).

19. M. V. Weckwerth et al., Superlattices and Microstructures **20**, 561 (1996).

20. J. A. Simmons et al., J. Appl. Phys. **84**, 5626 (1998).

21. M. A. Blount et al., Semiconductor Science and Technology **13**, A86 (1998).

22. J. S. Moon et al., Electron. Lett. **34**, 921 (1998).

23. J. S. Moon, J. A. Simmons, M. A. Blount, J. L. Reno, M. J. Hafich, Appl. Phys. Lett. **74**, 314 (1999).

24. The issue of whether tunneling through the two barriers is coherent or sequential is similar to that in conventional RTDs. For a discussion, see e.g. S. Luryi, Superlattices and Microstructures **5**, 375 (1989) and references therein.

25. We note that an alternative 3-layer DELTT device structure could allow the electrons to exit vertically from the collector and out the back of the device, rather than laterally. This would lower the effective contact resistance, and allow a smaller lateral device dimension.

26. We note that a second, smaller resonant peak also appears, for $V_{EC} \leq 0.05$ V at 77 K. This is attributed to resonant tunneling from the thermally occupied *second* subband of the emitter into the ground subband of the resonant layer. (At lower temperatures this peak is absent.) The Hartree simulation of Figure 3(a) yields an energy difference E_{R0}-E_{E1} = 2.44 meV, predicting a V_P for this second peak of 0.025 V, in fair agreement with the data.

27. For the more negative values of V_{TC} there is also apparent a small peak occurring near $V_{EC} = 0.39$ V, independent of V_{TC}. It is attributed to resonant tunneling in the ungated regions of the device.

28. Preliminary S–parameter measurements indicate that the charging time, like in RTDs, is more closely approximated by $\tau = C_{EC}\sqrt{R_S R_{NDR}}$, where R_{NDR} is the most negative value of the negative differential resistance, and R_s is the 2D channel resistance. See E. R. Brown et al., Appl. Phys. Lett. **58**, 2291 (1991). We note that the transit time delay through the wide collector region is roughly 1 psec and should have a nearly negligible effect on the high-speed performance.

29. For sample EA339, the tunneling resistance is roughly 4 orders of magnitude larger than the in-plane resistance of the 2D lead regions at 77 K, and clearly dominates the measurement of J_p. However, as the thickness of the tunneling barrier is decreased in the other samples, the resistance of the in-plane 2DEG leads begins to play a larger role. Thus our measurements of the PVR and current densities for samples EA492 and EA493 represent lower bounds. We estimate that subtraction of the in-plane 2DEG resistance in sample EA493 would result in a 77 K current density value that is ~50% higher than indicated in Fig. 4.

30. T. Inata et al., Jpn. J. Appl. Phys., **26** L1332 (1987).

31. J. R. Soderstrom et al., Appl. Phys. Lett. **58**, 275 (1991).

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Figure Captions

Fig. 1. (a) Typical conduction band profile of the 3-layer DELTT, with an emitter-collector bias applied. The wavefunction separations L_{ER} and L_{EC} are indicated. (b) Schematic diagram of the 3-layer DELTT device structure, showing the two 2DEGs, each selectively contacted via a selective gate depletion technique, and a control gate which controls the tunneling.

Fig. 2. Emitter-collector current I_{EC} vs. voltage V_{EC} of a single device from the EA339 wafer, measured at 77 K for several values of V_{TC}. The inset shows how the peak voltage V_P changes as a function of control gate voltageV_{TC}.

Fig. 3. (a) Results of an equilibrium self-consistent Hartree calculation of the band structure of 3-layer DELTT EA339. Zero energy represents the Fermi level. Significant free electron densities appear only in the emitter QW and at the far side of the collector. The energies of several subbands are indicated. The difference in energy between the emitter and ground subbands is 28.7 meV. (b) Photoluminescence data from wafer EA339. The difference in energy between the emitter and resonant QW ground subbands is 27.6 meV, close to the value obtained from the Hartree calculation.

Fig. 4. Measured peak current density J_P vs. emitter barrier thickness d_{EB} for the devices in Table 1, which all had emitter densities of ~2.5×10^{11}. The solid line is a fit to the data. Extrapolation of the fit to a barrier thickness of 28 Å yields a current density of 8.2

x 10^3 A/cm2, comparable to the higher values seen in RTDs. The dashed line represents the expected J_P for the case of an emitter QW with electron density of $1x10^{12}/cm^2$.

Fig. 5. (a) Emitter-collector I-V characteristics of 3-layer DELTT EA339 at $V_{TC} = 0$ and several different temperatures. A strong negative differential resistance persists to 250 K. The PVR decreases at higher temperatures, primarily due to an increase in valley current. (b) Emitter-collector I-V characteristics of 3-layer DELTT EA338 at 273 K at several different gate voltages V_{TC}. Clear gate-control of the NDR is apparent close to room temperature.

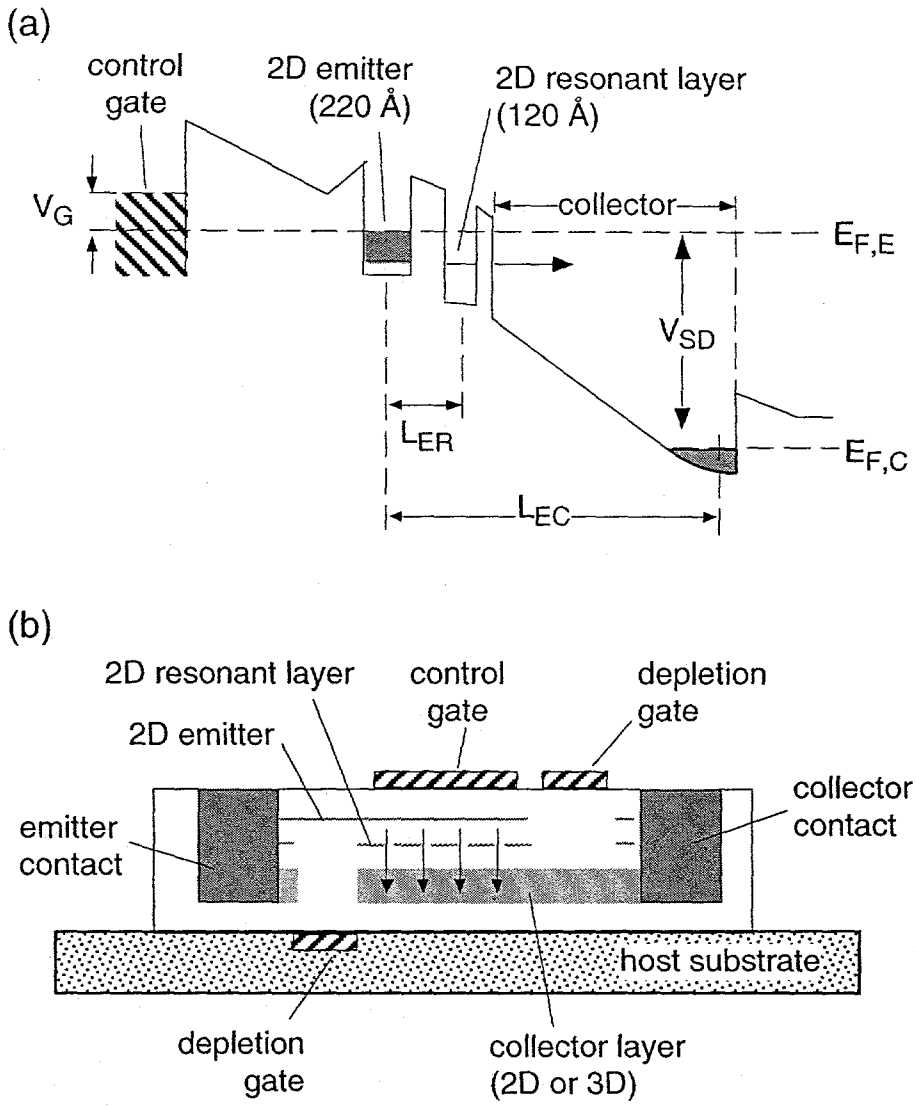
(a)
control gate
2D emitter (220 Å)
2D resonant layer (120 Å)
collector
V_G
$E_{F,E}$
V_{SD}
L_{ER}
$E_{F,C}$
L_{EC}
(b)
2D resonant layer
control gate
depletion gate
2D emitter
collector contact
emitter contact
host substrate
depletion gate
collector layer (2D or 3D)

Fig. 1

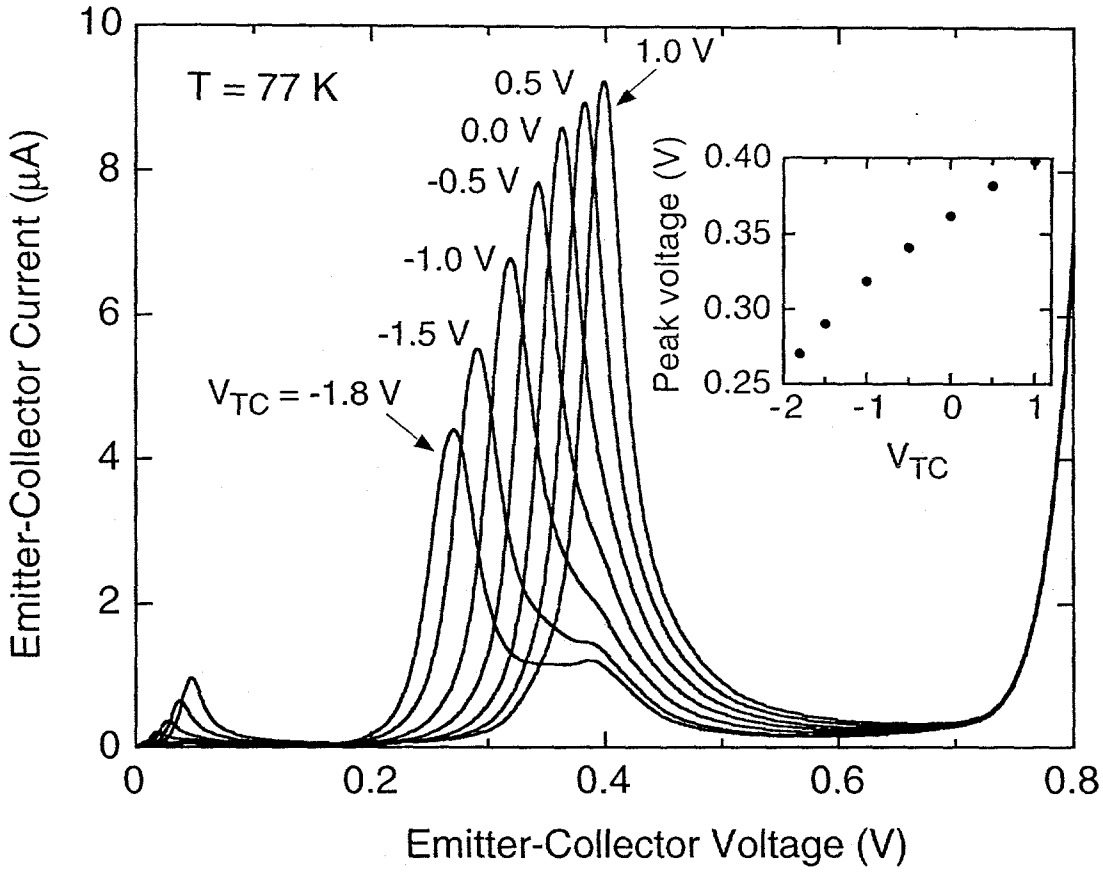
T = 77 K
1.0 V
0.5 V
0.0 V
-0.5 V
-1.0 V
-1.5 V
V_{TC} = -1.8 V
Emitter-Collector Current (μA)
Emitter-Collector Voltage (V)
Peak voltage (V)
V_{TC}
0
2
4
6
8
10
0
0.2
0.4
0.6
0.8
0.25
0.30
0.35
0.40
-2
-1
0
1

Fig. 2

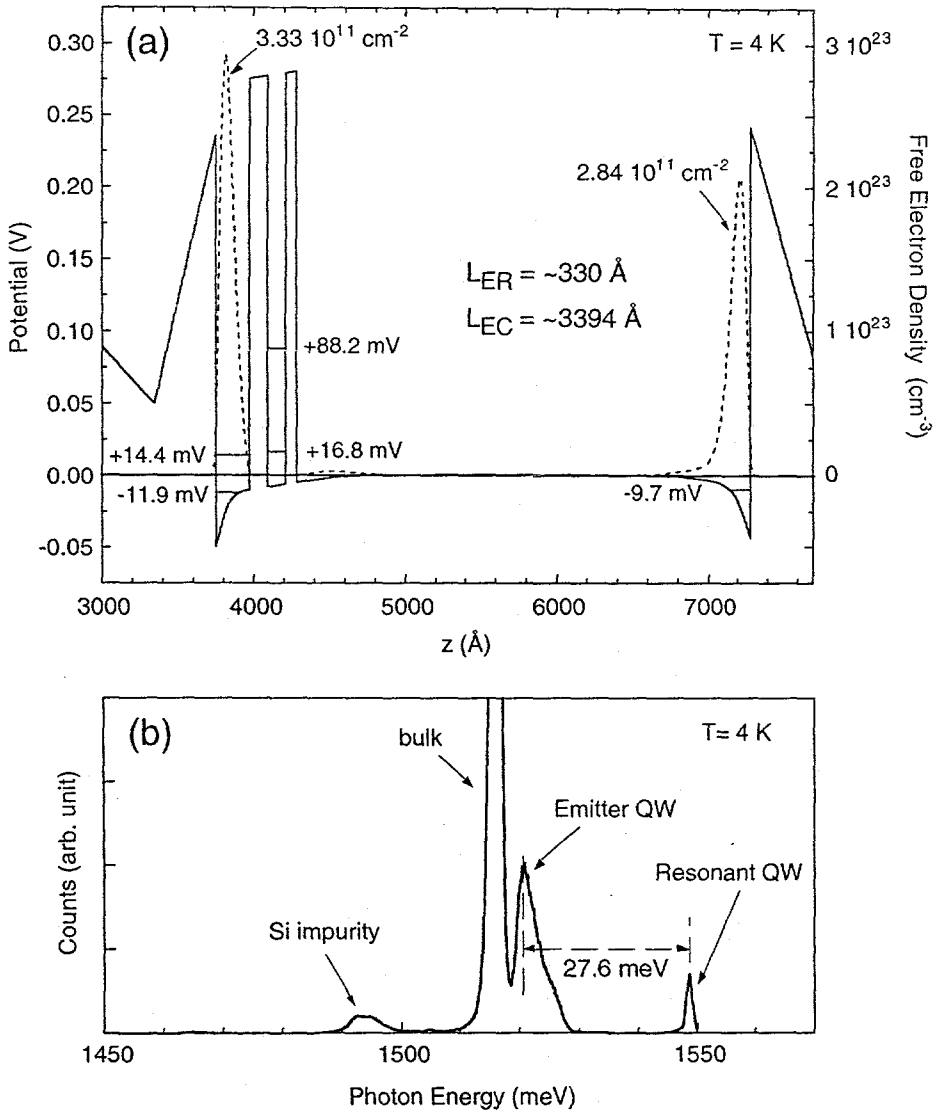
(a)
3.33 10^11 cm^-2
T = 4 K
2.84 10^11 cm^-2
L_ER = ~330 Å
L_EC = ~3394 Å
+88.2 mV
+14.4 mV
+16.8 mV
-11.9 mV
-9.7 mV
Potential (V)
Free Electron Density (cm^-3)
z (Å)
(b)
bulk
T= 4 K
Emitter QW
Resonant QW
Si impurity
27.6 meV
Counts (arb. unit)
Photon Energy (meV)

Fig. 3

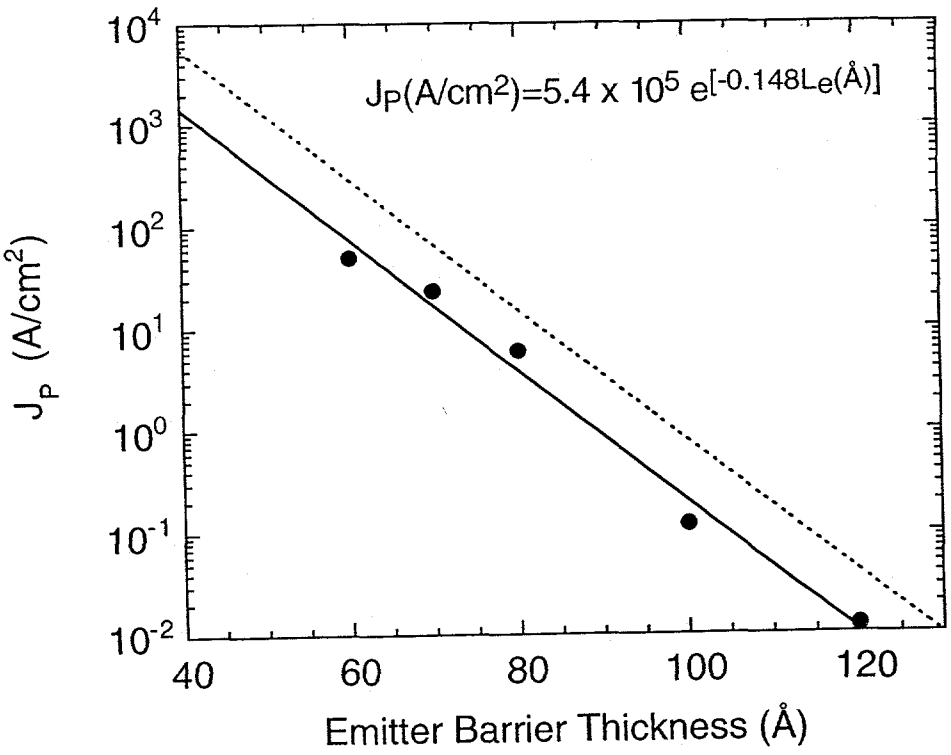
$J_P(A/cm^2)=5.4 \times 10^5 e^{[-0.148Le(Å)]}$
J_P (A/cm^2)
10^4
10^3
10^2
10^1
10^0
10^{-1}
10^{-2}
40
60
80
100
120
Emitter Barrier Thickness (Å)

Fig. 4

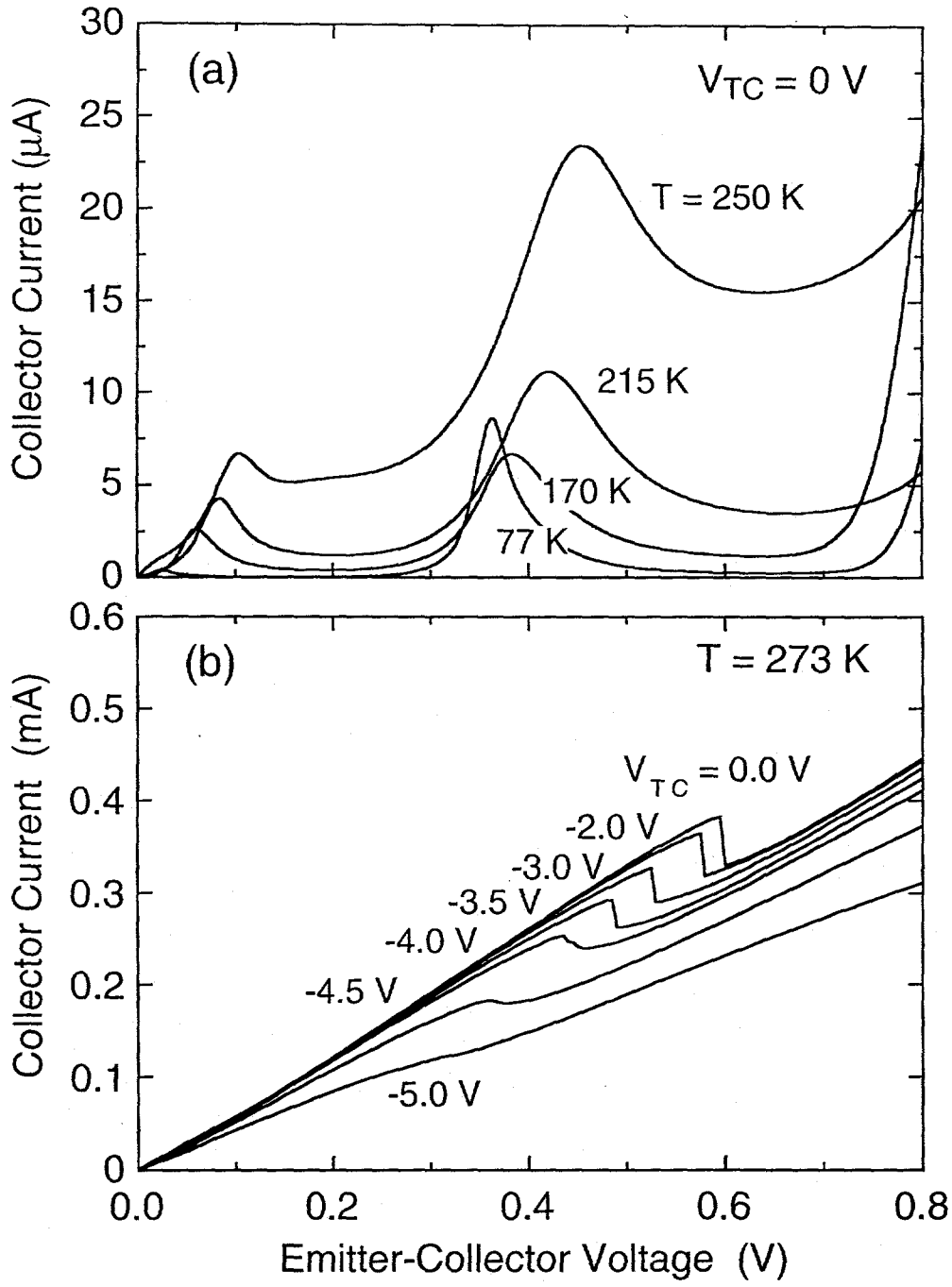
(a)
V_{TC} = 0 V
T = 250 K
215 K
170 K
77 K
Collector Current (μA)
30
25
20
15
10
5
0
(b)
T = 273 K
V_{TC} = 0.0 V
-2.0 V
-3.0 V
-3.5 V
-4.0 V
-4.5 V
-5.0 V
Collector Current (mA)
0.6
0.5
0.4
0.3
0.2
0.1
0
0.0
0.2
0.4
0.6
0.8
Emitter-Collector Voltage (V)

Fig. 5