

## Fabrication of Diffractive Optical Elements for an Integrated Compact Optical-MEMS Laser Scanner

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We describe the microfabrication of a multi-level diffractive optical element (DOE) onto a micro-electromechanical system (MEMS) as a key element in an integrated compact optical-MEMS laser scanner. The DOE is a four-level off-axis microlens fabricated onto a movable polysilicon shuttle. The microlens is patterned by electron beam lithography and etched by reactive ion beam etching. The DOE was fabricated on two generations of MEMS components. The first generation design uses a shuttle suspended on springs and displaced by a linear rack. The second generation design uses a shuttle guided by roller bearings and driven by a single reciprocating gear. Both the linear rack and the reciprocating gear are driven by a microengine assembly. The compact design is based on mounting the MEMS module and a vertical cavity surface emitting laser (VCSEL) onto a fused silica substrate that contains the rest of the optical system. The estimated scan range of the system is  $\pm 4^\circ$  with a spot size of 0.5 mm.

### INTRODUCTION

Micro-electromechanical systems (MEMS) is a primarily silicon-based technology that brings precision motion to the microscopic scale using batch fabrication processes developed as extensions from the silicon integrated circuit industry. Compared to the macroscopic systems whose functions they emulate, MEMS are smaller, lighter, lower cost, and more efficient (lower power consumption). For many applications, it is desirable to incorporate optical functions with MEMS. This requires a hybrid approach to integrate compound semiconductor-based light emitters and some form of microoptics, e.g., diffractive optical elements (DOEs), to create an integrated microsystem.

Integrated microsystems is an emerging technology in which electrical, optical, and mechanical functions are combined at the chip level into compact, lightweight, and [ultimately] low cost modules with performance equal to or even exceeding those of conventional macroscopic systems. The development of integrated microsystems is expected to revolutionize a broad range of fields, extending beyond electro/optomechanical systems to the fields of biology, chemistry and medicine. Just as the integrated circuit combines formerly discrete devices (transistors, resistors, capacitors) onto a single chip with increasing functionality at

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decreasing cost, the integrated microsystem combines formerly separate subsystems (electronics, photonics, optics, mechanics) onto a single multichip module. This results in significant size reduction and, hopefully, as the technology matures, to increased function with reduced cost.

One example of an integrated microsystem is the optical-MEMS laser scanner. Low-speed laser scanner systems (10-1000 Hz) can be used in a variety of applications including barcode scanners, video displays, laser print heads, optical data storage, and optical communication. Previous work<sup>1,2</sup> has used simple mirrors that tilt out of the plane of the wafer and rotate about an axis on torsion hinges. Potential problems with this technique include lack of flatness of the mirrors due to residual stress and mirror deformation during rotation. Additionally, these mirror-based systems use off chip laser sources and optics, and therefore do not qualify as fully integrated microsystems. The integration of MEMS and optics has been previously demonstrated in the form of a microoptical bench.<sup>3</sup> This demonstration, however, involved delicate manual assembly of hinged structures not suitable for large scale manufacture. The only microoptic demonstrated was a simple binary amplitude Fresnel zone plate with a maximum theoretical efficiency of less than 10%, inadequate for most applications.

Our approach is to assemble a MEMS module and a vertical cavity surface-emitting laser (VCSEL) onto a common fused silica substrate that contains the balance of the optical system. By fabricating the MEMS and VCSEL devices separately, the two components can be optimized independently and integrated later, providing greater design and manufacturing flexibility. The use of the fused silica substrate, flip-chip bonding and a custom precision die attach system greatly simplifies alignment issues in assembly. The compact optical design of this optical-MEMS laser scanner borrows heavily from previous work at Sandia on the “chem-lab-on-a-chip” that shares a similar architecture.<sup>4</sup> The design of the MEMS modules and overall system concept has been previously described.<sup>5</sup> The keys to the compact design of the Sandia system are the use of substrate-mode propagation for the optical path<sup>6</sup> and high performance DOEs for collimation of the laser beam. The unique aspect of the design is that the MEMS module contains a large polysilicon shuttle onto which a four-level binary optic is patterned. The shuttle is linearly

translated in the plane of the wafer, largely removing the potential for dynamic bending during operation. To our knowledge, this is the first demonstration of a multi-level DOE fabricated onto a MEMS.

In this work, we describe the microfabrication of a multi-level DOE onto a MEMS as a key element in an integrated compact optical-MEMS laser scanner. Lithographic challenges of the polysilicon DOE include submicron features (0.24  $\mu\text{m}$  minimum), non-planar topography on the MEMS, and issues of process compatibility. We also review the design concepts of the in-plane laser scanner and briefly describe the two generations of MEMS modules employed.

## DESIGN

The compact design of the optical-MEMS laser scanner is shown schematically in Fig. 1. Electrical contacts on the top surface of the fused silica substrate for the VCSEL and MEMS module are not shown. The leftmost DOE collimates the 680 nm wavelength VCSEL output beam and tilts the beam at a 25° angle off normal to the plane of the substrate. A mirror directs the beam to a second DOE, which in turn, focuses the beam in front of the shuttle DOE on the MEMS module. The focal point of this second DOE is chosen to maximize the scan range of the beam. The optical system is designed to give a beam diameter of 0.5 mm. The shuttle is linearly translated perpendicular to the plane of the page and the laser beam scans out of the plane of the page (forward and backward). All DOEs are coated with metal and operate in reflection. Note the extremely compact size of the assembly.

Two generations of MEMS modules were fabricated using the Sandia Ultra-planar Multilevel MEMS Technology (SUMMiT),<sup>7</sup> which is a four-level polysilicon MEMS technology. In the SUMMiT process, the sacrificial oxide below the fourth level of polysilicon is planarized using chemical-mechanical polishing (CMP), which removes the underlying topography from the shuttle surface and leaves a near optically flat surface. The SUMMiT process is optimized to reduce intrinsic stress and minimize roughness in the mechanical polysilicon layers. Typical surface roughness of the fourth-level polysilicon has been measured

to be on the order of 1 nm rms.

A shuttle from the second generation MEMS module is shown in Fig. 2 prior to patterning of the DOE. Shuttle dimensions are 1 mm by 0.5 mm. For maximum flatness and stiffness, the shuttle is fabricated out of three levels of mechanical polysilicon and has total thickness of 4.75  $\mu\text{m}$ . Flatness of a released shuttle was measured using a Wyco white light interferometer both before and after deposition of 8 nm Ti (for adhesion) and 50 nm Au. Prior to metal deposition, the shuttle was extremely flat. Measurements show an edge to center deflection (sag) of 0.16  $\mu\text{m}$  along the long axis of the shuttle and virtually no deflection across the short axis. After metallization, the deflection values increase to 0.56  $\mu\text{m}$  and 0.20  $\mu\text{m}$  for the long and short axes, respectively. For the design beam diameter of 0.5 mm, the aberrations introduced include 0.1 waves of astigmatism and 0.5 waves of defocus. These aberrations are small for the intended uses of this system. If necessary, the magnitude of the deflections could be reduced by optimizing the metal deposition for minimum stress or by compensating for the non-flatness in the design of the DOE. Etching of the relatively shallow profile DOE on the shuttle is not expected to have a significant effect on shuttle flatness.

The four etched crosses at the corners of the shuttle were included to serve as alignment marks for optical lithography post-processing. The 10  $\mu\text{m}$  width of the arms of the crosses is somewhat larger than desired for chip level marks used in electron beam lithography. Additionally, ‘global’ alignment marks, necessary for wafer-level alignment, were not included in the design at all. For these reasons, suitable metal marks were deposited in post-processing. This step could be avoided in the future by including appropriately sized etched marks in the MEMS design.

The first generation MEMS module uses a shuttle suspended on springs and displaced by a linear rack. The linear rack is attached to a rotary actuator, a type of microengine,<sup>8</sup> consisting of two orthogonal electrostatic comb drives operating 90° out of phase to convert the linear comb drive motion to rotational motion. In this design, the scan range of the shuttle is determined by the length of the linear rack and the number of revolutions of the microengine, within the limits

of the springs on which the shuttle is suspended. The first generation MEMS module contains a linear rack designed for a displacement of 100  $\mu\text{m}$ . This design has the disadvantage of requiring the microengine to reverse direction with each cycle of shuttle translation. This requires a more complex control signal and could result in less smooth and/or reliable operation. This design has also shown some tendency towards early failure attributed to wear debris fouling the linear rack. A second, more robust design was therefore developed.

The second generation MEMS module uses a shuttle guided by roller bearings and driven by a reciprocating arm linked to a single rotating gear. The gear is driven by a rotary actuator, but in this case, the actuator runs in a single direction. In this design, the scan range of the shuttle is determined by the diameter of the output gear, which in this case is designed to give a 100  $\mu\text{m}$  displacement. Preliminary testing indicates that this design will have superior reliability compared to the first generation design. This design is also extendable to scanning in two dimensions.

The design of the shuttle DOE is the same for each MEMS module. The DOE is a relatively simple off-axis lens, 0.7 mm by 0.5 mm in size. The DOE is designed for a wavelength of 680 nm and operates in reflection. The lens is implemented in four-levels (two etch steps) for a maximum theoretical efficiency of 81%, deemed adequate for this demonstration. This DOE produces a collimated beam output beam that is perpendicular to the substrate when the shuttle is at its center of travel. The shuttle DOE has a focal length of 700  $\mu\text{m}$  and a total travel of 100  $\mu\text{m}$ , resulting in a total scan angle of 0.14 radians or  $\pm 4^\circ$ . The optical system is diffraction limited on axis with a resulting spot size of 0.5 mm. The fabrication process is described below.

## FABRICATION

Fabrication of the shuttle DOE begins after completion of the SUMMiT processing of the MEMS modules but before release (removal of the sacrificial oxide). This provides a stable working surface and protects the MEMS structures from particle contamination or other damage. The MEMS modules are received from the foundry encased in oxide which must be removed

from the shuttle where the DOE is to be written and from the bond pads where metal is to be deposited. The opening of these windows in the oxide is accomplished with optical lithography and a buffered oxide etch. As mentioned previously, two sets of Cr/Au alignment marks were defined on each MEMS module prior to beginning the electron beam lithography levels.

The electron beam lithography is performed on a JEOL JBX-5FE thermal field emission system operating at 50 kV. Lithographic challenges of the DOE include submicron features (0.24  $\mu\text{m}$  minimum lines and spaces) and non-planar surface topography outside the shuttle window. Electron beam lithography is well suited to this task. While not a low-cost technique, it is the most efficient and productive during the development phase.

The process sequence for DOE fabrication is now described. The beam current used is 5 nA with a corresponding beam diameter of approximately 12 nm. The addressed pixel spacing is 15 nm in a 70  $\mu\text{m}$  field. The resist used is polymethylmethacrylate (PMMA) at a thickness of 200 nm for the first level (the finer level) and 400 nm for the second level (the coarser level). The resist thickness for the second level is increased to provide better step coverage on the first level etched features and because the feature sizes do not require a thinner resist. Both lens levels receive a dose of 400  $\mu\text{C}/\text{cm}^2$  and total exposure time per lens per level is 3 min. The PMMA is developed for 70 seconds in a 1:3 solution of methyl isobutyl ketone and isopropyl alcohol, followed by an isopropyl alcohol rinse. Even though the required etch depths are shallow, 85 nm and 170 nm for the first and second level etches, respectively, the patterned PMMA was not used as an etch mask directly. Instead, a metal etch mask consisting of 5 nm Cr/60 nm Ni was deposited by electron beam evaporation followed by liftoff in acetone. Etching is performed using reactive ion beam etching<sup>9</sup> with a Cl<sub>2</sub> chemistry. Desired etch depths are achieved by timed etches based on system calibration. Typical etch times are in the range of 2.5-5 minutes.

Two scanning electron micrographs of the completed DOE are shown in Fig. 3. Fig. 3(a) shows the central-edge portion of the DOE fabricated on the polysilicon shuttle prior to release and Au blanket evaporation. The arrows indicate the axis of shuttle movement. Fig. 3(b) shows

a portion of the DOE in more detail, showing the four-level Fresnel zones. The perforations in the shuttle are to facilitate the release etch by allowing the etchant to attack the sacrificial oxide beneath the large shuttle. Based on percentage of areal coverage, the release holes are expected to cause a reduction in efficiency of only 2%. The holes do not interfere significantly with the lithography. Methods are being considered that would allow release to occur from the backside of the shuttle therefore eliminating the need for the release holes.

After completion of the shuttle DOE, the MEMS module is ready for release, which is the removal of the sacrificial oxide layers. Release is performed by immersion in a 1:1 solution of hydrofluoric acid and hydrochloric acid for 90 min. After a series of cleaning steps, the module is ready for the critical steps of drying and self-assembled monolayer coating. In the final step, the MEMS module is coated with 8 nm of Cr (for adhesion) and 50 nm of Au, which is performed as a blanket evaporation. The bondpads and electrical leads to the comb drives are designed with overhanging ridges in the top polysilicon layer to prevent shorting. Unfortunately, in the few MEMS modules processed, functional devices were not obtained. The cause of the failure is attributed to particle contamination in the linear rack and gear assemblies. MEMS are inherently sensitive to particle contamination and the laboratory in which the post-processing is performed is only Class 100 compared to the foundry where the MEMS modules are processed which is a Class 1 facility. We believe that there is nothing inherent in the DOE post-processing that will preclude obtaining functional devices in the future once refinements to the release process are made. These include improved cleaning procedures, dedicated equipment, and reduced laboratory particle counts, each of which is being pursued.

## SUMMARY

We have demonstrated the first ever microfabrication of a multi-level DOE onto a MEMS module as a key element in an integrated compact optical-MEMS laser scanner. The DOE is a four-level off-axis microlens fabricated onto a movable polysilicon shuttle using electron beam lithography and reactive ion beam etching. The incorporation of the DOE onto the MEMS

shuttle allows for a design based on in-plane movement and avoids the flexure concerns of designs based on out of plane movement. The use of high performance DOEs and hybrid assembly of the MEMS module and a VCSEL onto a fused silica substrate enables achievement of an extremely compact design. The integration of high performance microoptics and MEMS is a significant step forward along the path to achieving a wide range of integrated microsystems.

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## FIGURE CAPTIONS

Figure 1. Schematic cross section along the optical path of the compact optical-MEMS laser scanner. The leftmost DOE collimates the VCSEL output beam and tilts it 25° off normal. A mirror directs the beam to a second DOE that focuses the beam in front of the shuttle DOE on the MEMS module. The shuttle is translated perpendicularly to the plane of the page and the laser beam scans out of the plane of the page (forward and backward). All the DOEs are coated with Au and operate in reflection.

Figure 2. Scanning electron micrograph of a shuttle from the second generation MEMS module prior to patterning of the shuttle DOE. Shuttle dimensions are 1 mm by 0.5 mm. For maximum flatness and stiffness, the shuttle is fabricated out of three levels of mechanical polysilicon and has a total thickness of 4.75  $\mu\text{m}$ .

Figure 3. (a) Scanning electron micrograph of the central-edge portion of the DOE fabricated on the polysilicon shuttle on the MEMS module prior to release and Au metal deposition. The axis of shuttle movement is indicated by the arrows. (b) Detail showing the four etch levels and Fresnel zones. The perforations facilitate the release etch that removes the sacrificial oxide layers and frees the shuttle for movement.

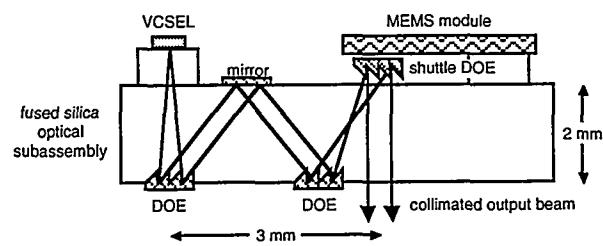


Fig. 1  
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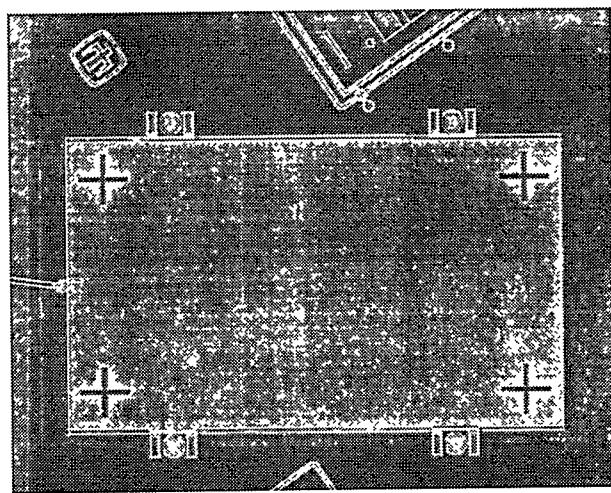
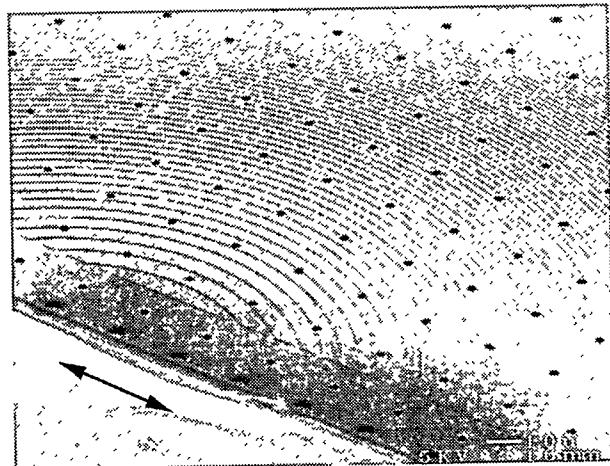
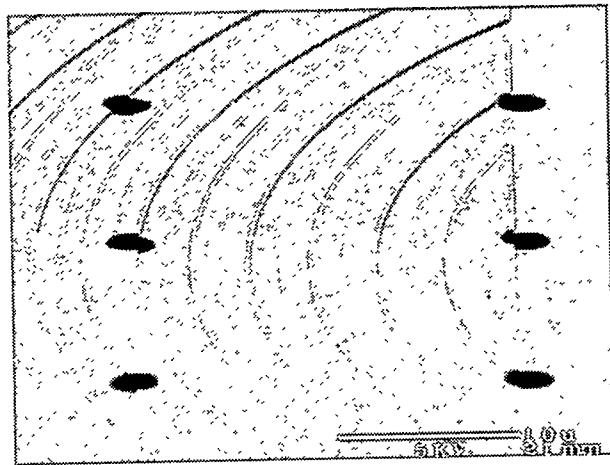


Fig. 2  
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(a)



(b)

Fig. 3  
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