LAWRENCE
LIVERMORE
NATIONAL
LABORATORY

LLNL-TR-747341

Semiconductor Manufacturing Modeling Final Report CRADA No. TC-1069-94

M. J. Fluss, R. Goosens

March 6, 2018

Disclaimer

This work performed under the auspices of the U.S. Department of Energy by Lawrence Livermore National Laboratory under Contract DE-AC52-07NA27344.

Semiconductor Manufacturing Modeling

Final Report
CRADA No. TC-1069-94

Date: 12/30/97 Revision: 3

A. Parties

The project is a relationship between the Lawrence Livermore National Laboratory (LLNL) and Semiconductor Research Corporation

University of California
Lawrence Livermore National Laboratory
7000 East Avenue, L-795
Livermore, CA 94550

Semiconductor Research Corporation
1101 Slater Road
Durham, NC 27703

B. Project Scope

The program is divided into four (4) project areas.

1. Bulk Processing (Implant and Diffusion)

The Semiconductor Industry Association (SIA) roadmap projection for 1 GHz on-chip clock speeds and 64 Gbits/Chip DRAM technology by the year 2005 requires scaling the minimum feature size of CMOS devices down to 100nm. This requirement has profound implications for device processing. Lateral broadening of source/drain junctions caused by transient enhanced diffusion of implanted dopants during Rapid Thermal Processing will be a critical process limiting the development of these new technologies. As these constraints begin to limit device integration and characteristics, existing processing techniques must increasingly be understood quantitatively and modeled with unprecedented precision. Indeed, revolutionary advances in the development of physics-based process simulation tools will be required to achieve the goals for cost efficient manufacturing required by the SIA roadmap, and to satisfy the needs of the defense industrial base. These advances will necessitate a fundamental improvement in our basic understanding of microstructure evolution during processing, and this can only be obtained through the development and validation of advanced physically-based predictive materials modeling computational tools. The work in this CRADA addressed these concerns directly, and the results will therefore greatly benefit the US semiconductor manufacturing and defense industries by aiding in the reduction of the time-to-market cycle, and by making it possible to substitute many high cost empirical design steps in manufacturing with much lower cost Technology Computer Aided Design (TCAD) processes.

2. *Interconnects*

Metallization

In addition to front-end-of-line (FEOL) issues, we also addressed thin film deposition associated with back-end-of-line (BEOL) metallization through the development of lattice-based Monte Carlo methods. This work was carried out in very close collaboration with George Gilmer at Lucent Technologies.

The difficulty in developing predictive models for thin film deposition is three fold: (1) lack of full understanding of the underlying physical processes, (2) lack of experimental data capable of distinguishing clearly between possible mechanisms, and (3) lack of simulators incorporating these models so that they can be tested against the experimental data. All three components are necessary if we are to develop the foundation required for predictive models. Thin film growth mechanisms are sufficiently complex that it is only through implementation in a simulator that they can be compared and evaluated against experimental observations.

The prospect of using atomistic computer simulations to model polycrystalline thin film growth in three dimensions has been a beckoning yet elusive goal. However, progress achieved in computational physics for accurate interatomic potentials, coupled with vast improvements in computational power and algorithms, have brought the possibility of computing microstructure evolution during growth to reality. This has large implications for the development of predictive deposition modeling tools for microelectronics applications.

Electromigration

This CRADA work seeks a fundamental understanding of important characteristics of electromigration (EM) in metal films. EM causes damage to metallic interconnects and may eventually limit the reliability of integrated circuits. Many qualitative and quantitative features of EM are incompletely understood; this lack of knowledge may result in design or manufacturing inefficiencies. Interconnects are known to support large mechanical stresses that inhibit EM, but existing models based on this effect may be inconsistent with observations. Interconnect durability can also be enhanced by dilute alloying, which raises the activation energy for grain boundary diffusion. The microscopic mechanism for this effect is not understood. We examine these effects at the level of the microscopic vacancy-solute-dislocation interactions.

3. *Etch*

As feature sizes on Si wafers continue to decrease, traditional design approaches based on trial experiments become prohibitively expensive. Therefore, one of the goals of the present SRC CRADA has been to help semiconductor manufacturers develop accurate and predictive topographic simulation tools by elucidating and quantifying the fundamental physical processes which occur at the gas-surface interface. The system that we have studied is Cl-Si, as Cl is one of most important regents in very-large-scale integrated circuit technologies such as etch and chemical vapor deposition.

4. *Ab Initio Computations*

The present CRADA has sought to improve critical fabrication processes such as doping, deposition, and etching by the use of computer simulations. In many cases, these simulations depend on *fundamental materials characteristics* which are incompletely known, and so an important adjunct of this effort has been the determination of these properties from first principles calculations. One obvious example is interatomic force laws, without which it is not possible to move atoms about in the course of the time evolution of a simulation. These interactions arise fundamentally from the atomic electron clouds, and rigorous electronic structure techniques have made great strides in this CRADA at understanding the diffusion of dopants in Si as well as the

halogen etching of Si surfaces.. These techniques, however, are limited to relatively small systems, e.g., one or two dopant-atom clusters in Si. One of the goals in this CRADA was therefore to develop less expensive "tight-binding" techniques for defining the various interatomic force laws between dopant, etchant, and Si atoms.

C. Work Plan

An extensive project work plan was developed by SRC, LLNL, SNL, and LANL. This is part of the overall CRADA agreement for each DOE Laboratory. Unfortunately, funding was made a levels significantly below the work plan. As a result continuous changes in level of effort were undertaken after consultation with SRC and where appropriate with LANL or SNL (when LLNL was providing input to their projects). The primary vehicle for these changes were the review meetings organized by SRC during the period of the CRADA. All milestones set out for the first two years of the program were met by LLNL scientists. A new project in interconnects was initiated but only operated for ~ 5 months prior to termination of the CRADA.

D. Benefits to DOE and Industry

Any comprehensive theoretical program must focus not only on the specific milestones of the projects at hand, but also on extending capabilities and building the tools of the future. Significant development under previous funding sources at LLNL had already gone into the plane wave-based electronic structure techniques which were available "off the shelf" for such successful use on the present CRADA. Large-scale atomistic simulations are now, however, limited by the computational cost of obtaining accurate interatomic force laws, and it is towards this critical future capability that the present tight-binding work was directed. These improvements in capability are of generic value to both DOE and industry, deriving their specific value in actual applications. For example, the techniques developed in this CRADA for B/Si interactions are equally applicable to the improvement of Pu interactions of great interest to DOE. While the problem of automatically generating tight-binding force representations has not been solved in this work, the new techniques developed here will greatly facilitate understanding of the "transferability" problem which has so far help up the achievement of this goal.

We have provided a critical new insight into the importance of including the effect of Cl coverage on Si surface reactivity. This insight as well as the new mechanism we have proposed can both be incorporated into the Sandia-developed CHEMKIN chemical kinetics code used by the semiconductor industry, thus enabling more accurate simulations of the etching process.

The proposed explanation for threshold behavior in EM may resolve some long-standing questions about EM mechanisms. Improved understanding of these fundamental processes could lead to advances in manufacturing of integrated circuits. At the least, it provides increased confidence in the treatment of this problem. This is relevant to the management of semiconductor device reliability by both industry and DOE. The issue of solute effects on fast diffusion paths in metals is of great interest for interconnect design and manufacture as well as for understanding and modifying the mechanical properties of metals in general. A thorough microscopic understanding of this effect is of importance to DOE programs such as ASCI.

E. Technical

1. General Approach

Molecular Dynamics and Monte Carlo

At present, there exist process simulators, based on continuum partial differential equation approaches, that can predict dopant and defect behavior using a set of assumptions concerning the atomic mechanisms involved. What is not known is the exact form that these assumption should take (e.g., the source term for dopant diffusion), and how to determine parameters in the models based on these assumptions. Experimental measurements are very difficult because the mechanisms may only be inferred indirectly, and many mechanisms may sometimes be used to explain the same observation. To overcome these difficulties, process simulators based on a physical understanding of the relevant phenomena are required. These process modeling tools must be capable of simulating the dopant implantation and diffusion during annealing for time scales of the order of seconds, but need physical input, i.e. the source term for diffusion, obtained from processes that take place in time scales ranging from picoseconds to milliseconds or longer.

The project relied on a wide variety of theoretical and simulation methodologies, all of which are widely used in the Department of Energy weapons laboratories for the purpose of designing materials from the atomic level up. At the highest level of the energy scale, classical methods based on the Binary Collision Approximation (BCA) were coupled to model-potential molecular dynamics simulations (MD). In this manner, the dopant distributions, the 3D distribution of resulting damage, and the short-term annealing kinetics (microseconds) of the primary damage microstructure were investigated. The evolution of the dopant distribution and the damage microstructure to length and time scales relevant to manufacturing processes was modeled with kinetic Monte Carlo (kMC) defect hopping codes. These MC calculations used Boltzmann factors (e.g. defect migration and formation enthalpies, cluster binding energies, etc.) obtained from *ab initio* and tight binding molecular dynamics (TBMD) calculations to describe the kinetics of defect and dopant diffusion during implantation and annealing.

Tight Binding

Tight-binding techniques are essentially fast, parameterized electronic structure calculations. Typically these parameters are determined by massive non-linear minimization algorithms which seek to summarize a large data base of ab initio calculated total energy and possibly force relations. For binary (e.g., Si/B) and more complex systems, these minimization approaches become more and more unmanageable. Therefore, in the course of this CRADA, we have developed a practical computational method whereby a large subset of the required parameters may be directly calculated. The method may be used by any band structure technique formulated in, or which can be projected onto, a localized basis. Application was made to the binary B/Si system of importance to both dopant diffusion and deposition thrusts of the CRADA.

2. Specific Challenges

Transient Enhanced Diffusion

Transient enhanced diffusion (TED) of ion implanted Boron in silicon has been a subject of significant interest over the last few years, and is one of the key issues that threatens the applicability of ion implantation and rapid thermal annealing technology to future generations of semiconductor devices. One of the key detrimental aspects of boron TED is the fact that reactions between boron atoms and silicon self interstitials often lead to boron clustering in the peak region of the implantation profile. The boron in these clusters is not substitutional and therefore is not electrically active. In addition, the reverse short channel effect induced by boron TED under the channel is also of concern.

While much experimental progress has been made recently by SRC companies such as Lucent technologies and Intel Corporation in understanding the nature and magnitude of TED, at the time of initiation of this CRADA there was relatively little understanding of the fundamental physical parameters and reactions that control the process. Consequently, the development of computer simulation models that can predict Boron TED for a set of arbitrary implantation energies, doses, dose rates, and annealing protocols and temperatures has proven difficult. Recent kinetic Monte Carlo (kMC) computer simulations of Boron TED such as those presented by the Bell laboratories group are mostly based on empirical parameters derived from fits to limited sets of experimental data. These models can not be readily used to understand boron TED behavior for experimental conditions far from the region of the fit. Continuum models based on solutions to a set of coupled diffusion equations are even coarser in their description of the actual physical phenomena. For example, these models assume that after the implant step all the interstitials are immediately stored in the form of {311} extended defects and ignore all the physical details associated with more complex reactions, including the possible effects of the vacancy population during the early stages of the anneal, or the kinetics associated with the various microscopic boron-interstitial clustering reactions.

Here we describe a new, fully atomistic kMC model for boron transient enhanced diffusion in silicon. The input database for the kMC simulations is taken mostly from the results of first principles calculations. Our results predict that during annealing of 40 keV boron implantation profiles at 800 C, there exists a time window over which all boron is substitutional and therefore electrically active. At earlier or later times, point defect and boron diffusion results in boron clustering with the consequent build up of an inactive boron fraction. We show that this model, with the set of calculated parameters described below, can describe boron TED in silicon over a very wide range of experimental conditions without fits to experimental profiles or parameter adjustments.

\In all previous investigations of TED in silicon, the input database for the kMC simulations was mostly taken from limited sets of experimental data and largely determined from phenomenological fits to these data. In our case, the input for the kMC simulations is obtained from a combination of *ab intio* planewave pseudopotential calculations for defect, dopant (boron) and impurity (carbon) energetics and diffusion in silicon, tight binding molecular dynamics (MD) simulations for vacancy cluster binding energies, Stillinger-Weber potential-based MD simulations for interstitial and vacancy diffusion in silicon, and where possible, experimental data. This approach obviates the need for empirical fits to limited experimental data, and as we will demonstrate below can predict boron TED under a wide variety of conditions with high accuracy and without a need for re-fitting of the parameter set.

Room temperature ion implantation is modeled as a two-stage process. Each ion track is simulated using the binary collision approximation (BCA) code UT-MARLOWE from Al Tasch's group at the University of Texas-Austin. The three-dimensional defect and dopant distribution thus obtained is taken as input for the full kMC model. For each ion track, diffusion of all the species is allowed to occur for a time determined by the chosen implantation dose rate. When the final dose is achieved, the resulting three-dimensional defect, dopant and impurity distributions are taken as input for a new kMC simulation of the thermal annealing process.

Details of the *ab intio* and other first principles calculations have been published in the literature (see reference list below) and a summary is presented in Table 1. The table contains all the point defect and boron clustering reaction energies, as obtained by the LLNL group. Also shown in the table is data for vacancy and interstitial cluster binding energies as a function of size (n), and data on the diffusivity of silicon point defects which was obtained by LLNL in collaboration with Lucent Technologies. In the simulation results presented below, no adjustments have been made in any of the quantities presented in the tables in order to fit experimental data. It is interesting to note

that based on the results of the *ab initio* calculations, boron clusters containing three boron atoms and one silicon self interstitial appear to be very stable.

Figure 1a shows a one-dimensional boron profile following room temperature implantation in silicon at 40 keV to a dose of $2x10^{14}$ ions/cm^2 at a dose rate of 10^{12} ions/cm^2/sec . The black line is experimental data provided to us by Martin Giles from Intel Corporation. The simulations, which as described above use a combination of UT-MARLOWE and the kMC calculations to model the profile, are in excellent agreement with the experimental data. In addition, the results also provide information on the fraction of boron in substitutional lattice sites, and the fraction in inactive boron-interstitial clusters and other complexes. The computed fraction of active boron on substitutional lattice sites after room temperature implantation is 56%. The rest of the boron is in the form of bound boron-interstitial pairs (BI pairs) and clusters containing two self-interstitials and one boron atom (BI2 clusters). It is also interesting to note that after implantation all the vacancies are in clusters, but 90% of the self-interstitial atoms are not.

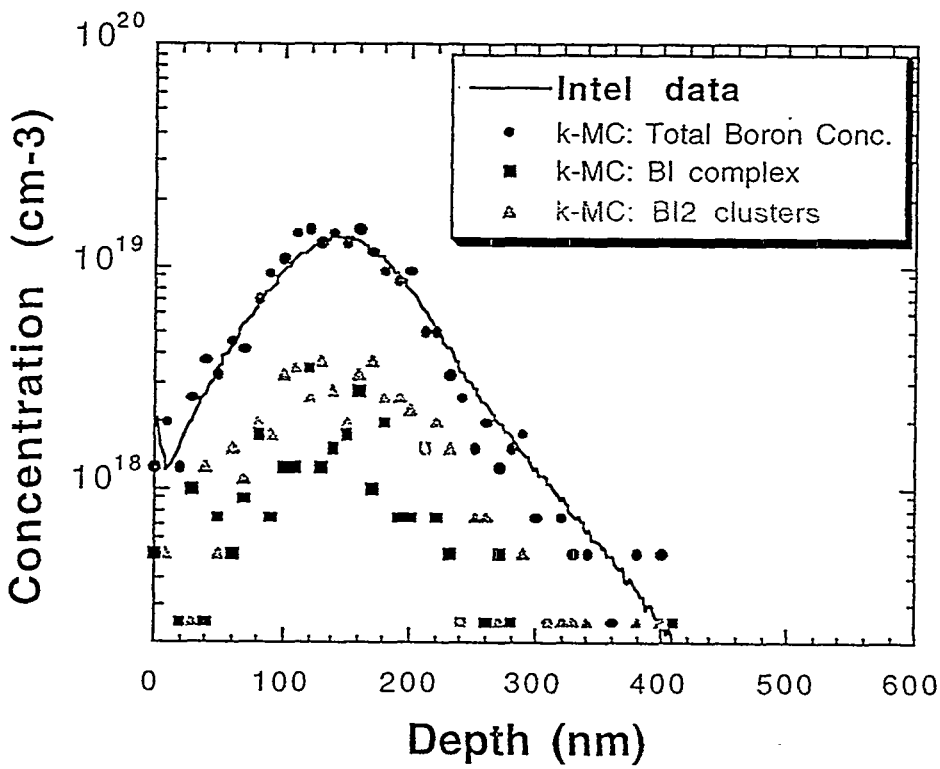


Figure 1. Experimental (black line) and simulated (red dots) profiles of 40 keV B as-implanted in silicon at room temperature to a dose of $2x10^{14}$ cm^{-2}. The figure also shows the fraction of boron in electrically inactive complexes after the implant.

Following the room temperature implant, we carry out an annealing simulation at 800 C. Figure 2a shows the time history of the populations of substitutional boron and boron-interstitial (B-I) complexes of various sizes and compositions during the anneal. Most interesting is the fact that for times between 10^{-2} s and 10 s all the boron is substitutional at least for concentrations above the resolution of the kMC simulation which is of the order of 10^{12} cm^{-3}. At early times ($t<10^{-2}$ s), small BI, BI2, and B2I (two boron atoms and one silicon self interstitial) complexes dissolve leaving behind a boron substitutional atom mainly through interaction with the mobile vacancy flux.

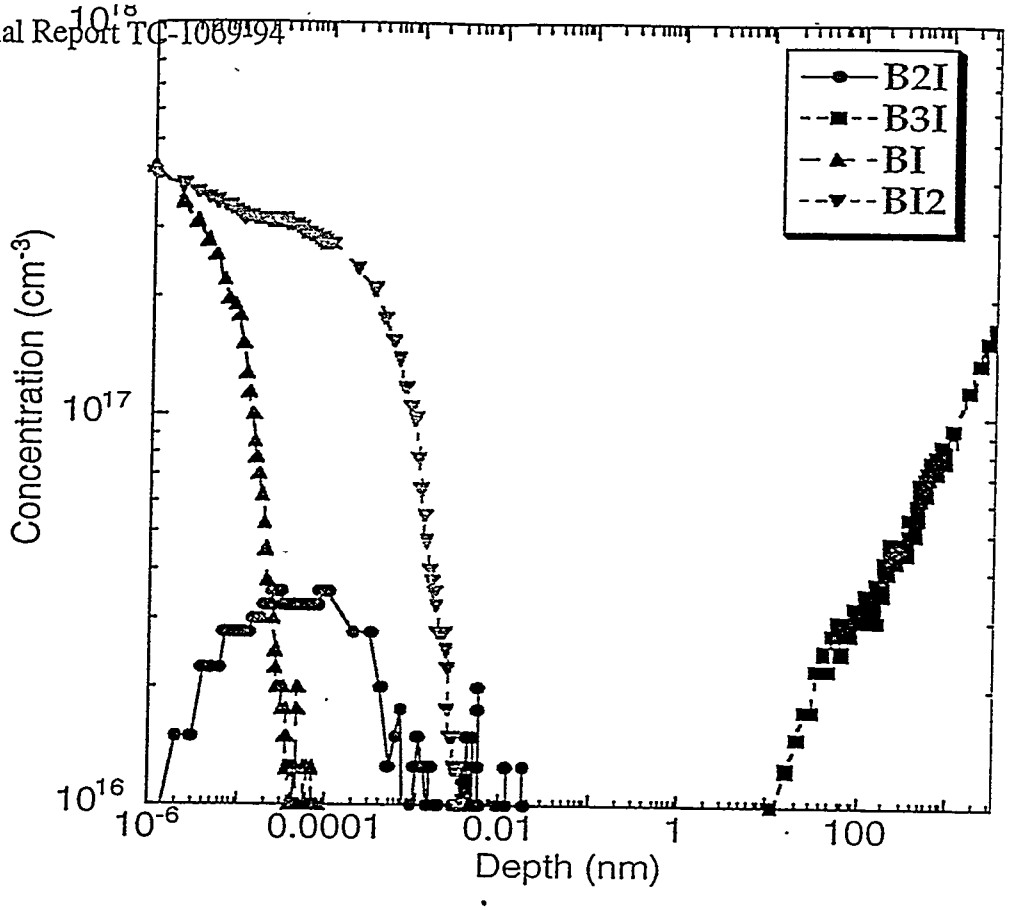


Figure 2. Time history of the inactive boron fraction. Between 10^{-2} s and 10 s, all the boron is in substitutional lattice sites.

During this time, the boron substitutional fraction increases from about 56% immediately after implantation at room temperature to 100%. This substitutional boron fraction remains constant between 10^{-2} and 10 s.

It is interesting to note that at early times during the anneal, the defect concentration is about two orders of magnitude higher than that of boron. The vacancies dissolve readily from the clusters at these temperatures, as discussed by Bedrossian et al on the basis of STM experiments and kMC simulations. After approximately 10 sec all the vacancies have disappeared from the lattice either through recombination with self-interstitials, with the B-I complexes described above, or with the surface. Concomitant with this lack of vacancy recombination sites for mobile self-interstitials, two things happen: an increase in the average interstitial cluster size, and an increase in the number of boron interstitial complexes. As the population of boron interstitials increases, the fraction of substitutional boron decreases and stable B3I complexes that contain three boron atoms and one silicon self-interstitial form.

After all the vacancies disappear, the remaining self-interstitials cannot recombine with vacancies, and this drives a very large increase in the average interstitial cluster size. Notice that contrary to current folklore, and in agreement with observations by Cowern et al, a large fraction of the boron TED occurs not when the largest interstitial clusters ({311}'s) dissolve, but rather all through the time while the interstitial clusters are growing and dissolving.

The kMC simulations afford a very rich and detailed description of the time history of the TED process. However, the results of the calculations are at best only as reliable as the accuracy of the input database. In order to check the reliability of our simulations under widely different conditions, we have carried out a very extensive set of investigations comparing experimental and a

simulated profiles of 40 keV room temperature implanted boron after annealing at 700, 800, and 900 C for various times. The agreement between the experiments and the simulations is excellent. Figure 3 shows boron profiles following 800 C anneals for 60 s and 60 minutes.

Al Thinfilm Deposition

Our new kinetic MC simulator, MC-Poly, includes the formation and coarsening of grain boundaries in polycrystalline thin films during deposition and the effect of these boundaries on surface and microstructure evolution. Grain boundaries form at the surfaces where clusters of atoms merge with one another and are included by assigning atoms in the vicinity of the boundaries an extra potential energy. Again, the GB energies are calculated by MD. Since most high angle, random boundaries have approximately the same energy, the first approximation for these energies is to assume a constant value, except at certain values of the crystalline orientations where special boundaries are formed. Moreover, it is also important to derive information on stress levels across various grain boundaries and the effect that this may have on bond energies at and near the boundaries. To study stress effects, MD simulations will be performed to calculate site energies as

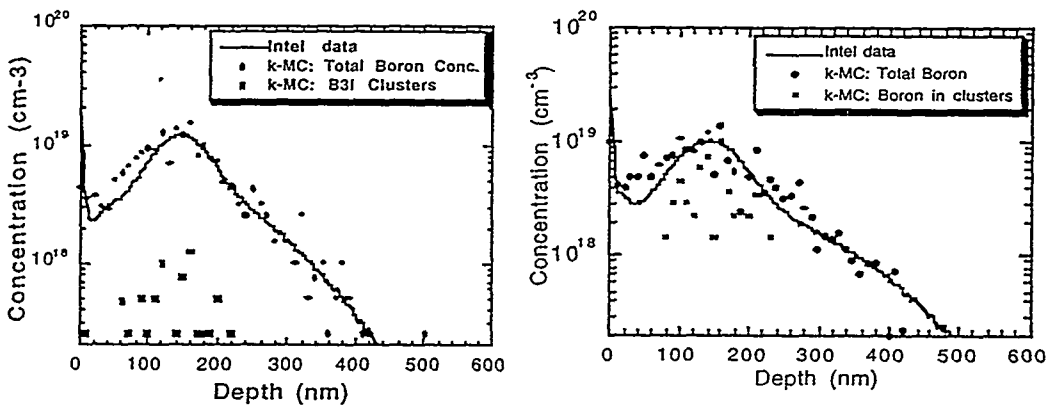


Figure 3. Experimental and simulated boron profiles following 800 C anneals at two different times. The agreement between Intel's experimental data and the simulation results in excellent.

a function of strain. In a typical MD simulation, a three dimensional GB energy surface is generated for two degrees of freedom (two rotation angles). The other three degrees of freedom at are fully relaxed via constant temperature and pressure MD. At the same time, the activation energy for GB diffusion can also be obtained as a 3D surface.

To demonstrate the predictive power of our simulator, we illustrate the role of shadowing during deposition of thin films at steps and other substrate inhomogenieties, such as the sputter deposition of Al into vias and trenches that is used in order to form electrical connections between different levels of metal in microelectronics manufacturing. Using the kinetic energies and angles of sputtered particles calculated by MD, and a simple single crystal implementation of our 3D MC simulator, we have investigated the role of shadowing on the filling of vias and trenches during Al deposition. A three-dimensional trench or via is constructed by placing substrate atoms at the appropriate sites. The simulation of sputter deposition proceeds by selecting one of two events, injecting a sputtered atom, or selecting a film surface atom for a diffusion jump. The relative probability of selecting one of these events depends on the conditions being simulated. In particular, it depends on the ratio of the flux of sputtered atoms to the surface diffusion hop frequencies and surface configuration. Sputtered atoms are injected at random positions in a plane above the substrate and are assigned angles selected randomly from the calculated distribution. The MC model moves atoms from the starting plane along the chosen trajectories in small increments until they reach a site of the lattice that has at least one neighboring site that is occupied by a film or

a substrate atom. The atom is placed at this position, and a new event is selected. Surface diffusion hops are performed by selecting a surface atom from a bookkeeping list using the random selection scheme described above, and moving it to a neighboring empty site up to the third neighbor distance. Atoms in different coordination sites on the surface are selected with different probabilities, based on their coordination number and the energy of an atom in that site and the diffusion barrier, as discussed in detail above in the description of the MC model. The trench and via cross-sections in Fig. 4 illustrate the morphology of the deposited films. Although the deposition conditions are identical, shadowing is more pronounced in the case of deposition onto the via, and better bottom coverage is achieved for the 3D trench. There is a tendency with large deposition rates or slow diffusion to form shoulders at the top of these structures and to leave a void region or a crevice. Fast surface diffusion, or a slower deposition rate is required to keep trenches and vias from deepening as more material is deposited. Our approach provides a very powerful tool for predicting the conditions under which thin film deposition results in high quality step coverage, and a "phase diagram" of the predicted deposition conditions for which a trench would fill or undergo void formation can be obtained.

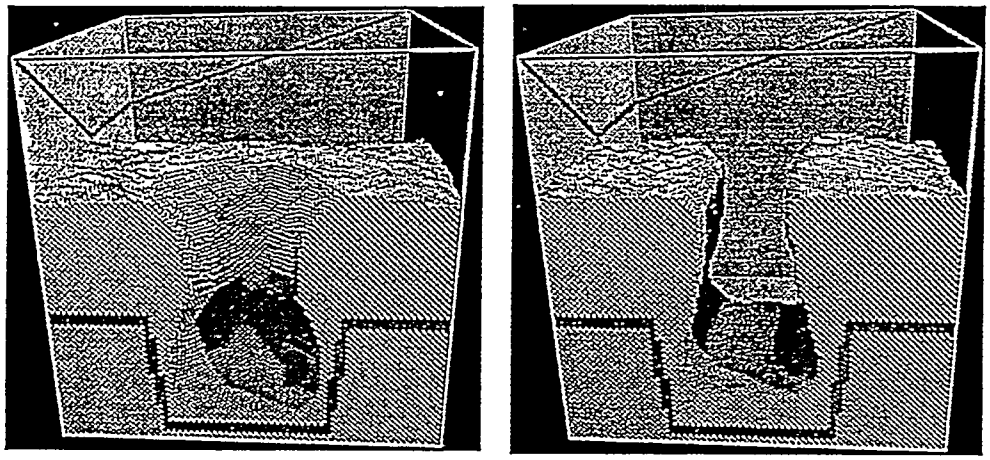


Figure 4. Via (a) and trench (b) cross-sections obtained for sputter deposition of Aluminum with our MC simulator

Electromigration

EM occurs when electrical currents dissipate by scattering on vacancies; the resulting force gives a net bias to vacancy diffusion. This driving force is proportional to the applied electrical current density scaled by a vacancy scattering parameter, Z^*. There is a threshold force below which only transient EM occurs. Existing models for the threshold magnitude based on mechanical strength are inconsistent with measurements of Z^*. We have completed numerical simulations to show that the interaction of dislocations and vacancies can account for the magnitude of the EM threshold and for an observed linear rate of mass flow above threshold. The simulations differ from previous studies in that the metal film is presumed to sustain both mechanical and osmotic stresses. Essentially, EM mass flux is inhibited by gradients in both the stress and vacancy concentrations, improving the agreement with experiment. There is, similarly, a simple model for the interaction of solute atoms and vacancies at a dislocation or grain boundary that may explain the effect of alloying on grain boundary diffusion. The implications (and validity) of this model are presently being examined.

Cl Etch (Support for SNL CRADA Task)

A critical issue which has not even been addressed previously is the effect of adsorbed Cl on Si surface reactivity. Under steady state etching conditions Si surfaces are saturated by Cl. Thus, if coverage by Cl significantly changes the Si surface reactivity then much of the previous work involving Cl adsorption onto clean Si surfaces cannot be applied directly to modeling of the etching process. It seems clear that surface conditions should play an important role in the chemistry of etching and our project has been to address this question quantitatively using first-principles density functional theory. The present first-principles study of Cl/Si(100) has shown a significant change in Si surface reactivity as the preexisting Cl coverage increases from 0 to 1 ML

(close to saturation coverage). This result shows that it is critical to consider the effect of Cl coverage when simulating Cl plasma etching of Si. In addition, we have suggested a new mechanism for Cl etching of Si(100).

F. Partner Contribution

The following individuals and groups maintained an ongoing technical dialogue with LLNL through the duration of the CRADA:

Lucent Technologies - Bell Laboratories:
David Eaglesham, George H. Gilmer, Hans Gossman, John Poate, and Conor Rafferty
Experimental data on delta doped boron spikes was provided by Bell laboratories on a regular basis.

Intel Corporation:
Martin Giles, and Francisco Leon
Experimental data on boron implanted and annealed profiles under a wide variety of conditions was provided by Intel Corporation.

University of Florida
Mark Law, and Kevin Jones

Boston University
Scott Duhnam

University of California
Department of Materials Science and Mineral Engineering
Prof. D.C. Chrzan, and Karin Lin

G. Documents/Reference List

All codes used in the present work were in existence prior to the CRADA. Although some modifications may have been made in these pre-existing codes to accomplish specific tasks no protected CRADA information was generated. The results of these computations, theory, simulation and modeling are described in detail in the collection of open literature publications listed above. No copy right or patent activity was initiated or is such initiation anticipated. Subsequent use of these codes and background intellectual property by CRADA partners is available on a "work for others basis" subsequent to DOE rules and regulations which may be in effect at such time.

A. K. McMahan and J. E. Klepeis, "Direct Calculation of Slater-Koster Parameters: Four-fold Coordinated Silicon/Boron Phases", Phys Rev. B, accepted

M.P. Surh and D.C. Chrzan, 'Threshold Behavior in Electromigration', to be submitted to Appl. Phys. Lett.

T. Diaz de la Rubia and G.H. Gilmer, "Structural Transformations and Defect Production in Ion Implanted Silicon: A Molecular Dynamics Study" Phys. Rev. Lett. 74, 2507 (1995)

J. Zhu, T. Diaz de la Rubia, L. Yang, C. Mailhiot and G.H. Gilmer. "Ab initio pseudopotential calculations of B diffusion and pairing in silicon", Phys. Rev. B 54, 4741 (1996)

M.J. Caturla, T. Diaz de la Rubia, L.M. Marques and G.H. Gilmer, "Ion Beam Processing of Silicon at keV Energies: A Molecular Dynamics Study" Phys. Rev. B 54, 16683 (1996)

T. Diaz de la Rubia, "Irradiation-induced Defect Production in Elemental Metals and Semiconductors: A Review of Recent Molecular Dynamics Studies" Ann. Rev. Mater. Sci. 26, 613 (1996)

M. Tang, L. Colombo, J. Zhu and T. Diaz de la Rubia, "Intrinsic Point Defects in Silicon" Tight Binding Molecular Dynamics Studies of Self-Diffusion, Interstitial-Vacancy Recombination and Formation Volumes" Phys. Rev. B 55, 14279 (1997)

O. Pankratov, H. Huang, T. Diaz de la Rubia and C. Mailhiot, "As-Vacancy Interaction and Ring Mechanism of Diffusion in Silicon" Phys. Rev. B 56, 13172 (1997)

J. Zhu, T. Diaz de la Rubia and C. Mailhiot, "Ab initio pseudopotential Calculations of Carbon Impurities in Silicon" Mater. Res. Soc. Symp. Proc. 439, 59 (1997)

M. Caturla and T. Diaz de la Rubia, "Dose Rate Effects in Damage Accumulation in Silicon" Mater. Res. Soc. Symp. Proc. 439, 125 (1997)

P. Bedrossian, M. J. Caturla and T. Diaz de la Rubia, "Damage Evolution and Surface Defect Segregation in Low-Energy Ion-Implanted Silicon" Appl. Phys. Lett. 70, 176 (1997)

M.D. Johnson, M.J. Caturla and T. Diaz de la Rubia, "A Kinetic Monte Carlo Study of the Effective Diffusivity of the Silicon Self-Interstitial in the Presence of Carbon and Boron" Submitted toJ. Appl. Phys. November 1997

M.J. Caturla, M.D. Johnson and T. Diaz de la Rubia, "The Fraction of Substitutional Boron in Silicon During Ion Implantation and Thermal Annealing" Submitted to Appl. Phys. Lett. December 1997

Christine J. Wu and John E. Klepeis, ``Effect of Cl coverage on Si(100) surface reactivity: Implications for Cl etching of Si", submitted to Phys. Rev. B.

H. Acknowledgment

Participant's signature of the final report indicates the following:

1) The Participant has reviewed the final report and concurs with the statements made therein.
2) The Participant agrees that any modifications or changes from the initial proposal were discussed and agreed to during the term of the project.
3) The Participant certifies that all reports either completed or in process are listed and all subject inventions and the associated intellectual property protection measures generated by his respective company and attributable to the project have been disclosed or are included on a list attached to this report.
4) The Participant certifies that if real property was exchanged during the agreement, all has either been returned to the initial custodian or transferred permanently.
5) The Participant certifies that proprietary information has been returned or destroyed by LLNL.

Ralph K. Cavin 8/22/98
Ralph Cavin ~~Date~~
Semiconductor Research Corp.

M. Fluss 9/17/98
Michael Fluss Date
Lawrence Livermore National Laboratory

Attachment I – Final Abstract
Attachment II – Project Accomplishments Summary
Attachment III – Final Quarterly Report

Semiconductor Maufacturing Modeling

Final Abstract
Attachment I
CRADA No. TC-1069-94

Date: 12/30/97 Revision: 1

The Semiconductor Industry Association (SIA) roadmap projection for 1 GHz on-chip clock speeds and 64 Gbits/Chip DRAM technology by the year 2005 requires scaling the minimum feature size of CMOS devices down to 100nm. This requirement has profound implications for device processing.. As physical constraints begin to limit device integration and characteristics, existing processing techniques must increasingly be understood quantitatively and modeled with unprecedented precision. Such advances will necessitate a fundamental improvement in our basic understanding of microstructure evolution during processing, and this can only be obtained through the development and validation of advanced physically-based predictive materials modeling computational tools. The work in this CRADA addressed these concerns directly, and the results will therefore greatly benefit the US semiconductor manufacturing and defense industries by aiding in the reduction of the time-to-market cycle, and by making it possible to substitute many high cost empirical design steps in manufacturing with much lower cost Technology Computer Aided Design (TCAD) processes.

Four research areas are described, Bulk Processing, Interconnects, Etch, and Fundamental Atomic Models. The technical program, based on an extensive project work plan developed by SRC, LLNL, SNL, and LANL, included extensive use of Local Density Approximation, Tight Binding Methods, and combined Molecular Dynamics and Monte Carlo methods (KINETIC Monte Carlo) to cover length and time scales neccessary to adequately model processes in the manufacturing of LSIC. The work was also of great benefit to DOE and LLNL. The improvements in capability are of generic value, deriving their specific value in actual applications. For example, the techniques developed in this CRADA for B/Si interactions, thin film growth, etch processing are all of interest to the electronics industry but are equally applicable to the improvement and understanding of aging of Pu which is of great interest to DOE. The effort has initiated new avenues of development at LLNL. While the problem of automatically generating tight-binding force representations has not been solved in this work, the new techniques developed here will greatly facilitate understanding of the "transferability" problem which has so far held up the achievement of this goal.

Semiconductor Manufacturing Modeling

Project Accomplishments Summary (Attachment II)
CRADA No. TC-1069-94

Date: 12/30/97 Revision: 1

A. Parties

The project was a relationship between the Lawrence Livermore National Laboratory (LLNL) and Semiconductor Research Corporation

University of California
Lawrence Livermore National Laboratory
7000 East Avenue, L-795
Livermore, CA 94550

National Semiconductor Research Corporation
1101 Slater Road
Durham, NC 27703

B. Background

Increasing development costs are making physics based modeling a viable alternative to Edisonian process development. Four tactical areas were assigned to LLNL as part of a three lab CRADAwith SRC.

1. Bulk Processing (Implant and Diffusion)

The Semiconductor Industry Association (SIA) roadmap projection for 1 GHz on-chip clock speeds and 64 Gbits/Chip DRAM technology by the year 2005 requires scaling the minimum feature size of CMOS devices down to 100nm. This requirement has profound implications for device processing. Lateral broadening of source/drain junctions caused by transient enhanced diffusion of implanted dopants during Rapid Thermal Processing will be a critical process limiting the development of these new technologies. As these constraints begin to limit device integration and characteristics, existing processing techniques must increasingly be understood quantitatively and modeled with unprecedented precision. Indeed, revolutionary advances in the development of physics-based process simulation tools will be required to achieve the goals for cost efficient manufacturing required by the SIA roadmap, and to satisfy the needs of the defense industrial base. These advances will necessitate a fundamental improvement in our basic understanding of microstructure evolution during processing, and this can only be obtained through the development and validation of advanced physically-based predictive materials modeling computational tools.

As described above, while the cost of modeling is rapidly decreasing, the cost and complexity of manufacturing has increased to the point where empirical approaches to process design are no longer practical. Simulations are being used extensively to guide the development of new technologies, but often the underlying models are flawed and inaccurate because of a lack of a good description of the physical processes involved. This is true of both FEOL and BEOL processes.

2. *Interconnects*

Metallization

In addition to front-end-of-line (FEOL) issues, we also addressed thin film deposition associated with back-end-of-line (BEOL) metallization through the development of lattice-based Monte Carlo methods. This work was carried out in very close collaboration with George Gilmer at Lucent Technologies.

The difficulty in developing predictive models for thin film deposition is three fold: (1) lack of full understanding of the underlying physical processes, (2) lack of experimental data capable of distinguishing clearly between possible mechanisms, and (3) lack of simulators incorporating these models so that they can be tested against the experimental data. All three components are necessary if we are to develop the foundation required for predictive models. Thin film growth mechanisms are sufficiently complex that it is only through implementation in a simulator that they can be compared and evaluated against experimental observations.

The prospect of using atomistic computer simulations to model polycrystalline thin film growth in three dimensions has been a beckoning yet elusive goal. However, progress achieved in computational physics for accurate interatomic potentials, coupled with vast improvements in computational power and algorithms, have brought the possibility of computing microstructure evolution during growth to reality. This has large implications for the development of predictive deposition modeling tools for microelectronics applications.

Electromigration

This CRADA work sought a fundamental understanding of important characteristics of electromigration (EM) in metal films. EM causes damage to metallic interconnects and may eventually limit the reliability of integrated circuits. Many qualitative and quantitative features of EM are incompletely understood; this lack of knowledge may result in design or manufacturing inefficiencies. Interconnects are known to support large mechanical stresses that inhibit EM, but existing models based on this effect may be inconsistent with observations. Interconnect durability can also be enhanced by dilute alloying, which raises the activation energy for grain boundary diffusion. The microscopic mechanism for this effect is not understood. We examine these effects at the level of the microscopic vacancy-solute-dislocation interactions.

3. *Etch*

As feature sizes on Si wafers continue to decrease, traditional design approaches based on trial experiments become prohibitively expensive. Therefore, one of the goals of the present SRC CRADA has been to help semiconductor manufacturers develop accurate and predictive topographic simulation tools by elucidating and quantifying the fundamental physical processes which occur at the gas-surface interface. The system that we have studied is Cl-Si, as Cl is one of most important regents in very-large-scale integrated circuit technologies such as etch and chemical vapor deposition.

4. *Ab Initio Computations*

The present CRADA sought to improve critical fabrication processes such as doping, deposition, and etching by the use of computer simulations. In many cases, these simulations depend on *fundamental materials characteristics* which are incompletely known, and so an important adjunct of this effort has been the determination of these properties from first principles calculations. One obvious example is interatomic force laws, without which it is not possible to move atoms about in the course of the time evolution of a simulation. These interactions arise fundamentally from the atomic electron clouds, and rigorous electronic structure techniques have made great strides in this CRADA at understanding the diffusion of dopants in Si as well as the halogen etching of Si surfaces.. These techniques, however, are limited to relatively small systems, e.g., one or two dopant-atom clusters in Si. One of the goals in this CRADA was therefore to develop less

expensive "tight-binding" techniques for defining the various interatomic force laws between dopant, etchant, and Si atoms.

C. Description

The work in this CRADA addressed manufacturing modeling concerns directly, and the results will therefore greatly benefit the US semiconductor manufacturing and defense industries by aiding in the reduction of the time-to-market cycle, and by making it possible to substitute many high cost empirical design steps in manufacturing with much lower cost Technology Computer Aided Design (TCAD) processes.The project relied on a wide variety of theoretical and simulation methodologies, all of which are widely used in the Department of Energy weapons laboratories for the purpose of designing materials from the atomic level up.

Tight-binding techniques are essentially fast, parameterized electronic structure calculations. Typically these parameters are determined by massive non-linear minimization algorithms which seek to summarize a large data base of ab initio calculated total energy and possibly force relations. For binary (e.g., Si/B) and more complex systems, these minimization approaches become more and more unmanageable. Therefore, in the course of this CRADA, we have developed a practical computational method whereby a large subset of the required parameters may be directly calculated. The method may be used by any band structure technique formulated in, or which can be projected onto, a localized basis. Application was made to the binary B/Si system of importance to both dopant diffusion and deposition thrusts of the CRADA.

Transient enhanced diffusion (TED) of ion implanted Boron in silicon has been a subject of significant interest over the last few years, and is one of the key issues that threatens the applicability of ion implantation and rapid thermal annealing technology to future generations of semiconductor devices. Here we describe a new, fully atomistic kMC model for boron transient enhanced diffusion in silicon. The input database for the kMC simulations is taken mostly from the results of first principles calculations. Our results predict that during annealing of 40 keV boron implantation profiles at 800 C, there exists a time window over which all boron is substitutional and therefore electrically active. At earlier or later times, point defect and boron diffusion results in boron clustering with the consequent build up of an inactive boron fraction. We show that this model, with the set of calculated parameters described below, can describe boron TED in silicon over a very wide range of experimental conditions without fits to experimental profiles or parameter adjustments.

Our new kinetic MC simulator, MC-Poly, includes the formation and coarsening of grain boundaries in polycrystalline thin films during deposition and the effect of these boundaries on surface and microstructure evolution. Grain boundaries form at the surfaces where clusters of atoms merge with one another and are included by assigning atoms in the vicinity of the boundaries an extra potential energy. Again, the GB energies are calculated by MD. Since most high angle, random boundaries have approximately the same energy, the first approximation for these energies is to assume a constant value, except at certain values of the crystalline orientations where special boundaries are formed. Moreover, it is also important to derive information on stress levels across various grain boundaries and the effect that this may have on bond energies at and near the boundaries. To study stress effects, MD simulations will be performed to calculate site energies as a function of strain. In a typical MD simulation, a three dimensional GB energy surface is generated for two degrees of freedom (two rotation angles). The other three degrees of freedom are fully relaxed via constant temperature and pressure MD. At the same time, the activation energy for GB diffusion can also be obtained as a 3D surface.

Electro migration (EM) occurs when electrical currents dissipate by scattering on vacancies; the resulting force gives a net bias to vacancy diffusion. This driving force is proportional to the

applied electrical current density scaled by a vacancy scattering parameter, Z^*. There is a threshold force below which only transient EM occurs. Existing models for the threshold magnitude based on mechanical strength are inconsistent with measurements of Z^*. We have completed numerical simulations to show that the interaction of dislocations and vacancies can account for the magnitude of the EM threshold and for an observed linear rate of mass flow above threshold. The simulations differ from previous studies in that the metal film is presumed to sustain both mechanical and osmotic stresses. Essentially, EM mass flux is inhibited by gradients in both the stress and vacancy concentrations, improving the agreement with experiment. There is, similarly, a simple model for the interaction of solute atoms and vacancies at a dislocation or grain boundary that may explain the effect of alloying on grain boundary diffusion. The implications (and validity) of this model are presently being examined.

A critical issue which has not even been addressed previously is the effect of absorbed Cl on Si surface reactivity. Under steady state etching conditions Si surfaces are saturated by Cl. Thus, if coverage by Cl significantly changes the Si surface reactivity then much of the previous work involving Cl absorption onto clean Si surfaces cannot be applied directly to modeling of the etching process. It seems clear that surface conditions should play an important role in the chemistry of etching and our project has been to address this question quantitatively using first-principles density functional theory. The present first-principles study of Cl/Si(100) has shown a significant change in Si surface reactivity as the preexisting Cl coverage increases from 0 to 1 ML (close to saturation coverage). This result shows that it is critical to consider the effect of Cl coverage when simulating Cl plasma etching of Si. In addition, we have suggested a new mechanism for Cl etching of Si(100).

D. Expected Economic Impact

The results from this CRADA are *already* in use. Lucent Technologies has made strategic decisions regarding implantation based on these results. Other manufacturers are preparing to use results from these codes to make decisions on future manufacturing methods involving shallow junction, low energy implantation, and rapid thermal diffusion. We anticipate that the principal contractural mechanism for accessing the results of these modeling tools is "work for others". Such contracts can be negotiated with the LLNL program partnership office. Implementation of these modeling tools promises better LSIC performance and reliability at lower cost than competing manufacturers abroad.

E. Benefits to DOE

Any comprehensive theoretical program must focus not only on the specific milestones of the projects at hand, but also on extending capabilities and building the tools of the future. Significant development under previous funding sources at LLNL had already gone into the plane wave-based electronic structure techniques which were available "off the shelf" for such successful use on the present CRADA. Large-scale atomistic simulations are now, however, limited by the computational cost of obtaining accurate interatomic force laws, and it is towards this critical future capability that the present tight-binding work was directed. These improvements in capability are of generic value to both DOE and industry, deriving their specific value in actual applications. For example, the techniques developed in this CRADA for B/Si interactions are equally applicable to the improvement of Pu interactions of great interest to DOE. While the problem of automatically generating tight-binding force representations has not been solved in this work, the new techniques developed here will greatly facilitate understanding of the "transferability" problem which has so far held up the achievement of this goal.

We have provided a critical new insight into the importance of including the effect of Cl coverage on Si surface reactivity. This insight as well as the new mechanism we have proposed can both be

incorporated into the Sandia-developed CHEMKIN chemical kinetics code used by the semiconductor industry, thus enabling more accurate simulations of the etching process.

The proposed explanation for threshold behavior in EM may resolve some longstanding questions about EM mechanisms. Improved understanding of these fundamental processes could lead to advances in manufacturing of integrated circuits. At the least, it provides increased confidence in the treatment of this problem. This is relevant to the management of semiconductor device reliability by both industry and DOE. The issue of solute effects on fast diffusion paths in metals is of great interest for interconnect design and manufacture as well as for understanding and modifying the mechanical properties of metals in general. A thorough microscopic understanding of this effect is of importance to DOE programs such as ASCI.

F. Industry Area

The work performed here was customized for application to the Si semiconductor industry. Other industries which may benefit from the present work include nuclear reactor industry, materials and surface processing, and in general those industries where detailed process modeling is shown to be a cost effective way to develop complex high technology products.

G. Project Status

An extensive project work plan was developed by SRC, LLNL, SNL, and LANL. This is part of the overall CRADA agreement for each DOE Laboratory. Unfortunately, funding was authorized at levels significantly below the work plan required. As a result continuous changes in level of effort were undertaken after consultation with SRC and, where appropriate, with LANL or SNL (when LLNL was providing input to their projects). The primary vehicle for these changes were the review meetings organized by SRC during the period of the CRADA. All milestones set out for the first two years of the program were met by LLNL scientists. A new project in interconnects was initiated but only operated for ~ 5 months prior to termination of the CRADA.

All codes used in the present work were in existance prior to the CRADA. Although some modifications may have been made in these pre-existing codes to accomplish specific tasks no protected CRADA information was generated. The results of these computations, theory, simulation and modeling are described in detail in the collection of open literature publications listed above. No copyright or patent activity was initiated or is such initiation anticipated. Subsequent use of these codes and background intellectual property by CRADA partners is available on a "work for others basis" subsequent to DOE rules and regulations which may be in effect at such time.

H. LLNL Point of Contact for Project Information

Michael J. Fluss, Project Manager
Lawrence Livermore National Laboratory
Chemistry and Materials Science Directorate,
B 235 MS L-323
7000 East Avenue
Livermore CA 94550

510-423-6665 office
510-423-4700 FAX

I. Company Size and Point(s) of Contact

The Semiconductor Research Corporation is the University Research funding arm of the semiconductor integrated circuit industry. Operating with a $30M budget they fund research and development based on industry needs and produce trained technical and professional scientists and engineers for the industry. Almost every major chip maker in the US is a member of SRC and hence the total revenues represented are in the ~$200 billion in sales regime, a significant fraction of the US GDP. The project manager for this CRADA was:

Ronald Goosens, SRC Project Manager
PO Box 12053
Research Triangle Park, NC 27709

181 Metro Drive, Suite 455
San Jose, CA 95110

tel. 408-453-9460 (SRC-San Jose)
tel. 919-941-9454 (SRC-Durham)
fax. 408-436-6646 (SRC-San Jose)
fax. 919-941-9450 (SRC-Durham)
tel. 408-721-2420 (NSC)
tel. 408-981-7632 (Cellular, Preferred)
tel. 800-607-3271 (Pager)
tel. 415-961-3952 (Private)

J. Project Examples

A number of charts and figures have been provided in the "Final Report". Additional figures from open literature publications are available on request.

K. Release of Information

I certify that all information contained in this report is accurate and releasable to the best of my knowledge.

Karena McKinley, *Director*
Industrial Partnerships
and Commercialization

9/29/98
Date

RELEASE OF INFORMATION

I have reviewed the attached Project Accomplishment Summary prepared by Lawrence Livermore National Laboratory and agree that the information about our CRADA may be released for external distribution.

Ralph Cavin, Vice President
~~National~~ Semiconductor Research Corp.

8/27/98
Date

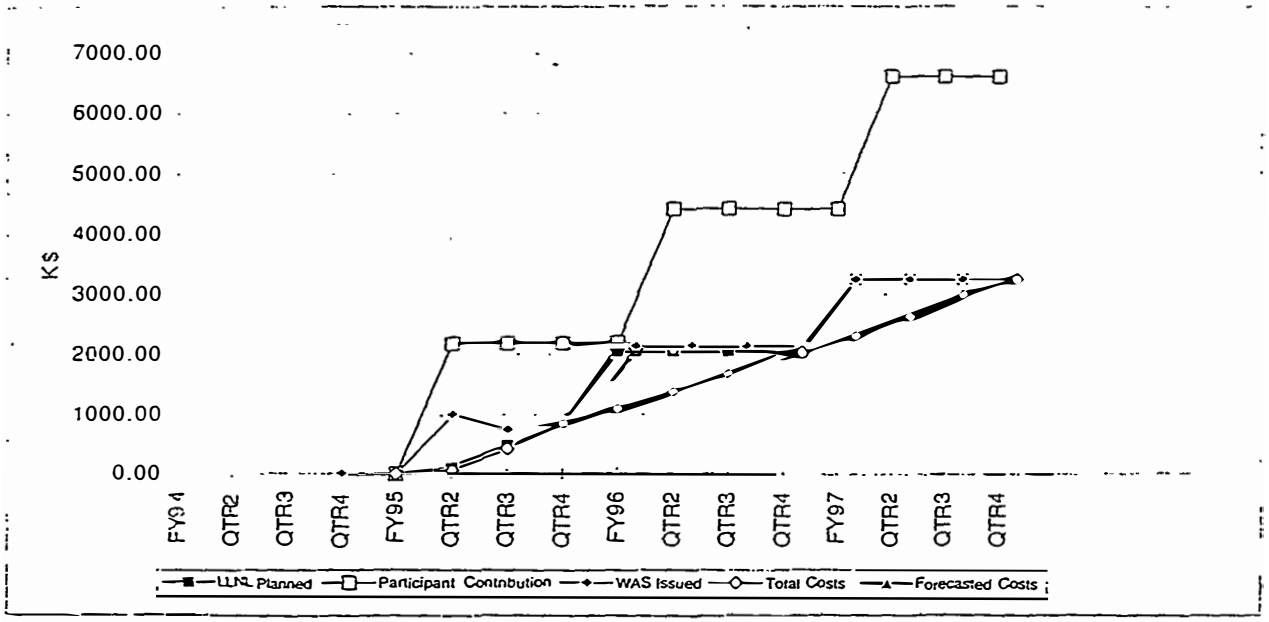
Lawrence Livermore National Laboratory

Title: Predictive Modeling and Simulation Tools
Participant: Semiconductor Research Corporation (SRC)
DOE TTI No.: 94-MULT-300-XX-1
CRADA No.: TC-1069-94
Account Numbers: 4775-28 to 34
Accounts Closed: N/A

Reporting Period: 09/30/96 - 09/30/97
Date CRADA Executed: 3/2/95
DOE Approval Date: 1/31/95
Scheduled Ending Date: 3/1/00
Completion Date:
B & R Code (S): DP0301

Approved Funding Profile (SK)

	FY94	FY95	FY96	FY97	FYOUT	Total
LLNL Planned	0	850	1200	1200	0	3250
Participant In-Kind	0	2200	2200	2200	2200	8800
Participant Funds-In	0	0	0	0	0	0
WAS Operating	0	850	1300	1097	0	3247
WAS Capital	0	0	0	0	0	0
Total Costs	0	850	1197	1208	0	3255



DP0301	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	July	Aug	Sep	FYTD	3255
FY94	0	0	0	0	0	0	0	0	0	0	0	0	0	
FY95	0	0	0	0	0	56	97	123	151	140	169	114	850	
FY96	103	84	60	71	94	116	105	81	113	111	80	179	1197	
FY97	94	98	79	109	112	98	135	114	111	94	90	74	1208	
FYOUT	0	0	0	0	0	0	0	0	0	0	0	0	0	

35DP03	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	July	Aug	Sep	FYTD	0
FY94	0	0	0	0	0	0	0	0	0	0	0	0	0	
FY95	0	0	0	0	0	0	0	0	0	0	0	0	0	
FY96	0	0	0	0	0	0	0	0	0	0	0	0	0	
FY97	0	0	0	0	0	0	0	0	0	0	0	0	0	
FYOUT	0	0	0	0	0	0	0	0	0	0	0	0	0	

STAFF w/phone:

Lab PI: Mike Fluss (510) 423-6655
Participant: William C. Holton (919) 541-9400
Resource Manager: Dave Boercker (510) 422-4187
DOE OAK: Jerry Scheinberg (510) 637-1653
DOE HQ: C. Fowler (202) 586-5834

Reporting Period: 09/30/96 - 09/30/97

DOE TTI No.: 94-MULT-300-XX-1

CRADA No.: TC-1069-94

Milestones and Deliverables:

List the complete set of milestones for all phases of the CRADA. Continue on a separate page if necessary.
Report any changes from the original CRADA or previous quarterly report on the CRADA Change Form.

	Completion Date: Scheduled	Actual
1 SEE ATTACHED LIST "Milestones and Deliverables"		
2		
3		
4		
5		
6		
7		
8		

Verification of participants' in-kind contribution was made in accordance with LLNL policy Explain basis of verification: Please initial YES X NO

List any subject inventions by either party (include IL# for LLNL inventions), additional background intellectual property, patents applied for, software copyrights, publications, awards, licenses granted or reportable economic impacts

Accomplishments

Describe Technical/Non-Technical lessons learned (address and be specific about milestones, participant contributions)
Summarize causes/justification of deviations from original scope of work. Continue on a separate page if necessary.

Reviewed by CRADA project Program Manager: _____ Date: _____

Reviewed by Karena McKinley, Director, LLNL/IP&C: Karena McKinley Date: 9/29/98

Direct questions regarding this Report to IP&C Resource Manager, Carol Asher, at (510) 422-7618