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# Fundamental Understanding and Development of Low-Cost, High-Efficiency Silicon Solar Cells

## Annual Progress Report: Sept. 1998 – Aug. 1999

A. Rohatgi, S. Narasimha, J. Moscher, A. Ebong, S. Kamra, T. Krygowski, P. Doshi, A. Ristow, and V. Yelundur

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## ABSTRACT

The overall objectives of this program are (1) to develop rapid and low-cost processes for manufacturing that can improve yield, throughput, and performance of silicon photovoltaic devices, (2) to design and fabricate high-efficiency solar cells on promising low-cost materials, and (3) to improve the fundamental understanding of advanced photovoltaic devices. Several rapid and potentially low-cost technologies are described in this report that were developed and applied toward the fabrication of high-efficiency silicon solar cells.

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# CHAPTER I

# RAPID THERMAL PROCESSING OF HIGH PERFORMANCE DIELECTRICS AND Si SOLAR CELLS

# 1. RAPID THERMAL PROCESSING OF HIGH PERFORMANCE DIELECTRICS AND SILICON SOLAR CELLS

Rapid and potentially low-cost process techniques are analyzed and successfully applied toward the fabrication of high-efficiency mono and multi crystalline Si solar cells. First, a novel dielectric passivation scheme (formed by stacking a plasma silicon nitride film on top of a rapid thermal oxide layer) is developed that serves as antireflection coating and reduces the surface recombination velocity (S) of the 1.3 Ω-cm p-Si surface to approximately 10 cm/s. The essential feature of the stack passivation scheme is its ability to withstand short 700-850°C anneal treatments used to fire screen printed (SP) contacts, without degradation in S. The stack also lowers the emitter saturation current density ($J_{oe}$) of 40 and 90 Ω/sq emitters by a factor of three and ten, respectively, compared to no passivation. Next, rapid emitter formation is accomplished by diffusion under tungsten halogen lamps in both belt line and rapid thermal processing (RTP) systems (instead of in a conventional infrared furnace). Third, a combination of SP aluminum and RTP is used to form an excellent back surface field (BSF) in 2 minutes to achieve an effective back surface recombination velocity ($S_{eff}$) of 200 cm/s on 2.3 Ω-cm Si. Finally, the above individual processes are integrated to achieve: 1) >19% efficient solar cells with emitter and Al-BSF formed by RTP and contacts formed by vacuum evaporation and photolithography, 2) 17% efficient manufacturable cells with emitter and Al-BSF formed in a belt line furnace and contacts formed by SP.

## 1.1 INTRODUCTION

For widespread implementation of PV, module cost should be reduced to $1-2/watt. This can be accomplished by lowering the cost of solar cell materials and processing without sacrificing cell efficiency. In addition, to reach a 50 MW/yr production capacity, close to 50,000 silicon cells with 15% efficiency (100-cm$^2$ cell producing 1.5 W) must be processed every day. This translates into approximately one cell per second [1]. Therefore processes must be invented that can significantly reduce the cell processing time and number of processing steps and corresponding equipment

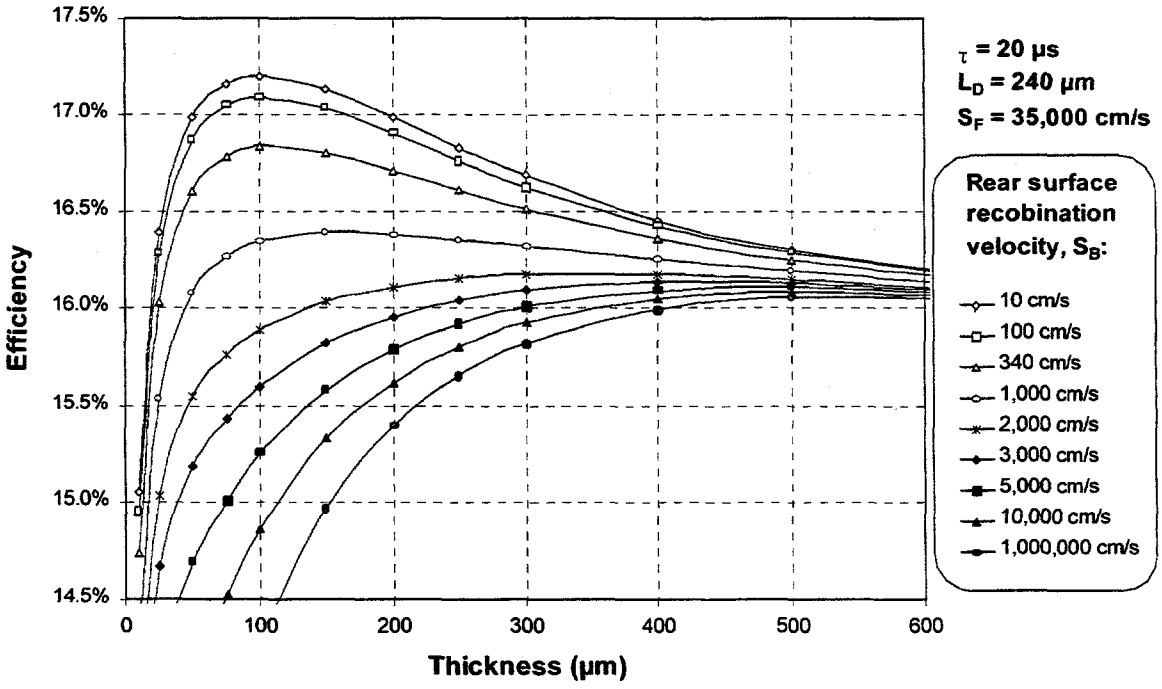


Fig. 1.1 Effect of rear passivation on optimum solar cell thickness.

must be developed that can handle more wafers per unit time. Rapid thermal processing (RTP) has the potential to accomplish high throughput, lower processing cost, and high performance solar cells simultaneously. Reduced number of processing steps and shorter processing times also reduce material handling. This may allow the use of thinner material in the future (100 μm thick Si as opposed to 300-400 μm being used today) which can also lead to significant cost reduction. In addition, as thinner materials are used to reduce cost, the backside recombination could have a bigger impact on the cell performance. Model calculations were performed using PC1D [2] computer program. Fig. 1.1 shows that if a metal grid is used on the back with the non-contacted back surface fully passivated to produce rear surface recombination velocity, $S_B$, of 10 cm/s, a thinner photovoltaic (PV) grade material, such as String Ribbon silicon, with low minority carrier lifetimes (20 μs) could actually produce over 17% efficient solar cells.

Most manufactures, in an attempt to reduce manufacturing cost, use a minimal number of low-cost processing steps. However, the resulting cell efficiencies are in the 10-14% range. In contrast to industrial cells, laboratory cells have reached efficiencies over 24% [3] by incorporating numerous processing steps and high efficiency features such as selective emitter, advanced light trapping and surface texturing, low front and back surface recombination velocity, and high quality contacts formed by vacuum evaporation and photolithography. Because of this, current laboratory cells are too expensive and industrial cells are not efficient enough to meet the cost and efficiency targets simultaneously. Therefore the objective of this study is to develop rapid thermal

processes that is compatible with manufacturing cost-effective solar cells on PV grade material with efficiencies higher than the present industrial solar cells. This paper presents rapid and improved formation of 1) dielectrics for surface passivation and antireflection coating 2) phosphorus diffused $n^+$- emitter and 3) Al alloyed back surface field 4) Gettering and passivation of bulk defects in string ribbon silicon. Rapid thermal technologies, such as RTP diffusion and oxidation, screen printed contacts, and plasma enhanced chemical vapor deposition (PECVD) of silicon nitride (SiN), are optimized and integrated to achieve high efficiency cells on mono and multi crystalline silicon.

## 1.2 Rapid Thermal Processing of Dielectrics for Front and Back Surface Passivation and Antireflection Coating for Silicon Solar Cells

Minimizing minority carrier recombination at the surfaces of silicon is crucial for performance of many semiconductor devices including solar cells [4]. The objective of this section is to provide a quantitative comparison of surface passivation quality of several promising dielectrics for diffused and non-diffused silicon surfaces. The emphasis is placed on rapid technologies like rapid thermal oxidation (RTO) under tungsten halogen lamps, PECVD SiN, and $TiO_2$. These technologies have much lower thermal budget than oxides grown in conventional furnace. Films like $TiO_2$ and SiN are investigated because they also provide good antireflection coating. Since cell fabrication often involves 400°C forming gas anneal (FGA) and 700-800°C firing of screen printed contacts, the impact of such heat treatments on dielectric passivation quality is also investigated.

To assess the surface passivation of p-type silicon, effective minority carrier lifetime ($\tau_{eff}$) measurements [5] were performed on 1.3 Ω-cm p-type <100> FZ silicon wafers coated with various passivating films. The investigation of $n^+$-emitter passivation was performed by $J_{oe}$ measurements by the photoconductance decay (PCD) technique [6] on phosphorus diffused, high-resistivity (750 Ω-cm), high bulk lifetime (> 1 ms) FZ Si wafers. Samples for the emitter passivation experiment were diffused on both sides in an RTP system using spin-on dopant sources. Emitters with sheet resistances of 40 and 90 Ω/□, which correspond to emitters that can accommodate screen-printed and evaporated contacts, respectively, were investigated.

After removal of the residual phosphosilicate glass, part of the diffused and non-diffused p-type samples were oxidized in the same RTP system used for the diffusions. This rapid thermal oxidation at 900°C for 150 s resulted in an oxide thickness of approximately 8-10 nm on diffused surfaces and about 6 nm on non-diffused 1Ω-cm p-Si. The oxidized low-resistivity samples were then annealed in forming gas at 400°C for 15 min. After this, deposition of SiN was performed at 300°C in a parallel plate reactor with high frequency (13.6 MHz) excitation. The thickness of SiN film was approximately that of an antireflection (AR) coating (~60 nm) and the refractive index measured at 632.8nm was between 2.15 and 2.27, which is in the optimum range for single-layer AR coatings under glass or the first film (directly in contact with silicon) of double-layer AR coatings in air [7].

Although its passivation is known to be poor, $TiO_2$ films are also compared for completeness because it is by far the dielectric most commonly employed by the PV industry as an AR coating. The deposition of $TiO_2$ was performed by evaporating titanium in an oxygen atmosphere under a low pressure of 15 mPa. After film deposition, the effective minority carrier lifetime ($S_{eff}$) was measured on all samples. Subsequently, a forming gas anneal (FGA) at 400°C was performed on all samples. As a final step, the samples were subjected to a short (30 s) temperature cycle with a maximum temperature of 730°C, which is typically used as a firing cycle for screen-printed Ag contacts. This step was performed in a belt line furnace with tungsten-halogen lamp heating in a compressed air ambient. The minority carrier lifetime was measured after each step using a commercially available inductively coupled PCD tester. From these data, the emitter saturation current $J_{0e}$ (for diffused samples) and the surface recombination velocity $S_{eff}$ were (for undiffused samples) calculated. The PCD measurement of $J_{0e}$ (equation 1) is discussed in Kane and Swanson [6] and $S_{eff}$ was calculated from the measured $\tau_{eff}$ value using equations 2 and 3, [18]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + Cn^2 + \frac{2J_o n}{qn_i^2 W} \qquad (1)$$

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \beta^2 \cdot D_n \qquad (2)$$

$$\tan\left(\frac{\beta \cdot W}{2}\right) = \frac{S_{eff}}{\beta \cdot D_n} \qquad (3)$$

where n is the injection level, $D_n$ is the diffusivity of minority carriers, and W is the sample thickness. In this study, an infinite bulk lifetime ($\tau_b \rightarrow \infty$) was assumed for high-quality 1.3 Ω-cm FZ wafers so the calculated $S_{eff}$ actually represents the worst-case (maximum) value. Thus dielectric passivation is not measure in terms of interface state density ($D_{it}$) but assessed in terms of S and $J_{oe}$ which are not only influenced by $D_{it}$ but also by the fixed charged density in the dielectrics [8,9].

### 1.2.1 Dielectric Passivation of Diffused Si Surfaces

The passivation of diffused front surfaces were investigated for both 40 Ω/□ and 90 Ω/□ emitters. On a relatively opaque 40 Ω/□ emitter (which is generally needed to accommodate screen-printed contacts), the surface is largely decoupled from the bulk, because of the high surface doping concentration and depth of the doping profile. Thus, the introduction of RTO or SiN passivation resulted in a moderate decrease in $J_{0e}$ of about a factor of two to three, as can be seen from Fig 1.2. While $TiO_2$ showed hardly any passivation, SiN was clearly inferior to RTO, which, in combination, resulted in the best passivation. Note that the high-temperature treatment during RTO growth changed the doping profile and lead to a lower surface doping concentration, which allowed for better surface passivation. The $J_{oe}$ values for textured samples were about 1.5 to 2 times higher than those for planar surfaces, which resembles the 1.73 times increase in surface area resulting from regular pyramidal texturing.

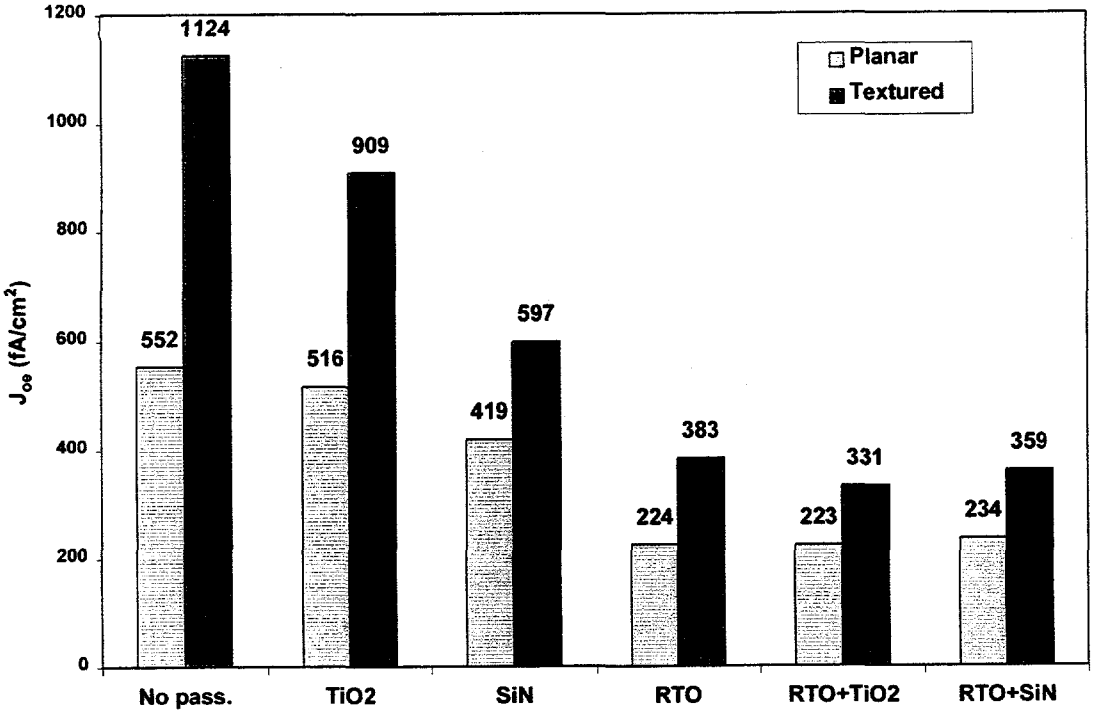


Fig.1.2 Emitter saturation current densities for 40 Ω/□ RTP emitter.

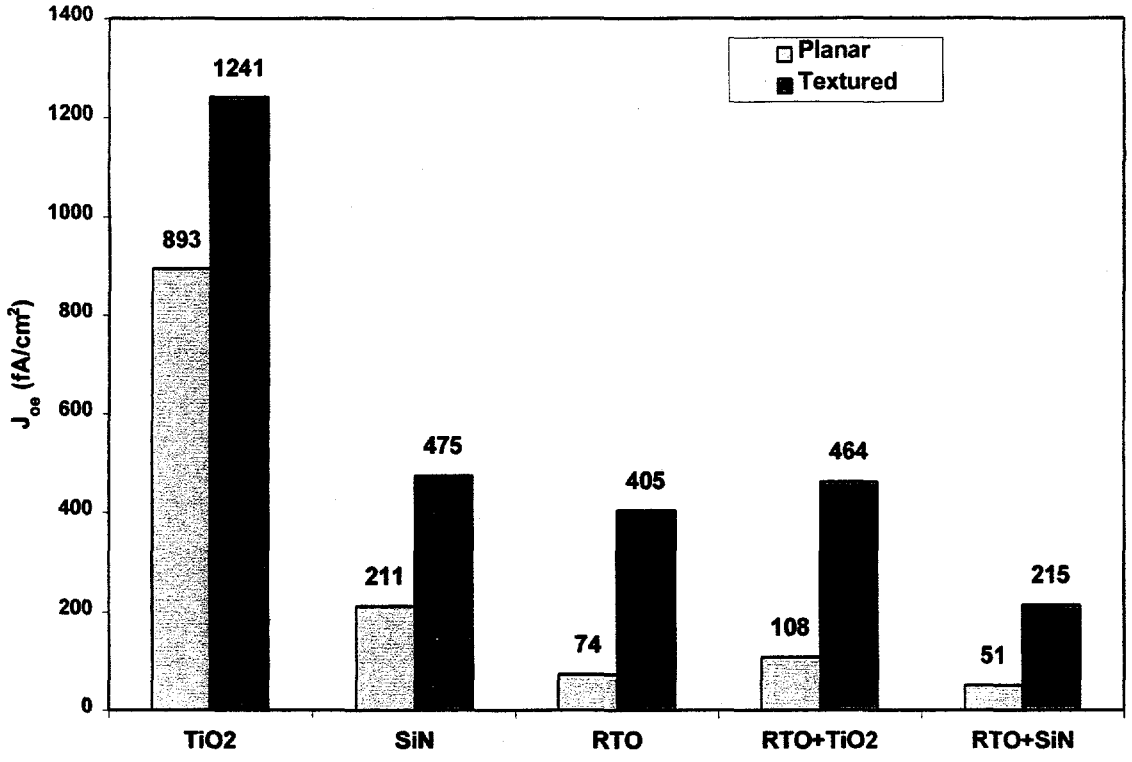


Fig. 1.3 Emitter saturation current densities for different passivation schemes on 90 Ω/□ RTP emitters.

On the relatively transparent 90 Ω/□ emitter, (which is generally used for evaporated or photolithographically-defined contacts) the difference in the degree of passivation for various dielectrics was more apparent, as shown in Fig. 1.3. Again, $TiO_2$ does not provide any appreciable reduction in $J_{0e}$. For the planar surface, RTO growth reduced $J_{0e}$ by more than a factor of ten to below 100 fA/cm$^2$, as does the deposition of SiN. However, on the textured surface, RTO is not as effective, resulting in a moderate $J_{0e}$ value of 400 fA/cm$^2$. Here, RTO+SiN double layer was clearly superior resulting in $J_{0e}$ values in the range of 215 fA/cm$^2$.

### 1.2.2 Dielectric Passivation of Undiffused Si Surfaces

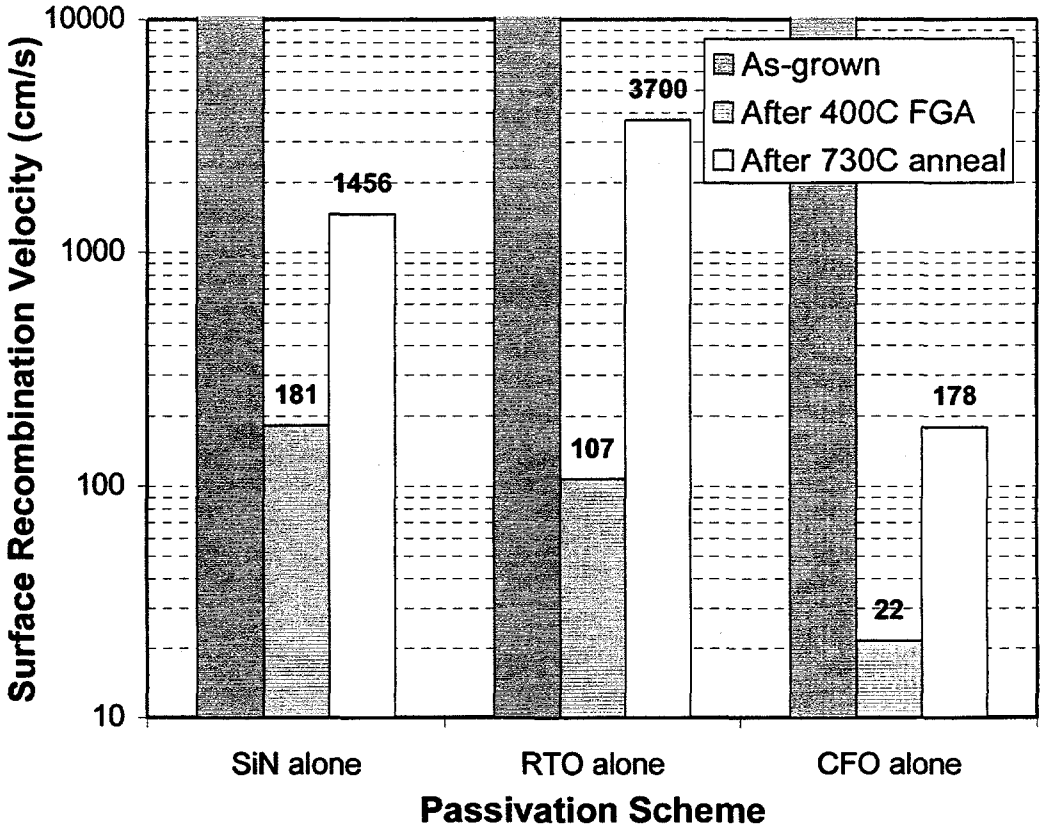


Fig. 1.4: The effect of belt line annealing on the S value of individual dielectric passivation schemes.

Dielectric passivation of undiffused surface is crucial for bifacial solar cells. Fig. 1.4 shows the effectiveness of several *individual*-passivating dielectrics. The dielectrics investigated include the 100 Å RTO alone, 100 Å thick conventional furnace oxide (CFO) alone, and 650 Å SiN alone. The individual layers result in S values in excess of 10,000 cm/s on 1.3 Ω-cm Si immediately after growth or deposition. This extremely poor S is reduced to lower levels (20-200 cm/s) if an additional FGA at 400°C is performed. However, a subsequent 730°C belt line anneal (simulating SP contact firing) degrades

each passivation, increasing S above 1000 cm/s for the RTO and SiN films and above 175 cm/s for the CFO.

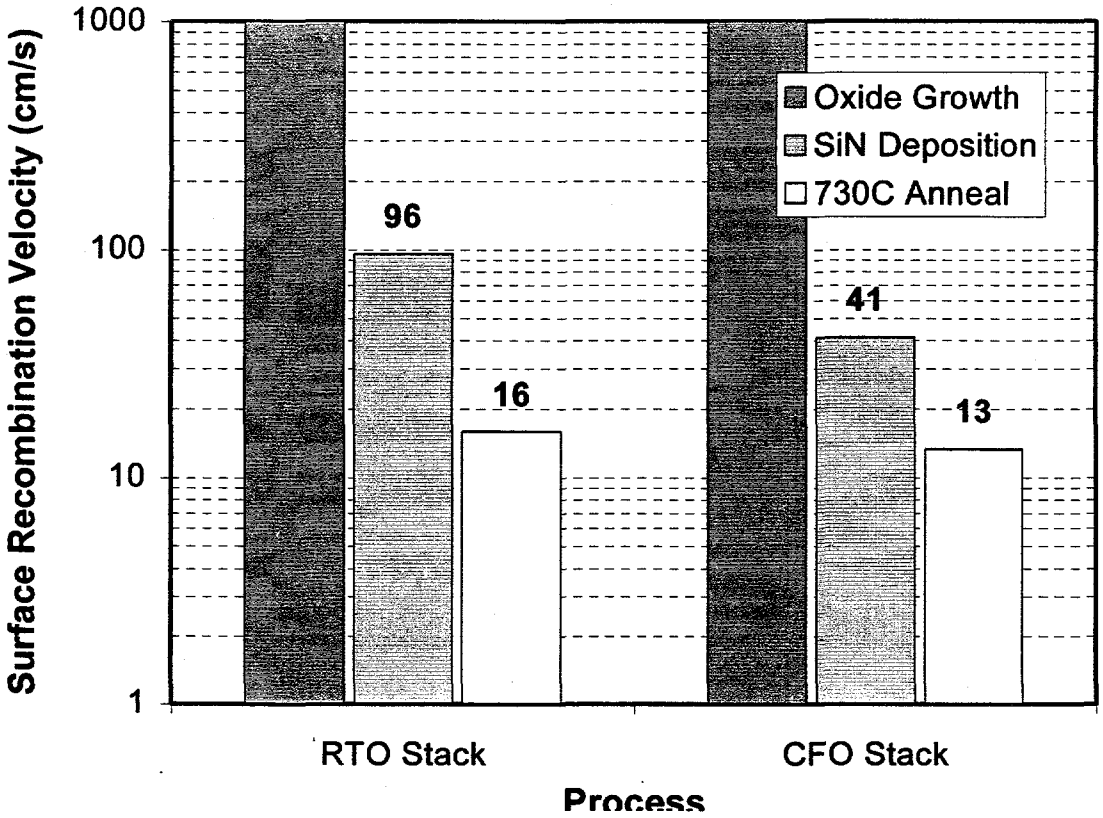


Fig. 1.5 Improvement in S of the stack passivation scheme after 730°C/30 sec annealing.

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ntr

ary to the response of the individual films, annealing the RTO/SiN and CFO/SiN stacks clearly *enhances* the passivation quality. The stepwise effect of stacking SiN on top of the RTO or CFO layer and then annealing at 730°C is shown in Fig. 1.5. An S value of nearly 10 cm/s is attained at the 1.3 Ω-cm Si surface after the final anneal. This anneal is believed to enhance the release and delivery of atomic hydrogen from the SiN film to the Si-$SiO_2$ interface, thereby reducing the interface state density ($D_{it}$).

## 1.3 Rapid Thermal Processing of Phosphorus Diffused Emitter for Silicon Solar Cells

The total process time for phosphorus diffusion in a conventional furnace requires on the order of one hour at 850-900°C to achieve emitters with appropriate junction depth for SP contact formation. This severely limits the throughput of a manufacturing line. In this section, emitter formation in a belt line furnace and RTP unit is described and compared with conventional furnace diffusion. Both belt line and RTP systems utilize tungsten halogen lamps to optically heat the sample. At normal diffusion temperatures, these lamps produce high-energy photons that increase the effective diffusion of phosphorous in Si when utilized in conjunction with spin-on dopants (SOD) [10,11].

In order to support this hypothesis, three different drive-in treatments were performed at 880°C after the application of SOD phosphorus. These were: 1) conventional furnace diffusion where the sample temperature is raised by standard resistance heating, 2) beltline furnace diffusion where the sample is heated by a combination of radiation from tungsten halogen lamps, conduction from the belt, and convection, and 3) single wafer RTP diffusion where the sample is heated primarily by radiation from the tungsten halogen lamps. In the conventional furnace, only infrared photons are present. In the RTP system the sample sees large number of higher-energy photons. In the lamp heated three-zone belt line furnace, the sample sees fewer high-energy photons because the lamps in the first two zones are not as hot as the third zone and there is additional heat via conduction and convection. Fig. 1.6 shows that

after the SOD application, an 880°C/6 minute RTP drive-in produces significantly more diffusion compared to conventional furnace processing (CFP). The diffusion profile attained with belt line processing (BLP) generally falls between the two. This is consistent with the high-energy photon content of the three spectra. As a result, it required 30 minutes, 6 minutes, and 3 minutes at 880°C to obtain a 40 Ω/□ emitter by CFP, BLP and RTP, respectively.

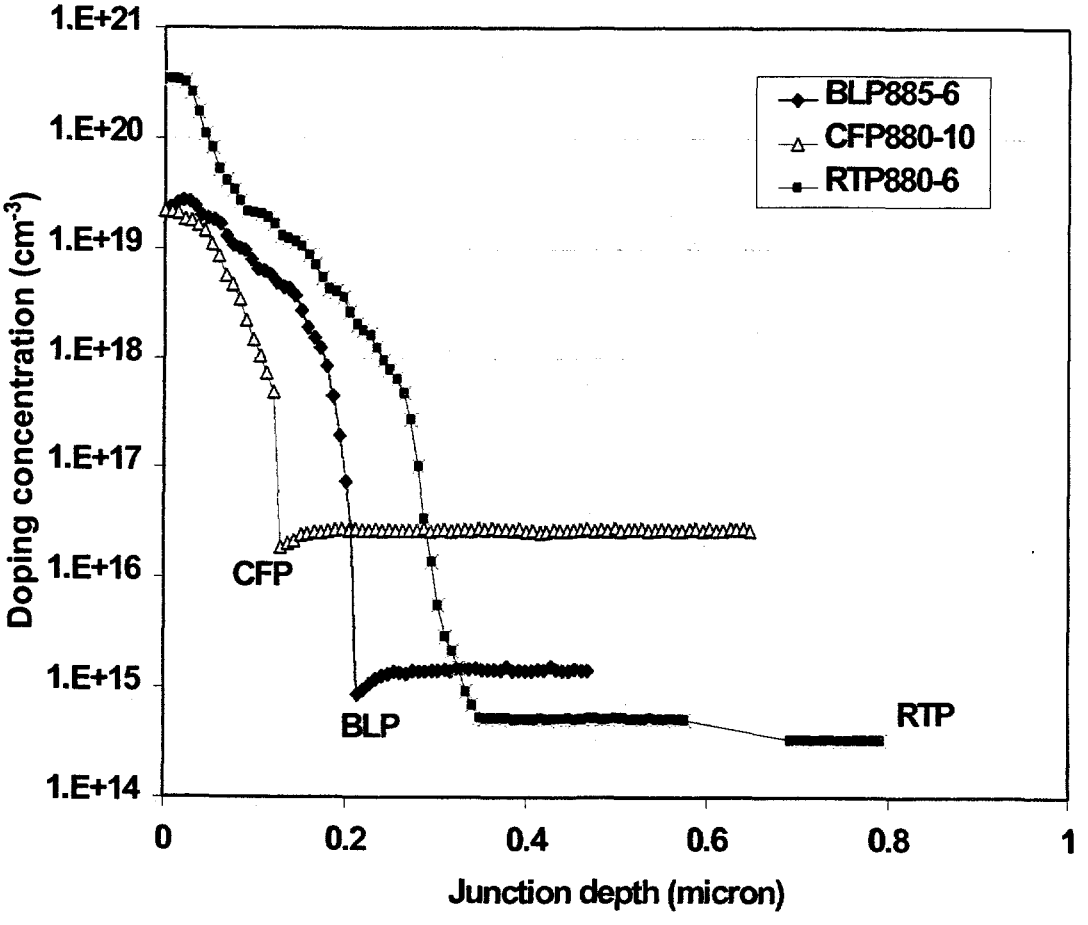


Fig. 1.6 Comparison of CFP, BLP, and RTP phosphorus diffusion (using SOD sources) at 880°C for 6 minutes.

## 1.4 Rapid Thermal Processing of Aluminum Back Surface Field for Silicon Solar Cells

The Al-BSF is widely used for reducing the effective back surface recombination velocity ($S_{eff}$) in solar cells with full metal rear contacts. The advantage of the Al-BSF (over a boron) is that the $p^+$ region can be formed in a short alloying step at lower temperature instead of a lengthy boron diffusion process at much higher temperatures. However, the electrical quality of an Al-BSF is extremely sensitive to uniformity and process conditions. If the $p^+$ is not formed appropriately, full performance gains will not be realized. This section demonstrates that both RTP and BLP of Al BSF reduce thermal budget and produce comparable high quality back surface field. The quality of back surface field is assessed in terms of effective surface recombination velocity at the $p^+$ -p interface. $S_{eff}$ value was determined from the long wavelength response by matching the measured and calculated internal quantum efficiencies.

An important factor that affects the electrical quality of an Al-BSF is junction uniformity. The uniformity of an Al-BSF, or any metal-Si junction in general, is controlled to a large extent by the ramp-up rate used to reach the alloying temperature. This effect was noted early on in Refs.[12-13]. The same effect was later observed, in qualitative terms, for the Al-Si system [14]. This study shows that effect under fast ramp condition in RTP the junction uniformity of Al-BSF is quite good as compared to BLP Al-BSF with set temperature at 850°C.

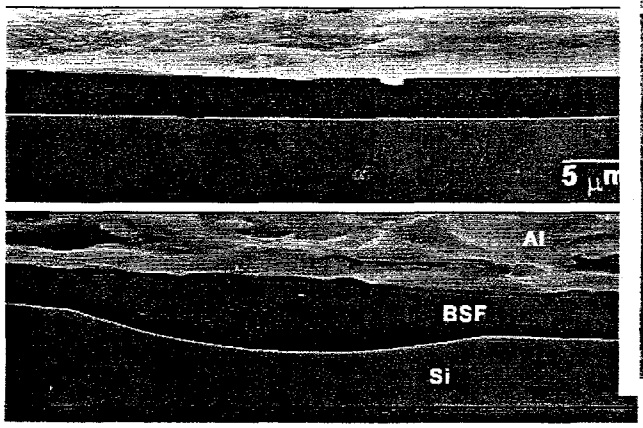


Fig. 1.7 BSF regions formed under fast ramp condition in RTP.

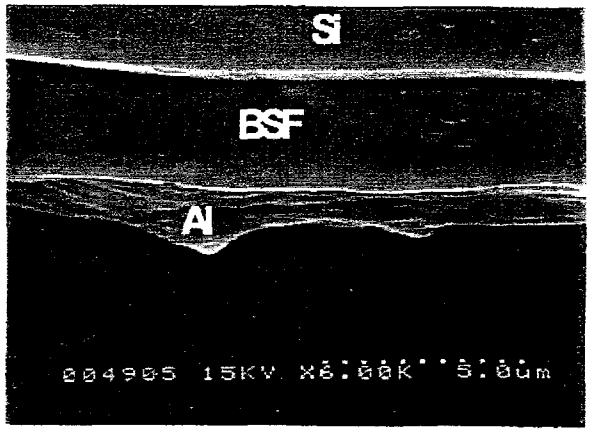


Fig. 1.8 BSF regions formed in BLP at 860°C temperature.

Under fast ramp conditions present in RTP, a sample goes through the Al-Si eutectic point and reaches the process temperature very quickly. At typical process temperatures (≈800-900°C), the Al layer becomes molten and readily wets the entire Si surface. This promotes more uniform alloying, which in turn improves Al-BSF uniformity.

Fig. 1.7 shows cross sectional SEM micrographs of the Al-BSF regions formed under fast ramp condition in RTP. The sample alloyed under fast ramp conditions shows a higher degree of junction uniformity and planarity. The cross sectional SEM micrograph of the Al-BSF region formed under BLP condition is shown in Fig. 1.8. The uniformity in the Al-BSF formed in BLP is as good as that shown in Fig. 7. Detailed study on slow and fast ramp and their effects on the cell efficiency is given elsewhere [15].

## 1.5 . Gettering and passivation of bulk defects in string ribbon silicon.

The String Ribbon silicon growth process can reduce the cost of substrate because substrates are grown directly without wafering [16]. Also, String Ribbon silicon can be grown to a thickness as low as 5 μm, resulting in further material and cost savings [17]. While the growth of String Ribbon makes it an attractive material for low-cost silicon photovoltaics, the as-grown minority carrier lifetime in the material is low, typically 1-10 μs. Therefore the overall objective of this study is to improve the bulk lifetime in String Ribbon silicon and apply a high quality, manufacturable rear surface passivation treatment to achieve high efficiency solar cells. In this section, the effectiveness of industrially viable gettering and passivation technologies, namely phosphorus gettering using a liquid phosphorus spin-on dopant, aluminum gettering using screen-printed Al paste, and PECVD SiN hydrogenation would be presented. The associated heat treatments were all performed in a lamp-heated continuous belt furnace. To monitor the effectiveness of each technology, minority carrier lifetime measurements were made using quasi-steady state photo-conductance technique (QSSPC) [18]. The experimental details to this section is given elsewhere [19].

Fig. 1.9 shows that there is some variability in the as-grown lifetime of various samples. Therefore the average of the lifetime measurements on four different regions of each sample, measured before and after the desired treatment, and the relative change are shown in Fig.1.9. Phosphorus gettering, PECVD SiN hydrogenation, and Al gettering were each moderately effective in improving the bulk lifetime, but were unable to

improve the measured lifetime to over 20 μs, previously identified as the targeted lifetime.

The combination of phosphorus gettering and PECVD SiN hydrogenation at 850°C improved the lifetime by 7 μs, which is nearly equal to the sum of the enhancement

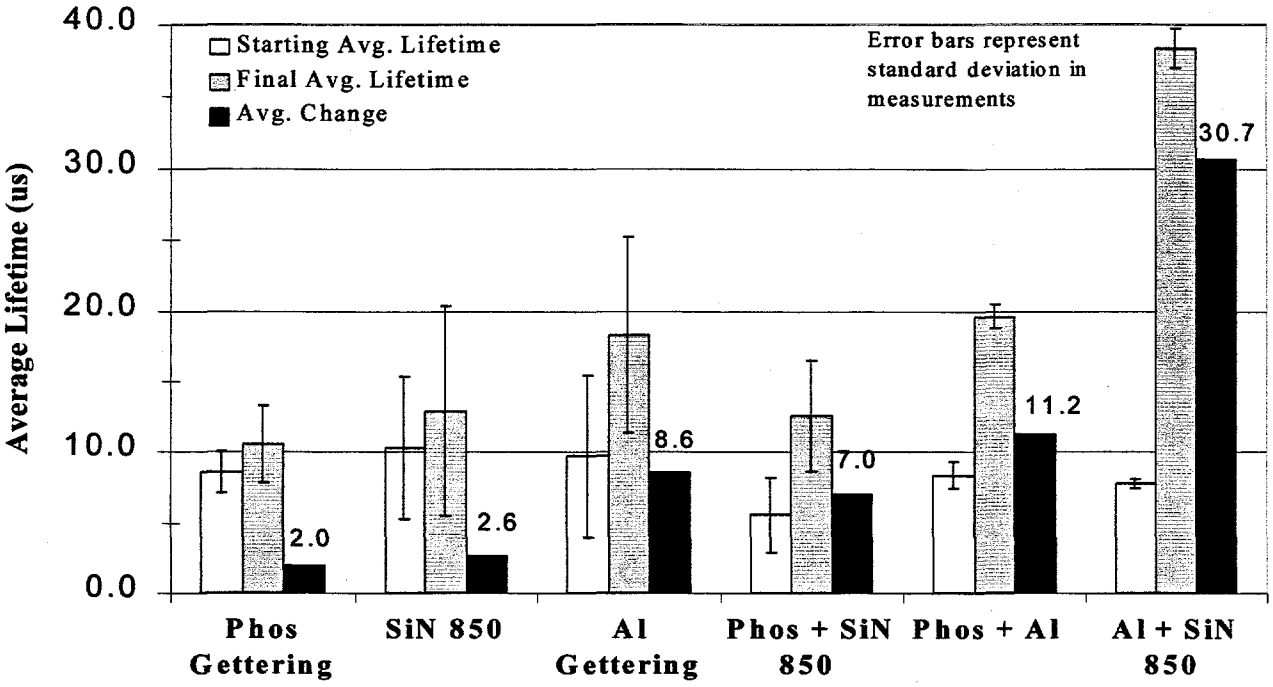


Figure 1.9 Effectiveness of gettering and passivation treatments

provided by individual phosphorus gettering and hydrogenation treatments. A similar additive effect is observed in the combination of phosphorus and aluminum gettering in which the lifetime improved by over 11 μs. Still the 20 μs threshold was not exceeded by any of the above combinations. In contrast, a noteworthy average lifetime of over 38 μs, an improvement of over 30 μs, was observed when the PECVD SiN hydrogenation treatment and aluminum gettering treatment were combined in one heat treatment at

850°C for 2 minutes. This improvement in lifetime treatment were combined in one heat treatment at 850°C hydrogenation and Al treatments alone suggesting that there may be a positive synergistic interaction between the hydrogenation from the front surface and the Al alloying process simultaneously occurring at the back surface of the substrate at 850°C.

A proposed mechanism that describes the interaction of hydrogenation and Al gettering involves the enhanced dissociation of molecular hydrogen in the presence of silicon vacancy [20]. A vacancy in a silicon lattice is believed to aid in the dissociation of molecular hydrogen into a fast diffusing hydrogen-vacancy pair and atomic hydrogen.

## 1.6 Integration of Rapid Process Technologies for High Efficiency Silicon Solar Cells

Silicon solar cell fabrication involves processing of emitter, back surface field, dielectric passivation, antireflection coating, and front and back contact formation. Previous sections demonstrated the use of belt line and RTP systems for rapid and improved formation of emitter and back surface field, and deposition of RTO/SiN stack that can provided not only an excellent passivation for front and back surfaces but also withstand 700-800°C firing of low-cost screen-printed contacts. In this section we show the integration of these rapid technologies for achieving high efficiency cells on mono and multi crystalline silicon.

### 1.6.1 Conventional Furnace Processing of Si Solar Cells with Photolithography contacts

Figure 1.10a shows the fabrication sequence of a baseline cell using conventional furnace processing (CFP) and photolithography contacts. In this process 80 Ω/□ phosphorus diffusion, 1 μm Al back surface field formation, and front oxide passivation was done in conventional furnace. Process sequence involved about 6 hours of high temperature processing, 2½ hours of metal evaporation, and 5 hours of photolithography resulting in a total cell processing time of about 6 hours with cell efficiencies of about 18% (Fig. 1.10a) without any surface texturing.

### 1.6.2 Rapid Thermal Processing of Si Solar Cells with Photolithography Contacts

The above process was modified and shortened significantly by replacing furnace processing by rapid thermal processing (RTP) in which phosphorus diffusion, screen printed Al BSF formation, and oxide passivation was done in a single wafer RTP system from AG Associates. Front contacts were formed by evaporation and photolithography. Figure 1.10b shows the detailed process sequence and the corresponding cell performance. The 80 Ω/□ phosphorus diffusion was performed in about 6 minutes by application of spin-on-dopant, followed by a short drive in the RTP unit under the tungsten halogen lamps. Al back surface field was formed by screen printing 15 μm thick Al paste in less than a minute followed by RTP in an oxygen

ambient for less than 5 minutes. Besides forming a very effective and deep BSF, this step also produced a high quality rapid thermal oxide on the front simultaneously. Thus, this RTP process sequence reduces the total high temperature processing time from 6 hours (conventional furnace processing in Fig 1.10a) to less than 15 minutes. In addition to reducing the total processing time from 16 hours to 8½ hours, this RTP process produced higher efficiency cells compared to conventional furnace processing. The RTP cell efficiencies of 19.1% on FZ, 17.7% on MCZ, 17.5% on Ga-doped CZ and 17.3% on boron-doped CZ were achieved. This is primarily due to the thicker and more uniform RTP SP Al back surface field.

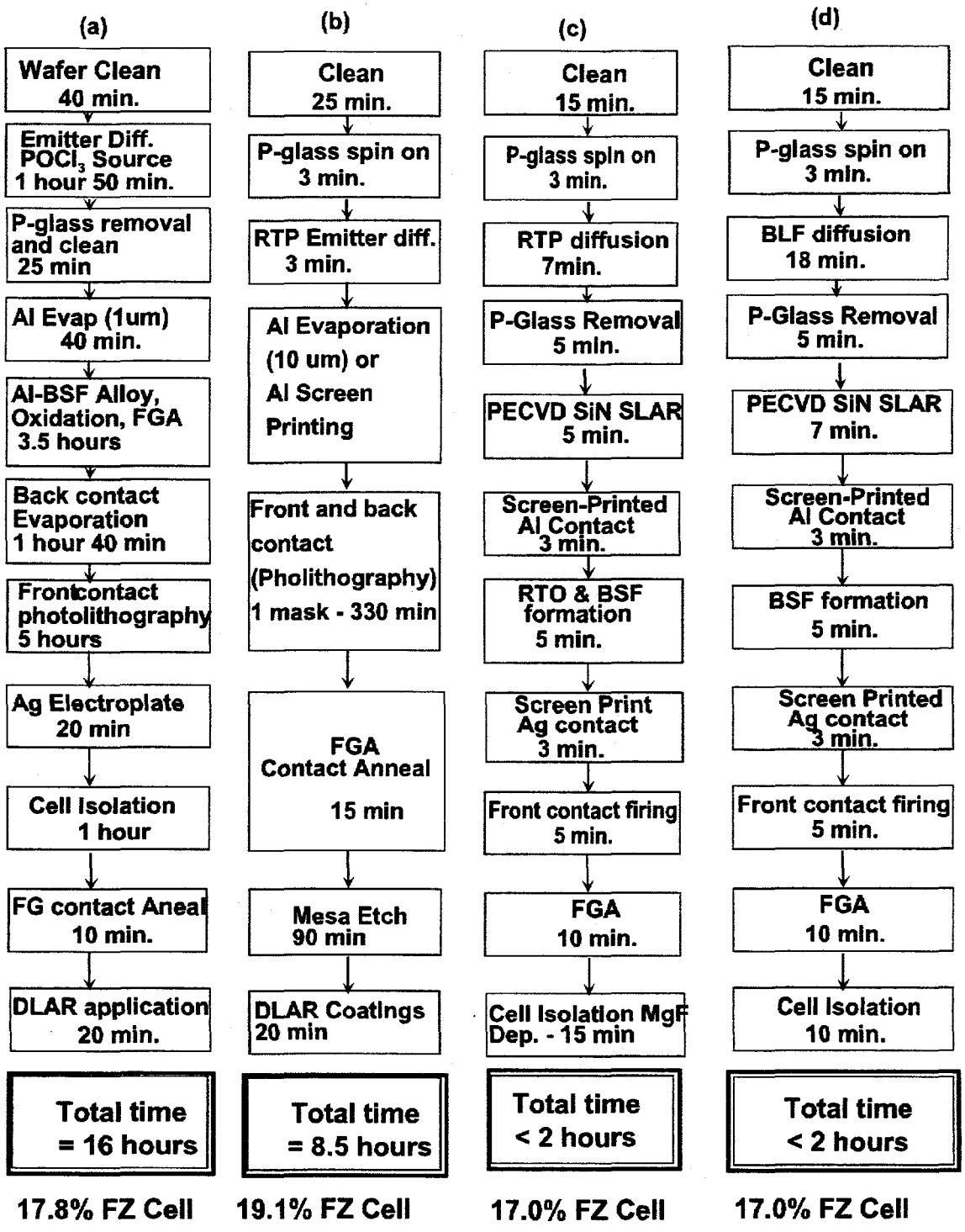


Fig. 10: Process sequence and cell performance for (a) baseline CFP cells with photolithography contacts (b) RTP cells with photolithography contacts (c) RTP cells with screen-printed contacts, and (d) BLP cells with screen-printed contacts.

### 1.6.3 Rapid Thermal Processing of Screen Printed Si Solar Cells

In an attempt to reduce the cell processing time further, the evaporation and photolithography contacts on the front were replaced by screen-printed Ag contacts. Due to the high contact resistance and junction shunting, the emitter sheet resistance of the SP cells was decreased from 80 to 40Ω/□ to achieve good contacts and high fill factors (FF). This increased the emitter diffusion time from 3 to 7 min. An 800 Å thick PECVD SiN coating was deposited on top of RTO for stack passivation and single layer AR coating. Ag contact grid was screen printed on the front and fired through the SiN AR coating in less than 5 min. This reduced the contact formation time from 330 min to 8 min. Fig. 1.10c shows the modified process sequence along with the cell performance. This RTP/SP process reduced the cell processing time from 8.5 hours to less than 2 hours and produced a planar cell efficiency of 17% with a fill factor of 0.798. The 2% reduction in absolute efficiency (19% to 17%) is largely attributed to heavy doping effects in the emitter, increased shading and reflectance, and somewhat inferior front surface passivation due to higher surface doping concentration [21]. Formation of selective emitter ($\leq$ 40 Ω/□ underneath the grid and $\geq$ 80 Ω/□ between the grid lines) for SP cells should be able to recover majority of the 2% loss in the efficiency.

### 1.6.4 Rapid Belt Line Processing of Screen Printed Si Solar Cells

Since there is no continuous RTP system available today, continuous belt line processing (BLP) has been modified to bridge the gap between the single wafer RTP and BLP cells. Recall that P diffusion in the belt furnace is slower than in an RTP system. In an effort to keep the BLP emitter diffusion time to 6 minutes, the diffusion temperature was raised from 880°C to 925°C to achieve a ≈40 Ω/□ emitter. Instead of the stack passivation scheme, SiN alone was utilized for emitter surface passivation and as a single layer AR coating. The SP Al-BSF was alloyed in a belt line furnace at a set point temperature of 850°C for 2 minutes. Finally, SP front contacts were fired through the SiN layer in 30 seconds at 730°C. The total belt line processing time was less than 2 hours, and this resulted in a planar cell efficiency of 17% on mono crystalline silicon (Fig.1.10d).

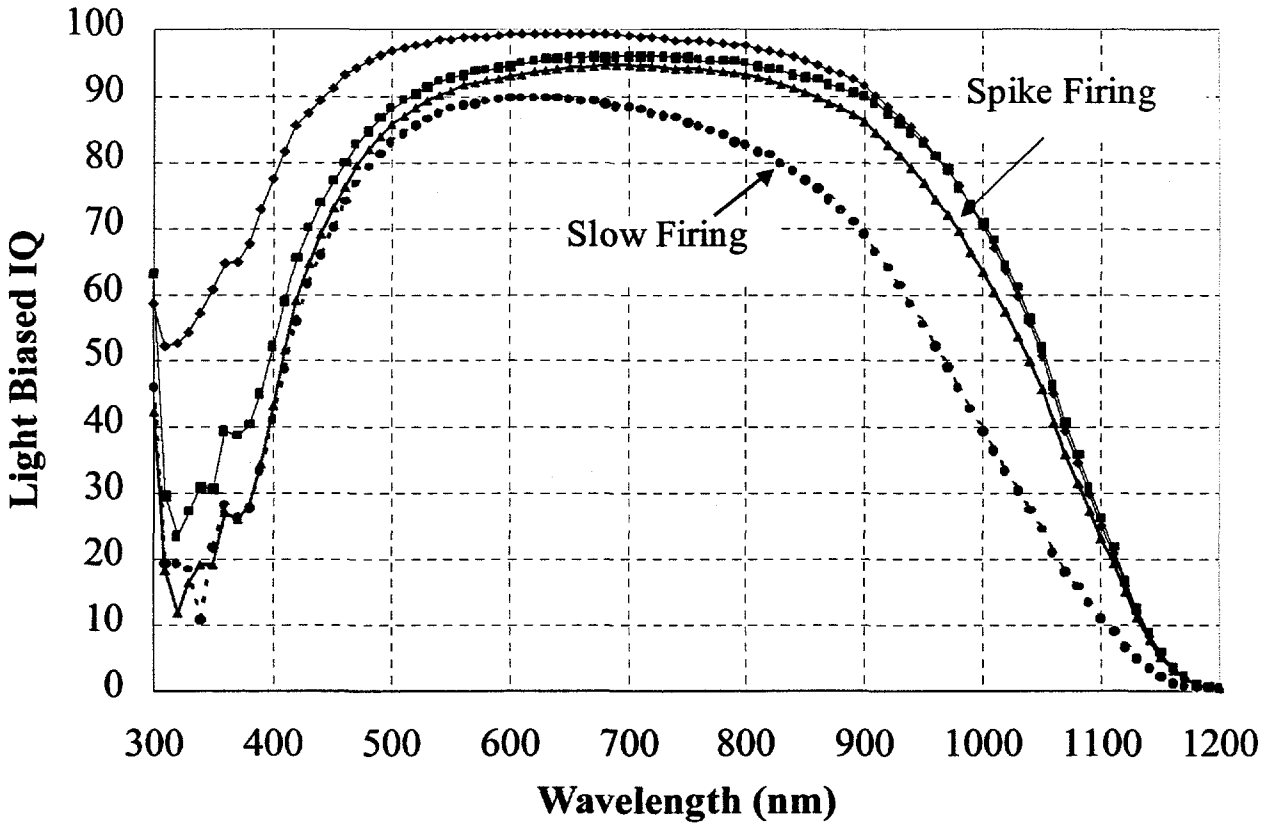


Fig. 1.11 Light-biased IQE of spike and slow fired cells

To further investigate the thermal stability of the defect gettering and passivation from the phosphorus gettering and simultaneous Al and PECVD SiN treatment, 4-$cm^2$, $n^+$-p-$p^+$ solar cells were fabricated on 3-Ω-cm string ribbon substrates. After the above gettering and hydrogenation treatments, which also form the emitter, BSF, and AR-coating, two screen-printed contact anneal furnace profiles were investigated for defect passivation preservation: i) slow firing – in which the peak temperature in the three zone belt line furnace was 700°C with a peak zone dwell time of 30 seconds and ii) spike firing – in which the peak temperature was increased while the dwell time was reduced.

Preliminary cell results shown in Table 1.1 illustrates that there is significant improvement in cell $V_{oc}$ and $J_{sc}$ that is attributed to the preservation of defect passivation during spike firing. The long wavelength IQE of devices shown in Fig. 1.11 also suggest that spike fired cells have higher effective diffusion length than slow fired cells. This study has resulted in a cell efficiency of 14.9% under AM1.5G, 100 W/cm$^2$, 25°C and independently confirmed on String ribbon silicon using industrially viable device fabrication technologies.

Table 1.1: Summary of IV characteristics of spike and slow fired solar cells

| **Process** | | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (mV) | FF | Eff. (%) |
|---|---|---|---|---|---|
| **Spike Firing** | **Average** | 31.2 | 582 | 0.736 | 13.7 |
| | **High** | 32.5 | 595 | 0.770 | **14.9** |
| **Slow Firing** | **Average** | 30.6 | 566 | 0.603 | 10.5 |
| | **High** | 31.0 | 565 | 0.688 | 12.0 |

Next generation cells will involve fabrication of belt line bifacial cells on thin PV grade Si. Model calculations (Fig.1.1) show that 100 μm thick cells with a bulk lifetime of 20 μs can produce 17% efficient SP cells, even without surface texturing, if the spatially averaged back surface recombination velocity can be reduced to ≈100 cm/s. Investigations on growing high-quality oxide layers in a belt line furnace are currently underway to realize the stack passivation with this equipment. The approach outlined in this paper can transform today's 12-14% efficient industrial cells on 300-400 μm thick Si to greater than 17% SP cells on 100-200 μm thick Si in the future.

## 1.7 Conclusions

Rapid Thermal Processing of each layer of a silicon solar cell was investigated and optimized. It was shown that an RTP alloyed, SP Al-BSF, formed in 2 minutes yields low $S_{eff}$ of 200 cm/s on 2.3 Ω-cm Si. In the same thermal cycle, an effective RTO layer can be grown for front surface passivation. A novel stack passivation scheme (consisting of plasma SiN stacked on top of an RTO layer) was developed that can attain S values approaching 10 cm/s on 1.3 Ω-cm Si and $J_{oe}$ values as low as 230 $fA/cm^2$ and 50 $fA/cm^2$ on 40 Ω/□ and 90 Ω/□ phosphorus diffused emitters, respectively. These emitters were formed in an RTP unit or a belt line furnace in 3 to 7 minutes by tungsten halogen lamp heating. Formation of the $n^+$ emitter, front surface oxide passivation, and Al-BSF by RTP resulted in a substantial reduction in cell processing time. Cell efficiencies of 19.1% and 17% were achieved on FZ Si using photolithography and SP contact techniques, respectively. SP bifacial cells with stack-passivated surfaces, as well as SP Al-BSF devices (full back metal coverage) formed rapidly in a commercial belt line machine also resulted in 17% efficiency. These results endorse the potential of rapid thermal technologies for cost-effective Si PV in the future.

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# CHAPTER II

# FABRICATION AND CHARACTERIZATION OF GRIDDED BACK CELLS (GBC)

# 2. FABRICATION AND CHARACTERIZATION OF GRIDDED-BACK CONTACT SOLAR CELLS

The RTO/SiN stack passivation scheme is applied to the fabrication of *gridded-back contact* (GBC) screen-printed solar cells. In order for these devices to be highly efficient, two important requirements must be met. First, the contact resistance ($\rho_c$) at the rear SP electrode must be low. Secondly, the area averaged $S_b$ (with contact coverage effect) must be reduced to levels well below 500 cm/s. Both of these issues are investigated in this section. A methodology for accurately extracting $\rho_c$ at the rear electrode is developed and applied in the analysis of GBC cells. The effect of rear electrode coverage on the overall surface passivation quality is also analyzed. Model calculations are performed to demonstrate whether the stack passivation and GBC scheme can be applied to thinner substrates without sacrificing performance.

## 2.1 Impact of the Back Contact on GBC Cells

The GBC device (Fig.2.1.a) has the potential for high-efficiency and bifacial performance. The structure is attractive from a manufacturing standpoint because it can be formed completely using rapid process techniques. Two features of the cell processing are particularly noteworthy. First of all, front and rear contacts can be fired in the same thermal cycle (*co-firing*), which simplifies processing and reduces cost. In contrast, the Al-BSF cell described in Chapter 1 requires a separate high-temperature (850°C) alloying step for $p^+$ junction formation. Moreover, the stress created by this Al-

BSF process can preclude application to thin wafers. Secondly, only a small quantity of metal paste is needed to form the back contact to the GBC structure. Simple calculations show that a gridded-back contact with a line height of 15 μm, line width of 200 μm, and line spacing of 2.5 cm requires ≈125 times *less* conductor paste than a full coverage BSF. Clearly, the GBC structure offers advantages from the standpoint of both process simplicity and material cost. The challenge, however, is to form a contact that reduces both resistance and recombination experienced at the rear side of the structure.

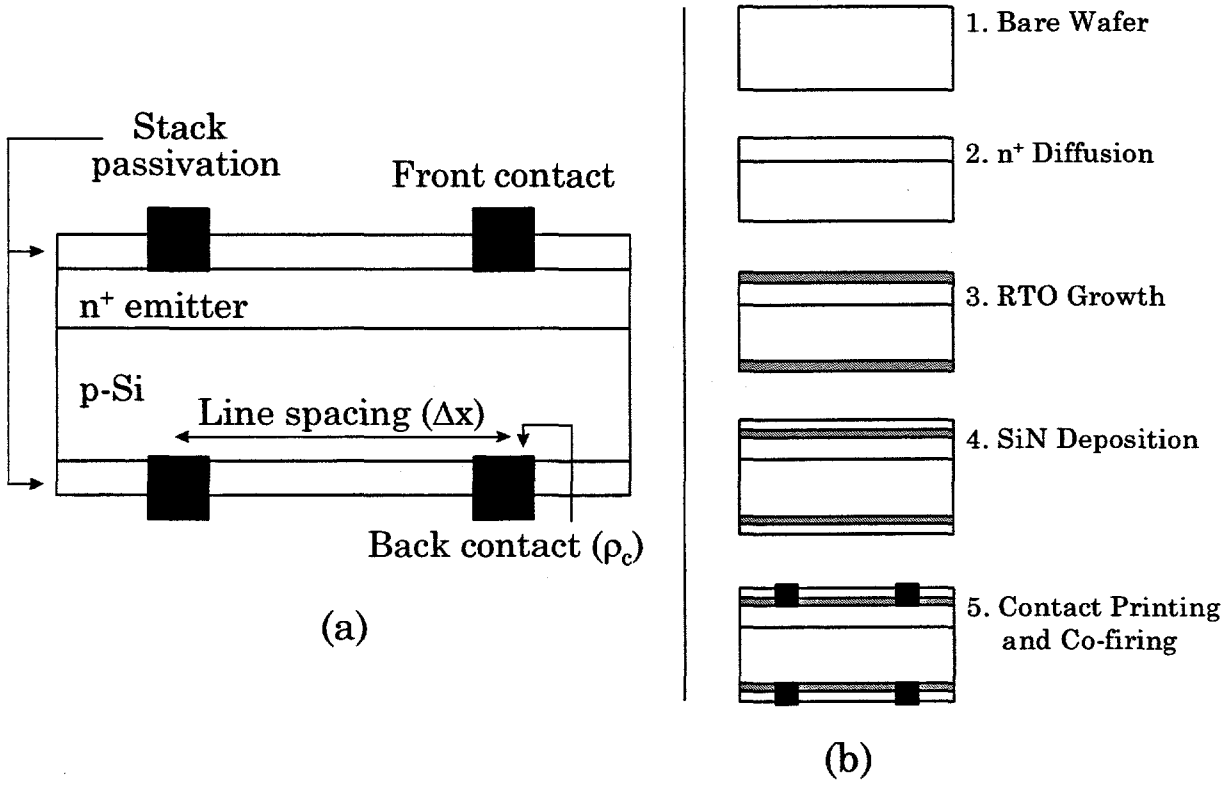
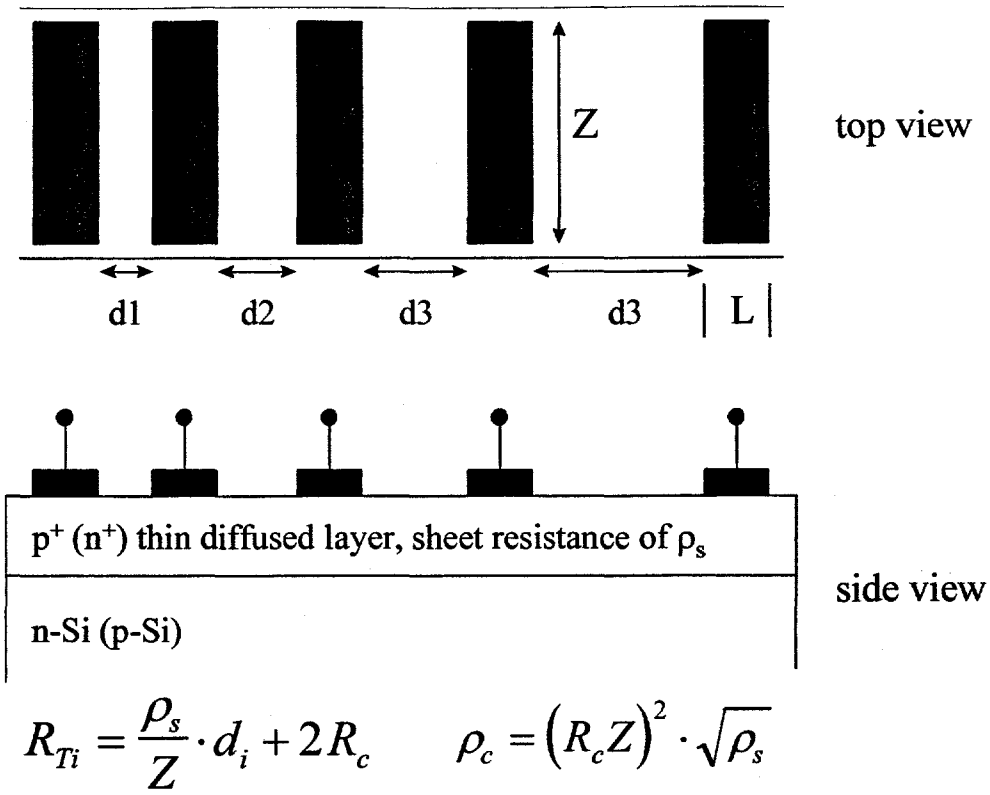



Fig.2.1. a) GBC solar cell structure. b) Simplified GBC process sequence.

In order to maximize the efficiency of a GBC device, the contact resistance ($\rho_c$) at the back must be low. This requirement is complicated by three factors. First, the bulk doping level of PV substrates is relatively low (<$310^{16}$ $cm^{-3}$), which creates a barrier to current flow at the metal-Si junction. Second, the printed lines must physically punch through the SiN layer before reaching and contacting the Si surface. Finally, to take advantage of the co-firing feature displayed in Fig.2.1.b, the above obstacles must be overcome with the same firing cycle used to form the front contacts. Because of these issues, selection and application of an appropriate rear contact conductor paste is imperative for achieving effective device performance.

### 2.1.1 Quantitative Assessment of $\rho_c$ for Rear Conductor Pastes

Two types of conductor paste (*Ferro Corp.*) were investigated for application to the back contact. The first was a pure Al paste and the second was a Ag paste mixed with a small fraction of Al additive. The pastes were printed in a special configuration known as the transfer length method (TLM), and fired in a beltline furnace using the 730°C/30 second SP firing cycle. A general TLM test structure is show in Fig. 2.2. It consists of a series of contacts separated by unequal distances.




$$R_{Ti} = \frac{\rho_s}{Z} \cdot d_i + 2R_c \qquad \rho_c = \left(R_c Z\right)^2 \cdot \sqrt{\rho_s}$$

Fig. 2.2. The TLM measurement structure.

Between any two adjacent pads, the resistance can be expressed as

$$R_T = \frac{\rho_s}{Z} \cdot d_i + 2R_c \tag{1}$$

where $R_c$ is the total contact resistance and $\rho_s$ is the semiconductor sheet resistance. Equation (1) represents a line with y-intercept equal to $2R_c$. Since $\rho_c$ is embedded in $R_c$, determination of the y-intercept from the $R_T$ versus $d_i$ plot allows for the extraction of $\rho_c$ [1]:

$$\rho_c = \left(R_c \cdot Z\right)^2 \sqrt{\rho_s}\,. \qquad (2)$$

It is important to realize that the semiconductor sheet thickness is assumed to be zero in the TLM technique. This is equivalent to saying the current flow in the diffused region is strictly one-dimensional. However, it is difficult to satisfy this requirement when attempting to measure $\rho_c$ to p-Si with $N_a$ of $\approx 10^{16}$ $cm^{-3}$ (typical for PV substrates). The problem is that substrate wafers are thick ($\approx$300 $\mu$m). This leads to two-dimensional current flow in the test structure. Clearly, the TLM technique is not ideally suited for thick wafers. More generally, simple techniques for determining $\rho_c$ to PV substrates are not readily available. Therefore, accurate determination of $\rho_c$ at the back contact is one of the challenges to developing the GBC structure.

In spite of this non-ideality, the TLM technique was applied as an initial characterization tool. Al and Ag pastes were printed onto p-Si wafers with varying $N_a$ (between $5x10^{15}$ and $2.2x10^{16}$ $cm^{-3}$) and different surface conditions. *Surface condition* refers to whether the Si wafer is bare or pre-coated with a SiN film. Again, this issue is particularly relevant for the GBC cell because the contacts must be fired through the passivating RTO/SiN stack (as shown in Fig.2.1.b). The TLM-extracted $\rho_c$ values for each process are shown in Fig. 2.3.

The lowest $\rho_c$ values are attained for Al paste fired directly on bare Si. This is attributed to the alloying reaction between Al and Si at elevated temperatures.

However, the same process is unsuccessful when the Al paste is fired through SiN. In this case, the SiN film serves as a diffusion barrier that prevents alloying between Al and Si. Since Al paste can not punch-through SiN at 730°C, $\rho_c$ values for this process are not measurable.

It is important to note that while the Al punch-through process is unsuccessful at the 730°C condition, a more energetic thermal cycle can be applied to achieve low $\rho_c$ with this paste. An example of this, where Al is fired through SiN at 850°C in two minutes, is shown in Fig. 2.3. The $\rho_c$ values for this process are nearly as low as those attained for Al fired on bare Si. However, it is important to remember that high-temperature can not be applied to a co-firing process because the front contacts would quickly diffuse through (shunt) the emitter junction and destroy the device. If such temperatures were required for back electrode formation, the front contacts would have to be fired separately. This would increase process complexity and fabrication time. For these reasons, the pure Al paste is essentially incompatible with the *co-fired* GBC structure. However, high-temperature firing could potentially be applied to form a local Al-BSF device.

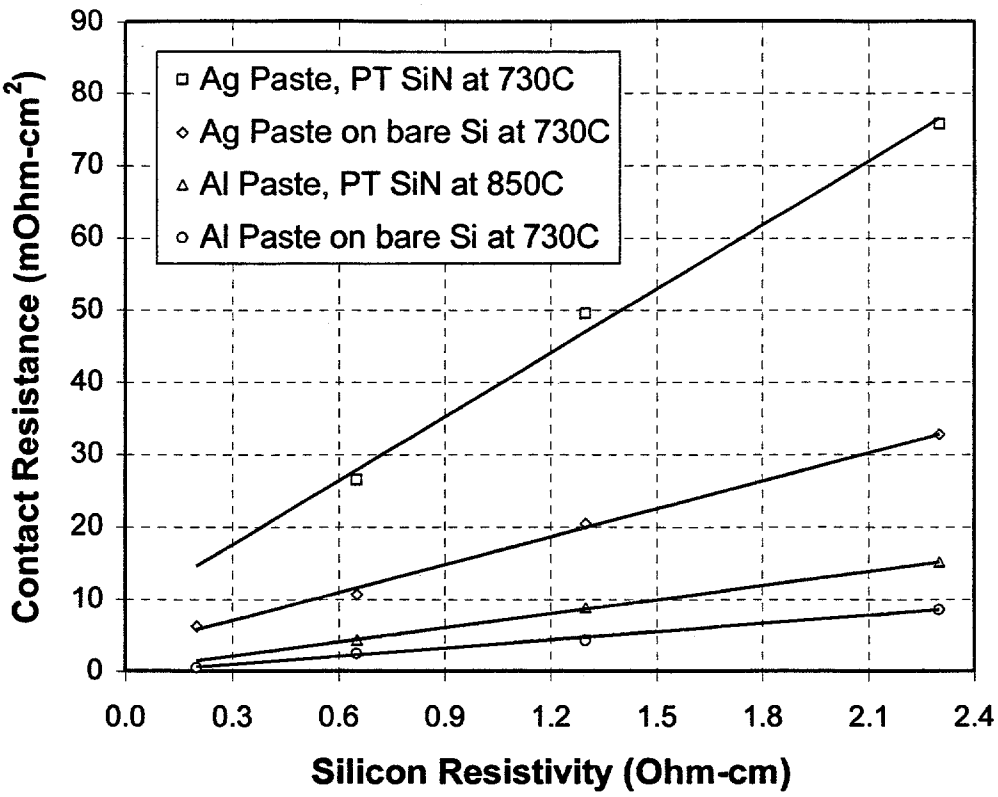



Fig. 2.3. Contact resistance for Ag and Al pastes on p-type Si. The hotzone firing temperature was set to 730°C. PT signifies a *punch-through* process.

The results are notably different for the Ag paste. When fired using the standard 730°C/30 second beltline condition, the Ag paste successfully punches-through the SiN layer. This punch-through ability is aided by the glass frit content in the mixture. A small amount of frit in the paste can induce etching of the underlying material (in this case SiN), which results in excellent adherence of the printed lines to the substrate. While the ability of the Ag paste to punch-through SiN is attractive, the $\rho_c$ values for this process are approximately two times higher than for the same paste fired on bare Si, and approximately 10 times higher than for the Al paste fired on bare Si. In the next section, model calculations are performed to determine whether these $\rho_c$ levels are acceptable for effective device operation.

While it is believed that the trends in Fig. 2.3 are representative of the $\rho_c$ behavior, it is probable that the absolute $\rho_c$ values are affected by the deviations from the ideal TLM setup. To further investigate this issue, an alternative $\rho_c$ extraction methodology particularly suited for solar cell back contacts was developed. The details of this methodology and the results of its application are described below.

### 2.1.2 Quantitative Assessment of $\rho_c$ by a Combination of One Dimensional Power Loss Modeling and Cell Fabrication

The ohmic losses associated with the contacts in a conventional cell (with full back coverage) are shown in Fig. 2.4. R1, R2, R3, R4, R5, and R6 represent the bus bar resistance, grid finger resistance, front contact resistance, emitter sheet resistance, substrate resistance, and rear contact resistance, respectively.

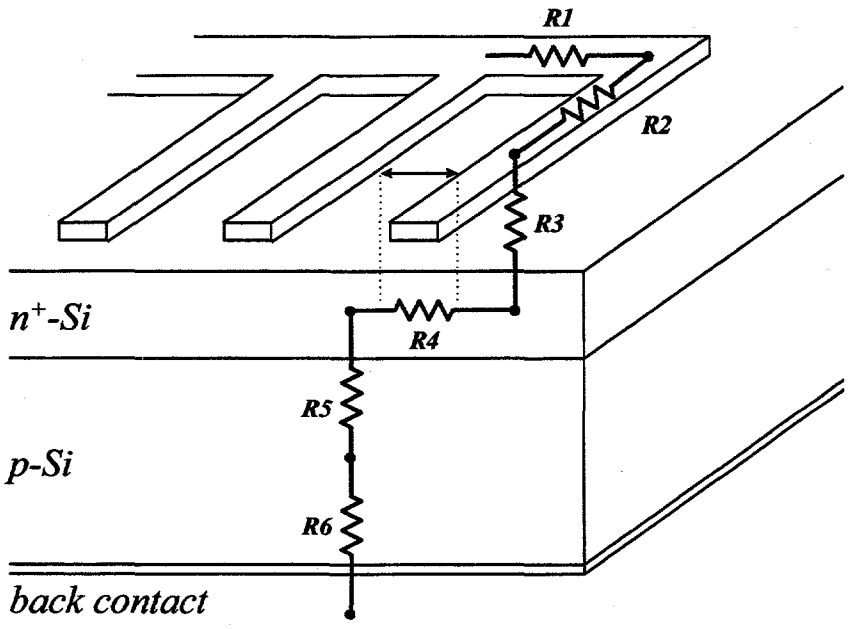



Fig. 2.4. Solar cell resistances. $R_1$, $R_2$, $R_3$, and $R_4$ exist for each gridline segment but are not shown in the figure.

Expressions for the power loss associated with each resistive component are given in Equations (3)-(7) [2]. (The power loss at the rear contact is typically neglected because of the full area coverage.) All geometric variables used in these equations are defined in Fig. 2.5.

$$P_{lateral-sheet} = \frac{2}{3} J_L{}^2 nab^3 \rho_{sheet} \tag{3}$$

$$P_{contact-front} = 2J_L{}^2 nab^2 \left(\rho_c \cdot \rho_{sheet}\right)^{1/2} \tag{4}$$

$$P_{finger} = \frac{4}{3}\left(J_L{}^2 na^3 b^2 \rho_{metal}\right) / \left(h \cdot w_{finger}\right) \tag{5}$$

$$P_{bus} = \frac{2}{3}\left(J_L{}^2 a^2 n^3 b^3 \rho_{metal}\right) / \left(h \cdot w_{bus}\right) \tag{6}$$

$$P_{bulk} = 2J_L{}^2 nab\rho_{bulk} t \tag{7}$$

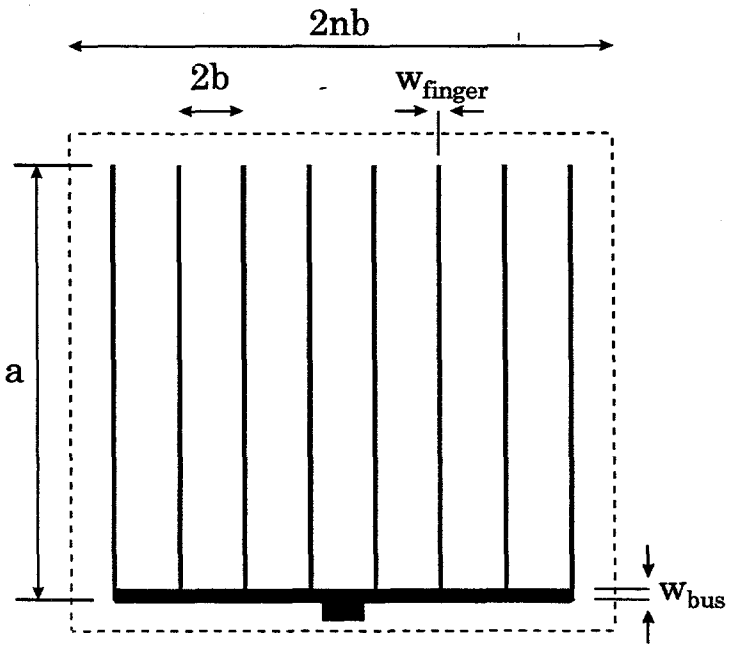



Fig. 2.5. Simple front contact pattern.

The analysis of this conventional cell can be extended to account for a gridded-back contact by simply adding a *rear contact resistance* and a *lateral bulk (sheet) resistance*. The expressions for these two loss components are direct analogies of Equations (3) and (4) with the bulk semiconductor properties substituted for the emitter sheet resistance:

$$P_{contact-back} = 2J_L^2 nab^2 \left(\rho_c \cdot \rho_{bulk}\right)^{1/2} \tag{8}$$

$$P_{lateral-bulk} = \frac{2}{3} J_L^2 nab^3 \rho_{bulk} \tag{9}$$

Together, Equations (7) and (9) represent a one-dimensional approximation to the two-dimensional problem at hand. The assumption is that the resistive losses created by the vertical and horizontal current flow in the base are independent and additive (a simplification that results in a "worst-case" resistance calculation). The validity of this assumption becomes evident later in this section. The overall solar cell series resistance can be calculated by summing all of the applicable power loss terms above and dividing by the *active area* current density $J_L$:

$$R_s = P_{total} / J_L^2 . \tag{10}$$

Equations (3)-(10) were incorporated into a computer model and used to simulate FF response for different back contact structures. The primary objective was to

determine the effects of the back $\rho_c$ and rear contact spacing ($\Delta x$) on $R_s$ and FF in GBC devices. Simulated FFs for 0.65 and 1.3 Ω-cm p-Si substrates are shown in Fig. 2.7 and Fig. 2.8. Experimental values were generated with the test structure shown in Fig. 2.6. The back contact to this test structure was formed by firing Ag paste through SiN at the standard 730°C/30 second condition. The measured data is also plotted in Fig. 2.7 and Fig. 2.8.

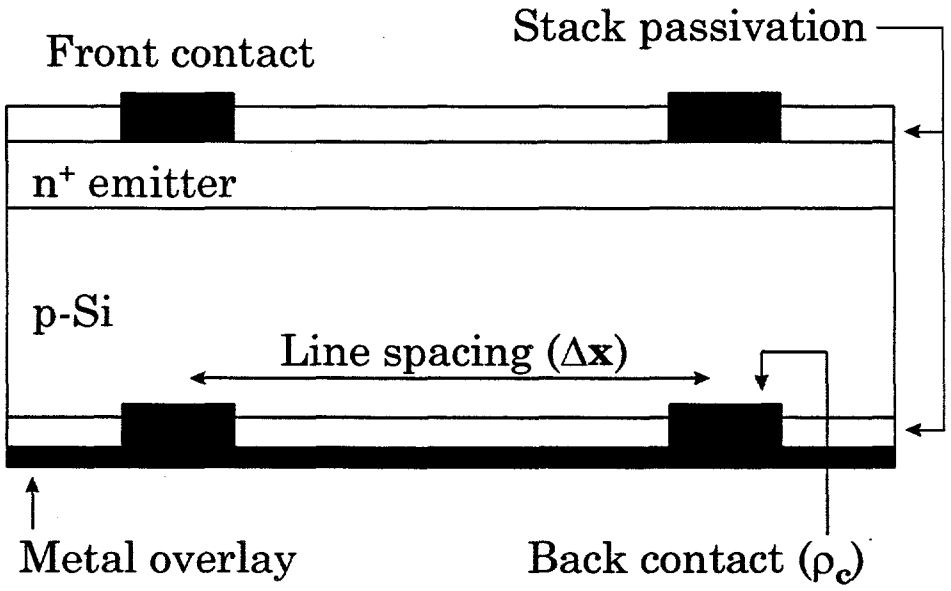



Fig. 2.6. Device structure used to study the effects of $\rho_c$ and x on FF. The effects of $P_{finger}$ and $P_{bus}$ for the rear electrode were removed by the metal overlay.

The simulations reveal that $\rho_c$ variation creates a shift in the FF versus $\Delta x$ plot. By comparing the measured data with simulation, the true $\rho_c$ value at the back electrode can be determined. Applying this methodology, $\rho_c$ values of approximately 10 mΩ-cm$^2$ and 1 mΩ-cm$^2$ are attained for Ag contacts to 1.3 Ω-cm and 0.65 Ω-cm p-Si, respectively. These values are substantially lower than the ones determined by the

TLM technique. The modeling also indicates that the TLM-extracted $\rho_c$ values are inconsistent with the true device operation.

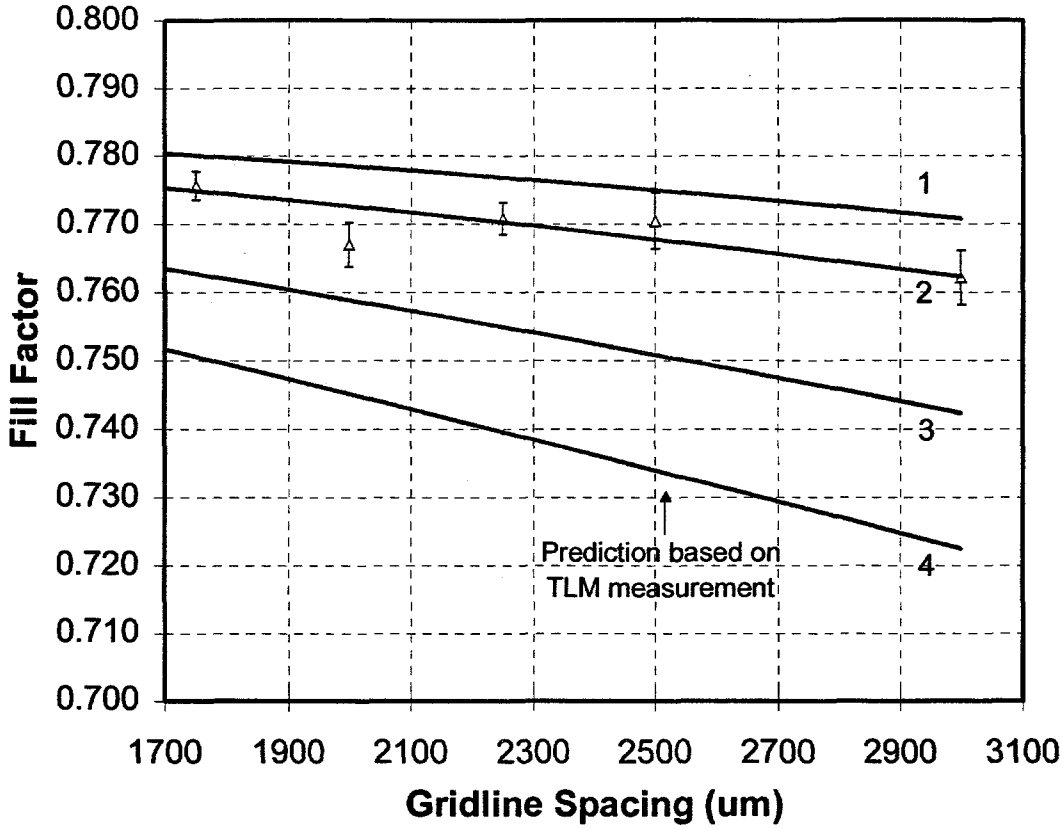



Fig. 2.7. Fill factor versus GBC rear line spacing for 1.3 Ω-cm substrate material. The solid lines are simulated values for rear $\rho_c$ values of: 1) 1 mΩ-cm$^2$, 2) 10 mΩ-cm$^2$, 3) 30 mΩ-cm$^2$, and 4) 50 mΩ-cm$^2$. The triangles represent experimental data.

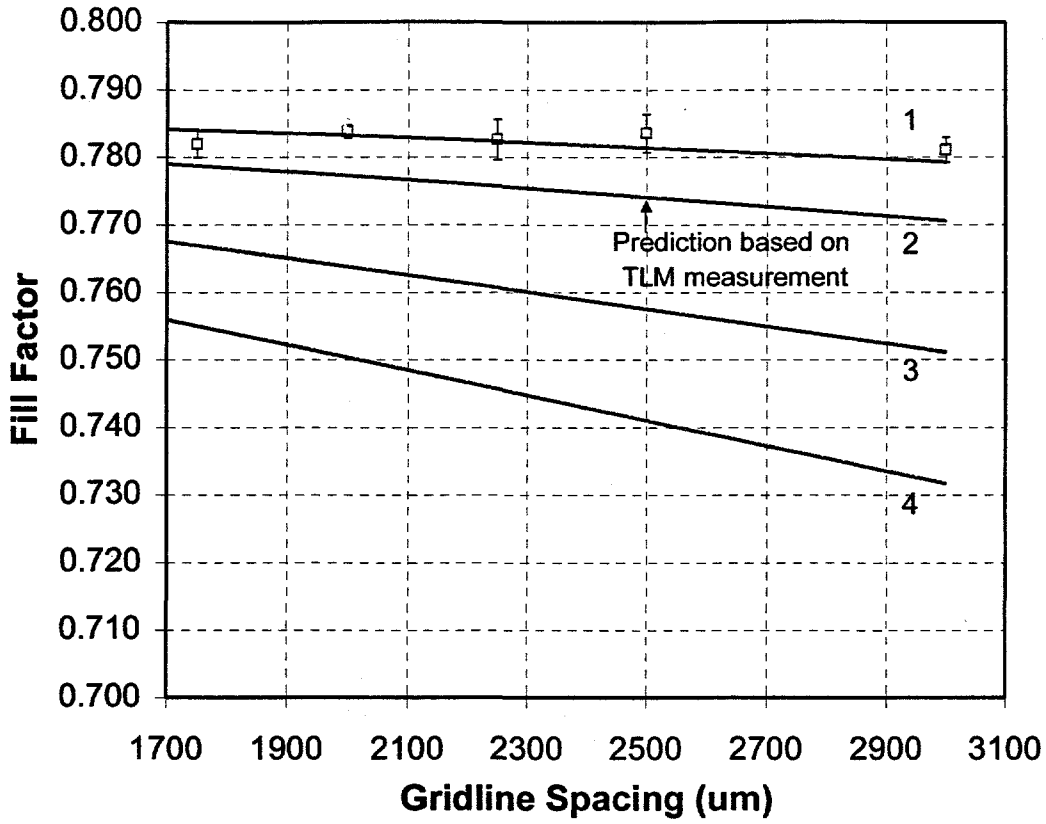



Fig. 2.8. Fill factor versus GBC rear line spacing for 0.65 Ω-cm substrate material. The solid lines are simulated values for rear $\rho_c$ values of: 1) 1 mΩ-cm$^2$, 2) 10 mΩ-cm$^2$, 3) 30 mΩ-cm$^2$, and 4) 50 mΩ-cm$^2$. The squares represent experimental data.

## 2.2 Fabrication and Analysis of GBC Solar Cells

In Table 2.1, GBC cells are compared to devices that lack an effective back surface treatment. (Here, *no passivation* refers to a fully SP Al co-fired with the front contact. This process results in poor $S_{eff}$.) The performance difference illustrates the stack's ability to effectively lower $S_b$. The Siemens CZ result is particularly noteworthy because it illustrates the importance of lowering $S_b$ for currently used PV grade Si. The importance of lowering $S_b$ will become more critical as PV substrates are cut (or grown) thinner. The 17% efficiency attained with the GBC structure on 0.65 Ω-cm FZ is essentially the same as the highest efficiency Al-BSF cell.

Bifacial devices with rear-illuminated efficiencies of 11.6% ($V_{oc}$=624 mV, $J_{sc}$=25.1 mA/cm$^2$, FF=0.743) were also achieved on 300μm thick 0.65 Ω-cm Si. The ratio of $J_{sc}$(*rear*)/$J_{sc}$(*front*) for these devices was ≈0.75.

As discussed previously, the effective $S_b$ for GBC cells is a combination of the recombination activity at the dielectric/Si interface and the metal gridline/Si interface. For reduced gridline spacing, the area coverage of the rear metal increases, which increases the effective $S_b$. This is clearly observed in Table 2.1. An IQE comparison for GBC devices with different Δx is shown in Fig.2. 9.

Table 2.1. Passivated rear SP solar cell performance. All cells contained rear metal overlays as in Fig. 2.6. The PV grade CZ Si was grown by Siemens Corporation. (*Verified at Sandia National Laboratory, †Average value of nine cells measured at UCEP)

| Material | Rear Surface | Grid Spacing | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF | Eff (%) |
|---|---|---|---|---|---|---|
| 0.65 Ω-cm FZ-Si | GBC | 2500 μm | 641 | 33.4 | 0.792 | 17.0* |
| | GBC | 1750 μm | 637 | 32.5 | 0.782 | 16.2† |
| | No Pass | --- | 622 | 31.8 | 0.801 | 15.8* |
| 1.3 Ω-cm FZ-Si | GBC | 3000 μm | 636 | 34.8 | 0.762 | 16.9† |
| | GBC | 1750 μm | 631 | 33.1 | 0.776 | 16.2† |
| | No Pass | --- | 609 | 32.8 | 0.786 | 15.7† |
| 0.8 Ω-cm CZ-Si | GBC | 2500 μm | 622 | 32.0 | 0.776 | 15.5† |
| | No Pass | --- | 611 | 31.0 | 0.782 | 14.8† |

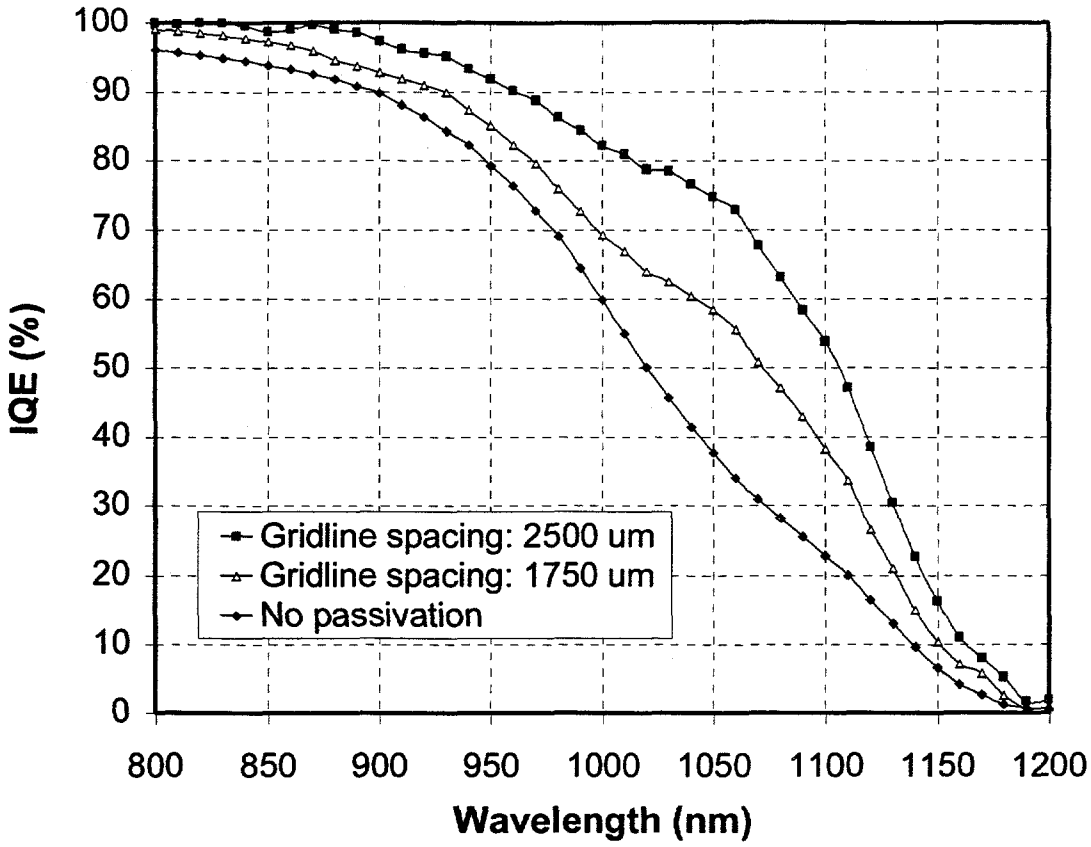



Fig.2. 9. Effect of rear gridline spacing on the long-wavelength IQE.

It was shown in the previous chapter that for 0.65 Ω-cm Si without any metal coverage, the stack passivation results in an S of ≈20 cm/s. However, for the GBC cell with $\Delta x$ of 2500 μm, the rear surface metal coverage is approximately 8.3%. The spatially averaged $S_b$ for the device is expected to be considerably higher than the S of 20 cm/s measured for the stack passivation alone. A combination of rear-illuminated IQE measurements and model calculation was performed in order to accurately extract $S_b$ for the cell.

The measured rear-illuminated IQE for the bifacial cell is shown in Fig. 2.10. (A light bias of roughly 0.25 suns was applied during the measurement.) Also shown in Fig. 2.10 is a family of simulated curves for the same device structure. A comparison of measurement to simulation shows that the GBC device experiences an effective $S_b$ of ≈340 cm/s near the $J_{sc}$ bias condition, which is a factor of 17 higher than the S value measured for the stack alone. It is evident that the 8.3% metal coverage has a substantial impact on the effective recombination at the rear side of the device. Nonetheless, this effective $S_b$ of 340 cm/s is within the target range established earlier by model calculations.

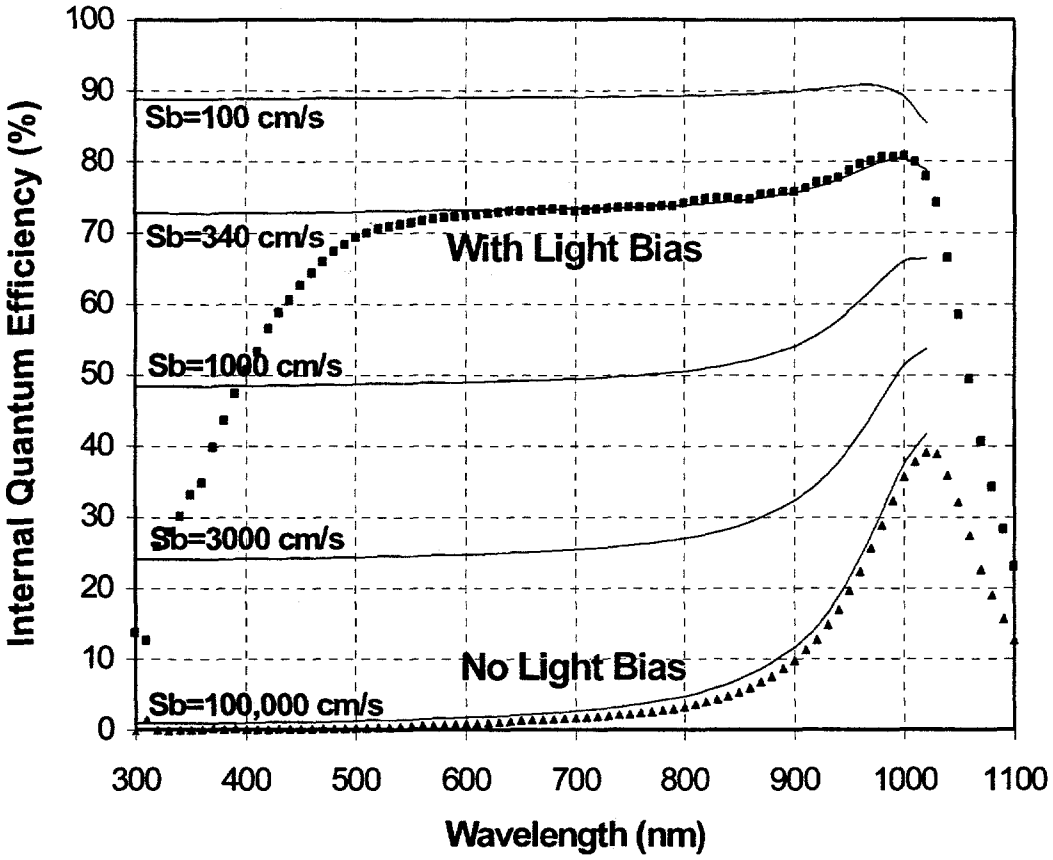



Fig. 2.10. Rear illuminated IQE of the bifacial solar cell. The solid lines represent simulation results. The dip in the measured IQE in the 300-500 nm range is caused by absorption in the SiN layer with index ≈2.25.

## 2.3 Modeling the Impact of the Stack Passivation for Thin Solar Cells

A primary advantage of the GBC structure is that it can be applied to thin substrates without causing breakage and yield problems. At the same time, however, the impact of $S_b$ on device performance becomes more pronounced for thinner substrates. If $S_b$ is high, the cell performance will suffer when substrate thickness is reduced. If $S_b$ is low, the performance will either remain the same or improve when the cell thickness is reduced. Model simulations were performed to predict the effect of substrate thickness for the GBC structure with effective $S_b$ of 340 cm/s on 0.65 Ω-cm Si.

All other important input parameters (emitter profile, $S_{front}$, surface reflectance) were gathered from separate measurements.

The results in Fig. 2.11 show that for the high $S_b$ case ($10^4$ cm/s), the $V_{oc}$ response falls significantly as substrate thickness is reduced. (This high $S_b$ situation is analogous to the rear surface being fully covered by a metal layer or a poorly formed Al-BSF region.) On the contrary, for the stack passivated GBC structure (with $S_{eff}$ of 340 cm/s), the $V_{oc}$ remains the same even after the cell thickness is substantially reduced. Corresponding cell efficiencies in Fig. 2.12 indicate that for thin ($\approx$ 100$\mu$m) material, the passivated GBC structure can result in an efficiency improvement of nearly 2% absolute over the non-passivated case. This compatibility with thin substrates makes the stack passivation scheme highly attractive for low-cost, high-efficiency commercial solar cell production.

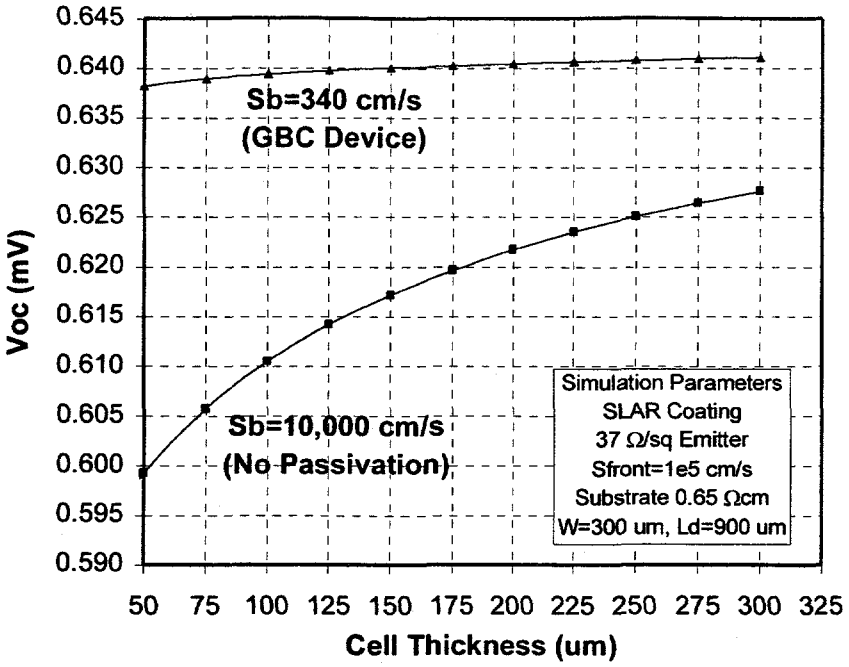



Fig. 2.11. Effect of reduced substrate thickness for $S_b$ of $10^4$ cm/s. $L_d$ signifies the minority carrier diffusion length in the bulk Si.

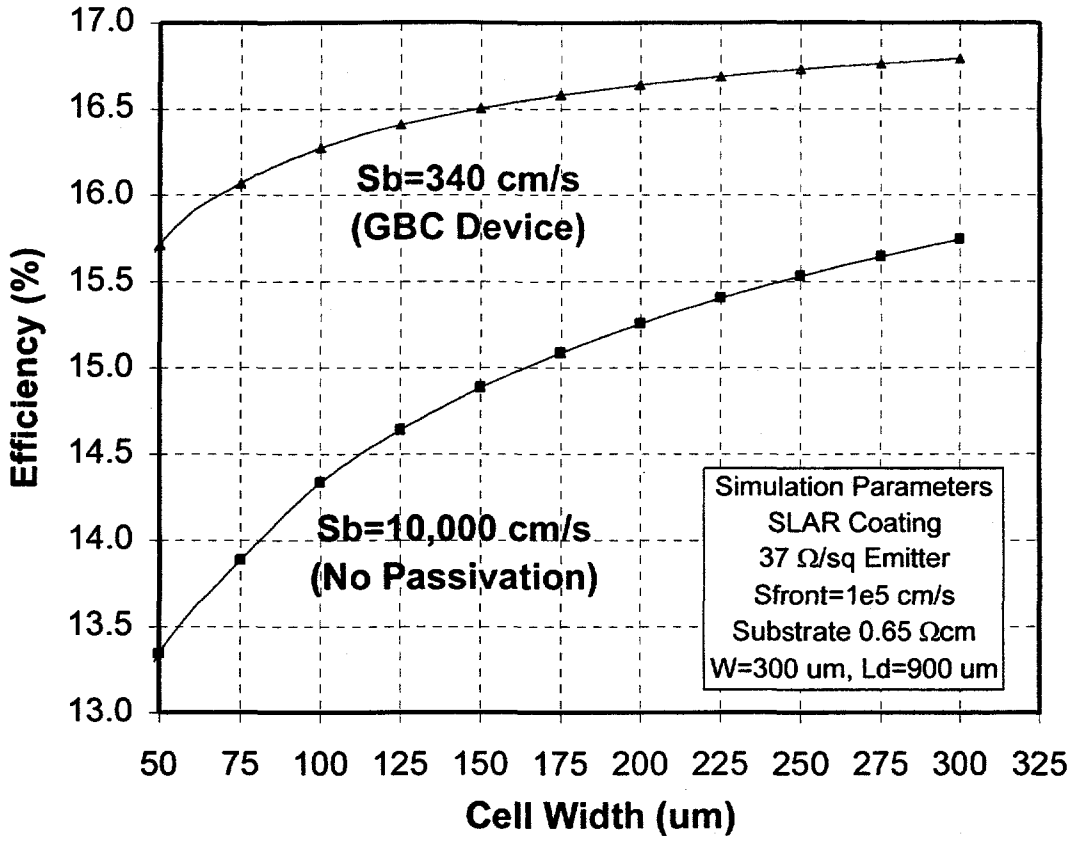



Fig. 2.12. Solar cell efficiency versus thickness for GBC and non-passivated cells. For the passivated rear device, the slight drop in efficiency for thin cells is caused by reduced light trapping quality and lower $J_{sc}$.

## 2.4 Conclusions

Screen-printed GBC cells with efficiencies as high as 17% have been fabricated on 0.65 Ω-cm Si. These cells are approximately 1% absolute higher in efficiency than those formed with ineffective rear surface treatments (or high $S_b$), and essentially equivalent to cells formed with optimized Al-BSF regions. In addition, rear-illuminated efficiencies as high as 11.6% have been achieved for fully SP bifacial structures. An attractive feature of the GBC fabrication process is that both front and rear contacts are co-fired together in the same thermal cycle. In this study, a methodology for accurately extracting the rear $\rho_c$ for GBC cells was developed. Applying this technique to the analysis of different conductor pastes showed that a Ag paste (containing a small

amount of glass frit and Al additive) is an appropriate material for a rear electrode. A low $\rho_c$ of $\approx$1m$\Omega$-cm$^2$ was measured for this material on 0.65 $\Omega$-cm p-Si, even after the metal was fired through a SiN layer. Rear-illuminated IQE measurements showed that the effective $S_b$ for the GBC device with rear metallization coverage of 8.3% was approximately 340 cm/s. Model calculations reveal that this passivation scheme can be applied to thinner substrates without experiencing any $V_{oc}$ degradation. This behavior, coupled with the fact that the RTO/SiN stack does not cause excess stress in thin substrates, demonstrates the strong potential of this GBC structure for future PV applications.

[1] D.K. Schroder, Semiconductor Material and Device Characterization, John-Wiler & Sons, 1990.

[2] D.L. Meier and D.K. Schroder, "Contact Resistance: Its Measurement and Relative Importance to Power Loss in a Solar Cell," *IEEE Trans. Electron. Dev*, **ED-31**, pp. 647-653, 1984.

# CHAPTER III

# LIGHT INDUCED DEGRADATION IN SCREEN-PRINTED FZ, CZ, AND MCZ SILICON SOLAR CELLS

# 3. LIGHT INDUCED DEGRADATION IN CZ, MCZ AND FZ SILICON CELLS FABRICATED BY FURNACE AND BELT LINE PROCESSING.

## 3.1 Introduction

Although Si grown by the Float Zone process is the highest quality silicon, Czochralski (Cz) grown silicon offers many advantages for cost effective solar cell fabrication because of lower cost and larger wafer size and a reasonably high quality single crystal substrate. In 1972, R.L. Crabb first observed a degradation in the minority carrier lifetime in 10 Ωcm Fz cell via a decrease in the long wavelength spectral response after photon illumination between 200-1000 nm over a period of 200 hours at 10 suns irradiation [1]. Then in 1973, Fischer and Pschunder observed a decrease in solar cell performance during the first few hours of illumination of 1 Ω-cm boron doped Cz Si. Light induced degradation (LID) of Cz material presents a problem for the overall performance of the finished solar cell [2]. Formation of interstitial oxygen ($O_i$) and boron ($B_i$) pairs after dissociation from a substitutional carbon ($B_i$-$C_s$) complex has been recently modeled as the source of LID [8]. Therefore, all boron doped silicon materials that have a high oxygen concentration should also suffer from LID. Multicrystalline Si was shown to degrade by Schmidt et. al. after a phosphorous gettering step, which raised the lifetime to a level that LID could be detected. Metallic impurities are generally not found in Cz materials and thus LID is readily observed. It has been shown that lifetime recovery of the light degraded samples is completely reversible by annealing the samples above ~175°C [5]. In addition, the degradation has been shown to be a strong function of $B_i$ and $O_i$ concentrations [8,9]. The degradation is found to decrease when

higher temperature steps are used during cell fabrication, possibly pointing to oxygen precipitation, which reduces the $O_i$ by forming clusters of oxygen [7].

Degradation is observed under forward bias and thermal treatments ≥ 100°C as well as under light bias indicating that the effect is not a photon-activated event but results from excess carrier injection [6]. The degradation decreases the long wavelength response and results in lower $V_{oc}$ , $J_{sc}$ and cell efficiency due to the lower lifetime [2].

### 3.2 Objective

The objective of this chapter is to improve the fundamental understanding of LID and observe its impact on low-cost screen printed devices fabricated with furnace as well as belt line diffusion. Ten different crystals were used with various amounts of B and O. Fz and MCz crystals were used to reduce $O_i$ content while Ga was used to replace B as the base dopant in some crystals.

### 3.3 Approach

Screen Printed (SP) devices reduce the production cost and shorten fabrication time, however, a 2% (absolute) loss in efficiency is incurred in the current SP cells as compared to photolithography (PL) cells. Single step furnace processing using the DOSS technique [14] and belt line processing (BLP) offer two viable solutions for high efficiency low cost solar cells. By using conventional furnace processing (CFP)

methods, similar to the DOSS technique an in-situ oxide can be grown for passivation, along with the front and back diffusion. This STAR process reduces the number of high temperature steps. On the other hand BLP offers shorter fabrication time. The losses due to BLP compared with CFP are analyzed in this paper with special attention paid to light induced degradation in CZ, MCZ and FZ Si cells fabricated by both techniques.

## 3.4 Experimental

Cell Fabrication Techniques

1. Conventional Furnace Processing (CFP) using DOSS Technique
   1.1. RCA clean
   1.2. Solid source preparation (spin-on phosphorous application 200°C)
   1.3. Sample diffusion and oxidation 60 minutes and 7.5 minutes at 925°C respectively
   1.4. $SiN_x$ single layer AR coating by direct HF PECVD 300°C
   1.5. Screen Printed Al BSF 860°C belt fired
   1.6. Screen Printed Front metallization 760°C

2. Belt Line Processing (BLP)
   2.1. RCA clean
   2.2. Spin-on phosphorous applied to sample 150°C hot plate bake
   2.3. Belt Line furnace diffusion 925°C 6 minutes

2.4. Spin-on glass removal, HF dip

2.5. $SiN_x$ single layer AR coating by direct HF PECVD 300°C

2.6. Screen Printed Al BSF 860°C belt fired

2.7. Screen Printed Front metallization 760°C

## 3.5 Results and Discussion

### 3.5.1 FTIR Measurements

Table 3.1 shows the C and O content for all ten crystals used in this investigation. FTIR measurements showed no appreciable substitutional carbon ($C_s$) content in the boron-doped samples. According to a recently proposed model by Schmidt and Aberle [3], $B_iC_s$ pairs dissociate to form the more detrimental $B_iO_i$ defect. Trap concentrations are estimated to be around $1x10^{12}$ $cm^{-3}$, which is below the detection limit of the FTIR measurement at room temperature. Therefore bulk lifetime and cell efficiency degradation with light exposure time were used to detect and understand evolution of defect.

Table 3.1: Material specifications

| *Measured at GT* | | | | | |
|---|---|---|---|---|---|
| **Material** | **Thickness** | **ρ(Ωcm)** | **NA ($cm^{-3}$)** | **$O_i$ (ppma / atoms per $cm^{-3}$)** | **$C_s$ (ppma / atoms per $cm^{-3}$)** |
| 1 Cz Boron | 15.5 mils | 0.72 | 2.20E+16 | 9.654 ppma / 4.827e17 | 0 ppma |
| 2 Cz Boron | 15.5 mils | 0.70 | 2.23E+16 | 13.629ppma / 6.814e17 | 0 ppma |
| 3 MCz Boron | 15.5 mils | 5.25 | 2.65E+15 | 9.618 ppma / 4.809e17 | 0 ppma |
| 4 MCz Boron | 15.5 mils | 1.20 | 1.24E+16 | 1.258 ppma / 6.289e16 | 0 ppma |
| 5 MCz Boron | 15.5 mils | 4.75 | 2.90E+15 | 1.829 ppma / 9.143e16 | 0 ppma |
| 6 Fz Boron | 15.5 mils | 0.63 | 2.47E+16 | 0 ppma | 0.07 ppma / 3.64e15 |
| 7 Fz Boron | 15.5 mils | 4.10 | 3.41E+15 | 0 ppma | 0.07 ppma / 3.6e15 |
| 8 Cz Galium | 10 mils | 2.55 | 5.71E+15 | 12.01 ppma / 6.005e17 | 0 ppma |
| 9 Cz Galium | 10 mils | 4.15 | 3.37E+15 | 14.772ppma / 7.386e17 | 0 ppma |
| 10 Cz Galium | 10 mils | 33.30 | 4.04E+14 | 14.306 ppma / 7.135e17 | 0.04 ppma / 2.0e15 |

### 3.5.2 Effective Lifetime Measurements

As grown materials were first passivated by a 70nm $SiN_x$ layer deposited in a direct plasma PECVD at 300°C. The samples were analyzed by PCD lifetime measurements after a FGA at 400°C for 15 minutes. Effective lifetime, $\tau_{eff}$, values were plotted as a function of injection level. Then all the samples in Table 3.1 were degraded under light bias of approximately 1 sun for more than 24 hours and re-measured. Figure 3.1 shows

how the Boron doped Cz sample #1 with 10 ppma $O_i$ degrades under light bias as a function of exposure time. Lifetime measurements were made every twenty minutes for the first hour then a final measurement was made for the stabilized degraded $\tau_{eff}$ after more than 24 hours of illumination. The number of traps is clearly seen to increase with the exposure time because of the $\tau_{eff}$ continually decreases until the saturation value is achieved for complete degradation. Sample degradation as a function of time occurs in both finished solar cells as well as un processed substrates.

### 3.5.3 Light Induced Efficiency Degradation Due to $B_i$ and $O_i$

Table 3.1 shows the thickness, resistivity, C and O content, and the growth technique for the ten Si crystals used in this investigation. All ten samples were subjected to approximately 1 sun bias light at 25-27°C over various periods of time. Figures 1 and 2 show a graph of efficiency versus time for light degraded CFP and BLP solar cells. Boron doped Cz showed the most degradation in efficiency, dropping over 0.5% in absolute efficiency in less than three hours, regardless of cell processing technique. The Boron doped MCz (crystal #3) with the high $O_i$ concentration also showed a slight degradation for both processes. Gallium doped Cz showed no degradation in spite of high $O_i$ concentrations (Fig. 3.2). This indicates that Boron plays an important role in LID. The other two Boron doped MCz samples (#4 and 5) with low $O_i$ concentration showed no degradation. Thus, by limiting the $O_i$ concentration in a crucible grown sample, using the MCz growth technique no degradation is observed. This indicates that $O_i$ also plays a key role in causing LID [13]. This is further supported by the fact

that B doped FZ Si does not degrade because of the very low (undetectable) $O_i$ concentration.

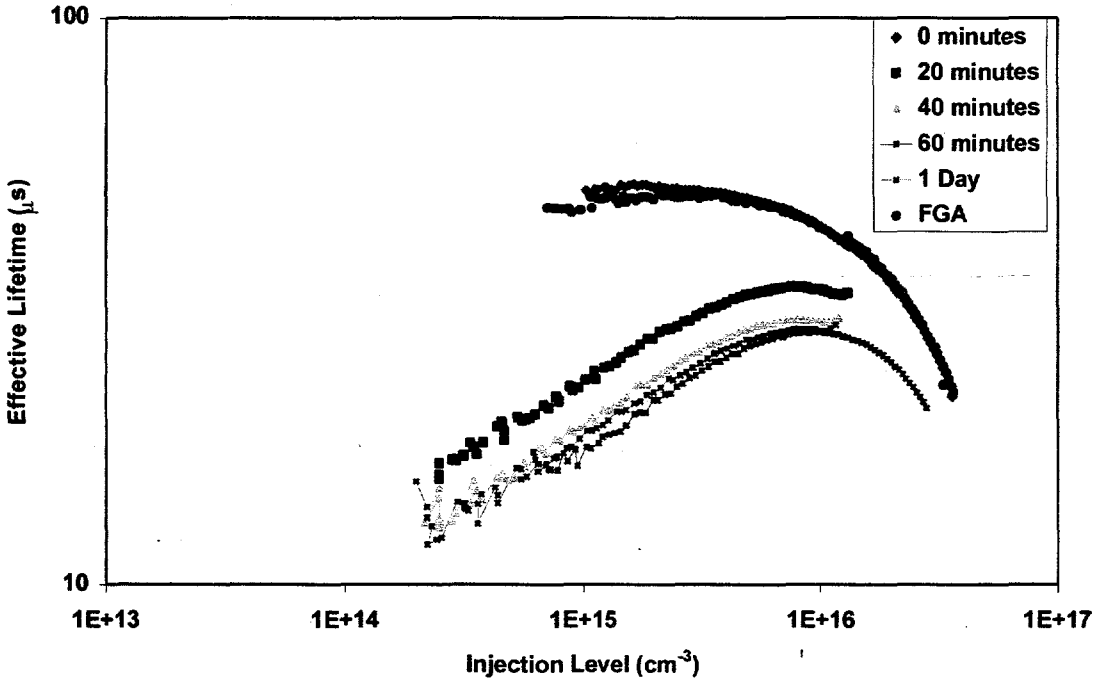



Fig. 3.1:Effective lifetime measured using Ron Sinton's lifetime tester. High $O_i$ and $B_i$ concentration cause up to 80% decrease in lifetime.

Figures 3.2 and 3.3 show that the overall degradation is similar for both cell technologies, CFP/SP and BLP/SP. The low resistivity samples Cz1 and Cz2 (0.6 cm) degrade 1% absolute in efficiency for both processes. The reduced $B_i$ in the MCz 3 sample (5 Ω-cm, 9.6 ppma $O_i$) sample due to the higher resistivity, resulted in a less severe efficiency decline of around 0.3% absolute. This indicates that LID trap concentration, $N_t$, is related to $B_i$. The direct correlation between $O_i$ concentration $N_t$

can also be seen in MCz samples. MCz3 and MCz5 samples have approximately equal $B_i$ concentrations but MCZ5 has an order of magnitude lower $O_i$ concentration and as a result MCz5 sample shows no degradation.

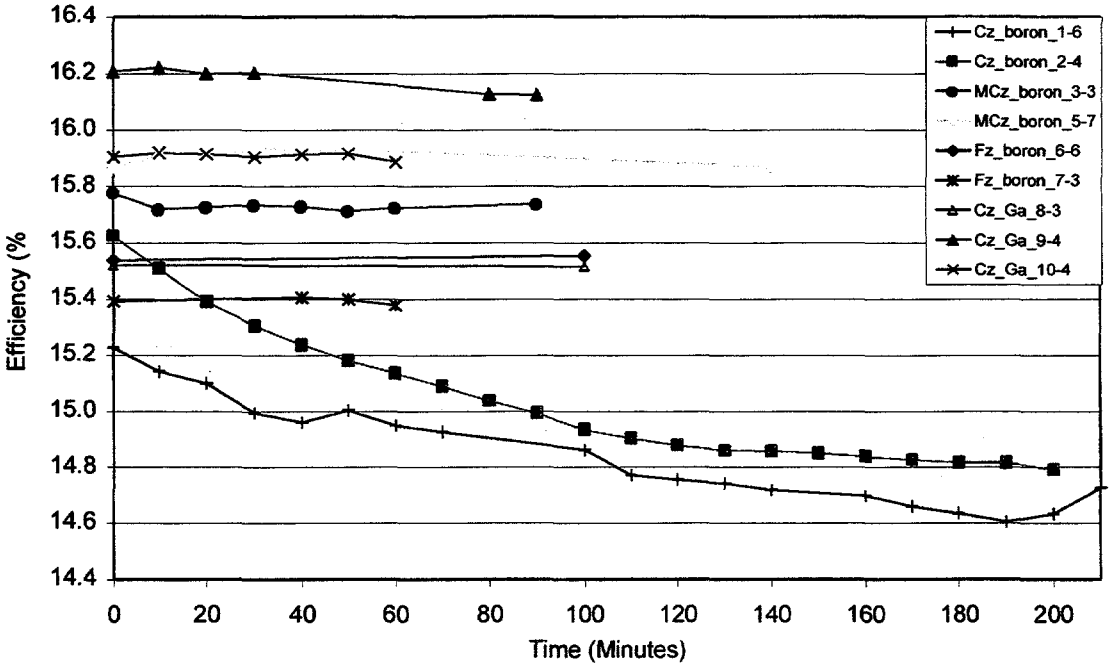



Fig. 3.2: Efficiency degradation of screen-printed BLP solar cells. Samples 1-7 are boron doped and 8-10 Ga doped according to table 3.1.

### 3.5.4 Role of Ga Doping and MCz Growth in Eliminating Light Induced Degradation

Many of the samples analyzed in this study showed no degradation (Fig. 3.1). Fz samples and Ga doped Cz material showed no decrease in either cell performance or initial lifetime values]. Boron doped magnetically grown Czochralski, MCz, showed

degradation only when the Oi concentration reached 10ppma. Figure 3.4 shows the annealed and degraded $\tau_{eff}$ for 4 different samples of similar base resistivity, 4-5 Ωcm, Ga or B doped, but varying $O_i$ concentrations. Only the Cz sample containing both $B_i$ and $O_i$ showed any degradation after 24 hours of 1 sun illumination. However, the Ga doped Cz sample with high $O_i$ concentration showed no degradation. Therefore the degradation is not inherent to the Cz process which traditionally contains high $O_i$ concentrations. It is also apparent from the B doped MCz sample with the low oxygen concentration that B alone does not cause the degradation. However, the MCz sample with high $O_i$ not shown in Fig. 3.4, does show same degradation, re-affirming that both $B_i$ and $O_i$ need to be present for degradation. This can be seen in Figs. 3.2 and 3.3. The increase in $\tau_{eff}$ for samples that do not show any degradation in Fig. 3.4, is currently being investigated and is believed to be the result of enhanced surface passivation due to the light exposure. The $SiN_x$ layer used for passivation achieved as low as 4 cm/s surface recombination velocity on the Ga doped 33 Ω-cm Cz sample at low $1x10^{14}$ injection level.

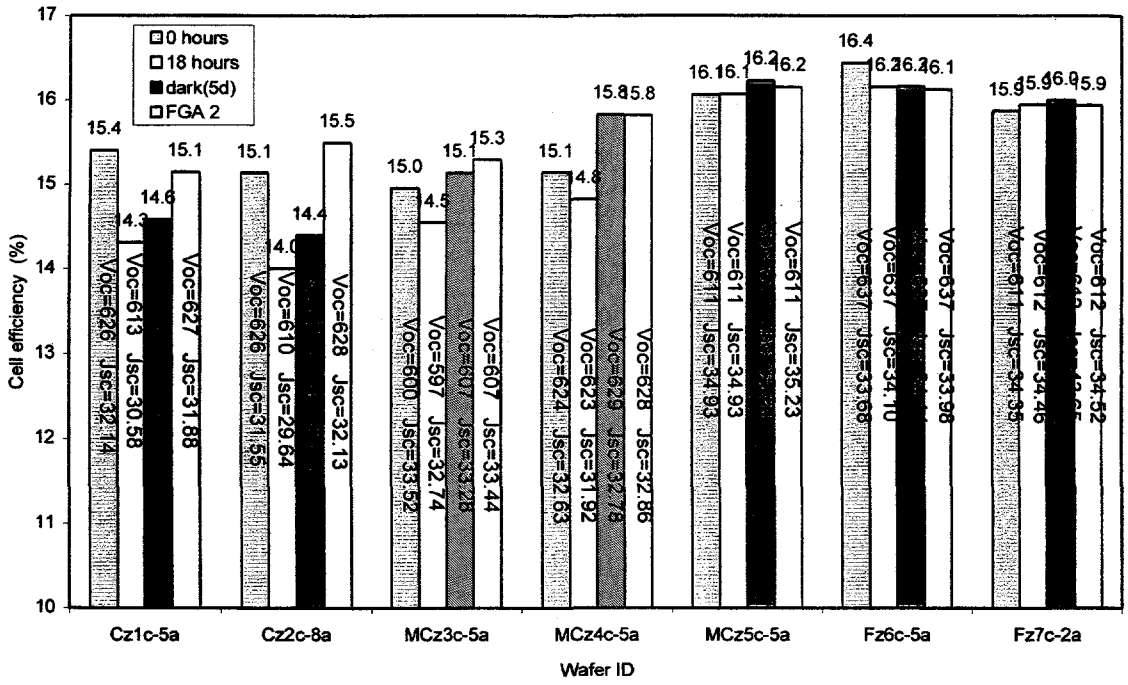



Fig. 3.3: Efficiency map of samples over a period of time initially after a FGA followed by light induced degradation then room temperature anneal in the dark for 5 days and finally another FGA at 450°C of the CFP cells.

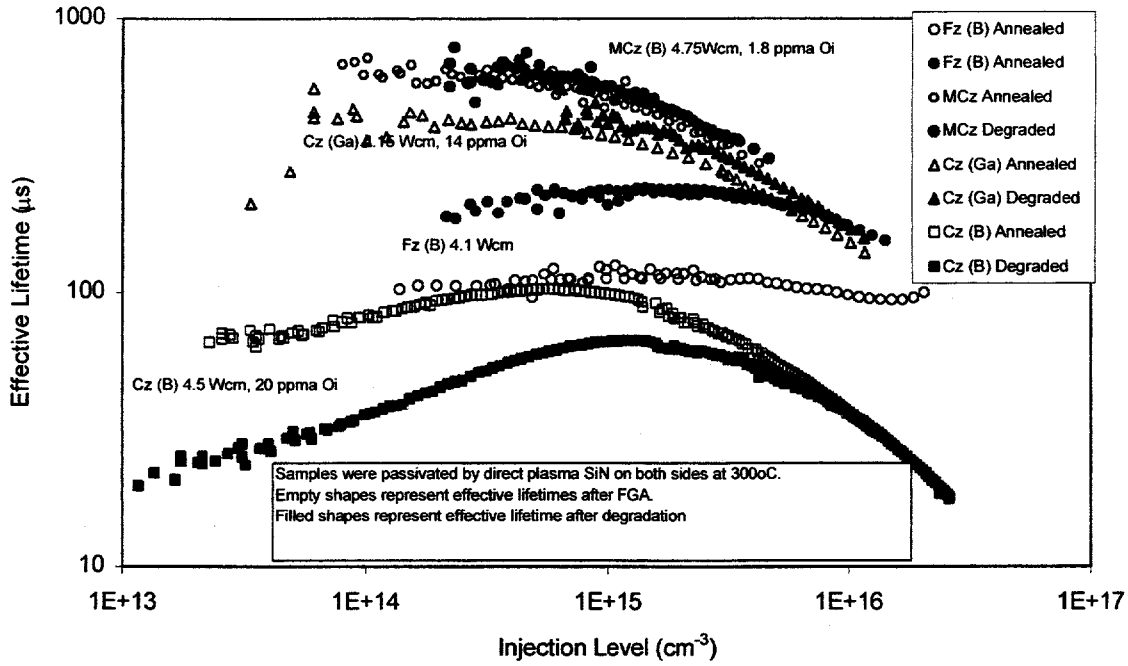



Fig. 3.4: Effective lifetime for 4-5 Ω-cm samples before and after degradation. Only samples with both high Oi and Bi content showed any degradation.

Figure 3.3 shows that the overall degradation of the finished solar cells was 8-10% of the initial values. This is similar to the degradation observed in the much higher efficiency cells (+20%) fabricated at Fraunhofer. Therefore the same amount of light exposure results in higher final efficiency of Fraunhofer cells. This suggest that the higher efficiency cells made at Fraunhofer perform better after LID either due to advance cell features or due to lower light induced trap concentration because of the higher temperature processing. Oxide precipitation during high temperature processing has been suggested to reduce degradation [5].

The two technologies (CFP and BLP) used to fabricate cells in this study gave similar starting efficiencies and showed similar amount of LID. This may be the result of a lower thermal budget and lower temperature processing used for both technologies which may not alter the basic material characteristics, such as $O_i$ concentration.

## 3.4 Conclusion

This study shows that light-induced degradation occurs only when both $B_i$ and $O_i$ are present in sufficient quantity. Boron doped FZ and low $O_i$ MCz, Boron doped Cz, and Galium high oxygen Cz samples analyzed in this paper clearly support the above observation. Samples with same oxygen concentration but higher resistivity showed lower degradation, due to a limited supply of $B_i$ available to form the trap level that causes the efficiency degradation. Gallium (Ga) doped samples showed no degradation regardless of the $C_s$ and $O_i$ content. MCz growth was able to limit the degradation by allowing lower $O_i$ content. This provides a means to achieve a more stable performance while still taking advantage of the Crucible growth method. Cz cells efficiencies were lower than FZ and MCz. However, low oxygen MCz cell efficiency was comparable to FZ cells Thus Ga doped MCz offers a great opportunity of low-cost high efficiency cells with no light induced degradation.

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# CHAPTER IV

# DEVELOPMENT OF HIGH EFFICIENCY MULTI-CRYSTALLINE SOLAR CELLS ON EUROSOLARE MULTI-CRYSTALLINE SILICON

# 4. DEVELOPMENT OF HIGH EFFICIENCY SCREEN-PRINTED MULTI-CRYSTALLINE SILICON SOLAR CELLS BY INCORPORATING BULK DEFECT PASSIVATION BY SIN

## 4.1 Introduction

In the previous chapters research was focused on single crystals. In the following chapters emphasis is placed on multi-crystalline silicon materials. Multi-crystalline silicon has the potential of achieving low cost and high efficiency solar cells. Multi-crystalline silicon substrates, however, contain defects and residual impurities as compared to single crystalline silicon. These impurities degrade the minority carrier lifetime in the bulk, which often lead to lower solar cell efficiency than in the single crystalline silicon. Therefore, in order to improve the bulk lifetime or the diffusion length of the minority carriers to meet the criterion of L/W >2, without adding to the cost of cell fabrication, low cost impurity gettering and defect passivation techniques must be developed.

Hydrogen from the SiN film has been reported to passivate the dislocations as well as grain boundaries [1] in multi-crystalline silicon substrates. In most of the work reported in the literature, the effect of high temperature anneal of the SiN film on multi-crystalline silicon without prior gettering has not been investigated systematically. Therefore, one of the objectives of this study was to investigate the bulk defect passivation due to SiN induced hydrogenation in Eurosolare grown cast multi-crystalline

silicon before and after the three high temperature anneals, namely emitter diffusion, BSF formation and contact firing, consistent with screen-printing technology.

In the present investigation, the bulk lifetime and hydrogen concentration measurements were performed before and after various heat treatments of the SiN film deposited on p-type, 0.8 Ω-cm, EuroSolare grown cast multi-crystalline silicon. Finally the screen-printed multi-crystalline silicon solar cells were fabricated and characterized.

## 4.2 Experimental

The process sequence used for the lifetime study and screen-printed solar cell fabrication on multi-crystalline silicon is outlined in Fig. 4.1. This sequence is completely manufacturable and is consistent with low-cost and high throughput.

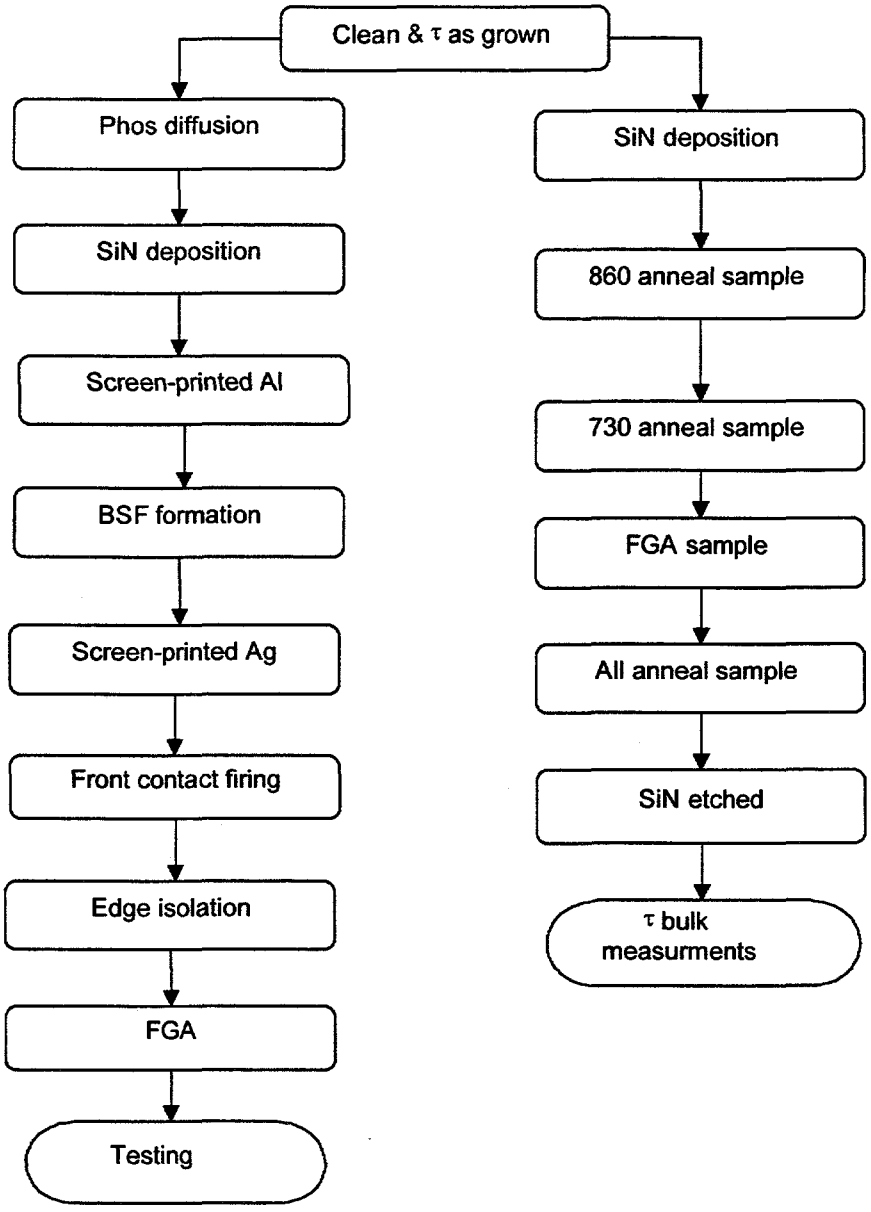



Fig. 4.1: Process sequence for belt line screen-printed silicon solar cell fabrication and lifetime studies.

### 4.2.1 Photo conductance decay (PCD) measurements of bulk lifetime after each high temperature anneal

Laser PCD lifetime measurements were performed on all the samples. To measure the bulk lifetimes in each sample, the SiN film was removed in 20% HF and then the samples were placed in 0.001M of $I_2$ (placed in sandwich zip lock bag) for the measurements. The results of the bulk lifetime measurements are summarized in Figure 4.2.

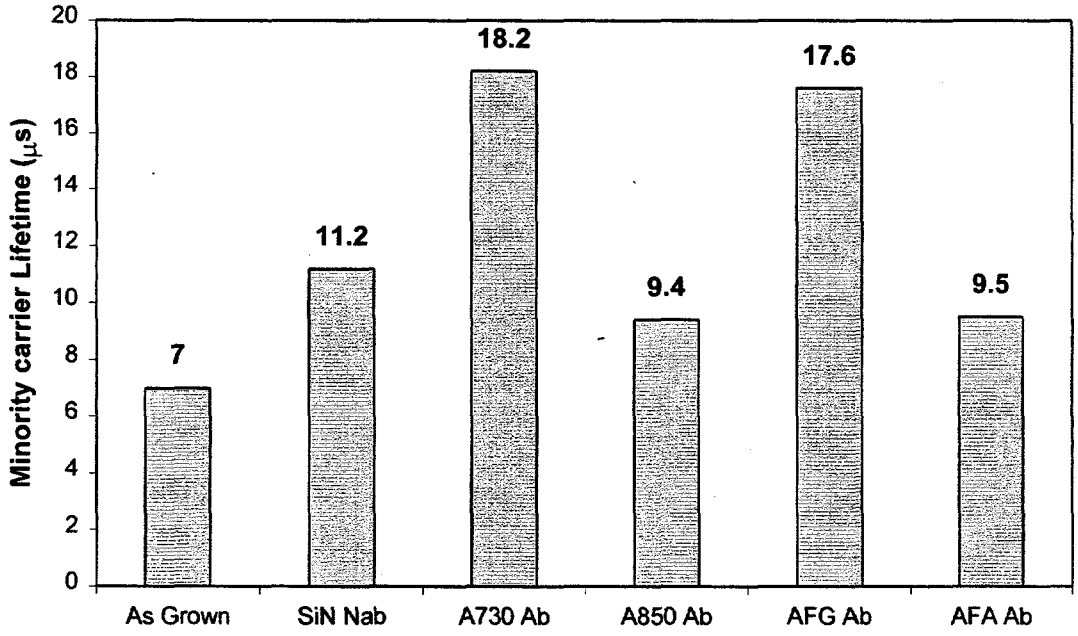



Figure 4.2: SiN-induced hydrogenation of cast (Euroslare) mc-Si (Note Nab – no anneal bulk lifetime; Ab – bulk lifetime after the prescribed heat treatment).

### 4.2.2 Hydrogen content measurements

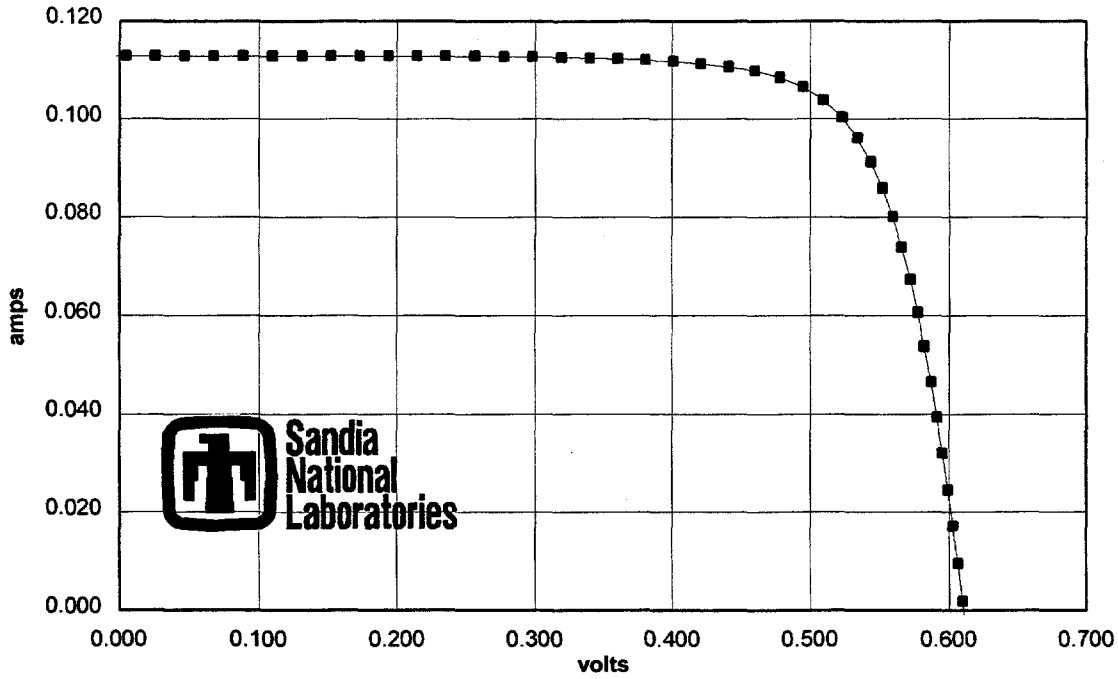
The hydrogen content of all the samples was measured by FTIR. The concentration of hydrogen for each sample was estimated using the Gaussian fit to the peak to determine the area under the absorption peaks.

### 4.2.3 Screen-printed solar cell characterization

The process sequence adopted for the fabrication of the screen-printed solar cells using the lamp heated belt line furnace is shown in Fig. 4.1. Selected solar cell results are given in Table 4.1. Figures 4.3 and 4.4 show the I-V characteristics of one of the cells and the corresponding internal quantum efficiency. Figure 4.5 shows the dark I-V analysis of this cell.

Table 4.1: Electrical characteristics of selected belt line screen-printed multi-crystalline silicon solar cells. Cell area is 4 $cm^2$ and the measurement is performed under AM1.5G, 100 $mW/cm^2$, 25°C.

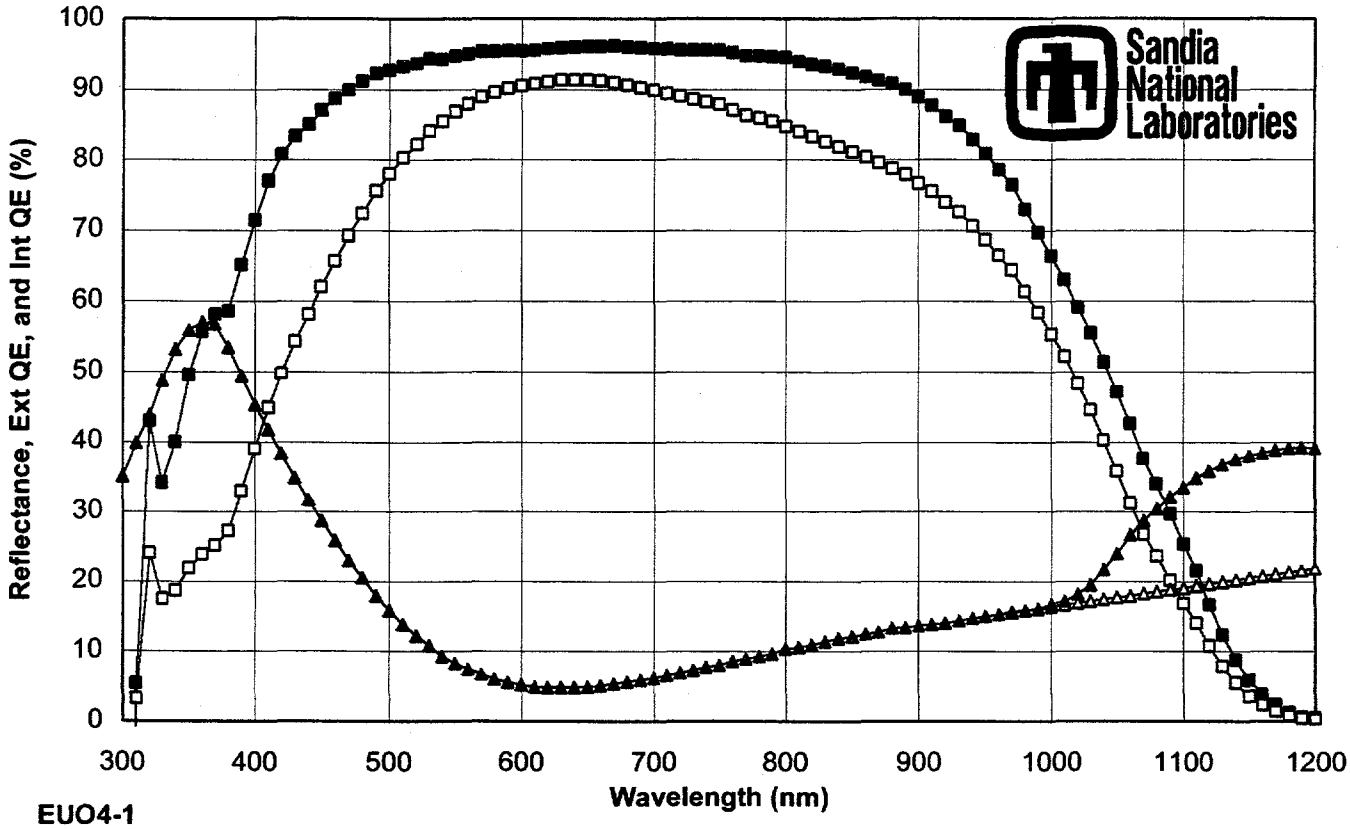
| Cell ID | $V_{oc}$ | $J_{sc}$ | FF | Eff | $n_{eff}$ | $Jo_{eff}$ | Rs | Rsh@-1 | Rsh@0 |
|---|---|---|---|---|---|---|---|---|---|
| | (mV) | ($mA/cm^2$) | | (%) | | ($A/cm^2$) | ($\Omega$-$cm^2$) | ($\Omega$-$cm^2$) | ($\Omega$-$cm^2$) |
| euo6-1 | 605 | 31.43 | 0.746 | 14.2 | 3.26 | 2.0E-12 | 0.59 | 680 | 1,590 |
| euo6-2 | 592 | 30.60 | 0.693 | 12.6 | 5.16 | 3.0E-12 | 0.54 | 82 | 318 |
| euo6-3 | 594 | 31.02 | 0.674 | 12.4 | 6.61 | 2.9E-12 | 0.56 | 67 | 190 |
| euo6-4 | 605 | 31.28 | 0.743 | 14.1 | 2.74 | 1.9E-12 | 0.59 | 5,648 | 25,456 |
| euo6-5 | 596 | 30.55 | 0.744 | 13.6 | 3.15 | 2.7E-12 | 0.50 | 1,183 | 2,320 |
| euo6-6 | 601 | 31.40 | 0.725 | 13.7 | 4.05 | 2.3E-12 | 0.77 | 381 | 790 |
| euo6-7 | 605 | 31.57 | 0.750 | 14.3 | 2.74 | 1.9E-12 | 0.49 | 20,122 | 46,465 |
| euo6-8 | 597 | 30.51 | 0.748 | 13.6 | 3.11 | 2.6E-12 | 0.53 | 1,510 | 3,437 |
| euo6-9 | 598 | 30.66 | 0.752 | 13.8 | 2.91 | 2.5E-12 | 0.61 | 1,835 | 2,545 |
| Average | 599 | 31.0 | 0.731 | 13.6 | | | | 3501 | 9235 |
| | | | | | | | | | |
| EUO4-1 | 612 | 32.37 | 0.757 | 15.0 | 2.34 | 1.4E-12 | 0.67 | 8,077 | 27,736 |
| EUO4-2 | 603 | 31.11 | 0.756 | 14.2 | 2.59 | 2.0E-12 | 0.55 | 8,828 | 21,582 |
| EUO4-3 | 602 | 31.25 | 0.765 | 14.4 | 2.43 | 2.0E-12 | 0.60 | 4,621 | 15,740 |
| EUO4-4 | 594 | 31.14 | 0.737 | 13.6 | 2.92 | 2.8E-12 | 0.69 | 3,842 | 8,153 |
| EUO4-5 | 605 | 31.61 | 0.745 | 14.2 | 2.96 | 1.9E-12 | 0.69 | 3,555 | 3,471 |
| EUO4-6 | 608 | 32.00 | 0.761 | 14.8 | 2.46 | 1.7E-12 | 0.63 | 25,261 | 30,488 |
| EUO4-7 | 599 | 31.68 | 0.713 | 13.5 | 4.77 | 2.4E-12 | 0.78 | 421 | 426 |
| EUO4-8 | 609 | 32.19 | 0.754 | 14.8 | 3.55 | 1.7E-12 | 0.56 | 1,324 | 1,441 |
| EUO4-9 | 602 | 31.64 | 0.750 | 14.3 | 3.04 | 2.1E-12 | 0.67 | 2,437 | 2,442 |
| Average | 610 | 32.18 | 0.757 | 14.9 | | | 0.62 | 11554 | 19888 |
| | | | | | | | | | |
| EUO1-1 | 597 | 32.10 | 0.680 | 13.0 | 6.54 | 2.7E-12 | 0.56 | 211 | 215 |
| EUO1-2 | 595 | 31.31 | 0.671 | 12.5 | 6.55 | 2.9E-12 | 1.22 | 163 | 172 |
| EUO1-3 | 592 | 31.58 | 0.650 | 12.2 | 9.17 | 3.2E-12 | 0.59 | 108 | 114 |
| EUO1-4 | 589 | 31.75 | 0.685 | 12.8 | 5.27 | 3.6E-12 | 0.66 | 312 | 331 |
| EUO1-5 | 591 | 31.77 | 0.690 | 12.9 | 5.77 | 3.3E-12 | 0.67 | 235 | 258 |
| EUO1-6 | 603 | 32.37 | 0.683 | 13.3 | 6.85 | 2.1E-12 | 0.85 | 154 | 184 |
| EUO1-7 | 584 | 33.22 | 0.638 | 12.4 | 7.15 | 4.6E-12 | 0.51 | 125 | 131 |
| EUO1-8 | 594 | 32.01 | 0.673 | 12.8 | 7.25 | 3.0E-12 | 0.66 | 168 | 164 |
| EUO1-9 | 598 | 31.91 | 0.711 | 13.6 | 5.49 | 2.6E-12 | 0.64 | 287 | 308 |
| Average | 595 | 31.93 | 0.694 | 13.2 | | | 0.63 | 244 | 260 |




| | | | | | |
|---|---|---|---|---|---|
| 03/03/99 12:50 PM | 25.0 °C | 3.58 $cm^2$ | 31.58 $J_{sc}$(mA/$cm^2$) | 0.768 FF | AM1.5G |
| **EUO4-1** | 0.9951 M* | 610.4 $V_{oc}$(mV) | 0.113 $I_{sc}$(A) | 14.80 % Eff | ONE SUN |
| | 1.0000 S* | 503.5 $V_{mp}$(mV) | 0.105 $I_{mp}$(A) | | |

Used mask #007

Figure 4.3: Lighted I-V curve for lamp heated belt line screen-printed multi-crystalline (EUO4-1) solar cell.




**EUO4-1**

Spectral Response: x:\ruby\asr\99028-07.s01 Reflectance: x:\ruby\rfl\99028-07.csv
Current Density at 1 kW/m2 (mA/cm2): 31.9 (Global), 31.7 (Direct), 27.9 (Space)
Weighted Front Reflectance (%): 12.8 (Global), 12.2 (Direct), 13.4 (Space)

Figure 4.4: Spectral response of the lamp heated belt line screen-printed multi-crystalline (EUO4-1) silicon solar cell.

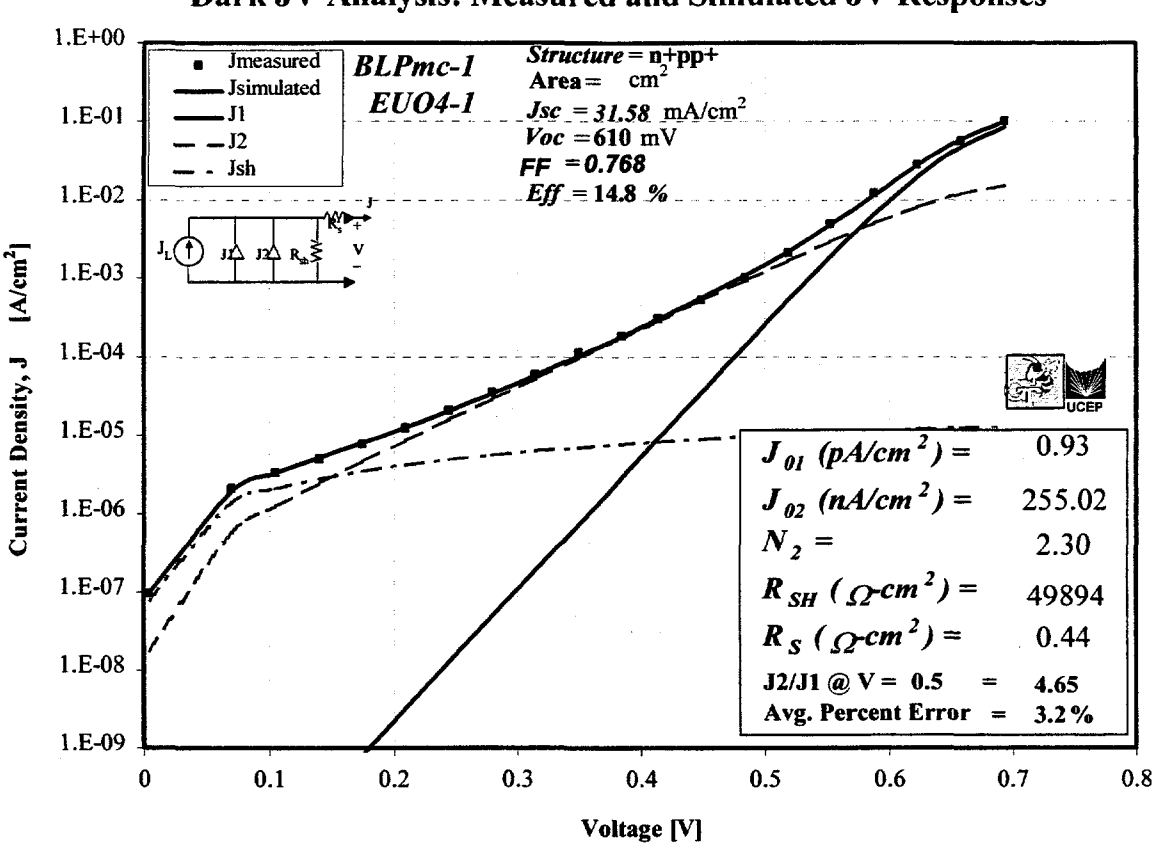



Figure 4.5: Measured and simulated J-V response for belt line screen-printed multi-crystalline (EUO4-1) silicon solar cell.

## 4.3 Results and Discussion

### *4.3.1 Bulk defect passivation and hydrogen concentration measurements in SiN film.*

#### *4.3.1.1 Bulk defect passivation by SiN induced hydrogenation*

As shown in Figure 4.2, the bulk lifetime improved remarkably, immediately after the SiN deposition. Since silicon nitride film was deposited at 300°C, increased bulk lifetime suggests that some of the defects responsible for the low as-grown lifetime in

Eurosolare material have been passivated by hydrogen incorporated during the SiN deposition. In another study we found that certain multi-crystalline silicon material like EFG do not respond to SiN hydrogenation alone without prior or post heat treatment [2]. The bulk lifetime in Eurosolare silicon showed additional improvement after SiN anneal at 730°C. However, post deposition anneal at 850°C showed some reduction in lifetime. The maximum improvement in the bulk lifetime was observed after a 400°C forming gas anneal treatment. Notice that no phosphorus or Al gettering was performed in this experiment. This suggests that either SiN is ineffective or lifetime is being dictated by impurities when no gettering treatment is performed.

#### *4.3.1.2 Hydrogen content of SiN by FTIR Measurements*

Figure 4.6 shows the FTIR spectra of SiN film after each heat treatment. Figure 4.6 shows the two absorption bands, N-H and Si-H, which indicate that the films contain large amount of hydrogen to passivate the bulk defects. It was observed that both the N-H bands shrink rapidly due to the evolution of the hydrogen after the 730°C anneal and N-H band is completely eliminated after the 850°C anneal. This indicates that large amount of atomic hydrogen is released from SiN during the annealing process.

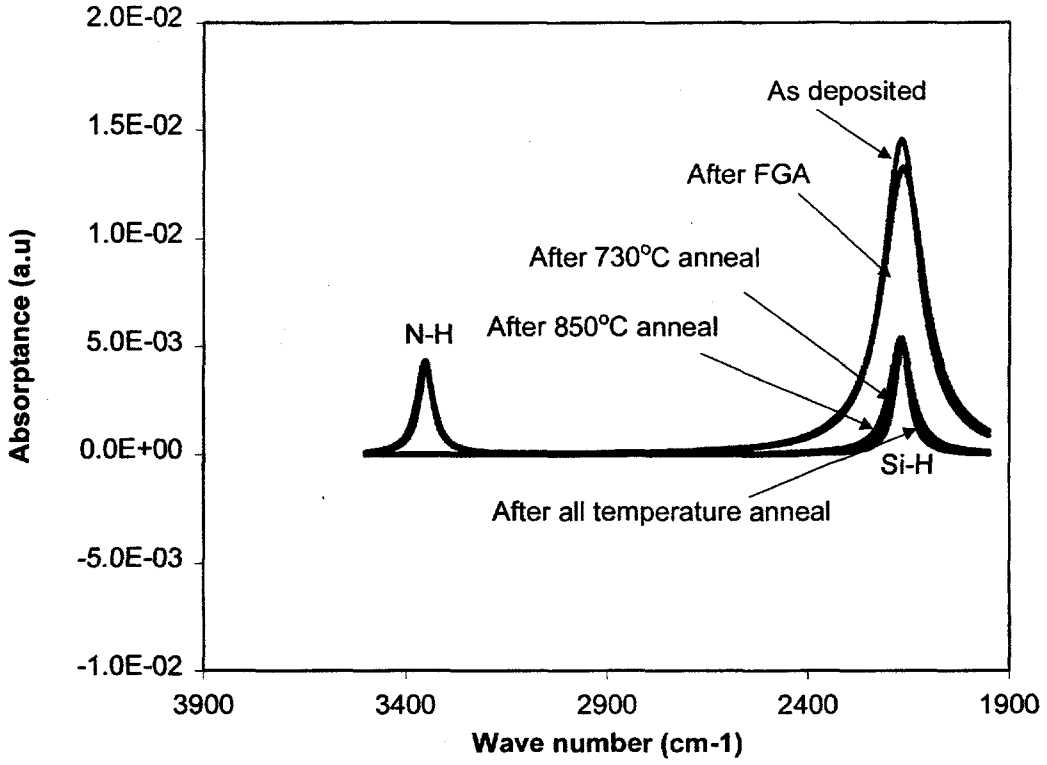



Fig. 4.6: Hydrogen concentration in SiN film deposited on multi-crystalline silicon after each high temperature anneal.

### *4.3.2 Belt line screen-printed multi-crystalline silicon solar cells*

Table 4.1 shows the electrical characteristics of 4 $cm^2$ multi-crystalline silicon solar cells. The data represents the average efficiency on three wafers, which varied from 13.2 to 14.8% indicating a wide spread in the bulk lifetime of the substrate. Sandia National Laboratories confirmed the cell EUO4-1 to be 14.8% with a 76.8% fill factor and a short circuit current density of 31.58 $mA/cm^2$ which suggest a bulk lifetime of over 20 μs based on PC-1D device modeling. This indicates that phosphorus and Al gettering, along with SiN hydrogenation, are playing a significant role in enhancing the as-grown bulk lifetime. Dark I-V measurements and analysis gave $Jo_2$ value of 255

nA/cm$^2$, $R_{sh}$ of 49894 Ω-cm$^2$ and series resistance of 0.44 Ω-cm$^2$ (Fig. 4.5). These numbers are quite respectable for a screen printed cell except for the $Jo_2$ value which was on the high side of the limit for achieving fill factors in excess of 78% on multi-crystalline silicon.

## 4.4 Conclusion

The bulk lifetime of the Eurosolare multi-crystalline has been measured before after SiN deposition and various high temperature anneals. It was found that the bulk defect in Euro-solare material could be passivated effectively with hydrogen from SiN and/or forming gas anneal without any prior gettering.

The hydrogen contents of the SiN films on all the samples showed the same trend as observed in the FZ material [2]. The as-grown film had enough hydrogen for the bulk defect passivation of the material, yet the effects were quite different. Thus the impurities in the bulk may need to be gettered first before realizing the full potential of the bulk defect passivation by hydrogen.

The lamp heated belt line screen-printed multi-crystalline silicon solar cells fabricated showed promising results. The fill factors averaging 69.4-75.7% for the three cells indicate some difference in these substrates. The short circuit current density of 31.58 mA/cm$^2$ and open circuit voltage of 610 mV indicated a lifetime value of about 20

μs. The initial efficiency of 14.8% with a fill of 77% looks quite promising for a screen-printed manufacturable process on multi-crystalline silicon.

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# 4. 5 FABRICATION OF PHOTOLITHOGRAPHY SOLAR CELLS ON EUROSOLARE MC-Si MATERIAL

This section summarizes cell fabrication done using our standard baseline (SBLC) process involving all conventional furnace processing (CFP). The Eurosolar solar cells were made by photolithography contacts on two different resistivity materials, 1 Ω-cm and 0.3 ohm-cm, with a thickness of ~14 mills.

In the SBLC CFP-CFO PL process (Fig. 1-10a, Chapter 1) the Eurosolare wafers were subjected to $POCl_3$ diffusion at 845°C. The wafers were placed in the furnace at 800°C then ramped up to 845°C temperature and finally ramped back down to 800°C before being pulled. After the removal of phosphorus glass in HF, a sheet resistance of ~ 90 ohm/□ was measured. Remainder of the SBLC process involved Al BSF formation by Evaporation of 2 μm thick Al on the back of the wafer followed by a furnace annealing at 850° C for 10 min in Oxygen and 25 min drive in Nitrogen. Then all the wafers were ramped down to 400° C and subjected to a 2 hr min Forming Gas Anneal (FGA) in an attempt to improve surface and bulk defect passivation via hydrogen. This results in ~ 1 μ deep lower quality BSF with a back surface recombination velocity in excess of $10^4$cm/s. The back contact was formed by evaporation of Al-Ti-Pd-Ag and the front metal grid was formed by photolithography and thin lift-off of Ti-Pd-Ag. These cells were then plated to ~8 μm thick Silver by Silver Plating. The cells were isolated by mesa etching followed by an anneal in FGA at 400° C. Finally $MgF_2$-ZnS double layer antireflection coating was applied by evaporation. Cells were analyzed by light and dark I-V and spectral response measurements.

Table 4.2 shows the Efficiency Distribution of cells fabricated on 1 ohm-cm and 0.3 ohm-cm wafers. Both 1cm x 1cm and 2 cm x 2 cm cells were fabricated on large area (10 cm x 10 cm) wafer which gave cell efficiencies in the range of 17.1 to 15.7% with an average efficiency of 16.4% on 1 ohm-cm material. Cells made on low resistivity material had cell efficiencies in range 14.8 to 16.8% with an average efficiency of

15.9%. It is noteworthy that a very high $V_{oc}$ of 645 mV was achieved on the low resistivity material. Resistivity was measured to be quite non-uniform in different regions of this material and varied from 0.2 to 2 Ω-cm.

Detailed analysis shows that further optimization and development of quality enhancement techniques such as gettering defect passivation, and thicker Screen printed BSF by RTP or BLP can produce greater than 18% efficiency on Eurosolare material without any surface texturing and point contacts.

Table 4.2: Efficiency Distribution of cells fabricated on 1 ohm-cm and 0.3 ohm-cm wafers

| Cell ID | $V_{oc}$ | $J_{sc}$ | FF | Eff | $n_{eff}$ | $Jo_{eff}$ | Rs | Rsh@-1 | Rsh@0 |
|---|---|---|---|---|---|---|---|---|---|
| | (mV) | ($mA/cm^2$) | | (%) | | ($A/cm^2$) | ($\Omega$-$cm^2$) | ($\Omega$-$cm^2$) | ($\Omega$-$cm^2$) |
| | 1 Ω-cm resistivity | | | | | | | | |
| E1-1 | 608 | 34.02 | 0.792 | 16.4 | 2.10 | 1.9E-12 | 0.65 | 86,524 | 87,892 |
| E1-2 | 608 | 34.49 | 0.788 | 16.5 | 2.17 | 1.9E-12 | 0.65 | 86,524 | 87,892 |
| **E1-3** | **621** | **34.74** | **0.791** | **17.1** | **1.49** | **1.2E-12** | **0.47** | **88,074** | **88,230** |
| E1-4 | 603 | 33.91 | 0.788 | 16.1 | 2.01 | 2.3E-12 | 0.46 | 87,520 | 88,006 |
| E1-5 | 605 | 34.02 | 0.787 | 16.2 | 1.83 | 2.1E-12 | 0.56 | 86,406 | 87,759 |
| E1-6 | 612 | 34.45 | 0.789 | 16.6 | 2.10 | 1.6E-12 | 0.57 | 88,160 | 87,796 |
| E1-7 | 602 | 33.56 | 0.786 | 15.9 | 2.02 | 2.4E-12 | 0.39 | 88,444 | 88,128 |
| E1-9 | 598 | 33.53 | 0.783 | 15.7 | 2.14 | 2.8E-12 | 0.51 | 86,371 | 87,703 |
| ***Ave*** | ***608*** | ***34.17*** | ***0.789*** | ***16.4*** | ***1.96*** | ***1.9E-12*** | ***0.54*** | ***87379*** | ***87958*** |
| | 0.3 Ω-cm resistivity | | | | | | | | |
| E3-1 | 620 | 31.82 | 0.750 | 14.8 | 2.22 | 1.10E-12 | 0.82 | 81,625 | 52,233 |
| **E3-2** | **641** | **32.58** | **0.800** | **16.7** | **2.19** | **5.00E-13** | **0.44** | **87,042** | **51,799** |
| E3-3 | 635 | 31.72 | 0.798 | 16.1 | 2.24 | 6.20E-13 | 0.36 | 112,239 | 80,826 |
| E3-6 | 632 | 32.06 | 0.779 | 15.8 | 1.95 | 7.10E-13 | 0.40 | 113,190 | 211,527 |
| E3-7 | 633 | 31.70 | 0.760 | 15.3 | 2.49 | 6.80E-13 | 0.64 | 60,960 | 18,116 |
| **E3-9** | **645** | **32.61** | **0.799** | **16.8** | **1.87** | **4.20E-13** | **0.40** | **76,748** | **112,619** |
| ***Ave*** | ***634*** | ***32.08*** | ***0.781*** | ***15.9*** | ***2.16*** | ***6.7E-13*** | ***0.51*** | ***88634*** | ***87853*** |

# CHAPTER V

# HIGH FILL FACTOR FOR SCREEN-PRINTED CELLS – PASTE AND FRONT METAL CONTACT FIRING SCHEME

# 5. OPTIMIZATION OF PASTE AND FRONT METAL CONTACTFIRING SCHEME TO ACHIEVE HIGH FILL FACTORS ON SCREEN PRINTED SILICON SOLAR CELLS

For widespread implementation of silicon PV, the module cost must be reduced by a factor of 2 to 4. This can be accomplished by lowering the cost of solar cell materials and processing without sacrificing cell efficiency. A combination of high throughput belt line processing, SP contacts and mc-Si material offers an opportunity for significant cost reduction. However, most cell manufacturers who use the above combination are only able to achieve fill factors in the range of 0.68-0.75 with cell efficiencies in the range of 10-14%. Thus throughput gains are attained at the expense of device performance. In addition, there is considerable scatter in the fill factor of the SP cells in the literature with no clear guidelines for achieving high fill factors. This paper shows that proper understanding of loss mechanisms and optimization of SP paste and firing cycle, can lead to fill factors approaching 0.77 and 0.79 on mc-Si and single crystal silicon, respectively, on a 45 Ω/□ rapidly formed belt line emitter with a shallow junction depth of ~0.27 μm. It was observed that, deep and shallow emitters on mc-Si could lead to the same values of fill factors ~ 0.77 when the proper combination of paste and firing cycle is applied. The peak firing temperature for deep emitter is higher than the shallow ones with superior value of junction leakage current.

## 5.1 . Introduction

One of the most difficult aspects of large-scale solar cell production is the formation of high quality front contacts. The photolithography and buried contact metallization techniques are somewhat expensive and time consuming for large-scale application. On the contrary, the screen-printing (SP) is a simple, cost effective contact formation technique that is consistent with the requirements for high volume manufacturing. However, the throughput gains achieved with SP usually come at the expense of device performance. The losses associated with SP metallization include: a) increased minority carrier recombination in the required heavily doped $n^+$ regions, b) increased shading due to wider grids (> 100 μm), and c) lower fill factor (FF) due to poor contact quality. The purpose of this research is to investigate the combination of firing cycle and Ag paste composition to improve the contact quality of screen-printed solar cells to achieve high FF on both mono and multi-crystalline substrates.

Model calculations, Fig. 5.1, show that high fill factors (FF), ≥0.78, can be achieved on screen-printed mono-crystalline silicon solar cells if the following requirements are met; junction depth ≈ 0.5 μm on 40 Ω/□ emitter, $J_{02} \approx 10^{-8}$ A/cm$^2$, $R_s \leq 0.5$ Ω-cm$^2$ and $R_{sh} \geq 1$ kΩ-cm$^2$ [1]. However, for low-cost solar cells, multi-crystalline Si materials are used and the emitter is formed in a belt furnace, resulting in a junction depth of ~ 0.25-0.35 μm. In addition, low quality materials prefer shorter time at high temperature in order to preserve the bulk lifetime. Therefore, a junction depth of 0.5 μm as a criterion for achieving high fill factor, as in the case of mono-crystalline silicon, may not be as applicable and cost effective for multi-crystalline silicon cells. Also, defect density, defect non-uniformity, and

paste/defect interaction in multi-crystalline silicon material could further complicate the process, so that even if the 0.5 μm junction depth criterion is met, the FF may still be lower than 0.78. To investigate these issues, a study was conducted on multi-crystalline, CZ and FZ silicon materials using both rapid belt line and conventional furnace processing of the emitter in conjunction with screen-printed contacts. A 40-50 Ω/□ emitter was formed by a 925°C/6 min and 890°C/30 min diffusion, in a lamp heated belt line system and conventional furnace, respectively. The belt line process gave a junction depth of 0.25 μm while the conventional furnace diffusion resulted in a junction depth of 0.5 μm. It should be noted that even though 45 Ω/□ emitter with a junction depth of only 0.25 μm (lamp heated furnace emitter) minimizes the heavy doping effects, it makes the emitter more vulnerable to junction shunting and leakage. That is why it is necessary to use the appropriate paste and the compatible firing cycle in order to achieve high FF on defective materials. On the other hand, for the conventional furnace emitter with junction depth of $\geq$ 0.5 μm, the fill factor is expected to be higher due to reduced junction leakage and shunting.

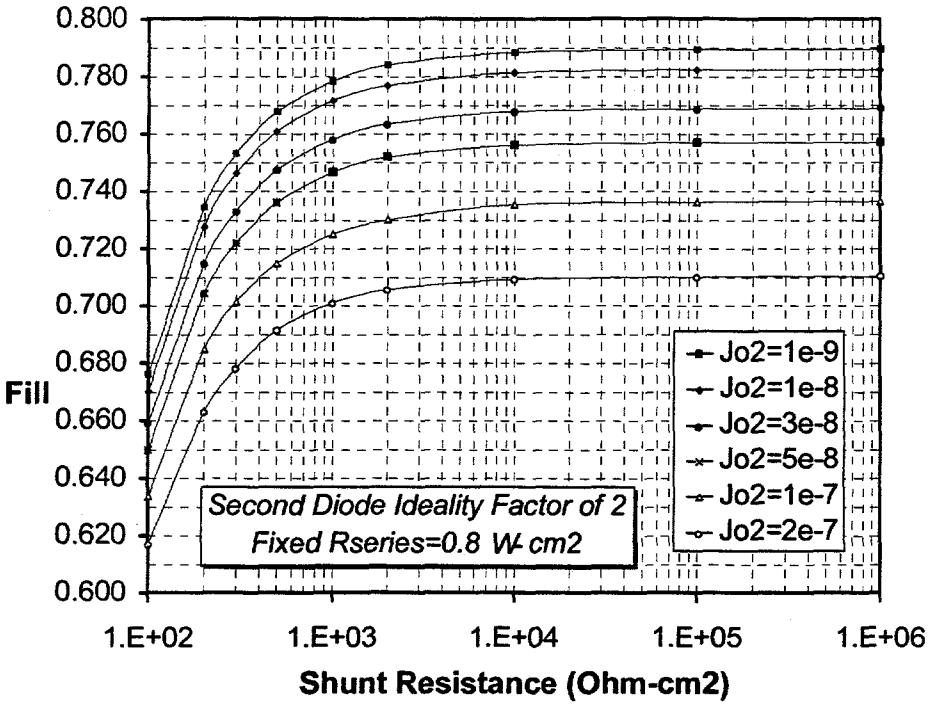


Fig. 5.1: The effect of $R_{sh}$ and $J_{o2}$ on FF for 4 $cm^2$ cells

We investigated the effects of two different Ag pastes and two firing cycles on the FF of screen-printed shallow junction solar cells on both multi and mono crystalline silicon. These pastes, (A and B, obtained from Ferro Corporation), had the same frit content but different frit composition. The effect of slow and fast firing cycles was examined on FF using both pastes.

### 5.2. Cell fabrication

A rapid cell fabrication sequence was used which involved emitter formation by spin-on, bake, and 6-min belt line diffusion at 925°C. This resulted in a 40-45 Ω/□ emitter with a junction depth of ~ 0.25 μm and peak (near surface) concentration of $6.4 \times 10^{19}$ (Fig. 5.2). It should be noted that a 45 Ω/□ diffusion in the conventional diffusion furnace could take up to 60 minutes from start to finish. After the phosphorus glass removal and DI water rinse, a

single layer PECVD SiN antireflection coating was deposited on the front at 300°C. This was followed by screen-printing of Al on the back and a 2 min drive-in at 860°C in the belt furnace to form a very effective Al back surface field. A Ag grid was screen printed on top of the SiN and then fired through the SiN for various times and temperatures to optimize the firing cycle for each paste. Even though 45 Ω/□ emitter with a junction depth of only 0.27 μm minimizes the heavy doping effects, it makes the emitter more vulnerable to junction shunting and leakage. Frit composition or impurity content in the paste can also degrade junction quality if the impurity can migrate to the junction. That is why a compatible firing cycle needs to be established for each paste. Firing cycles involving belt speeds of 15-30 inch/min in conjunction with low firing temperatures (700-800°C) are referred to as slow firing cycles and belt speeds of 60-75 inch/min with firing temperatures of 750-900°C are referred to as spike firing cycles in this study.

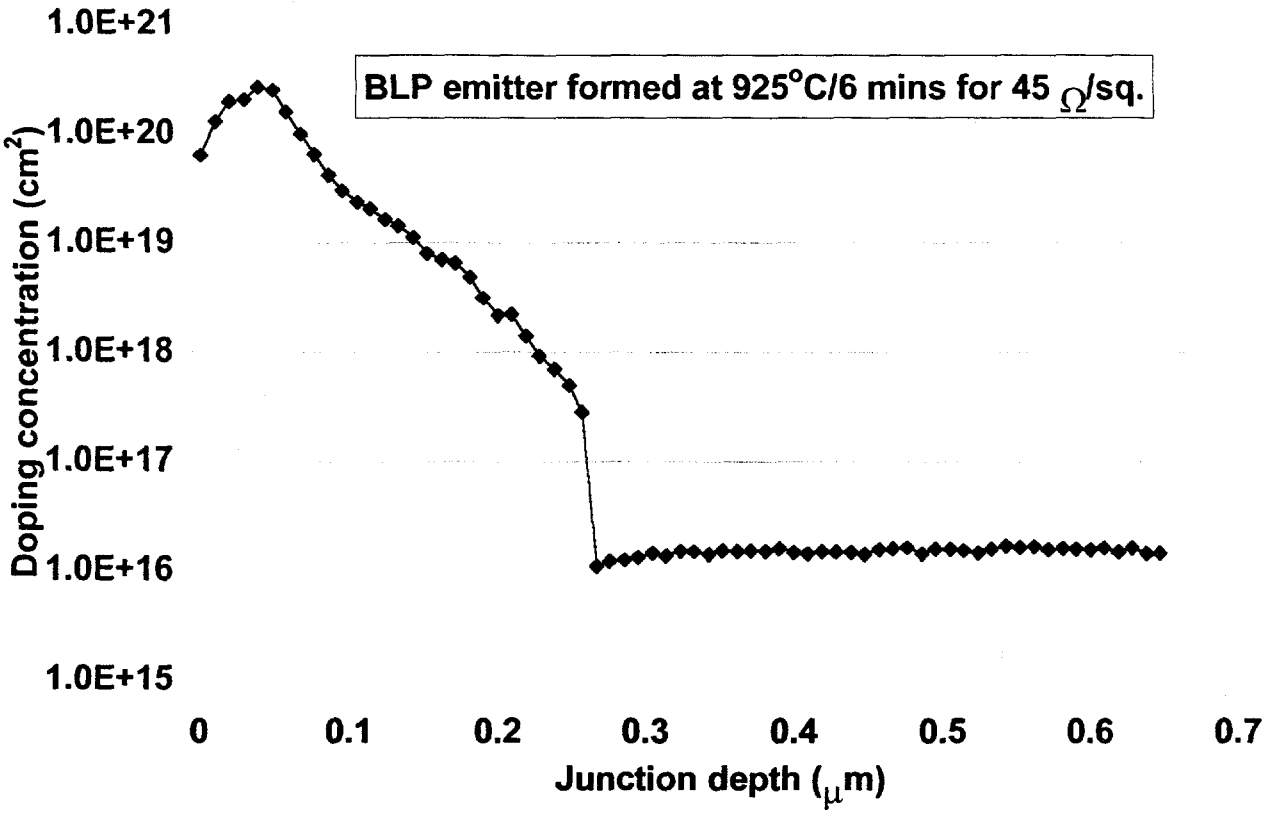


Fig. 5.2: BLP emitter profile deposited at 925°C for 6 minutes.

## 5.3. Results and Discussion

### *5.3.1. The effect of slow and spike firing cycles on FF for shallow junction cells*

Since the primary fill factor loss mechanism associated with SP metallization are contact/series resistance, shunt resistance, and junction leakage ($J_{o2}$ and n), detailed dark I-V measurements were performed to decouple $R_s$, $R_{sh}$, $J_{o2}$ and n values by the measured I-V fit to the double exponential model

$$I = I_{o1}\left(e^{\frac{q(V-IR_s)}{kT}} - 1\right) + I_{o2}\left(e^{\frac{q(V-IR_s)}{nkT}} - 1\right) + \frac{V - IR_s}{R_{sh}} \qquad (1)$$

Change in fill factor was assessed and explained on the basis of above parameters for various pastes, firing cycles and silicon materials used in this study. Figure 5.3 shows fill factors and the corresponding values of $R_s$, $R_{sh}$, $J_{o2}$ and n for the two pastes fired under slow and spike firing conditions. These cells were fabricated on 1 Ω-cm mc-Si from Eurosolare. There are several noteworthy features; slow firing condition (730°C with a belt speed of 15 inch/min) gave a very low fill factor (0.689) for paste A primarily due to junction shunting ($R_{sh} \approx 329$ Ω-cm$^2$) and high junction leakage ($J_{o2} \approx 4700$ nA/cm$^2$). This suggests that metal or impurities from this paste are able to get to the depletion region and give rise to generation/recombination centers. On the other hand, the contaminant resistant paste B gave decent fill factor of 0.765 with reasonable series and shunt resistances ($R_s \approx 0.44$ and $R_{sh} \approx 48{,}000$ Ω-cm$^2$) but slightly higher junction leakage current of 45 nA/cm$^2$ with an n factor of 2.3. Model calculations were performed to show that $R_s \leq 0.5$ Ω-cm$^2$, $R_{sh}$>1KΩ-cm$^2$ and $J_{o2} \leq 10^{-8}$ A/cm$^2$ are generally required for very high fill factor in excess of 0.78.

Figure 5.3 shows that a fill factor of ~ 0.76 was also achieved on Euroslare mc-Si cells using paste A when spike firing (850°C with a belt speed of 75 inch/min) is used. However spike firing gives higher series resistance, 1.23 Ω-cm$^2$ for paste B and 0.65 Ω-cm$^2$ for paste A. Thus slow firing works well for paste B while spike firing gives better result with paste A.

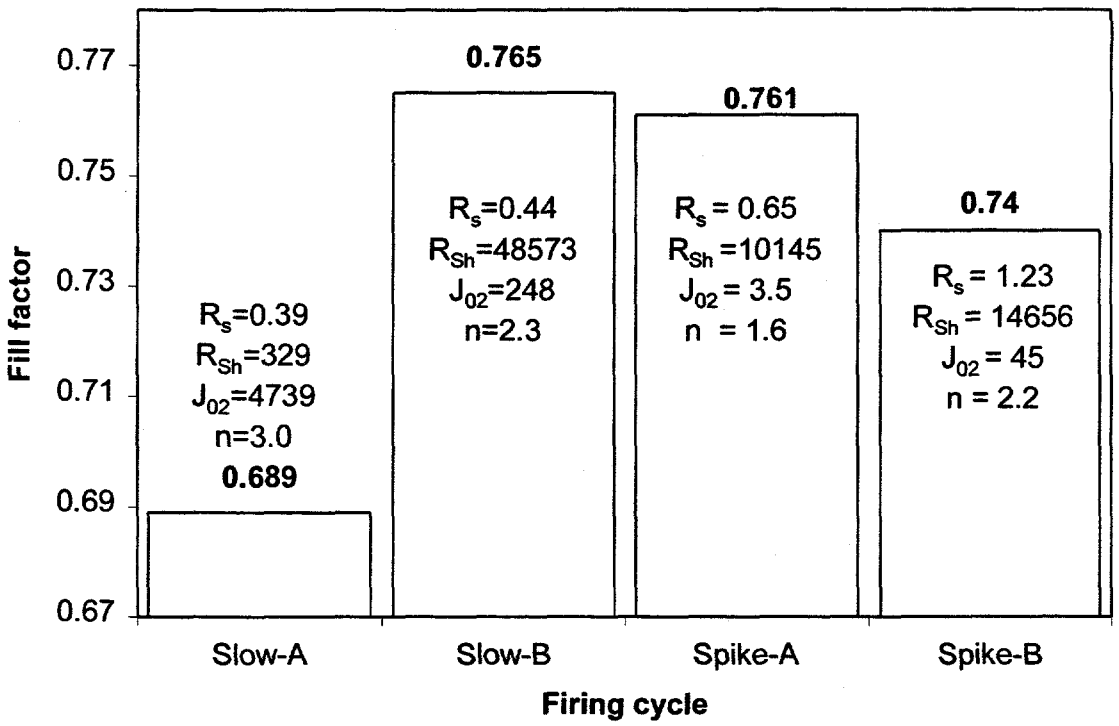


Fig. 5.3: Effect of paste and firing cycle on fill factor of screen-printed solar cells on mc-Si with 0.25 μm deep emitter.

*5.3.2. Effect of contact firing temperature on FF of shallow junction cells.*

In an effort to achieve even higher fill factor we decided to raise the slow firing temperature gradually from 730 to 770°C using paste B. In this experiment cells were fabricated on Solarex mc-Si, CZ Si from Siemens Solar and a FZ silicon. Figure 5.4 and table 5.1 show the result of this study. We observed a slight increase in the fill factor for all materials, with the exception of FZ, which remained same, when the firing temperature was raised from 730 to 750°C. This is because series resistance decreased below 0.7 $\Omega$-cm$^2$ and junction leakage improved slightly. It was found that for single crystals, fill factor value

peaked at a firing temperature of 760°C while the peak temperature for mc-Si was 750°C. Dark I-V analysis showed that, beyond the peak temperature, fill factor begins to degrade due to high junction leakage current. This suggests that mc-Si are somewhat more vulnerable to junction leakage due to the defect/paste interaction. Therefore firing cycle should be optimized for each mc-Si due to the difference in the defect structure.

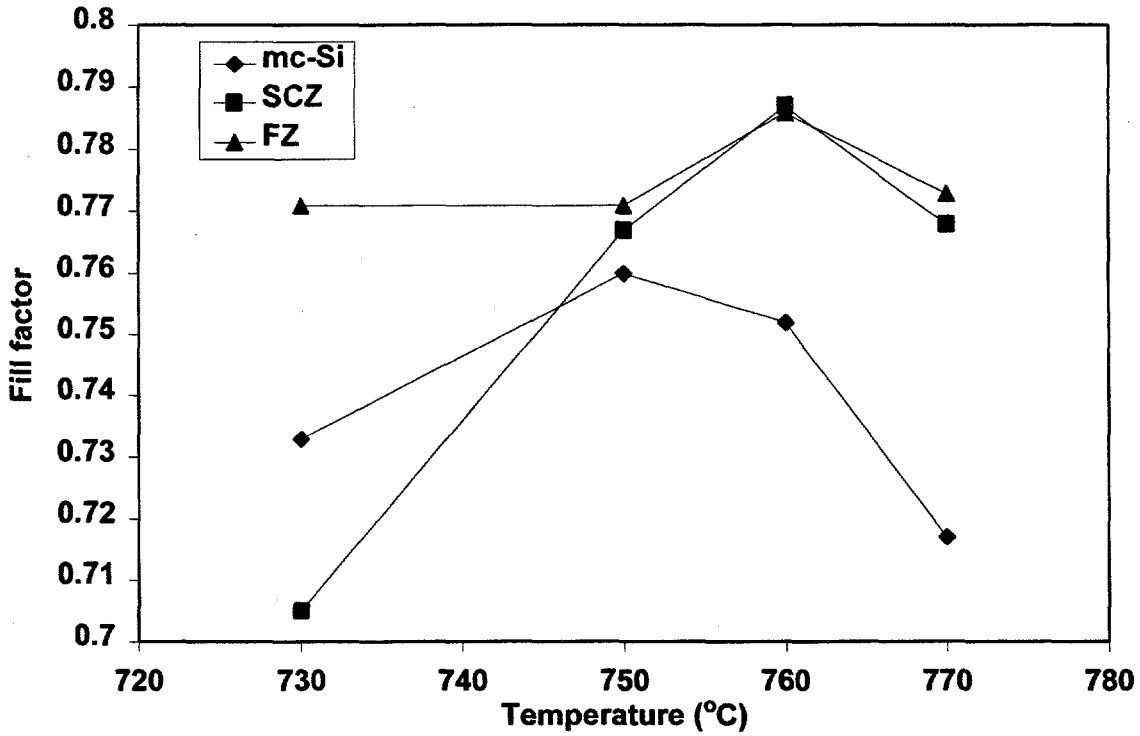


Fig. 5.4: Effect of temperature cycle and paste B on fill factor

Figure 5.4 and table 5.1 show that in this study a best fill factor value of 0.77 was achieved on mc-Si cells with efficiency of ~ 15%, while single crystal cells gave a fill factor of 0.79 with an efficiency of 16.5%. These fill factors are much higher than what is currently achieved on industrial cells. In addition, the combination of belt line diffusions and screen-printed contact offers a low-cost, high throughput, manufacturable technology. Further

understanding and optimization can lead to even higher fill factor and efficiencies, reducing the gap between the screen-printed and buried or photolithography contact technologies.

Table 5.1: The Electrical output parameters for the screen-printed solar cells on different materials.

| Material | Slx1 | SCZ1 | FZ1 | Slx2 | SCZ2 | FZ2 |
|---|---|---|---|---|---|---|
| Fill Factor | 0.733 | 0.705 | 0.771 | 0.76 | 0.767 | 0.771 |
| $R_s$ (ohm-cm$^2$) | 0.83 | 0.76 | 0.48 | 0.66 | 0.5 | 0.43 |
| $R_{sh}$(ohm-cm$^2$) | 6292 | 4590 | 44391 | 14985 | 59643 | 67557 |
| $J_{o2}$ (nA/cm$^2$) | 612 | 1268 | 123 | 154 | 117 | 160 |
| n | 2.3 | 2.5 | 2.2 | 2.2 | 2.2 | 2.3 |
| Material | Slx3 | SCZ3 | FZ3 | Slx4 | SCZ4 | FZ4 |
| Fill Factor | 0.752 | 0.787 | 0.786 | 0.717 | 0.768 | 0.773 |
| $R_s$ (ohm-cm$^2$) | 0.44 | 0.37 | 0.37 | 0.55 | 0.49 | 0.42 |
| $R_{sh}$(ohm-cm$^2$) | 2843 | 4668 | 1616 | 1160 | 60000 | 68789 |
| $J_{o2}$ (nA/cm$^2$) | 832 | 43 | 8.2 | 4956 | 89 | 86 |
| n | 2.6 | 2.2 | 1.8 | 3.0 | 2.1 | 2.1 |

*5.3.3 Effect of contact firing temperature on the FF of deep junction cells*

In order to assess the impact of paste/defect interaction on FF in multi-crystalline silicon, the conventional furnace was used to form the emitter at 890°C for 30 minutes. This resulted in 45 Ω/□ emitter with a junction depth of ~ 0.5 μm and peak (near surface) concentration of $4x10^{19}$. After the diffusion, the cells were fabricated by the same process sequence outlined in section 2. Paste B was used and the slow firing temperature was gradually raised from 730°C to 770°C. The idea was that deeper junction may permit higher firing temperature, according to Mertens et al [2], without excessive junction leakage which may be caused by paste/defect interaction at the junction.

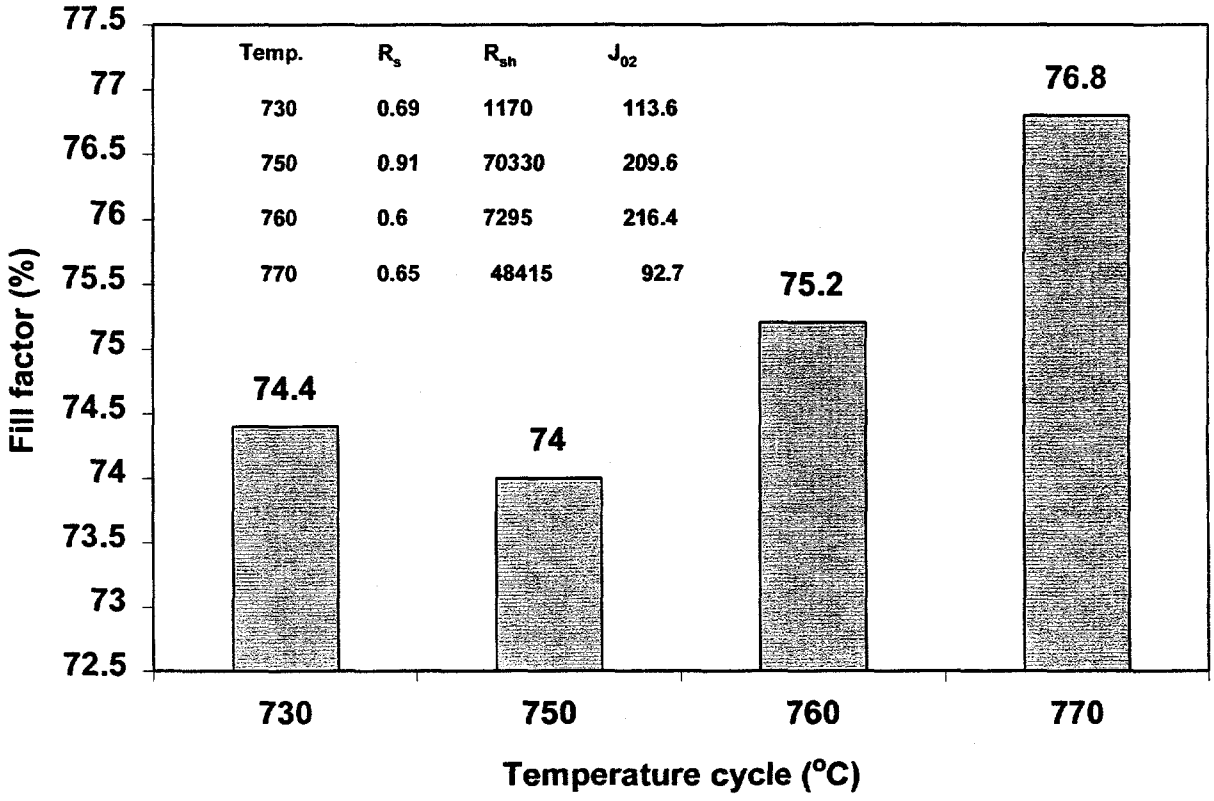


Fig. 5.5: Effect of contact firing temperature on fill factor of 0.5 μm deep emitters formed by CFP.

Figure 5.5 shows the results of this study. We observed a slight increase in the fill factor of mc-Si cell when the firing temperature is raised from 730°C to 770°C. Firing time was maintained at 30 seconds. It was interesting to note that the fill factor value peaked at a firing temperature of 770°C for the deep junction while 750°C was the peak for the shallow junction devices. The dark I-V analysis showed that before the peak temperature fill factor is poor due to high junction leakage current ($J_{02}$). This suggests that for mc-Si, even

though the junction is deep, the low fill factor can result from increased junction leakage due to paste/defect interaction.

## 5.4. Conclusion

The understanding and optimization of SP paste, firing cycle, and loss mechanisms has led to the achievement of fill factors approaching 0.77 and 0.79 on mc-Si and single crystal silicon, respectively, on a 45 Ω/□ rapidly formed belt line emitter. It was found that, for mc-Si, even the deep emitter of ~0.5 μm does not guarantee high fill factor because of the paste/defect interaction which tend to increase the junction leakage current. However, it was observed that the deep junction could stand higher temperature firing cycle than the shallow junction. The shallow junction FF peaked at 750°C firing temperature, while the FF peaked at 770°C for deep junction devices for a firing time of 30 seconds. Even though we have demonstrated high FF for SP cells, further research on paste composition and firing cycles is necessary to achieve FF in excess of 0.78 repeatedly on mc-Si.

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# CHAPTER VI

# DEVELOPMENT OF FRONT SURFACE FIELD AL BACK JUNCTION $n^+$-n-$p^+$ SCREEN-PRINTED CELLS ON DENDRITIC WEB SILICON.

# 6. DEVELOPMENT OF FRONT SURFACE FIELD ALUMINUM ALLOY BACK JUNCTION $n^+$-n-$p^+$ SCREEN PRINTED CELLS ON DENDRITIC WEB SILICON

A new silicon solar cell structure is fabricated in which the p-n junction is formed by alloying aluminum with n-type silicon, and where this p-n junction is located at the back (non-illuminated) surface of the cell. With a phosphorus front diffusion, the resultant $n^+np^+$ structure has been implemented using dendritic web Si substrates which are 100 μm thick and doped with antimony to 20 Ω-cm. Such a structure eliminates shunting of the p-n junction, provides an effective front surface field, enables a high minority carrier lifetime in the base, and is immune to light-induced degradation. Using only production-worthy, high-throughput processes, aluminum alloy back junction dendritic web cells have been fabricated with efficiencies up to 14.2% and corresponding minority carrier (hole) lifetime in the base of 115 μs (diffusion length of 370 μm).

## 6.1. Introduction

Silicon substrates of sufficiently high quality that minority carrier diffusion length exceeds the substrate thickness lend themselves to non-conventional solar cell structures. Dendritic web silicon ribbon, which can be grown quite naturally at a thickness of 100 μm, is such a substrate. A solar cell structure designed to exploit this property is illustrated in Fig 6.1. The most striking feature of this cell is the aluminum alloy p-n junction on the back (non-illuminated) side. The substrate is doped lightly with antimony in order to ensure a high minority carrier (hole) diffusion length. A phosphorus-doped layer, which gives rise to

a strong electric field for effectively passivating the front surface, leads to an $n^+np^+$ structure. With a silicon nitride anti-reflective (AR) coating and solderable silver contacts as a grid on the front and as two stripes over the aluminum-silicon eutectic metal on the back, the cell is complete. This front surface field cell has been named "PhosTop" because the top surface is doped with phosphorus rather than boron, as is usually the case for an n-base cell.

A comparison of a conventional silicon cell with the dendritic web silicon PhosTop cell is given in Table 6.1. There are several potential advantages of the PhosTop cell over the conventional cell. First, shunting of the p-n junction is eliminated. The junction is formed by alloying aluminum with n-type silicon to form a $p^+n$ structure. The aluminum-silicon eutectic remains as a self-aligned metal to contact the $p^+$ surface. Aluminum cannot shunt the p-n junction because the aluminum creates a junction everywhere it contacts silicon. Moving the p-n junction from the front of the cell to the back opens the possibility of making the front diffused layer thinner without fear of shunting. The prospect of enhancing the blue response of the cell in this way was recognized previously in fabricating cells with a $p^+pn^+$ structure using 100 μm thick wafers sawn from a three-grain ingot [1].

A second advantage of the PhosTop cell is the existence of a strong front surface field. This arises from the phosphorus-diffused layer on the lightly doped n-type substrate, which creates a strong electric field. The recombination velocity of minority carrier holes at the front $n^+n$ junction is therefore, quite low. A previous study of such an $n^+n$ junction in a

dendritic web silicon cell concluded that the effective recombination velocity must be <100 cm/s at the $n^+n$ junction, with a value of 25 cm/s at the maximum power point [2].

Table 6.1: Conventional silicon solar cells versus dendritic web $n^+np$ cell

| Cell Feature | Conventional Cell | Dendritic web $n^+np$ cell |
|---|---|---|
| Substrate thickness | 300 μm | 100 μm |
| Substrate type (dopant) | p-type (B) | n-type (Sb) |
| Substrate resistivity | 1 Ω-cm | 20 Ω-cm |
| Junction (dopants) | $n^+p$ (P,B) | $p^+n$ (Al,Sb) |
| Junction location | Front ($n^+pp^+$) | Back ($n^+np^+$) |

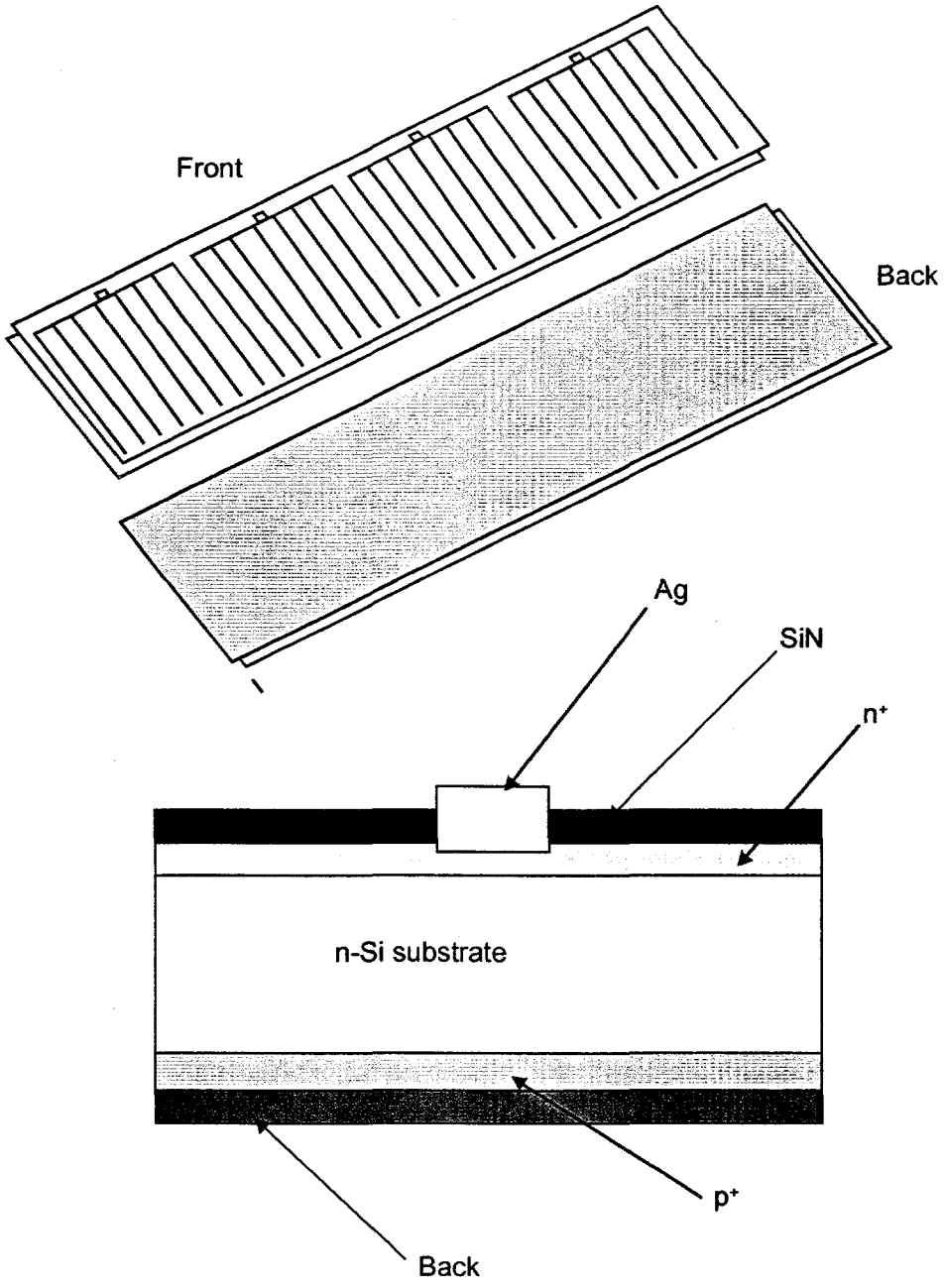



Fig. 6.1: Structure of aluminum alloy back junction silicon solar cell

The dendritic web silicon PhosTop cell holds a third potential advantage over the conventional cell in its high lifetime for minority carriers in the base. Light substrate doping

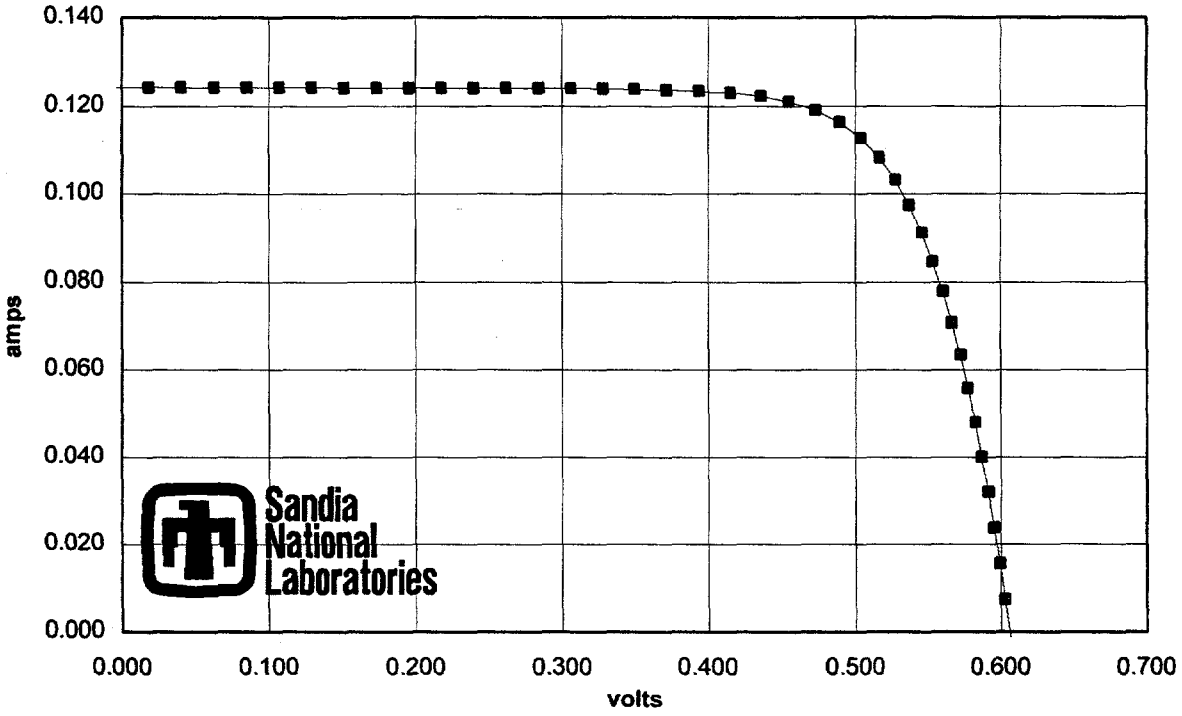
(20 Ω-cm) reduces the recombination activity associated with electrically active defects in the material by virtue of the location of the Fermi level near the center of the bandgap [3]. The choice of n-type is also important because minority carrier holes carry a positive charge. The principal defect in dendritic web silicon is an oxide precipitate decorating a dislocation core. The surface of such an oxide precipitate is expected to have a positive charge, which would repel holes from the defect but attract electrons. Lifetime degradation associated with oxygen precipitates has been observed to be much more severe in p-type silicon than in n-type [4]. Thus, the choice of n-type dopant having low concentration ensures a large minority carrier diffusion length for typical dendritic web silicon crystals.

A final advantage of the PhosTop cell is that there is no light-induced degradation since it has an n-type base. Conventional cells using Czochralski grown wafers doped with boron to 1 Ω-cm exhibit a stabilized 4% drop in Voc after exposure to one-sun illumination for only six hours [5]. This degradation has been traced to the existence of boron-oxygen pairs [6]. Since PhosTop substrates have no boron they are free from light-induced degradation.

## 6.2. Experimental Results

The PhosTop cell of Fig. 6.1 was fabricated from dendritic web silicon substrates nominally 100 μm thick and doped with antimony to 20 Ω-cm. Only simple, high-throughput processes, thought to be compatible with a production environment, were used. The front surface field ($n^+n$) was created by applying a phosphorus liquid dopant

with diffusion in a radiantly-heated belt furnace to approximately 42 Ω/□. Silicon nitride was deposited on the front by plasma-enhanced chemical vapor deposition (PECVD) as an anti-reflective coating. The back junction ($p^+n$) was formed by screen-printing aluminum,




then alloying with silicon in a belt furnace. Finally the front metal contact was formed by screen-printing silver, baked and fired in a belt furnace.

Fig. 6.2: Lighted I-V data for $n^+np^+$ aluminum alloy back junction solar cell, 4 $cm^2$ in area. Cell fabricated from a dendritic web silicon substrate (100 μm thick, antimony-doped to 20 Ω-cm).

The lighted I-V curve, as measured at Sandia National Laboratories, of a dendritic web silicon PhosTop cell 2 cm x 2. cm in size is shown in Fig. 6.2. In this case, cell efficiencies up to 14.2% were realized, with $J_{sc}$ of 31.0 mA/cm$^2$, $V_{oc}$ of 0.606 V, and FF of 0.756. Spectral data taken with a one-sun light bias for the same cell are given in Fig.6.3. The location of the p-n junction at the back of the cell is clearly indicated by the positive slope of the internal quantum efficiency (IQE) curve over its central portion. The reflectivity from the front surface is fairly high with a weighted value of 13.0% for the global spectrum. This represents a loss of 2.0% (absolute) in efficiency.

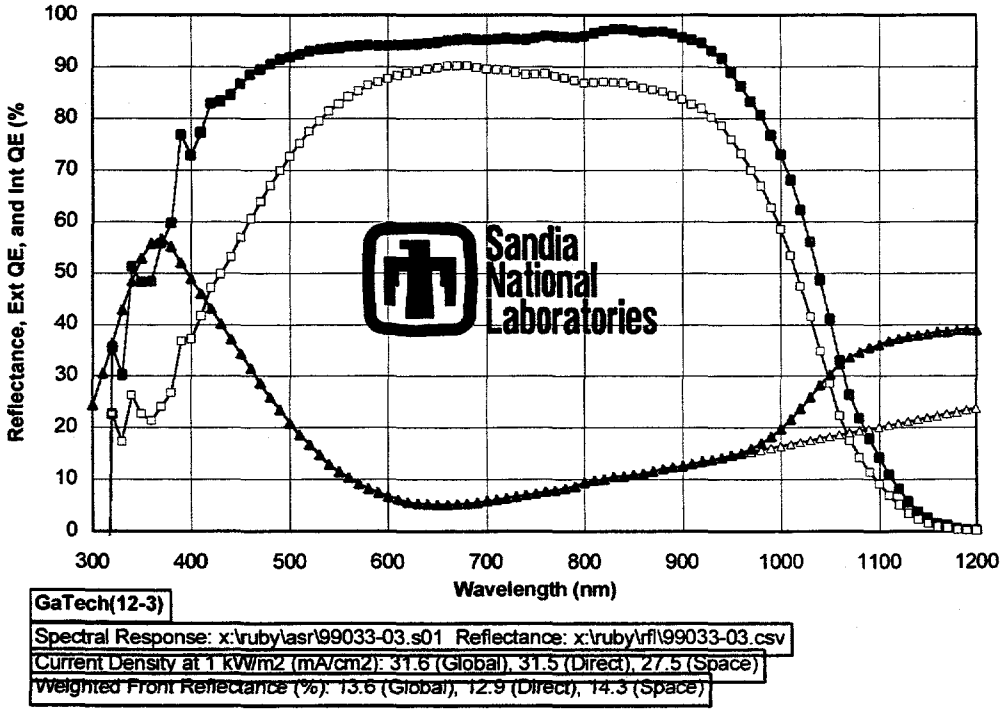



Fig. 6.3: Measured spectral data for 14.2% aluminum alloy back junction solar cell fabricated from 100 μm thick dendritic web silicon.

An estimate of the minority carrier (hole) lifetime in the base was obtained by fitting the IQE curve using PC-1D. This gave a value of 115 μs, equivalent to a hole diffusion length

of 370 μm which significantly exceeds the 100 μm substrate thickness. This was also validated experimentally by etching the cell down to silicon and measuring the bulk lifetime by PCD measurement. Bulk lifetime value of 96 μs was obtained at an injection level of ≈ $10^{14}$ $cm^{-3}$.

### 6.3. Discussion

Attempts are being made to boost the efficiency beyond the 14% value already demonstrated for 100 μm thick dendritic web PhosTop cells to date. Experimental data shows that the values of $V_{oc}$ and FF are quite reasonable, but $J_{sc}$ is lower than desired. This is largely because significant amount of light is lost to reflection and because the blue response of the cell is relatively poor. Methods of texturing the (111) surface of dendritic web silicon are currently being explored to reduce reflection losses. Efforts to improve blue response are aimed at reducing phosphorus doping concentration near the front surface. This may require a more sophisticated surface passivation scheme, such as RTO/SiN stack, and a modification of the front metallization process to retain low resistance ohmic contacts.

It may also be desirable to segment the back aluminum in some fashion. This would reduce the consumption of aluminum paste and also alleviate the bowing that sometimes occurs because of the mismatch in thermal expansion coefficient between aluminum and silicon. Preliminary attempts to reduce the back aluminum coverage have shown that even a modest openings in the aluminum cause a severe reduction in cell performance. It is

clear that the exposed silicon must be passivated in some way. Promising approaches include thermal oxide, deposited dielectric layers, and a light diffusion with boron or phosphorus. If an effective method for passivating exposed back silicon is found, the front metal contact could be moved to the back in an interdigitated back contact configuration. Such an approach not only eliminates grid shadowing but also enables simpler methods to interconnect cells.

## 6. 4. Conclusions

From this work the following conclusion can be drawn:

1. The quality, uniformity, and reproducibility of aluminum alloy p-n junctions are satisfactory for silicon solar cells;
2. A high-throughput, low-cost process utilizing screen-printing and belt furnace diffusion, alloying, and firing can be applied to 100 μm thick dendritic web silicon substrates with acceptable yield;
3. Cell efficiency in excess of 14% and minority carrier lifetime in excess of 100 μs can be achieved with the PhosTop cell structure using 100 μm thick dendritic web silicon substrates and high-throughput processes.
4. Reduced front surface reflectance, surface texturing and improved surface passivation can raise the PhosTop efficiency beyond 15%.

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# CHAPTER VII

# DEVELOPMENT OF HIGH EFFICIENCY $n^+$-p-$p^+$ CELLS ON STRING RIBBON SILICON

## 7. 1 FABRICATION OF RECORD HIGH 16.2% EFFICIENT SOLAR CELLS ON EVERGREEN STRING RIBBON MATERIAL BY PHOTOLITHOGRAPHY

This section summarizes recent cell fabrication done using our standard baseline (SBLC) process involving all conventional furnace processing (CFP). The solar cells were made by Photolithography contacts on different resistivity of Evergreen materials to study the effect of dependent-defect interaction and doping dependence on the final cell performance.

In this SBLC CFP-CFO PL process, the Evergreen materials were subjected to a $POCl_3$ diffusion at 845°C. The wafers were placed in the furnace at 800°C then ramped up to 845° C temperature and finally ramped back down to 800°C before being pulled. After the removal of phosphorus glass in HF, a sheet resistance of ~ 80 Ω/□ was achieved. No emitter etch back was used in this SBLC process. Remainder of the SBLC process involved Al BSF formation by Evaporating of 2 μm of Al on the back of the wafer followed by annealing at 850° C for 10 min in Oxygen and 25 min drive in nitrogen. Then the Evergreen samples were ramped down to 400° C in Nitrogen and subjected to 2 hours of forming gas anneal to provide defect passivation by hydrogenation.

The back contact consisted of evaporated Al-Ti-Pd-Ag and the front metal grid was formed by photolithography and thin lift-off of Ti-Pd-Ag. These cells were then plated to ~8 μm by silver plating. The cells were then mesa etched and annealed in forming gas at 400°

C for 10 min. Finally ZnS-$MgF_2$ double layer antireflection coatings was applied by evaporation. Dark and Light IV and spectral response were performed for the analysis of these devices.

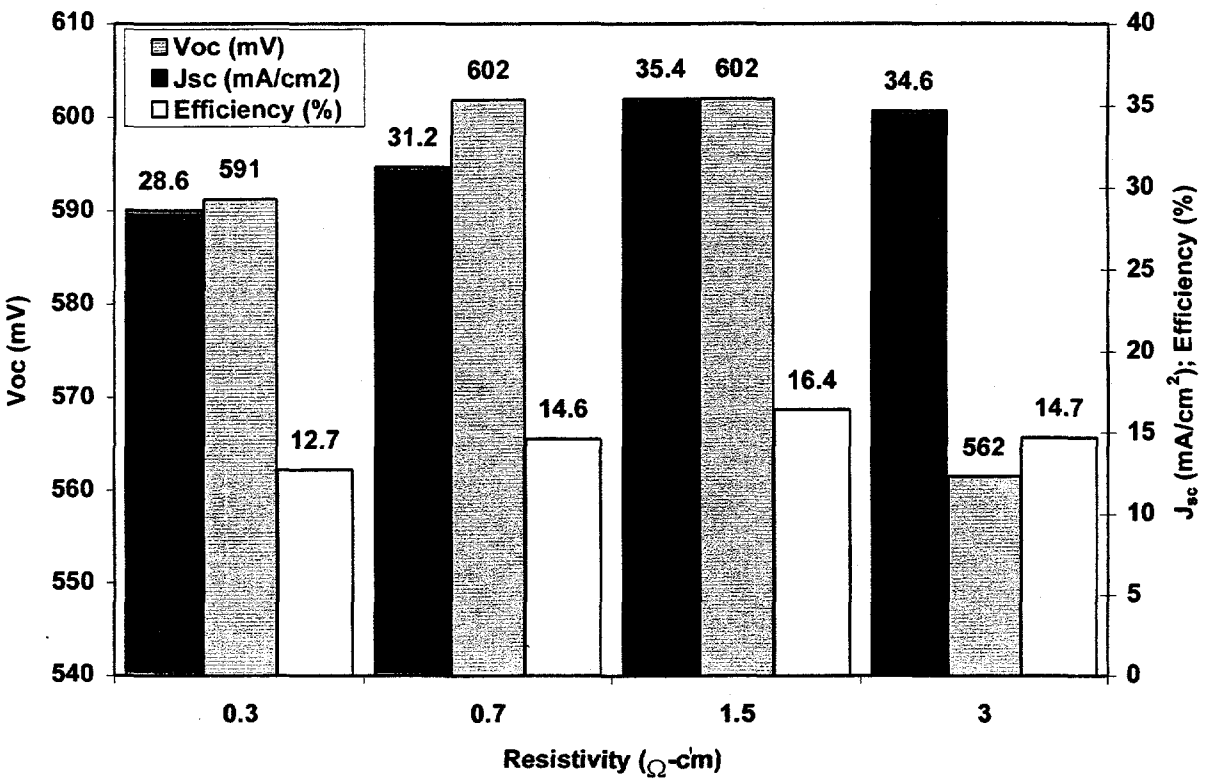



Fig. 7.1: Doping dependence of string ribbon cell efficiency.

Figure 7.1 shows the doping dependence of string ribbon cell efficiency. In this experiment, optimum resistivity was found to be 1.5 Ω-cm, which also gave the highest $V_{oc}$ and $J_{sc}$. This is indicative of best combination of bulk lifetime and surface recombination velocity. IQE measurements in Fig 7.2 clearly demonstrate that the 1.5 Ω-cm cell had the best long wavelength response. This is due to the fact that lower resistivity material has

lower bulk lifetime and higher resistivity (3 Ω-cm) has higher $J_{ob}$ due to higher base doping. This is especially true in these SBLC cells where thin evaporated Al BSF results in high back surface recombination velocity.

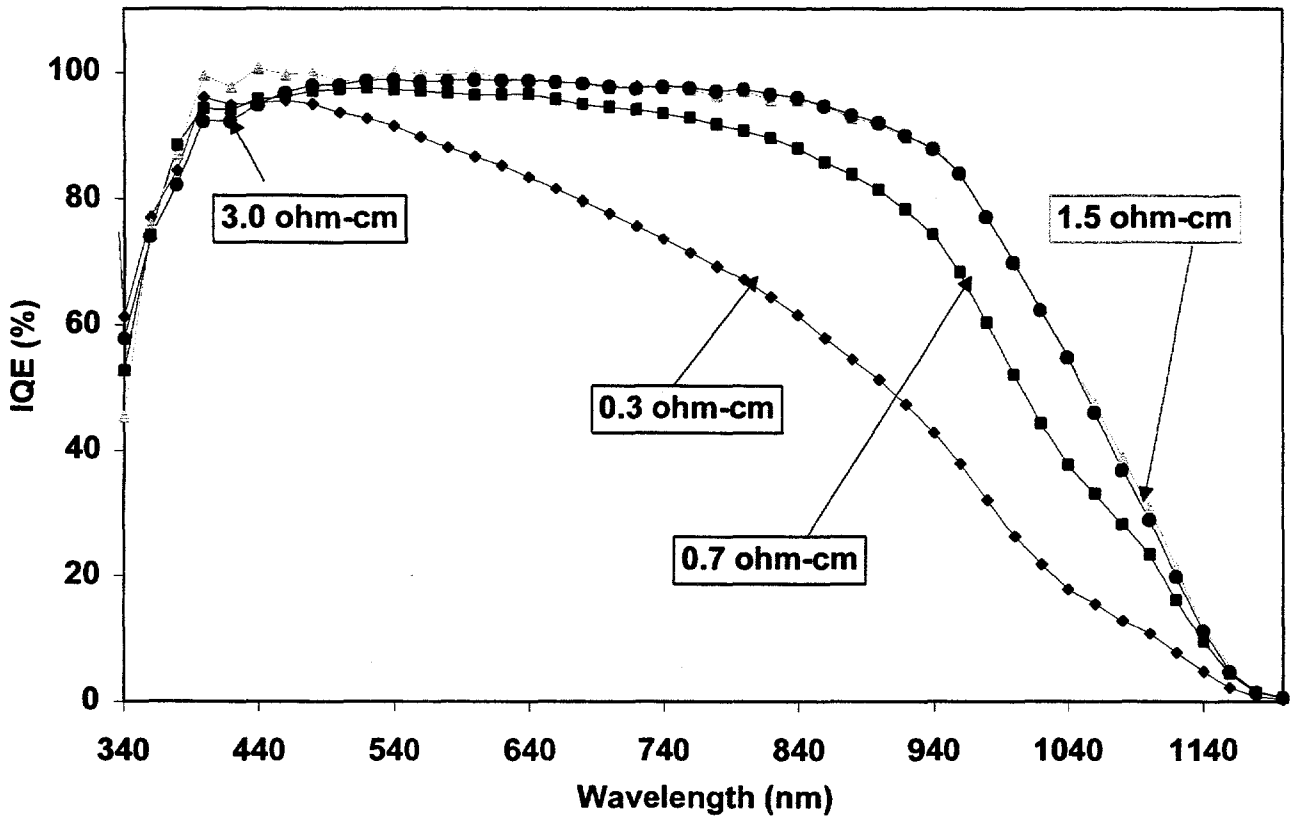
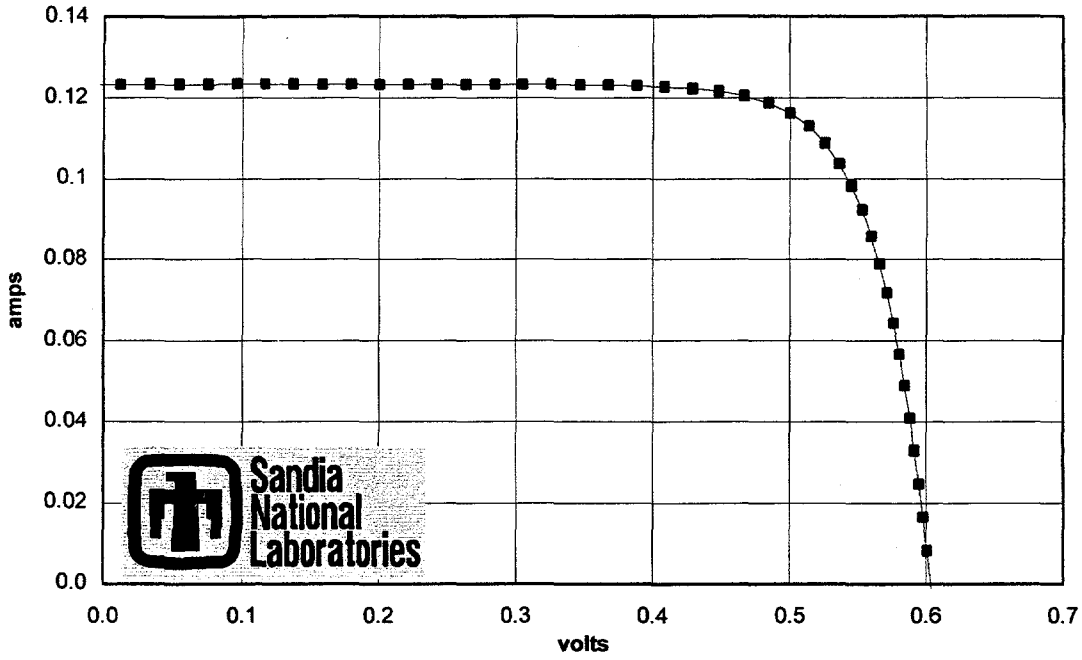



Fig. 7.2: Resistivity effect on string ribbon IQE.




| | | | | | |
|---|---|---|---|---|---|
| 07/06/99 9:16 AM | 24.9 °C | 3.58 $cm^2$ | 34.41 $J_{sc}(mA/cm^2)$ | 0.781 FF | AM1.5G |
| **Box1-11-1** | 1.0002 M* | 603.5 $V_{oc}(mV)$ | 0.123 $I_{sc}(A)$ | 16.22 % Eff | ONE SUN |
| | 1.0000 S* | 502. $V_{mp}(mV)$ | 0.116 $I_{mp}(A)$ | | |

masked.

Fig. 7.3: Light I-V measurements for the 16.2% cell

Table 7.1: Effect of doping concentration on the efficiency of string ribbon silicon solar cells.

| Cell ID | $V_{oc}$ | $J_{sc}$ | FF | Eff | Voc | Eff25 | $n_{eff}$ | $Jo_{eff}$ | Rs | Rsh@-1 | Rsh@0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | (mV) | ($mA/cm^2$) | | (%) | (mV) | (%) | | ($A/cm^2$) | ($-cm^2$) | ($-cm^2$) | ($-cm^2$) |
| **Rs = 0.3 ohm-cm** | | | | | | | | | | | |
| EK01-1 | 591 | 28.60 | 0.752 | 12.7 | 591 | **12.7** | 1.68 | 3.0E-12 | 0.33 | 60,594 | 53,734 |
| EK01-2 | 584 | 28.63 | 0.762 | 12.7 | 584 | **12.7** | 2.43 | 4.1E-12 | 0.65 | 68,187 | 59,779 |
| ***Ave*** | ***587*** | ***28.61*** | ***0.757*** | ***12.7*** | ***587*** | ***12.7*** | ***2.06*** | ***3.6E-12*** | ***0.49*** | ***64391*** | ***56756*** |
| **Rs = 0.7 ohm-cm** | | | | | | | | | | | |
| EK71-1 | 602 | 31.24 | 0.778 | 14.6 | 602 | **14.6** | 2.08 | 2.2E-12 | 0.32 | 108,899 | 56,003 |
| EK71-2 | 600 | 30.86 | 0.776 | 14.4 | 600 | **14.4** | 2.35 | 2.3E-12 | 0.38 | 99,578 | 55,418 |
| ***Ave*** | ***601*** | ***31.05*** | ***0.777*** | ***14.5*** | ***601*** | ***14.5*** | ***2.22*** | ***2.2E-12*** | ***0.35*** | ***104238*** | ***55711*** |
| **Rs = 1.5 ohm-cm** | | | | | | | | | | | |
| EK11-1 | 602 | 35.42 | 0.769 | 16.4 | 602 | **16.4** | 2.21 | 2.5E-12 | 0.47 | 85,579 | 82,999 |
| EK11-2 | 600 | 34.87 | 0.760 | 15.9 | 600 | **15.9** | 2.54 | 2.7E-12 | 0.46 | 46,141 | 46,758 |
| ***Ave*** | ***601*** | ***35.14*** | ***0.765*** | ***16.1*** | ***601*** | ***16.1*** | ***2.38*** | ***2.6E-12*** | ***0.47*** | ***65860*** | ***64879*** |
| **Rs = 3.0 ohm-cm** | | | | | | | | | | | |
| EK31-1 | 562 | 34.65 | 0.756 | 14.7 | 562 | **14.7** | 2.21 | 1.2E-11 | 0.65 | 79,445 | 84,772 |
| EK31-2 | 549 | 33.40 | 0.754 | 13.8 | 549 | **13.8** | 2.02 | 1.9E-11 | 0.61 | 91,234 | 87,729 |
| ***Ave*** | ***555*** | ***34.02*** | ***0.755*** | ***14.3*** | ***555*** | ***14.3*** | ***2.12*** | ***1.5E-11*** | ***0.63*** | ***85339*** | ***86251*** |

Table 7.1 shows the data for several 2cm x 2cm cells made on each material. The *best cell efficiency achieved in this study* was 16.2%. This was confirmed by SNL, as shown in Figs 7.3 & 7.4. This also happens to be the record high cell efficiency on String ribbon to date.

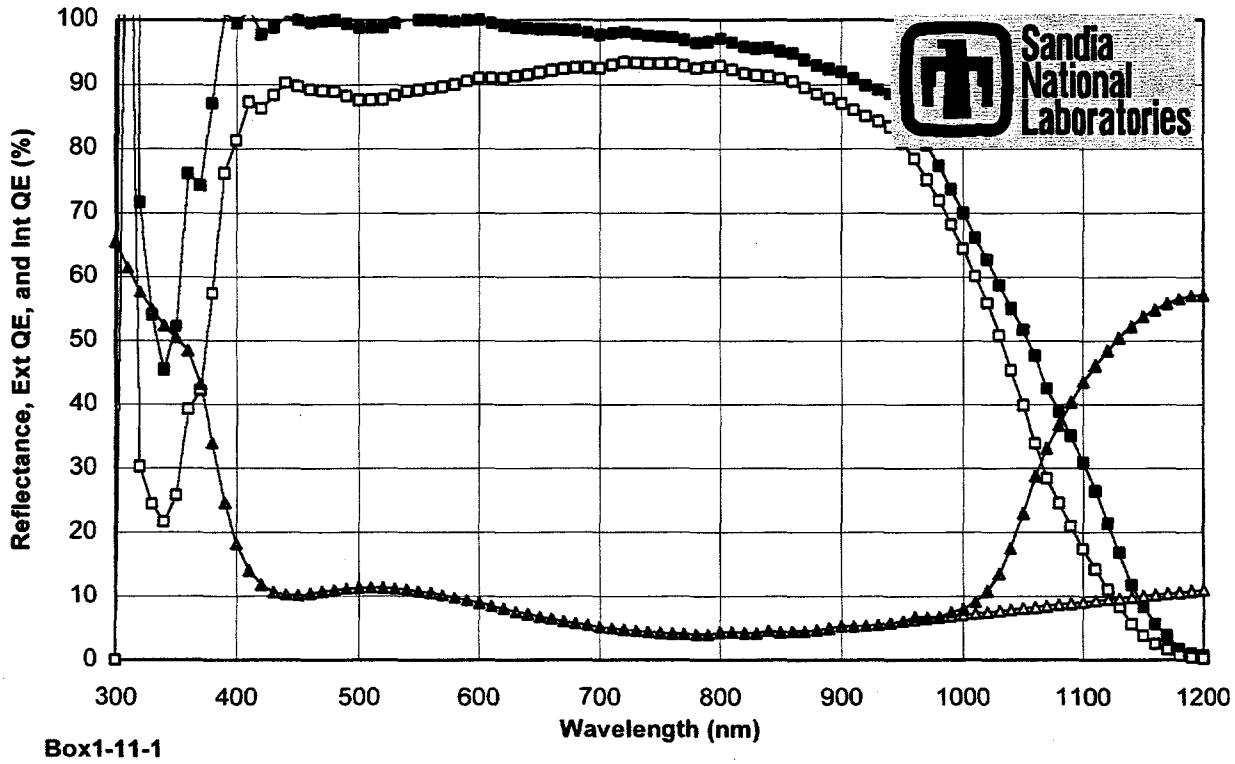



Fig. 7.4: Spectral response data for the 16.2% string ribbon silicon solar cell.

## 7.2 Fabrication of High Efficiency Cells on EFG Material using Photolithography Contacts

In this section we summarize the results of applying various technologies on EFG sheet silicon. In an effort to achieve high efficiency, EFG cells were fabricated by different technologies or process sequences. The objectives of this study were to:

a) Evaluate the effect of ramp-up rate on Al BSF and cell efficiency.
b) Evaluate the effect of Al BSF thickness on EFG cell efficiency.
c) Compare the effect of furnace oxide and rapid thermal oxide passivation on cell efficiency.
d) Compare the full CFP and RTP cells on EFG
e) Evaluate the impact of PECVD AR coating hydrogenation.

In order to accomplish the above objectives, six different runs were made. Run A involved standard SBLC process with furnace diffusion and oxidation, 1 - 2 microns evaporated Al BSF, photolithography contacts and double layer ZnS/MgF2 AR coating. In this run a slow ramp-up of 10°C / min was used during the Al BSF formation. Run B, was similar to Run A except 5 microns Al BSF was used to see the effect of deeper BSF. In Run C a thin 1 - 2 microns Al BSF was used but a fast ramp-up of 25°C / min was employed during the Al alloying process. In Run D, emitter was formed in a furnace but the 1 - 2 microns evaporated Al BSF and 100 Å RTO was formed simultaneously in the RTP system. The ramp rate in RTP was much higher 20°C /

seconds. Run E involved a full RTP process in which emitter diffusion, 1 - 2 microns Al BSF formation and front surface passivation were done in the RTP system. Runs A to E were coated with two layer ZnS/MgF2 AR coating. Finally, Run F involved a full RTP/RTO process, similar to Run E, with the exception of a PECVD SiN/MgF2 AR coating which was annealed at 720$^0$C in Air for 1.5 min for hydrogenation of bulk defects in EFG.

Tables 7.2 and 7.3 summarize the cell data from the above six runs. In all six runs cell efficiencies in excess of 14% were achieved (Table 7.2). Table 7.3 shows that there was only a slight improvement in going from 1 to 5 micron Al BSF using the slow ramp condition (Runs A and B). Switching from the slow ramp-up to fast ramp-up condition in the CFP process (Runs A and C) again did not show much improvement. This may be the result of smaller diffusion length in EFG (L<W), therefore changes in BSF quality due to increased thickness and fast ramp-up rate do not show a strong influence in cell performance which remained about 15.5%. Therefore, the EFG material used in this study needs to be thinned down to take advantage of the beneficial effect of thickness and fast ramp rate for higher efficiency EFG cells.

Runs D, E, and F involved RTP processing. Run E shows that RTP Al BSF and RTO formation reduced the EFG cell efficiency by about 1%. This is reflected in lower Voc and $J_{sc}$, which also indicates low bulk lifetime. This could be the result of ineffective Al gettering during the short 2 min RTP process. Run E, which is a full RTP process gave an efficiency of 14.9% (Table 7.3), which is about 0.5% lower than the counterpart

full CFP cell.

Run F, which involved a combination of full RTP and PECVD SIN, hydrogenation gave the best result with cell efficiencies exceeding 16%. High $V_{oc}$ (582 mV) and $J_{sc}$ (35.9 $mA/cm^2$) values in this run relative to the above five runs indicate higher bulk lifetime due to PECVD SiN induced hydrogenation of defects in EFG Si. Thinning the EFG Si and applying a thicker Screen Printed BSF should be able to give even higher EFG cell efficiency.

## Table 7.2: High Efficiency Solar Cells Fabricated on EFG ribbon material with Various Technologies.

(Thickness=11 mills, Rs=2-3 ohm-cm, Area = 1 sq cm)

| Cell ID # | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF (%) | Eff (%) |
|---|---|---|---|---|
| Run A - CFP/CFO (Slow Ramp, 1 - 2 micron Al BSF) | | | | |
| N3-1 | 570 | 33.3 | 78.3 | 14.9 |
| N3-2 | 566 | 32.9 | 77.9 | 14.5 |
| N3-3 | 565 | 32.7 | 77.7 | 14.4 |
| N3-4 | 563 | 32.4 | 77.7 | 14.1 |
| ET2-2 | 564 | 32.6 | 78.5 | 14.4 |
| N5-5 | 577 | 33.7 | 78.5 | 15.3 |
| N5-6 | 558 | 32.3 | 77.7 | 14.0 |

| | | | | |
|---|---|---|---|---|
| **N5-9** | **560** | **32.4** | **77.7** | **14.1** |
| Run B - CFP/CFO (Slow Ramp, 5 micron Al BSF) | | | | |
| **N21a1-1** | **578** | **34.6** | **77.1** | **15.4** |
| **N21a1-2** | **577** | **34.9** | **77.1** | **15.5** |
| **N21a1-3** | **574** | **34.7** | **77.3** | **15.4** |
| **N21a1-9** | **562** | **32.4** | **77.3** | **14.1** |
| **N21a1-10** | **560** | **32.5** | **77.4** | **14.1** |
| **N21a1-11** | **560** | **31.4** | **77.1** | **14.0** |
| **N4-2** | **570** | **33.6** | **77.0** | **14.8*** |
| Run C - CFP/CFO (Fast Ramp, 1 - 2 micron Al BSF) | | | | |
| **N1-1** | **567** | **33.3** | **78.1** | **14.7** |
| **N1-2** | **565** | **33.1** | **78.1** | **14.6** |
| **N1-3** | **560** | **32.8** | **77.7** | **14.3** |
| **N1-4** | **565** | **33.3** | **77.8** | **14.6** |
| **N1-8** | **559** | **32.6** | **77.5** | **14.1** |
| **N1-10** | **569** | **33.6** | **78.4** | **15.0** |
| **N1-11** | **573** | **33.9** | **77.5** | **15.0** |

| | | | | |
|---|---|---|---|---|
| **N1-12** | **575** | **34.3** | **78.0** | **15.4** |
| Run D - CFP/RTO (Fast Ramp, 1 - 2 micron Al BSF) | | | | |
| **N3-10** | **550** | **33.9** | **76.0** | **14.1** |
| **N3-11** | **556** | **33.3** | **75.9** | **14.1** |
| Run E - Full RTP /RTO (1 - 2 micron Al BSF) | | | | |
| **N1-3** | **569** | **34.1** | **77.0** | **14.9** |
| **N1-11** | **554** | **33.5** | **76.5** | **14.2** |
| Run F - Full RTP /RTO (1 – 2 micron Al BSF, PECVD SiN anneal @720C in air, etch thru , SiN/MgF2 ARC) | | | | |
| **E1-10** | **578** | **36.1** | **77.0** | **16.0** |
| **E1-13** | **554** | **34.0** | **75.1** | **14.1** |
| **E1-14** | **582** | **36.0** | **76.7** | **16.1** |

***Area 4 sq cm**

**Table 7.3: Effect of Various Processes on the Cell Performance on EFG Ribbon Material**

| Run # | Voc (mV) | Jsc ($mA/cm^2$) | FF (%) | Eff (%) | Process |
|---|---|---|---|---|---|
| Run A | 577 | 33.7 | 78.5 | 15.3 | CFP/1 – 2um-Al BSF,slow ramp/CFO/DLAR/PL |
| Run B | 577 | 34.9 | 77.1 | 15.5 | CFP/5um-Al BSF,slow ramp/CFO/DLAR/PL |
| Run C | 575 | 34.3 | 78.0 | 15.4 | CFP/1 – 2um-Al BSF,fast ramp/CFO/DLAR/PL |
| Run D | 553 | 33.7 | 76.1 | 14.2 | CFP/1 - 2um-Al BSF/RTO/DLAR/PL |
| Run E | 569 | 34.1 | 77.0 | 14.9 | Full RTP/1 - 2um-Al BSF/RTO/DLAR/PL |
| Run F | 582 | 35.9 | 76.7 | 16.1 | Full RTP/1 – 2um-Al BSF/RTO/ etch thru. SiN/MgF2/PL Anneal Air @ $720^0$ C for 90 sec |

## 7.3 Fabrication of High Efficiency SBLC cells on p-type Dendritic Web Silion Ribbon

This section summarizes cell fabrication done on P Web material from Ebara Solar Inc. using our standard base line (SBLC) process. This process involves conventional furnace processing (CFP) and photolithography contacts. Two different resistivity of P-Web material (0.3 and 7 ohm-cm) were used to study the effect of dopant-defect interaction and doping dependence on the final cell performance. In the standard SBLC process only 2 microns of evaporated Al BSF is used which results in high surface recombination velocity of > $10^4$cm/s. The cells were analyzed by light and dark J-V measurements and the results are summarized in Tables 7.4 and 7.5.

**Table 7.4: LIGHT IV**

| P-Web Resist. | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF (%) | Eff (%) | $n_{eff}$ | $J_{oeff}$ | $R_s$ | $R_{sh-1}$ |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| **0.2** | 632 | 33.0 | 80.9 | **16.8** | 1.89 | 7.2e-13 | 0.22 | 23,098 |
| | 630 | 32.9 | 80.4 | **16.7** | 2.02 | 7.7e-13 | 0.21 | 23,149 |
| | | | | | | | | |
| **7.0** | 575 | 34.6 | 79.5 | 15.8 | 1.53 | 7.0e-12 | 0.18 | 23,067 |
| | 570 | 34.7 | 78.6 | 15.6 | 1.60 | 8.3e-12 | 0.17 | 23,016 |

**Table 7.5: DARK J-V ANALYSIS OF BEST CELL**

| P-WEB Resistivity (Ω-cm) | $J_{o1}$ (pA/cm$^2$) | $J_{o2}$ (nA/cm$^2$) | $R_{sh}$ (Ω-cm$^2$) | $R_s$ (Ω-cm$^2$) | $n_2$ |
|---|---|---|---|---|---|
| | | | | | |
| **0.2** | 0.64 | 58.82 | 27879 | 0.19 | 2.41 |
| | | | | | |
| **7.0** | 2.28 | 5.33 | 24719 | 0.10 | 1.46 |

In this experiment low resistivity material gave an impressive cell efficiency of 16.8% while the high resistivity material gave an efficiency of 15.8%. The data shows that 0.2 ohm-cm silicon gave very high $V_{oc}$ of 630 mV and fill factors in excess of 0.8 while the 7 ohm-cm cell gave high $J_{sc}$ (34 – 35 mA/cm$^2$) but lower $V_{oc}$ (570 mV) and Fill Factor (<0.8). Higher resistivity cell gave lower cell efficiency (15.8%) because of higher Jo1 value, inspite of higher bulk lifetime. This is partly because of the 2 microns deep poor Al BSF which gives a recombination velocity of > $10^4$cm/s. Detailed analysis and model calculations show that the high resistivity material with a good BSF (BSRV <500 cm/s) and high lifetime should outperform low resistivity cells with low lifetime. Therefore a screen-printed deeper BSF is expected to give higher efficiency on high resistivity web material. Experiments are in progress to make screen-printed RTP BSF cells to achieve > 17% efficient p-web cells.

## 7.4 Development of 14+% EFG solar cells using Rapid thermal processing

Rapid thermal anneal process has been optimized and applied to achieve 14+% efficiency in large area (10×10 $cm^2$) screen-printed EFG silicon solar cells. Large area EFG silicon cells were fabricated in collaboration with ASE Americas. The n+ emitter, PECVD SiN single layer AR coating, and printing of silver contacts on the front and Al on the back were done at ASE Americas. The co-firing was done using a rapid thermal processor at Georgia Tech. During the RTP co-firing, PECVD silicon nitride on the front, aluminum paste on the back, and silver front contact metals were annealed simultaneously to achieve silicon nitride induced hydrogenation, aluminum back-surface-field, and ohmic contact of silver grids through the silicon nitride film. The objective was to optimize the rapid thermal processing to enhance hydrogenation, obtain a uniform deep Al-BSF, and Ag ohmic contacts on the front with good fill factor.

Figure 7.5 shows the temperature profile used during the rapid thermal processing that produced 14+% efficient large area EFG silicon solar cells. The profile includes a 60 sec anneal at 350 °C to burn off the organics in the Al and Ag pastes. The ramp-up rate from the burn-off step to the peak temperature found to be critical for achieving high fill factor. An optimum ramp-up rate was found to be 50 °C/sec. At the peak temperature, the wafers were heated for 5 sec. Finally, samples were cooled down to room temperature with a rate of 33 °C/sec. Total processing time was less than 110 sec.

Table 7.6 summarizes the cell data as a function of peak temperature. The co-firing peak temperature of 680 °C produced the best cell efficiency of 14.12 %. Figure 7.6 shows the lighted I-V curve for the 14.12 % large area EFG cell. Detailed analysis is in progress to understand the competition between SiN-induced hydrogenation and Al-BSF formation during the co-firing. Higher temperature is expected to give better Al-BSF but it may hurt the hydrogenation because of the lower retention probability of hydrogen at defects. Figure 7.7 shows that co-firing of Al and SiN is much more effective for hydrogenation compared to sequential firing of Al and SiN. More work is in progress to optimize the final firing cycle to achieve superior Al-BSF, higher bulk lifetime, better FF, and greater than 15 % efficient large area RTP fired EFG solar cells.

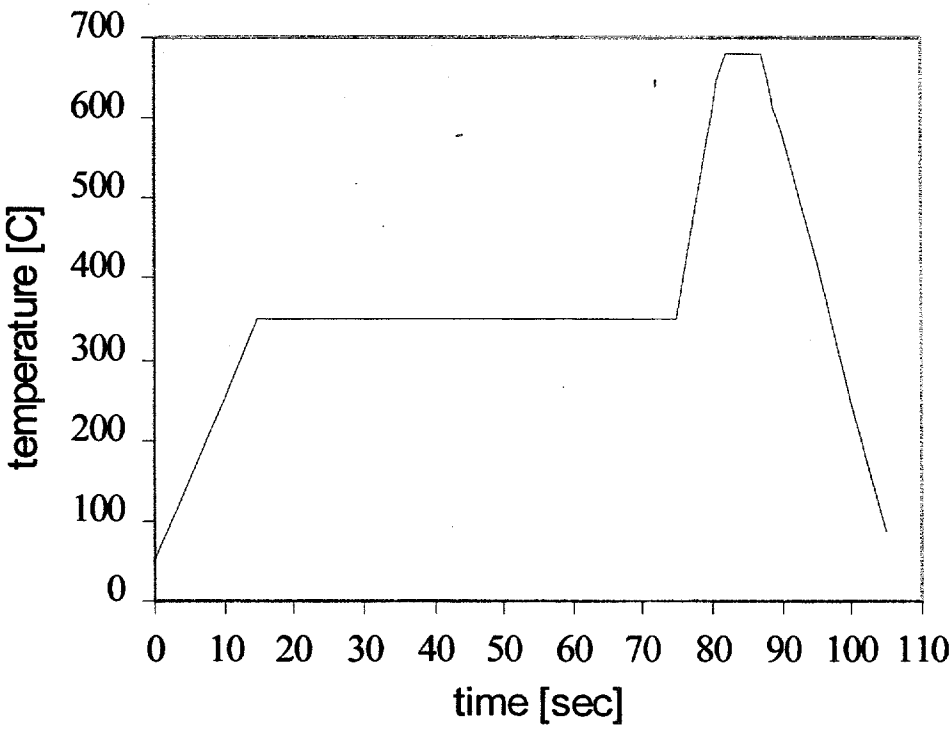



Figure 7.6. The temperature profile of RTP co-firing that produced 14.12 % efficiency on large area EFG silicon solar cell.

Table 7.6. Summarized data for lighted I-V measurement on RTP fired large area EFG silicon solar cells.

| Peak Temp | Jsc | Voc | FF | Efficiency |
|---|---|---|---|---|
| 680 | 32.42 | 0.592 | 0.735 | 14.12 |
| 720 | 32.57 | 0.588 | 0.727 | 13.93 |

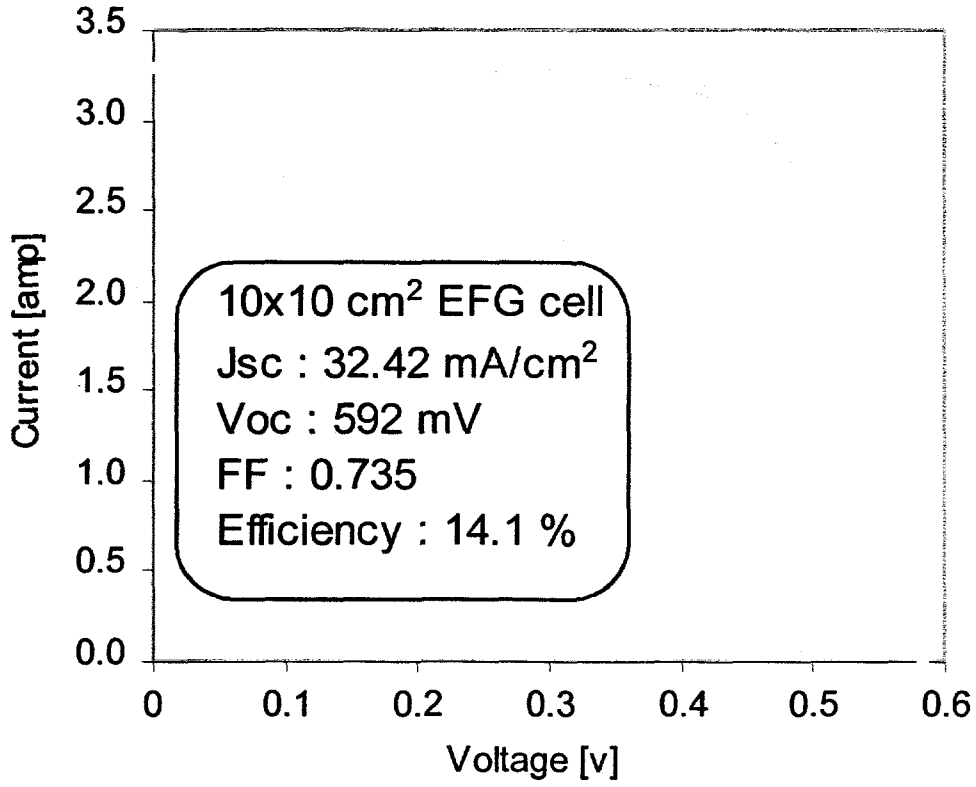



Figure 7.7. Lighted I-V curve for the 14.12 % cell.

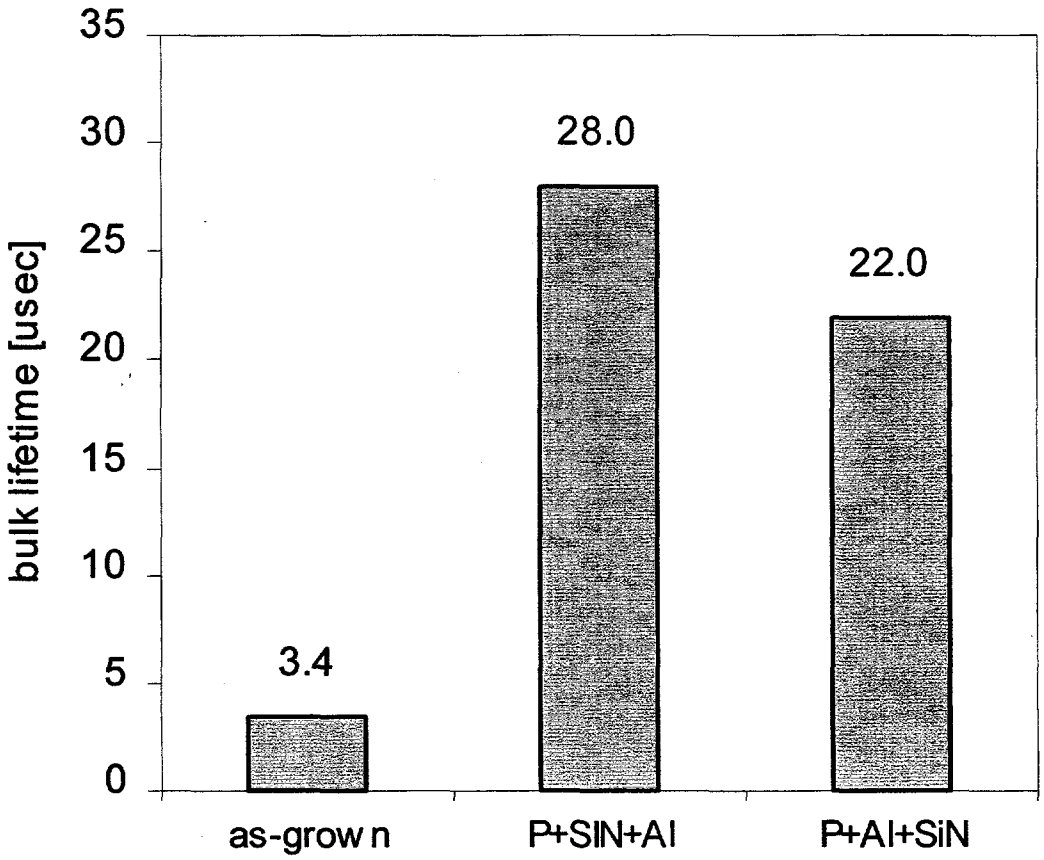



Figure 7.8. Measured minority carrier bulk lifetimes for co-firing (P+SiN+Al) and sequential (P+Al+SiN) firing in a conveyor lamp heated belt furnace.

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