**ATM Forum Technical Committee**
**ATM Forum/98- 0697**

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**TITLE:** Proposed Utopia Bus Structure for OC192 Data Rates



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**SOURCE:**

Dave King
GTE Government Systems
77 A Street
Needham MA, 02194
(781) 455-5832
dave.king@gsc.gte.com

Lyndon Pierson
Sandia National Laboratories
Box 5800
MS 0806
Albuquerque NM, 87185
(505) 845 8212
lgpiers@sandia.gov

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**ABSTRACT:** This contribution proposes a 64 bit wide bus structure that will operate at rates in excess of 10Gbps as a strawman for a OC192c Utopia Specification.

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# 1. Introduction

The presently adopted Utopia Specifications (Level 1 and 2) as well proposed Utopia Level 3 are limited to operating up to 3.2Gbps data rates. Since OC48 interfaces are already appearing commercially, this contribution is intended to start the process necessary for the migration to the 10Gbps rates found with OC192c.

# 2. Description

The presently proposed Utopia Level 3 is a 32 bit wide, point-to-point, CMOS interface which operates at a maximum frequency of 104MHz. Therefore, the Level 3 specification will transfer data rates up to 3.2Gbps. This specification was the starting point of this contribution.

In order to reach the 10Gbps necessary for OC192c, three major changes where made to the Utopia 3 structure: 1) bus width expanded to 64 bits, 2) low voltage Pseudo ECL (PECL) drivers and receivers, and 3) an operating frequency of in excess of 180MHz.

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## 2.1 Bus Structure

Figure 1 shows the proposed bus structure. The HEC byte has been removed and four user-defined bytes have been introduced to the ATM cell format.

**FIGURE 1, Octet Format**

| Bit 63 | Bit 55 | Bit 47 | Bit 39 | Bit 31 | Bit 23 | Bit 15 | Bit 7 | Time |
|---|---|---|---|---|---|---|---|---|
| Header 1 | Header 2 | Header 3 | Header 4 | UDF 1 | UDF 2 | UDF 3 | UDF 4 | 1 |
| Payload 1 | Payload 2 | Payload 3 | Payload 4 | Payload 5 | Payload 6 | Payload 7 | Payload 8 | 2 |
| Payload 9 | Payload 10 | Payload 11 | Payload 12 | Payload 13 | Payload 14 | Payload 15 | Payload 16 | 3 |
| Payload 17 | Payload 18 | Payload 19 | Payload 20 | Payload 21 | Payload 22 | Payload 23 | Payload 24 | 4 |
| Payload 25 | Payload 26 | Payload 27 | Payload 28 | Payload 29 | Payload 30 | Payload 31 | Payload 32 | 5 |
| Payload 33 | Payload 34 | Payload 35 | Payload 36 | Payload 37 | Payload 38 | Payload 39 | Payload 40 | 6 |
| Payload 41 | Payload 42 | Payload 43 | Payload 44 | Payload 45 | Payload 46 | Payload 47 | Payload 48 | 7 |

## 2.2 Interface Definitions

The I/O definitions for this proposal are based heavily on the present work on the Utopia Level 3 specification. Tables 1 and 2 define the basic interface necessary to support this interface. This structure only supports a point-to-point connection between the ATM and PHY devices. It also supports an optional multi PHY device given all the PHY devices are housed in one physical device.

The interface technology necessary to support 180MHz operation is proposed to be Low Voltage, Pseudo Emitter Coupled Logic (LvPECL). This is a 3.3v supplied, high speed I/O supported by the mainstream ASIC foundry houses.

**TABLE 1 Transmit I/O**

| Pin Name | Direction | Type | Definition |
|---|---|---|---|
| TxClk | ATM to PHY | Dif LvPECL | Transmit transfer frequency. Rising edge of TxClk_P is the active edge for data transition. |
| TxData(63:0) | ATM to PHY | LvPECL | The 64 bit data path for Transmit data, from ATM to PHY. TxData[63] is the MSB, TxData[0] is the LSB. |
| TxClav/ TxFull* | PHY to ATM | LvPECL | Cell Available. To indicate that space for at least one cell is available in the PHY transmit cell buffer. |
| TxSOC | ATM to PHY | LvPECL | Transmit Start Of Cell. Active high signal asserted by the ATM Layer to indicate the start of cell position. |
| TxEnb* | ATM to PHY | LvPECL | Transmit Enable. Active low signal asserted by the ATM Layer during cycles when the TxData contains valid cell data. *Optional, transition indicates valid address on the TxAdd bus for multi PHY use.* |
| TxAdd(4:0) *(Optional)* | ATM to PHY | LvPECL | Transmit Address. To select the PHY port for which the transmit data is to be destined. The address is used in both Direct Status indication mode and the Single Clav (polling) mode. |
| TxPrty *(Optional)* | ATM to PHY | LvPECL | Data path parity. The TxPrty parity bit serves as the odd parity bit over TxData[63:0]. |

**TABLE 2 Receive I/O**

| Pin Name | Direction | Type | Definition |
|---|---|---|---|
| RxClk | ATM to PHY | Dif LvPECL | Receive transfer frequency. Rising edge of RxClk_P is the active edge for data transition. |
| RxData(63:0) | PHY to ATM | LvPECL | The 64-bit data path for Receive data, from PHY to ATM. RxData[63] is the MSB, RxData[0] is the LSB. |
| RxClav/ RxFull* | PHY to ATM | LvPECL | Cell Available. To indicate that at least one cell is available in the PHY receive cell buffer Receive Interface. |
| RxSOC | PHY to ATM | LvPECL | Receive Start Of Cell. Active high signal asserted by the PHY Layer to indicate the start of cell position. |
| RxEnb* | ATM to PHY | LvPECL | Receive Enable. Active low signal asserted by the ATM Layer during cycles when the PHY port is allowed to send data. This then also indicates that the RxData contains valid cell data. *Optional, transition indicates valid address on the TxAdd bus for multi PHY use.* |
| RxAdd(4:0) *(Optional)* | ATM to PHY | LvPECL | Receive Address. To select the PHY port from which receive data is to be read. The address is used in both Direct Status indication mode and the Single Clav (polling) mode. |
| RxPrty *(Optional)* | PHY to ATM | LvPECL | Data path parity. The RxPrty parity bit serves as the odd parity bit over RxData[63:0]. |

## *2.3 Timing*

Figures 2 and 3 give some examples of the timing, which would be supported, by this interfaces.

**FIGURE 2, Transmit Timing Examples**

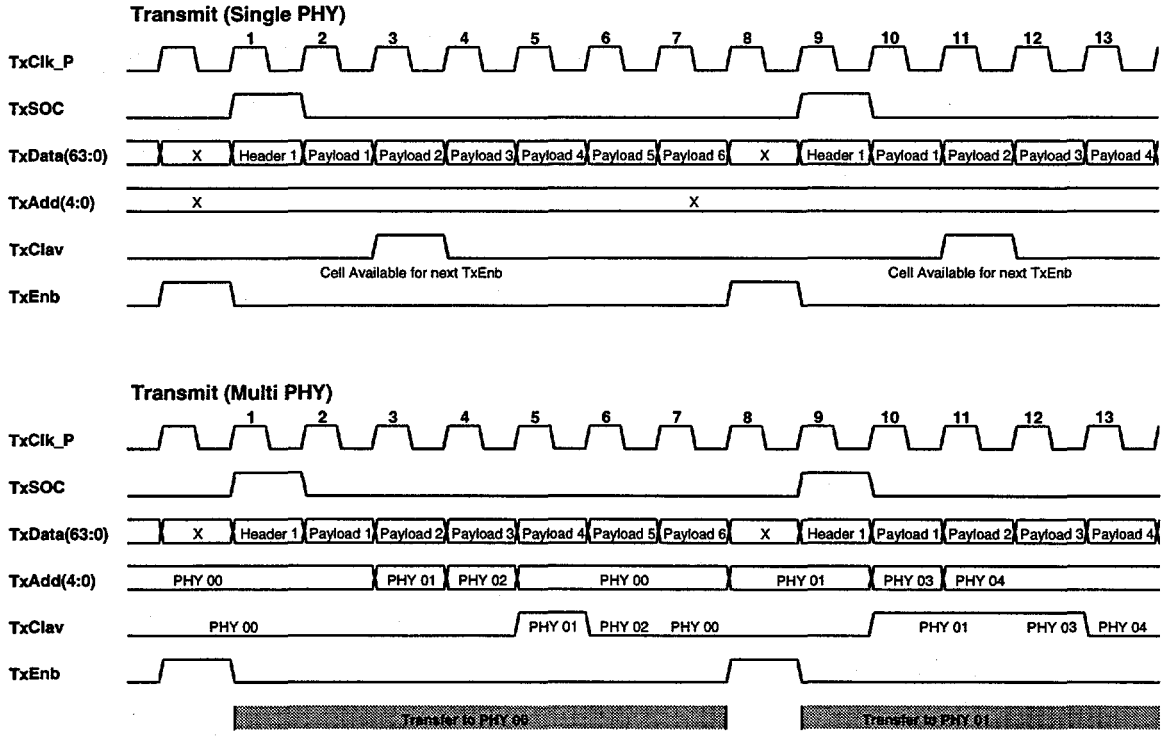
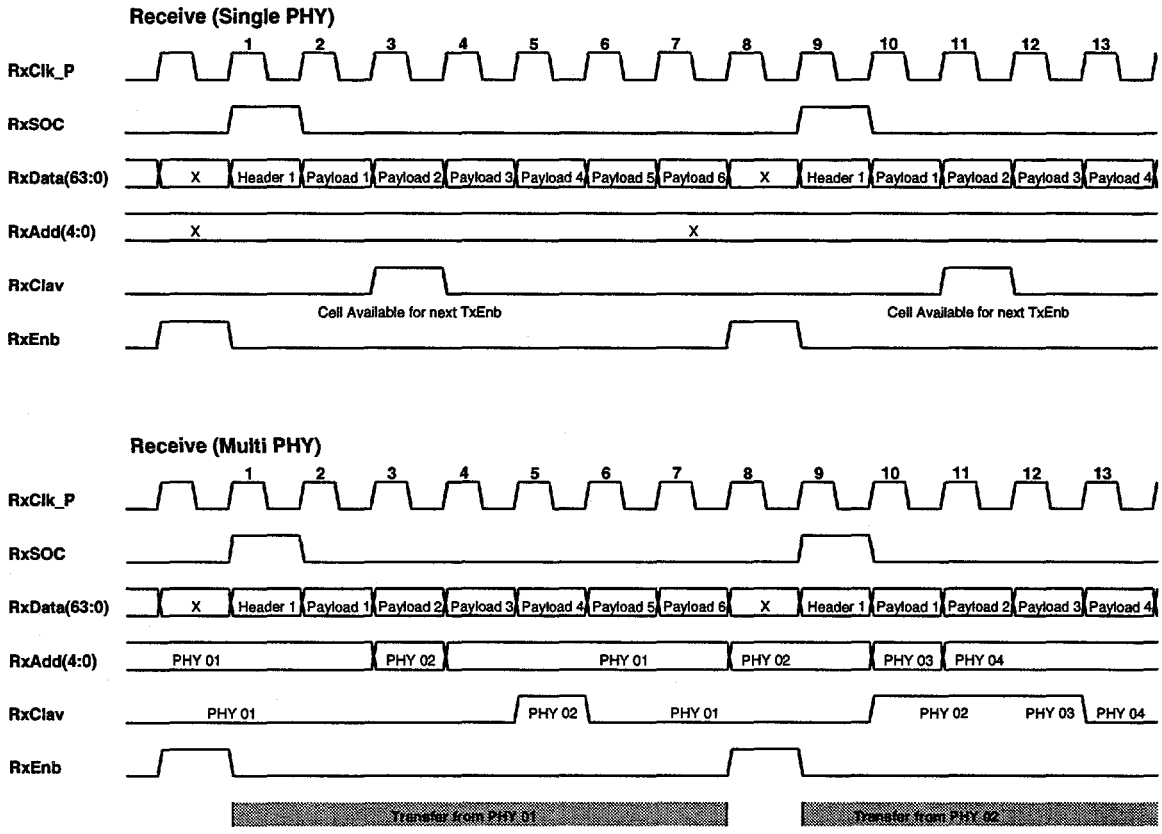


**FIGURE 3, Receive Timing Examples**




# 3. Motions

This contributions includes four motions:

## *3.1 Creation of a Utopia Level 4 Work Item and Living List Document*

The first motion of contribution 98-0697 is for the creation of an OC192 Work Item and it's accompanying Living List Document.

## *3.2 Incorporation of a 64 Bit Wide Bus Structure*

The second motion is to incorporate section 2.1 (Bus Structure) of this contribution onto the newly defined OC192 Living List Document.

## *3.3 Incorporation of an I/O Definition*

The third motion is to incorporate section 2.2 (Interface Definitions) of this contribution onto the newly defined OC192 Living List Document.

## *3.4 Incorporation of Timing Examples*

Lastly, motion is made to incorporate section 2.2 (Interface Definitions) of this contribution onto the newly defined OC192 Living List Document.