Characterization of Electrical Linewidth Test Structures Patterned in (100) Silicon-on-Insulator for Use as CD Standards¶

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ABSTRACT¶

This paper describes the fabrication and measurement of the linewidths of the reference segments of cross-bridge resistors patterned in (100) Bonded and Etched Back Silicon-on-Insulator (BESOI) material. The critical dimensions (CD) of the reference segments of a selection of the cross-bridge resistor test structures were measured both electrically and by Scanning-Electron Microscopy (SEM) cross-section imaging. The reference-segment features were aligned with <110> directions in the BESOI surface material and had drawn linewidths ranging from 0.35 to 3.0 μm. They were defined by a silicon micro-machining process which results in their sidewalls being atomically-planar and smooth and inclined at 54.737° to the surface (100) plane of the substrate. This (100) implementation may usefully complement the attributes of the previously-reported vertical-sidewall one for selected reference-material applications. For example, the non-orthogonal intersection of the sidewalls and top-surface planes of the reference-segment features may alleviate difficulties encountered with atomic-force microscope measurements. In such applications it has been reported that it may be difficult to maintain probe-tip control at the sharp 90° outside corner of the sidewalls and the upper surface. A second application is refining top-down image-processing algorithms and checking instrument performance. Novel aspects of the (100) SOI implementation that are reported here include the cross-bridge resistor test-structure architecture and details of its fabrication. The long-term goal is to develop a technique for the determination of the absolute dimensions of the trapezoidal cross-sections of the cross-bridge resistors' reference segments, as a prelude to developing them for dimensional reference applications. This is believed to be the first report of electrical CD measurements made on test structures of the cross-bridge resistor type that have been patterned in (100) SOI material. The electrical CD results are compared with cross-section SEM measurements made on the same features.

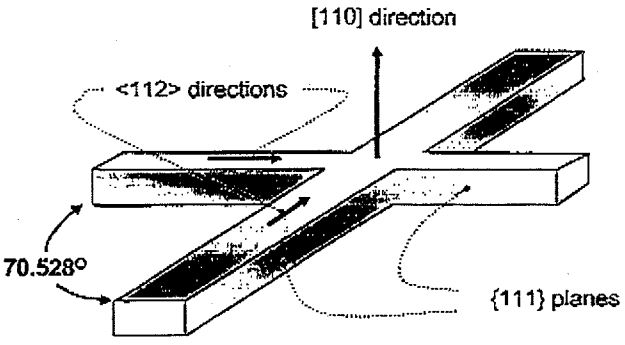

Figure 1. Lattice vectors pertinent to the (110) SOI implementation.

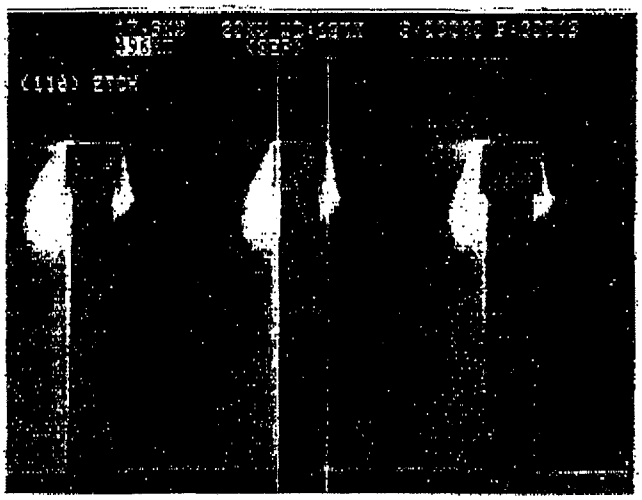

Figure 2. SEM image of line-features characteristic of the (110) implementation.

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BACKGROUND

A. *Relationship to Earlier Work*

Earlier papers have described electrical linewidth test structures replicated in (110) SOI material, referred to here as the "(110) implementation."[1,2,3] In the previously-reported (110) implementation, intersecting features are oriented non-orthogonally in lattice ⟨112⟩ directions.[4] **Figure 1** illustrates the relevant lattice vectors. An example of features delineated by KOH etching, otherwise known as silicon micro-machining, a {110} bulk silicon surface having silicon-nitride *in-situ* masking, and with features aligned in a [112] direction having sub-micrometer linewidths, is shown in **Figure 2**. The vertical sidewalls are coincident with lattice {111} planes and generate high levels of contrast which may be used for the pitch calibration of electron-beam CD systems.[5] Note that the silicon-nitride caps on the features, having served for *in-situ* masking, had not been removed when this image was recorded. The aspect ratio of their overhang is a measure of the lattice-plane selectivity of the KOH etching and/or misalignment of the axes of the lithographically-projected reference features with respect to a lattice <112> direction in the substrate surface plane.

In the (100) implementation, the subject of this paper, intersecting features of cross-bridge resistors are orthogonal

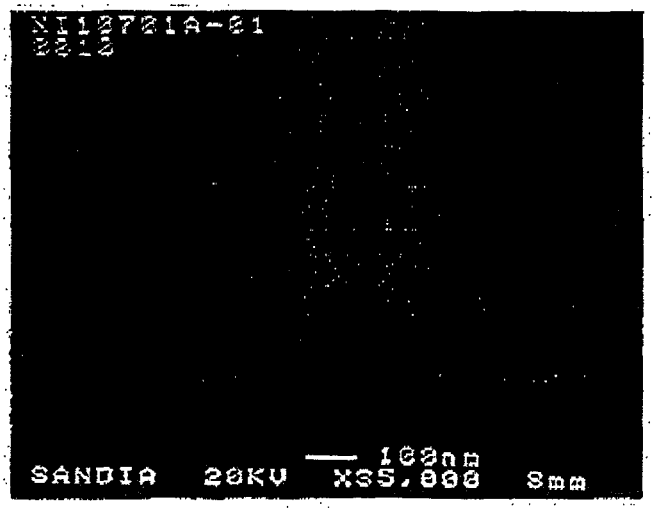

Figure 3. SEM image of orthogonal intersecting line-features characteristic of the (100) implementation.

and are oriented to lattice ⟨110⟩ directions. Their sidewalls have slopes inclined at exactly 54.737° to the surface (100) plane of the substrate. In both implementations, feature delineation by silicon micro-machining provides atomically-smooth feature sidewalls coincident with lattice {111} planes.

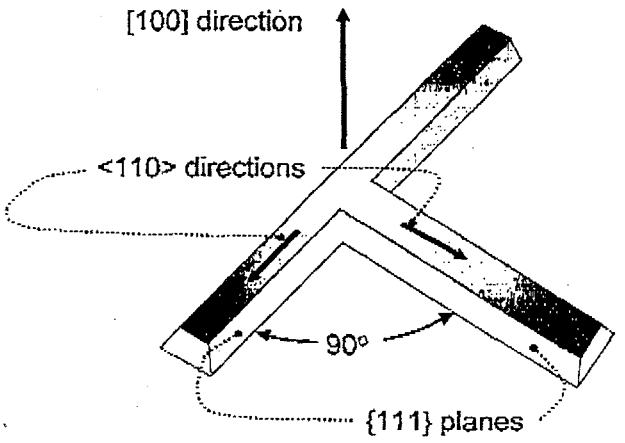

Figure 4. The pertinent lattice vectors of the (100) SOI implementation.

B. *Purpose of the Current Work*

The purpose of the current work is to supplement the potential usefulness of the reference vertical sidewall features of the (110) implementation with ones having known sidewall slopes less than 90°. Such reference features may be of comparable, or greater, value in metrology applications, such as instrument calibration, either when used alone, or when used in conjunction with the those generated in the (110) implementation. The new (100) implementation also opens the possibility of developing traceable reference materials for step-height applications. However, the specific near term purpose is to assess the repeatability and robustness of the new (100) implementation and its suitability for applying the proposed CD reference-material traceability strategy described below.

C. *End Use and CD-Traceability Strategy*

As in the case of the (110) implementation, we intend in the future to develop traceability of the new (100) reference materials through HRTEM (High Resolution Transmission-Electron Microscopy) imaging of the silicon lattice constituting the respective structures.[6] However, the cost and destructiveness of the HRTEM technique renders it impracticable when it alone is used for the purposes of traceability. The current strategy is, therefore, after wafer fabrication, and after whole-wafer electrical CD test, to perform HRTEM imaging at a selection of reference segments

at a selection of die sites. Lattice plane counts provided by a selection of HRTEM images are then used, effectively, to calibrate all the electrical CD measurements made on that wafer. In this way, traceability is imparted to all reference features whose electrical CDs have been measured. Without calibration by HRTEM or some other means, electrical CD measurements have not yet been shown to be able to provide traceability with usefully low levels of uncertainty.

TECHNICAL APPROACH

A. *Feature-Lattice Orientation for the (100) Implementation*

As mentioned previously, in the (100) implementation, test-structure features, such as those serving as bridge resistors, test-pads, and voltage taps, are orthogonal and oriented to lattice ⟨110⟩ directions. **Figure 3** and **Figure 4** respectively show an SEM image of the cross-section of a line feature and a map of pertinent lattice vectors of the (100) implementation.

B. *Selection of BESOI-Substrate Starting-Material*

The merits of SIMOX (Separation by Implantation with Oxygen) and BESOI silicon-on-insulator options for the subject application have been compared previously.[7] Each of these materials has previously been shown to provide physically uniform features with planar vertical sidewalls in the (110) implementation. While the SIMOX material is relatively inexpensive, and easy to acquire, the BESOI material has physical advantages that include a user's ability to specify an arbitrary thicknesses of the surface film in which the cross-bridge resistors are patterned, and a more sharply defined interface to the buried oxide. Additionally, the Kelvin-measurement $\langle V/I \rangle$ databases from which sheet resistance and reference-segment ECDs are extracted generally have much less statistical variability. ECDs extracted from cross-bridge resistors replicated on BESOI material are generally more consistent with the drawn CDs than those extracted from SIMOX wafers. Because of the resulting metrology advantages, BESOI material is preferred for this CD reference-material application.

C. *Sheet-Resistance Metrology Issues*

Sheet resistance, R_S, is typically the largest contributor to uncertainty in the measured electrical CD value, w_E, of the reference segment of the cross-bridge resistor. The electrical CD value, w_E, is derived from sheet resistance, R_S, and Kelvin $\langle V/I \rangle$ measurements, and is given by

$$w_E = \frac{(L - \delta L)}{V/I} \cdot R_S \qquad (1)$$

where δL is the reference-length shortening factor introduced previously.[8] One approach to obtaining an appropriate value of R_S is to determine a correction factor, obtained by means of current-flow modeling, to apply to the *apparent sheet resistance* determined from the set of $\langle V/I \rangle$ measurements normally extracted from the planar four-terminal sheet resistors.[9] The difference between the apparent sheet resistance, R_S', and the value R_S needed for the extraction of w_E from Eq. (1), is obtained by solving the equation

$$\exp\left(\frac{-\pi \cdot \langle V/I \rangle_1}{R_S'}\right) + \exp\left(\frac{-\pi \cdot \langle V/I \rangle_2}{R_S'}\right) = 1 \qquad (2)$$

where $\langle V/I \rangle_1$ and $\langle V/I \rangle_2$ are the respective complementary current-force/voltage-read Kelvin measurements made on the four-terminal sheet resistor. A second approach is to use four-terminal Greek-Cross configurations, for example, formed from lines with relatively large CDs to minimize the impact of the *non-planarity* that is characteristic of the (100) implementation. In this context, non-planarity is the attribute of structures patterned in a film of uniform composition and thickness with vertical sidewalls on its entire perimeter.

Additional current-flow modeling has now been performed to show the extent of the errors that are likely to be generated by non-planarity in the application of the second approach, specified above, in particular situations. For example, in Table 1 we show the relationship between R_S' and R_S, based on the results of current modeling, for two Greek-Crosses patterned in the same film and distinguished only by the widths of the lines constituting the cross. The important thing to note in

Table 1. The relationship between R_S' and R_S, based on the results of current modeling. In all three cases the actual film sheet resistance was 0.952 Ω/□. The apparent sheet resistance values were obtained from the application of Eq. (2) to values of $\langle V/I \rangle_1$ and $\langle V/I \rangle_2$ obtained from current-flow modeling.

Drawn top CD (μm)	Actual sheet resistance R_S (Ω/□)	Apparent sheet resistance R_S' (Ω/□)
0.20	0.952	1.163
5.00	0.952	0.961
10.00	0.952	0.955

Table 1 is that the application of Eq. (2) to $\langle V/I \rangle_1$ and $\langle V/I \rangle_2$ measurements extracted from the four-terminal sheet resistors generates R_S values that are too high by approximately 0.9% for the 5-μm linewidths used for forming the four-terminal Greek-Cross sheet resistor. A selection of results obtained by the application of this 0.9% correction to measurements made on four-terminal sheet resistors with 5-μm CDs, regardless of the drawn CDs of the reference segments of the cross-bridge resistors in which they were incorporated, is shown in **Figure 5**. The diminution of sheet resistance for structures having the lower row numbers is due to actual variations of the film's sheet resistance with the location of the respective test structures. The drawn top CDs are the only distinguishing characteristic of each of the eight test structures in the module.

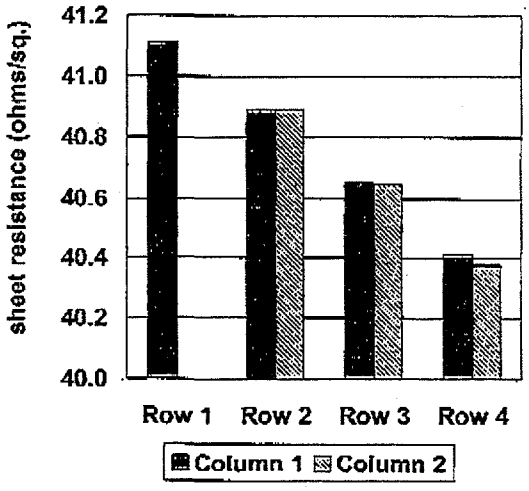

Figure 5. Results of R_S measurements made on a set of Greek-Cross four-terminal sheet resistors that were tested at a particular die site.

D. Test-Structure Design and Test-Chip Layout

Figure 6 shows a cross-bridge resistor test structure having 22 different reference segments ranging in length from 7.45 μm to 45.0 μm. It is patterned with 7 different drawn reference-segment linewidths ranging from 0.35 μm to 3.0 μm within a single test-structure module. Seven identical modules are replicated on each die site as shown in **Figure 7**.

The multiple reference-segment architecture of the cross-bridge resistor allows the determination of δL from the electrical measurements by two different methods. This quantity may, on the one hand, be extracted from measurements of the width of the single, tapped, voltage tap in **Figure 6** in conjunction with an expression for it in terms

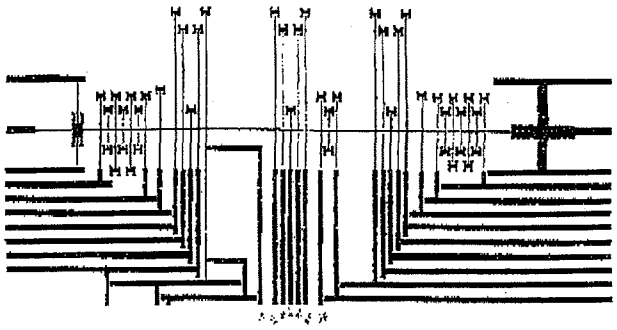

Figure 6. Test structure of (100) implementation which is patterned with 7 different drawn linewidths ranging from 0.35 μm to 3.0 μm on each die site.

of bridge and tap linewidths derived from current-flow modeling, as in the case of the (110) implementation.[10] On the other hand, applicable values of δL may be extracted from analysis of a set of $\langle V/I \rangle$ measurements made on the multiple reference-length segments of each test structure at a particular die site, as in previous work.[11]

The test-structure architecture shown in **Figure 6** features two four-terminal sheet resistors. The one on the left is a boxed structure with narrow CD lines. The one on the right has the 5-μm feature-top CDs. According to the results shown in Table 1, Eq. (2) generates a value of R_S' that is 0.9% in excess of the correct value of R_S needed for insertion into Eq. (1) for the estimate of the associated reference-segment ECD.

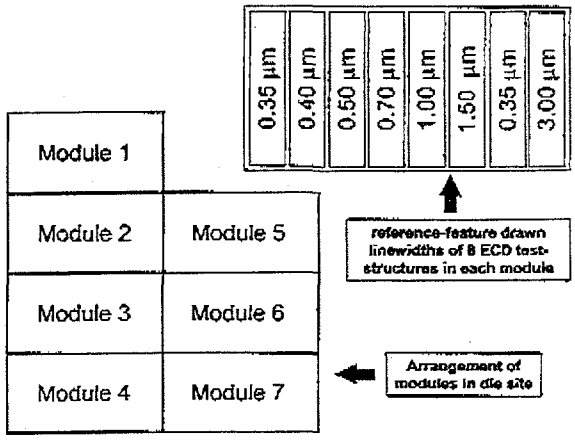

Figure 7. The test structure is patterned with 7 different drawn reference-segment linewidths within a single test-structure module. Seven identical modules are replicated on each die site.

Table 2. Selection of cross-bridge resistor reference-segment CDs as measured from cross-section SEM micrographs of the type shown in **Figure 3**.

Drawn CD (μm)	top (μm)	bottom (μm)	mean (μm)
0.35	0.34	1.88	1.10
0.35	0.34	1.80	1.10
0.40	0.34	1.89	1.12
0.50	0.49	2.03	1.26
0.70	0.69	2.23	1.46
1.00	0.90	2.44	1.67
1.50	1.48	3.03	2.25
3.00	2.97	4.52	3.75

E. Test Structure Fabrication

The BESOI wafers which generated the feature shown in **Figure 3** were fabricated according to an established SOI micro-machining process flow that has been reported previously.[4] An etch of 19% by weight of KOH in water at 80°C is commonly used to define structures in bulk silicon material having {111}-planar faces. The pattern to be transferred is typically replicated first in a 500-Å silicon-nitride hard mask. The buried BESOI oxide layer serves as an etch stop normal to the wafer surface. It allows over-etching of the order of 150-200% which is effective in clearing out all remaining silicon not having a {111} surface. An alternative etch is tetramethyl ammonium hydroxide. An appropriate hard mask in this case is silicon dioxide. In either case, the {111} planes of exposed silicon etch significantly slower than any others. Material surfaces remaining at the completion of an etch are either those that are protected by the *in-situ* hard masking or by surfaces having one of the orientations of the {111} family.[2]

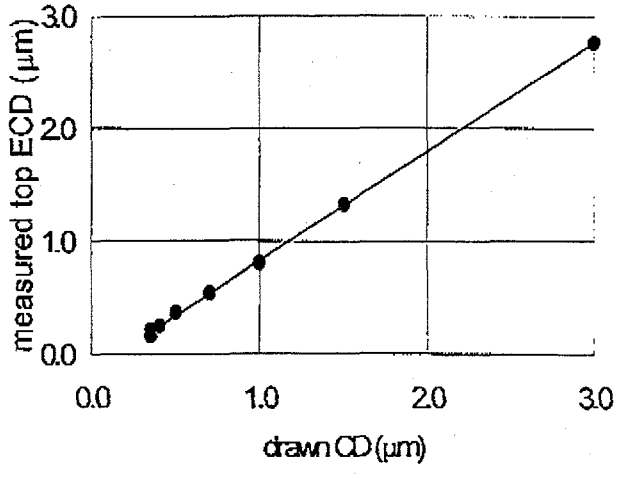

Figure 8. An example of the top-surface widths, computed from their known height and measured electrical CDs, as a function of drawn linewidths for a selection of structures.

F. SEM Measurements

A selection of reference-segment features from Block 5 at die site C7R3 on wafer NI-10702A-01, having drawn linewidths ranging from 0.35 μm to 3.0 μm were measured from cross-section images of the type shown in **Figure 3**. In order to avoid reliance on the use of the SEM magnification marker, the magnification of each image was estimated from the assumed spatial constancy of the film thickness and the known feature sidewall slope. Specifically, the difference between the top and bottom linewidths of a given feature is uniquely expressed in terms of the feature's height. On this basis, a set of eight scaling factors for the eight reference-feature images, and the height, that minimized the sum of the squares of the differences between the scaled top widths and the drawn top widths was selected. In the minimization process, each replicated top width was adjusted by a constant representing the difference between it, and its respective drawn top width. In reality, this quantity is determined by factors such as the amount of hard-mask undercut sustained during the pattern-replication process. For the measurements illustrated, it amounted to -0.031 μm.

The height value of 1.092 μm was found to minimize the sum of the squares of the differences between the scaled CDs of the feature-top images and their corresponding drawn CDs, when each of the latter was adjusted by a fixed constant, as described above. The absolute value of the height extracted from a neighboring test chip on the wafer, by HRTEM imaging, was 1.075 μm.[12] This level of agreement supports the validity of the minimization approach described above for this particular application, although it is not being claimed here as universally valid. The application of the same set of scaling factors to the feature heights of the respective SEM cross-section images resulted in an average height value, for the eight reference segments, of 1.078 μm with a standard deviation of 0.018 μm.

For the reader's cross-reference purposes, the summary results in Table 2 include the SEM-determined width at half height, which is the dimension registered by corresponding electrical CD measurements.

G. Electrical Measurements for a Particular Test Chip

An example of the electrical vs. drawn linewidths for the same selection of structures is shown in **Figure 8.** The electrical CDs, in principle, correspond to the half-height physical widths of the reference feature. In **Figure 8**, the electrical CDs have been converted to feature-top widths for the purposes of facilitating a comparison with the drawn CDs. This of course needs knowledge of the feature height. The number that was used for the results that have been shown in **Figure 8** was 1.092 μm. This is the value obtained from the SEM-image analyses, and supported by an independent measurement technique, as described previously. We observed that an uncertainty of 10 nm in feature height translated into approximately the same amount of uncertainty in the resultant feature-top ECDs.

Finally, in **Figure 9** the feature-top ECD is plotted against the SEM-determined feature-top CD. The origin of the offsets, ranging from 82 nm to 186 nm in this case, between the two measurement techniques, is not clear at this time. Various tests have suggested that the SEM measurements are likely to be correct to within less than 50 nm. A likely origin of the offsets is thought to be that the electrical height of a reference feature is up to 100 nm less than its physical height due to, as yet, unknown variations in the electronic properties of the surface-silicon material near its interface with the underlying BESOI oxide layer. If, for example, the features are attributed an electrical height of approximately 0.91 μm, then the SEM and electrical measurements typically match to within less than 10 nm. However, such a disparity between effective electrical height and physical height can not be explained by surface-charge-induced majority carrier depletion since the known doping level of the material generates a depletion depth of less than 10 nm. On the other hand, we have very recently observed evidence of a discontinuity in the electronic properties of the surface silicon approximately 200 nm from its lower boundary. In any event, the variability of the offset experienced with the two measurement techniques suggests that a larger measurement-comparison data base should be completed before a determination can be made as to whether electrical CD measurements, when made on reference features of the (100) implementation, and when properly calibrated by absolute measurements, are able to provide a suitable traceability path.

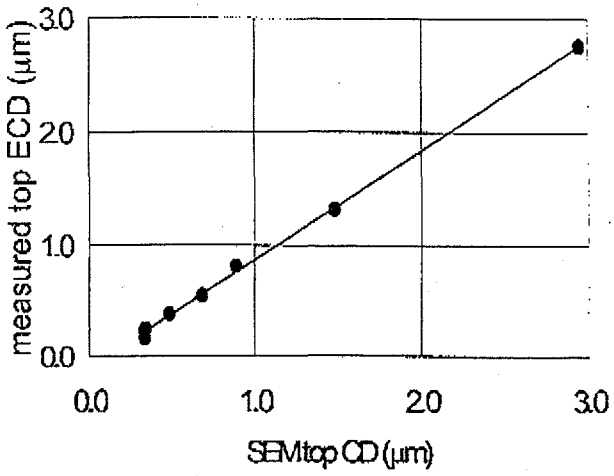

Figure 9. The electrically-determined feature-top CD is plotted against the SEM-determined feature-top CD.

SUMMARY

Electrical CD test structures fabricated in (100) SOI films have been fabricated and tested. Their top-surface linewidths determined from the electrical CDs have been measured and compared with SEM cross-section measurements. Both sets of measurements show close correlation with the drawn CDs but exhibit respective offsets of approximately -200 nm, and -31 nm. The long-term goal is to develop a technique for determination of the absolute cross-sectional dimensions of the reference segments. However, one of the implications of the limited selection of results so far available, and presented here, is that the use of appropriately calibrated cross-section SEM measurements might be as satisfactory as, or even preferred over, electrical measurements as the secondary reference means in establishing a traceability path for CD reference materials configured in the (100) implementation.

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imaging to the subject structures. The authors acknowledge layout and drawing services provided by Christine Murabito and Colleen Ellenwood. Drs. Jeffrey Sniegowski, Curt Richter, and Stephen Knight are acknowledged for technical reviews and Jane Wilkes, Kate Cresswell, and Erik Secula are thanked for editorial reviews.

REFERENCES

[1]. R.A. Allen, P. M. Troccolo, J. C. Owen III, J. E. Potzick, and L. W. Linholm, "Comparisons of Measured Linewidths of Sub-Micrometer Lines Using Optical, Electrical, and SEM Metrologies," SPIE Vol. 1926, Integrated Circuit Metrology, Inspection, and Process Control VII, pp. 34-43 (1993).

[2]. M.W. Cresswell, R.A. Allen, W.F. Guthrie, J.J. Sniegowski, R.N. Ghoshtagore, and L.W. Linholm, "Electrical Linewidth Test Structures Fabricated in Mono-Crystalline Films for Reference Material Applications," IEEE Transactions on Semiconductor Manufacturing, Vol. 11, pp. 182-193 (1998).

[3]. Mono-crystalline Test Structures, and Use for Calibrating Instruments, M. W. Cresswell, R. N. Ghoshtagore, L. W. Linholm, R. A. Allen, and J. J. Sniegowski, United States Patent Number: 5,684,301.

[4]. M.W. Cresswell, J. J. Sniegowski, R. N. Ghoshtagore, R. A. Allen, W. F. Guthrie, A. W. Gurnell, L. W. Linholm, R. G. Dixson, and E. C. Teague, "Recent Developments in Electrical Linewidth and Overlay Metrology for Integrated Circuit Fabrication Processes," Jpn. J. Appl. Phys. 35, Part I (12B), 6597-6609 (1996).

[5]. Y. Nakayama and K. Toyoda, "New Sub-micron Dimension Reference for Electron-Beam Metrology System," Integrated Circuit Metrology, Inspection, and Process Control, Vol. 2196, pp. 74-78 (1994).

[6]. R. A. Allen, T. J. Headley, S. C. Everist, R. N. Ghoshtagore, M.W. Cresswell and L.W. Linholm, "High-Resolution Transmission Electron Microscopy Calibration of Critical Dimension (CD) Reference Materials", to be submitted to IEEE Transactions on Semiconductor Manufacturing.

[7]. R.A. Allen, R.N. Ghoshtagore, M.W. Cresswell, L.W. Linholm, and J.J. Sniegowski, "Comparison of Properties of Electrical Test Structures Patterned in BESOI and SIMOX Files for CD Reference Material Applications," Proceedings of SPIE, Vol. 3332, 124-131, (1998).

[8]. R.A. Allen, M.W. Cresswell, and L.M. Buck, "A New Test Structure for the Electrical Measurement of the Widths of Short Features with Arbitrarily Wide Voltage Taps," IEEE Electron Device Letters, 13 (6), 322-324 (1992).

[9]. M.W. Cresswell, N.M.P. Guillaume, W.E. Lee, R.A. Allen, W. F. Guthrie, R.N. Ghoshtagore, Z. Osborne, N. Sullivan, and L.W. Linholm, "Extraction of Sheet Resistance from Four-Terminal Sheet Resistors Replicated in Monocrystalline Films With Non-Planar Geometries," IEEE Transactions on Semiconductor Manufacturing, Vol. 12, pp. 154-165 (1999).

[10]. W. E. Lee, W. F. Guthrie, M. W. Cresswell, R. A. Allen, J. J. Sniegowski, and L. W. Linholm, "Reference-Length Shortening by Kelvin Voltage Taps in Linewidth Test Structures Replicated in Mono-Crystalline Silicon Films," Proceedings of the IEEE International Conference on Microelectronic Test Structures, Vol. 10, pp. 35-38 (1997).

[11]. M. W. Cresswell, J. J. Sniegowski, R. N. Ghoshtagore, R. A. Allen, W. F. Guthrie, and L. W. Linholm, "Electrical Linewidth Test Structures Fabricated in Mono-Crystalline Silicon Films for Reference-Material Applications," IEEE Transactions on Semiconductor Manufacturing, Vol. 11, pp. 1-12 (1998).

[12]. M.W. Cresswell, J. E. Boncvich, T. J. Headley, R.A. Allen, L. A. Giannuzzi, S.C.Everist, R.N Ghoshtagore, and P.J. Shea, "Comparison of Electrical CD Measurements and Cross-Section Lattice-Plane Counts of Sub-Micrometer Features Replicated in Silicon-on-Insulator Material," Proceedings of SPIE, February, 2000, to be published.