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Electrical Breakdown in Thin Oxides During Bias-Temperature Ramps

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35-word abstract

Electrical breakdown in thin oxides is assessed by a new bias-temperature ramp technique. No significant effect of radiation exposure on breakdown is observed for high quality thermal and nitrided oxides, up to 20 Mrad(SiO_2).

DISCLAIMER

Introduction

As MOS gate oxides have become thinner than about 10 nm, concerns about threshold voltage shifts in ionizing radiation environments have largely been displaced by concerns about the long-term reliability of the dielectric layer. For example, recent work at the University of Padova [1-3] has shown that high doses of ionizing radiation can lead to Radiation Induced Leakage Current (RILC) in oxides thinner than ~ 7 nm. RILC is enhanced leakage current through the gate oxide caused by defects in the insulator, and is analogous to the Stress Induced Leakage Current (SILC) [1-8] commonly observed in thin oxides exposed to high current electrical stress. Doses at which significant levels of RILC are observed typically exceed 1 Mrad(SiO_2) [1,3]. It is not known whether RILC or other types of oxide degradation lead to decreased device reliability at lower radiation doses typical of common system applications.

We have developed a new technique to assess the high-field electrical breakdown of thin oxides that is based on monitoring the current at fixed, high voltage during a temperature ramp. This technique takes advantage of the high-precision current measurements possible using a thermally stimulated current test system [9-11] in a different mode of operation. In this summary, we briefly describe these measurements, illustrate results for thin Al and Si gate capacitors from R&D and industrial-class facilities, and present the results of a study on the effects of radiation exposure on the breakdown of thermal and nitrided oxides.

Experimental Results and Discussion

Measurements of dielectric breakdown during high-field electrical stress are typically performed at or near room temperature via constant voltage or current stress methods [8,12]. Here we explore whether useful information can also be obtained by performing current measurements during a temperature ramp at high electric field. In Fig. 1 thermal Al-gate 6.5 nm oxides from a research and development class fabrication facility [13] are ramped from 20°C to ~ 300°C at ~ 0.11°C/s at 5.5–6.5 V biases (9.4–10.9 MV/cm electric fields, including gate-to-Si work function differences). These curves are representative of the responses of more than 20 devices measured from this wafer. At the two lowest voltages, the current I increases monotonically until the temperature T is high enough and/or enough charge has passed through the oxide that it breaks down. At higher voltages and lower values of T, there is a competition between defect creation and annealing at high currents and temperatures, leading to erratic I-T curves. For example, for the 6.5 V stress, an early apparent breakdown recovers before the oxide truly breaks down above 150°C. Although there is increasing current with increasing T, there is not a monotonic relationship between the applied voltage and the temperature at which breakdown occurs in Fig. 1, apparently due to differences in as-processed defect densities.

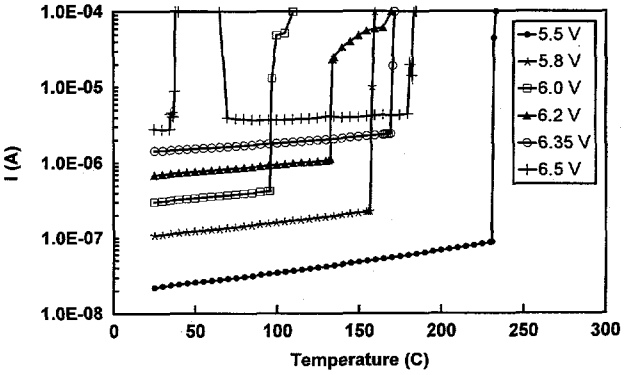

Figure 1. I-T plots versus applied gate bias for 0.00024 cm^2 n substrate capacitors with Al gates and 6.5 nm thermal oxides.

Industrial grade thermal and N_2O-nitrided 7.0 nm oxides [13] with poly-Si gates show strikingly more uniform I-T curves in Figs. 2 and 3, respectively. These curves are representative of more than 20 devices measured of each type. Here, the current increases monotonically with increasing voltage and temperature, and the breakdown temperature T_{BD} decreases monotonically with increasing electric field. Comparing the two device types, there is less current in the N_2O oxides than the thermal oxides at a given temperature. Moreover, T_{BD} is higher for the N_2O nitrided oxides than the thermal oxides when the T_{BD} is plotted versus applied bias in Fig. 4.

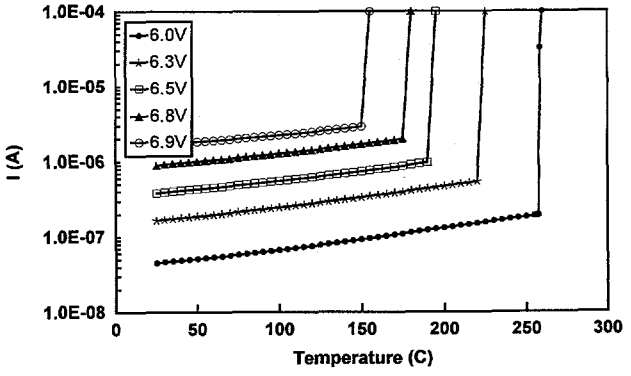

Figure 2. I-T plots versus applied gate bias for 0.00035 cm^2 n substrate capacitors with poly-Si gates and 7.0 nm thermal oxides.

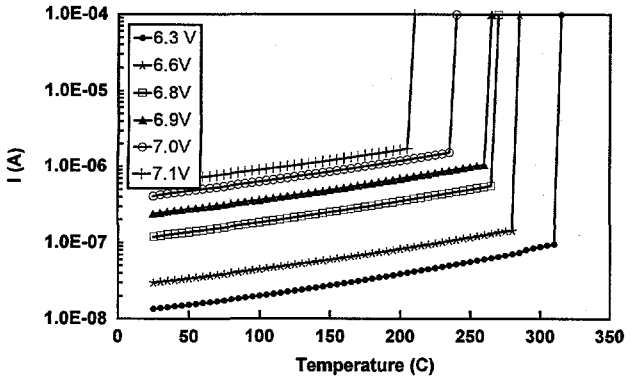

Figure 3. *I-T* plots versus applied gate bias for 0.00035 cm^2 *n* substrate capacitors with poly-Si gates and 7.0 nm nitrided oxides.

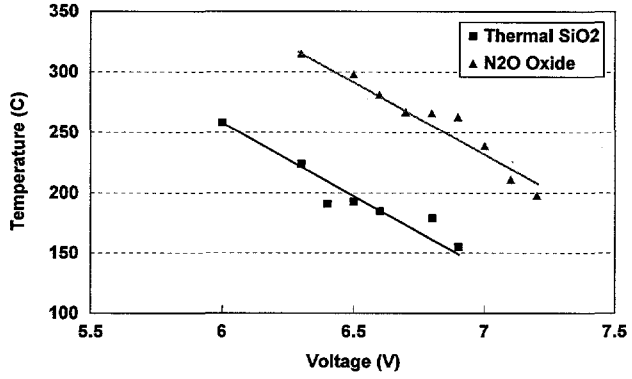

Figure 4. Breakdown temperature vs. applied gate bias for the devices of Figs. 2 and 3.

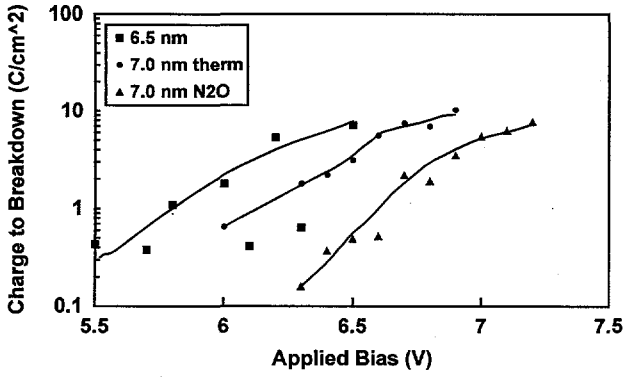

Figure 5. Charge-to-breakdown vs. applied gate bias for the devices of Figs. 1-3.

Charge-to-breakdown Q_{BD} is a parameter that is commonly used to compare the reliability of different oxides. Figure 5 is a plot of Q_{BD} as a function of applied gate bias for the devices of Figs. 1-3. To obtain an estimate of Q_{BD}, charge is integrated over time only to the temperature of the first breakdown-like event, as beyond that point the oxide conduction changes character, and Q_{BD} loses its usefulness as a figure of merit. Note that Q_{BD} increases at higher electric fields (corresponding to lower values of T_{BD}), until reaching a level comparable to breakdown levels at room temperature for these oxides (5-10 C/cm^2 [14]), which is a typical breakdown level for a high-quality 7 nm oxide at ~ 300 K [8,12]. Thus, for these devices, the charge that can flow through an oxide before high-*T* breakdown is less than or equal to the room temperature value of Q_{BD}. Because it is ultimately the amount of charge that transports through the oxide at a given temperature, or range of temperatures, that ultimately causes electrical breakdown, the value of T_{BD} is expected to decrease with decreasing ramp rate. The particular ramp rate selected here was chosen as a fastest rate that we can use in this particular system, while still preserving accurate thermometry [12,15].

We conclude from the discussion above that, for the highest electric fields in Figs. 1-4, the breakdown mechanisms at room and elevated temperatures are similar. Hence, the current-temperature ramp technique provides a useful way to look at oxide reliability. During these ramps, breakdown occurs "prematurely" (i.e., at reduced values of Q_{BD}) at lower fields and higher temperatures, consistent with trends in previous work performed at constant field and temperature [5,12,16,17]. In the full paper, a simple deconvolution analysis will be presented which shows that the current-temperature ramp technique illustrated here leads to significantly increased values of Q_{BD} with increasing temperature than previously expected, especially for the nitrided oxides. That is, these parts break down at higher temperatures and greater values of Q_{BD} than one would have predicted from prior work on different devices that exhibit similar values of Q_{BD} at room temperature [12]. Specifically, the reduction in Q_{BD} with increasing temperature for thermal oxides is found to be ~ 2 times less in Fig. 2 than in previous work on thermal oxides, and the relative decrease in Q_{BD} for the nitrided oxides is another factor of ~ 3 less than for the thermal oxides.

Some of the differences in temperature response between this and prior work may be due to differences in as-processed defect densities among the devices. However, the increased levels of Q_{BD} at elevated temperature in this work may also occur because the ramp technique allows the oxide to relax as the device is heated under bias, in contrast to methods in which high electric fields are established at high temperatures. The further improvement in Q_{BD} for the ni-

trided oxides at elevated temperature is likely a result of the nitride-inhibited motion of hydrogen-related species that can degrade the reliability of the oxide [12], as we will discuss further in the full paper.

Figure 6 shows the effects of ionizing radiation exposure on the breakdown response of the thermal oxides of Fig. 2. Here devices were irradiated with 10-keV x rays at a dose rate of ~ 3000 rad(SiO_2)/s to doses as high as 20 Mrad(SiO_2) at 3 V bias. Threshold voltage shifts due to oxide and interface trap charge were less than ~ 100 mV, even at the highest doses, showing that there is little net charge trapping in these thin oxides [18,19], although the presence of neutral defects and/or dipole charge cannot be excluded [20]. Figure 6 shows that there is no significant effect of radiation exposure on T_{BD}. Similar trends were observed for more than 15 other thermal or N_2O-nitrided oxides irradiated at positive, negative, or zero bias. For example, *I-T* ramps are compared in Fig. 7 for (a) nitrided oxides, and (b) thermal oxides, where devices are either unirradiated, irradiated to 20 Mrad(SiO_2) at ± 3 V at a rate of ~ 3000 rad(SiO_2)/s with 10-keV x rays, and/or (for one of the nitrided oxides) given a 1-week room-temperature anneal at 3 V between x-ray irradiation and breakdown testing. In none of these or other examples we have examined have either the levels of current at low temperature or the values of Q_{BD} or T_{BD} been affected significantly by radiation exposure. If, as one suspects, ionizing radiation exposure breaks weak bonds in SiO_2 and/or releases hydrogen species in the gate oxide, it is clear these defects are not significantly affecting the *I-T* curves here.

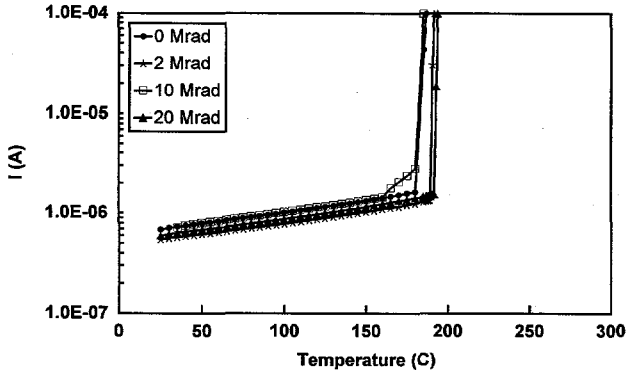

Figure 6. *I-T* plots versus radiation dose for the thermal oxides of Fig. 2. The applied gate bias was 3 V during irradiation and 6.6 V during postirradiation *I-T* stress. Values of Q_{BD} were ~ 5.6, 4.7, 5.7, and 5.1 C/cm^2 for capacitors irradiated to 0, 2, 10, and 20 Mrad(SiO_2), respectively.

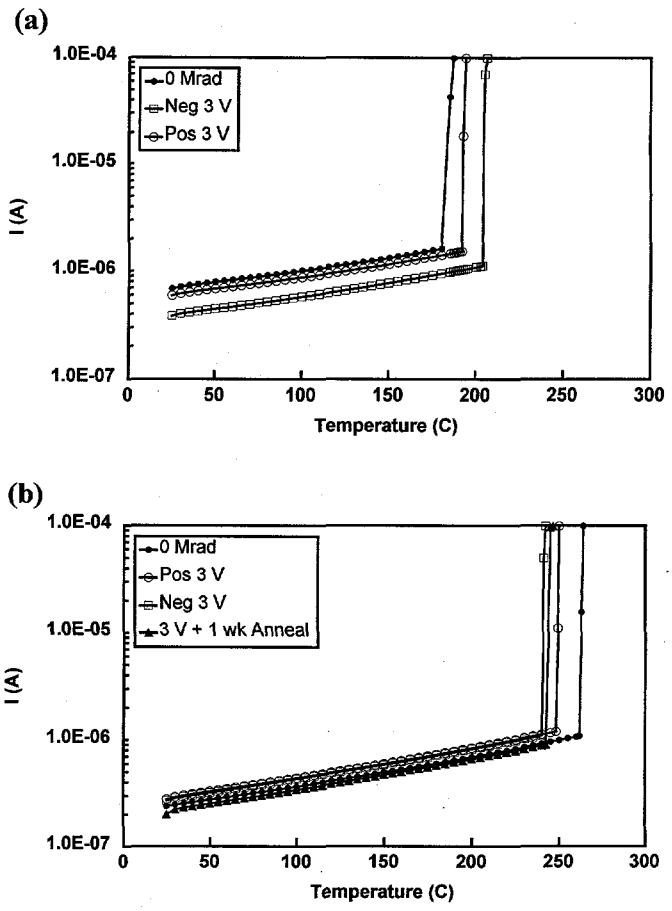

Figure 7. *I-T* plots versus radiation dose and/or postirradiation room-temperature annealing for (a) the N_2O nitrided oxides of Fig. 3, and (b) the thermal oxides of Fig. 2. The applied gate bias was ± 3 V during irradiation; the postirradiation *I-T* stress voltage was 6.9 V for the nitrided oxides, and 6.6 V for the thermal oxides. Values of Q_{BD} were ~ 3.5, 4.0, 3.7, and 3.1 C/cm^2 for the N_2O oxides of (a), in order of appearance in the caption, and ~ 5.6, 5.1, and 3.8 C/cm^2 for the corresponding oxides in (b).

Summary and Conclusions

We have found that *I-T* measurements can provide useful information about electrical breakdown in thin oxides. High-quality oxides (e.g., the Si gate devices in Figs. 2 and 3) can show exceptionally well-behaved characteristics with high reproducibility from device to device. Other oxides like that the Al gate capacitor in Fig. 1 can show much more erratic response. Hence, *I-T* measurements can potentially be used as a figure-of-merit to evaluate the intrinsic reliability of MOS gate insulators. Moreover, we have also found that these measurements can provide a useful test for the effects of radiation exposure on intrinsic oxide reliability, as illustrated in Figs. 6 and 7.

The results of Fig. 4 show differences in conduction at high fields between N_2O-nitrided and thermal oxides. These differences are evidently due to differences in effective barrier heights, conductivity, and/or material quality, as we will discuss further in the full paper. The results of Figs. 6 and 7 suggest no significant decrease in thin MOS dielectric reliability for radiation doses up to 20 Mrad(SiO_2) for high-quality 7 nm nitrided or thermal oxides. However, radiation-induced leakage currents have been reported in other devices with still thinner gate oxides [1-3], and more defective oxides may be more sensitive to reliability degradation with radiation exposure. Hence, while these results show there is no fundamental reduction in the reliability of high-quality oxides due to radiation exposure, they do not prove that the reliability of other types of oxides will be similarly unaffected. In the future, it would be extremely interesting to perform these measurements on alternative gate dielectrics to SiO_2.

Acknowledgments

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References

[1] A. Scarpa, A. Paccagnella, F. Montera, G. Ghibaudo, G. Pananakakis, G. Ghidini, and P. G. Fuochi, "Ionizing Radiation Induced Leakage Current in Ultra-Thin Gate Oxides," IEEE Trans. Nucl. Sci. **44**, 1818 (1997).

[2] M. Ceschia, A. Paccagnella, A. Cester, A. Scarpa, and G. Ghidini, "Radiation Induced Leakage Current and Stress Induced Leakage Current in Ultra-Thin Gate Oxides," IEEE Trans. Nucl. Sci. **45**, 2375 (1998).

[3] A. Candelori, A. Paccagnella, M. Cammarata, G. Ghidini, and P. G. Fuochi, "Fowler-Nordheim Characteristics of Electron Irradiated MOS Capacitors," IEEE Trans. Nucl. Sci. **45**, 2383 (1998).

[4] P. Olivo, T. N. Nguyen, and B. Riccò, "High-Field-Induced Degradation in Ultra-Thin SiO_2 Films," IEEE Trans. Electron Dev. **35**, 2259 (1988).

[5] K. F. Schuegraf and C. Hu, "MOSFET Substrate Current During Fowler-Nordheim Tunneling Stress and SiO_2 Reliability," J. Appl. Phys. **76**, 3695 (1994).

[6] D. J. DiMaria and E. Cartier, "Mechanism for Stress-Induced Leakage Current in Thin SiO_2 Films," J. Appl. Phys. **78**, 3883 (1995).

[7] P. E. Blöchl and J. H. Stathis, "Hydrogen Electrochemistry and Stress-Induced Leakage Current in Silica," Phys. Rev. Lett. **83**, 372 (1999).

[8] R. Degraeve, B. Kaczer, and G. Groeseneken, "Degradation and Breakdown in Thin Oxide Layers: Mechanisms, Models, and Reliability Prediction," Microel. Reliab. **39**, 1445 (1999).

[9] D. M. Fleetwood, R. A. Reber, Jr., and P. S. Winokur, "Effect of Bias on Thermally Stimulated Current (TSC) in MOS Devices," IEEE Trans. Nucl. Sci. **38**, 1066 (1991).

[10] R. A. Reber, Jr. and D. M. Fleetwood, "TSC Measurements of SiO_2 Defect Density and Energy in Irradiated MOS Capacitors," Rev. Sci. Instrum. **63**, 2244 (1992).

[11] D. M. Fleetwood, R. A. Reber, Jr., L. C. Riewe, and P. S. Winokur, "TSC in SiO_2," Microel. Reliab. **39**, 1323 (1999).

[12] D. J. DiMaria, E. Cartier, and D. Arnold, "Impact Ionization, Trap Creation, Degradation, and Breakdown in SiO_2 Films on Si," J. Appl. Phys. **73**, 3367 (1993).

[13] F. W. Sexton, D.M. Fleetwood, M.R. Shaneyfelt, P.E. Dodd, and G. Hash, "Single Event Gate Rupture in Thin Gate Oxides," IEEE Trans. Nucl. Sci. **44**, 2345 (1997).

[14] F. W. Sexton, D. M. Fleetwood, M. R. Shaneyfelt, P. E. Dodd, G. L. Hash, L. P. Schanwald, R. A. Loemker, K. S. Krisch, M. L. Green, B. E. Weir, and P. J. Silverman, "Precursor Ion Damage and Angular Dependence of Single Event Gate Rupture in Thin Oxides," IEEE Trans. Nucl. Sci. **45**, 2509 (1998).

[15] D. M. Fleetwood, P. S. Winokur, M. R. Shaneyfelt, L. C. Riewe, O. Flament, P. Paillet, and J. L. Leray, "Effects of Isochronal Annealing and Irradiation Temperature on Radiation-Induced Trapped Charge," IEEE Trans. Nucl. Sci. **45**, 2366 (1998).

[16] S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981), pp. 402-407.

[17] D.J. DiMaria and J.H. Stathis, "Non-Arrhenius temperature dependence of reliability in ultrathin silicon dioxide films," Appl. Phys. Lett. **74**, 1752 (1999).

[18] J. M. Benedetto, H. E. Boesch, Jr., F. B. McLean, and J. P. Mize, "Hole Removal in Thin Gate MOSFETs by Tunneling," IEEE Trans. Nucl. Sci. **32**, 3916 (1985).

[19] N. S. Saks, M. G. Ancona, and J. A. Modolo, "Generation of Interface States by Ionizing Radiation in Very Thin MOS Oxides," IEEE Trans. Nucl. Sci. **33**, 1185 (1986).

[20] D. M. Fleetwood, P. S. Winokur, O. Flament, and J. L. Leray, "Stability of Trapped Electrons in SiO_2," Appl. Phys. Lett. **74**, 2969 (1999).