Hybrid Microcircuit Board Assembly with Lead-Free Solders

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Abstract

An assessment was made of the manufacturability of hybrid microcircuit test vehicles assembled using three Pb-free solder compositions 96.5Sn-3.5Ag (wt.%), 91.84Sn-3.33Ag-4.83Bi, and 86.85Sn-3.15Ag-5.0Bi-5.0Au. The test vehicle substrate was 96% alumina; the thick film conductor composition was 76Au-21Pt-3Pd. Excellent registration between the LCCC or chip capacitor packages and the thick film solder pads was observed. Reduced wetting of bare (Au-coated) LCCC castellations was eliminated by hot solder dipping the I/Os prior to assembly of the circuit card. The Pb-free solders were slightly more susceptible to void formation, but not to a degree that would significantly impact joint functionality. Microstructural damage, while noted in the Sn-Pb solder joints, was not observed in the Pb-free interconnects.

Introduction

Recent interest has grown with respect to the use of alternative, non-Pb bearing solders in the manufacture of electronic devices as well as the assembly of electronic circuit boards. A number of potential solder alloys have been identified for circuit board assembly, including the compositions: 93.9Sn-4.7Ag-1.7Cu (wt.%), 96.2Sn-2.5Ag-0.8Cu-0.5Sb, and 91.84Sn-3.33Ag-4.83Bi[1,2,3]. Several of these solders have been evaluated in test vehicle studies based upon organic laminate substrate systems[4,5,6]. Those evaluations have included manufacturability and defect assessments as well as thermal cycling reliability studies.

Another area of electronics assembly that warrants further study regarding Pb-free replacement solders is that of hybrid microcircuits (HMC) technology. Unlike circuit board technology based upon organic laminates and Cu conductor features, HMC circuit boards utilize a ceramic substrate and thick film conductive features[7]. Although the traditional ceramic substrate remains as largely alumina (Al_2O_3), low-temperature co-fired ceramic (LTCC) materials are also being identified, particularly for many high-frequency applications that require multi-layer substrate capabilities[8]. The surface conductive features of HMC products were constructed by screen printing an ink containing metal powders, glass adhesive ("frit"), and binder agents onto the substrate in the desired pattern. The metal powders are typically comprised of noble metals such as Ag, Au, Pt, and Pd, or mixtures of one or more of these elements. The screen printed circuit board is then fired at elevated temperatures (800-900°C), causing the following processes to occur simultaneously: (1) the binder agents are driven off; (2) the metal powder particles fuse and/or alloy together into a single layer; and (3) the glass frit

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migrates to the alumina surface and serves as the adhesive between that surface and the newly formed metal layer. The conductive features remain solderable owing to the noble metal components that comprise them. Therefore, the solder joint is made to an "alloy" layer comprised of Au, Pt, Pd, or Ag; it is this feature that distinguishes these interconnects from those made to the more traditional Cu pads. The conductive layer thickness ranges from 10 - 30 μm and, as such, is often referred to as a "thick film" coating.

An extensive amount of study has been performed at Sandia National Laboratories in the area of HMC assemblies and associated soldering issues, including manufacturability as well as solder joint reliability. These efforts have included the characterization of HMC circuit board test vehicles assembled with several Pb-free solder compositions [9,10]. Besides the development of an appropriate test vehicle to investigate solder joint manufacturability and reliability, the Sandia studies have examined the role of intermetallic compound layer development on Sn-Pb and Pb-free solder joint microstructure and mechanical strength. Solid-state intermetallic compound layer growth is particularly rapid in joints made between Sn-based solders and noble metal materials. Thus, a heightened concern prevails with regards to intermetallic compound layer development and the reliability of HMC solder interconnects.

A manufacturability study is described in this report. This study investigated the use of three Pb-free solders on a HMC test vehicle board. The test vehicle included several sizes of both leadless ceramic chip carriers (LCCC) and surface mount capacitors. The solder compositions used to make the interconnects were: 96.5Sn-3.5Ag (wt.%), 91.84Sn-3.33Ag-4.83Bi, and 86.85Sn-3.15Ag-5.0Bi-5.0Au. The circuit board substrate was alumina (96%) and the thick film conductor was comprised of Au, Pt, and Pd metals. The study included two detailed defect analyses of the solder joints. First, a low-magnification, visual inspection was made of all of the solder joints; defects such as solderability, pores, component registration, and solder ball formation were noted. Then, a selected number of solder joints representing each component configuration were metallographically cross sectioned to reveal the macro- and microstructure of the joints. The solder fillet profile was evaluated with regards to wettability of the package I/O and solder coverage of the conductor pad. The other properties that were examined included void formation; registration between the package I/O and the thick film pad; as well as any microstructural damage to the solder in the form of plastic deformation and/or cracks. The metrics of the individual solder joint were combined into a single value that represented each solder composition and package type provided on the test vehicle.

Experimental procedures

Three high-Sn, Pb-free solders were chosen for this study; those compositions (wt.%) along with their solidus (T_s), liquidus (T_l), or onset (effective solidus point) temperatures were: 96.5Sn-3.5Ag ($T_s = T_l = 221°C$), 91.84Sn-3.33Ag-4.83Bi ($T_{onset} = 212°C$), and 86.85Sn-3.15Ag-5.0Bi-5.0Au ($T_{onset} = 195°C$). Test vehicles were also assembled with the 63Sn-37Pb solder to provide baseline data. The Sn-Ag and Sn-Pb solders were obtained as commercial pastes (90% metal load, 30-70 μm diameter particles, RMA flux). Solder pastes for the Sn-Ag-Bi and Sn-Ag-Bi-Au alloys were made by the

following steps: (1) ingots of the alloys were fabricated at Sandia National Laboratories; (2) the metal was blown into powder 30-70 μm nominal diameters by Ames Laboratories, Ames IA; and (3) the powder was mixed to a 90% metal load using a commercially available vehicle that contained an RMA flux. The commercial paste vehicle was purchased from the same vendor that supplied the Sn-Pb and Sn-Ag pastes, thereby ensuring that the same RMA flux was used with all solders. The compositions of the solder alloy powders were confirmed by recording their respective melting properties using differential scanning calorimetry (DSC).

A photograph of the HMC test vehicle is shown in Figure 1. The test vehicle was comprised of 96% alumina substrate measuring 86.4 x 63.5 x 1.0 mm. The thick film conductor had a composition of 76Au-21Pt-3Pd (wt.%). A double print-dry-fire (850°C) process was used to build up a layer thickness of approximately 23 μm. A burnishing step on the pads was not required. The LCCC package I/O counts ("50 mil" pitch) and the number of packages per test vehicle (in parentheses) were: 16 (4); 20 (4); 32, rectangular (2); and 68 (1). Chip capacitor sizes and quantities were: 0805 (8), 1210 (8), 1810,4), 1825 (4), and 2225 (3). All of the packages and capacitors were daisy chain connected, although this capability was not utilized in the current study. The chip capacitors were verified to have been provided with 100% Sn terminations by the supplier. The LCCC castellations had the traditional Au finish. A property of the LCCC castellation that was evaluated in this study was the impact had by the 100Au finish on defect formation. For comparison, hot solder dipped coating was applied to the castellations of a second group of LCCC packages. In the coating process, each row of castellations was immersed into the solder bath at a 45°degree angle. The LCCC remained in that position for a time duration of 10 s. A bath temperature of 230°C was used for the Sn-Pb alloy; the Pb-free solder coatings were applied using a bath temperature of 255°C.

For each solder composition, two test vehicles were assembled, one with the LCCC castellations having the 100Au finish and the other test vehicle having been assembled with hot solder dipped, LCCC castellations.

Figure 1 - HMC test vehicle

The HMC test vehicles were assembled in the following sequence: (1) The paste was screen printed onto the substrate using a 0.2 mm thick stencil. The LCCC's and chip capacitors were hand-placed onto the paste deposits. Reflow of the solder paste to form the solder joints was performed in a four-zone, Sikama™ conductive oven using a nitrogen blanket (30 SCFH). The zone peak temperatures (zone #3) were 246°C, 266°C, and 260°C for the Sn-Pb, Sn-Ag, and Sn-Ag-Bi solders, respectively. The Sn-Ag-Bi-Au alloy used the same profile as the Sn-Ag-Bi solder. The "sweeper" speed was approximately 18 cm/min.

The defect evaluation was performed in two parts. First, a visual inspection was performed of the solder joints. The particular metrics of interest were: (1) wettability

(solderability) of the substrate (thick film) pads; (2) solderability of the LCCC castellations or chip capacitor terminations; (3) pores in the solder fillet; (4) mis-registration between the package I/O and the substrate pad; and (5) solder balls. A numerical value between 0 and 5, in 0.5 increments, was assigned to each metric. A value of 0 was assigned to the "poor" condition, be it alot of non-wetting in the case of solderability, or numerous solder balls for metric (5). Conversely, a metric value of 5 denotes the "good" condition such as good wetting and no solder balls.

The second defect analysis was performed on metallographic cross sections of the joints. Due to the sample preparation effort required by this analysis, not all of the solder joints could be examined. Therefore, the solder joints of selected chip capacitors and LCCC packages were evaluated; the components, their designations (e.g., U_ for the LCCCs), and solder joints are denoted in Figure 2. Solder joints on the LCCC packages were identified according to a row designation. For example, rows 1, 5, 9, 13, and 17 were sectioned on the U1 LCCC, resulting in an evaluation being made on each of ten solder joints. The LCCCs U4 and U5 were both 20 I/O packages from which six solder joints were examined (two joints per each of three sections 1, 3, and 5). Although having the same package configuration, the results from U4 were not combined with U5; similarly, the data from the four solder joints of U10 were kept separate from those of U11. The chip capacitors that were examined were four of the eight 1210 capacitors (C5 - C8) comprising the "small capacitors" group and the three 2225 capacitors (C17 - C19) designated as the "large capacitors" group. The metrics from the solder joints of each individual capacitor were combined into a single mean and standard deviation that represented the two groups.

The metrics that were evaluated in the metallographic cross sections were: (1) wettability of the substrate; (2) wettability of the LCCC castellation or chip capacitor termination; (3) void formation; (4) package mis-registration; and (5) damage to the solder in the form of cracks or permanent deformation. A quantitative value of between 0 and 5 with increments of 0.5 was assigned to each solder joint, per each metric parameter. The metric values were combined from amongst all of the solder joints per LCCC package (16 I/O, 20 I/O, etc.) or chip capacitor group size ("small" and "large"). A mean value was computed; an error term was represented by $\pm$ one standard deviation from the data.

Figure 2 - Photograph of the HMC test vehicle showing the chip capacitors, LCCC packages, and their solder joints that were metallographically cross sectioned. A U_ designation was given to the LCCCs; the 1210 and 2225 chip capacitors were grouped into the "small capacitors" and the "large capacitors."

Results.

A summarization of the visual inspection results will be made. The predominant feature observed from all of the test vehicles, irrespective of the Pb-free solder or baseline Sn-Pb alloy composition, was poor solder wetting of the LCCC castellations that did not have the Au layer removed by a hot solder dipping step. This defect even persisted for Sn-Pb solder joints as is illustrated in Figure 3a. Generally, Sn-Pb solder fillets rose between

40-80% of the castellation height; the Pb-free solders showed slightly poorer performance with fillet rises of 30-55%, 30-80%, and 40-80% for the Sn-Ag-Bi, Sn-Ag-Bi-Au, and Sn-Ag alloys, respectively. When the hot solder dipping step was introduced into the process flow, wetting of the LCCC castellations greatly improved (Figure 3b). Non-wetting was also observed on the substrate thick film pads for the LCCC packages assembled with the Sn-Ag solder. The solder joints of all chip capacitors exhibited good wettability by both the chip termination and thick film pad. A hypothesis is presented for this phenomenon following discussion of the cross sectional observations.

Figure 3 - Stereo photographs of the LCCC castellation formed by Sn-Pb solder: (a) non-hot solder dipped castellation and (b) hot solder dipped castellations.

The other metrics showed high values, indicating few, if any, defects. Void formation was not observed in any cases. The only observable instance of package misregistration was caused by the operator mishandling an LCCC package during the placement activity. Finally, a minimal extent of solder ball formation was observed. Those cases in which solder balls were observed, showed no dependence upon component package nor the specific solder alloy. Also, the degree of recorded solder ball formation would normally be eliminated by a further fine-tuning of the process parameters.

The defect analyses of metallographic cross sections taken from selected solder joints will now be described. The in-depth discussion will be limited to those metrics that exhibited significant changes; they included: (1) wettability of the LCCC castellation or chip termination, (2) void formation, and (3) solder damage. In nearly every case of alloy composition and component I/O, solder wetting of the thick film pad was excellent. Likewise, cross section views of the solder joints exhibited no instances of significant misregistration between the LCCC castellation or capacitor termination and the underlying substrate pad.

Solder wettability of the LCCC castellations was most strongly a function of whether or not the castellations had been hot solder dipped prior to assembly of the test vehicle. The discrepancy was significant for all of the solders. Shown in Figures 4a and 4b are optical micrographs taken from cross sections of the Sn-Pb solder joints on an LCCC package for the conditions of (a) having hot solder dipped castellations and (b) without hot solder dipped castellations. The optical micrographs in Figures 4c and 4d show the similar behavior for the Sn-Ag solder.

The absence of a hot solder dipping process resulted in a significant concentration of Au-Sn intermetallic compound particles in the solder. This artifact is illustrated by the high magnification, optical micrographs of LCCC, Sn-Ag solder joint fillets in Figure 5 showing joints that were made to (a) a hot solder dipped castellation and (b) a castellation that did not have the Au layer removed. The presence of Au-Sn intermetallic compound particles ("needles") is evident in the latter case. These particles imply that a significant compositional change has occurred to the solder which can potentially impact melting properties and subsequently, degrade solderability. Also, at sufficient concentration,

these brittle particles can impart a lower ductility to the overall, solder joint mechanical performance. This situation would be particularly troubling, given the already higher strength (and thus, reduced ductility) of the Pb-free solders.

Figure 4 - Optical micrographs of LCCC solder joints illustrating the effects of the hot solder dipping process on castellation wettability: (a) Sn-Pb solder and a hot solder dipped castellation; (b) Sn-Pb solder and no hot solder dipped coating; (c) Sn-Ag solder with hot solder dipped castellation; and (d) Sn-Ag solder with no hot solder dipped coating.

Figure 5 - Optical micrographs of LCCC solder joint fillets made with the Sn-Ag solder: (a) fillet microstructure resulting from an LCCC castellation having the hot solder dipped coating and (b) fillet microstructure containing Au-Sn intermetallic compound particles ("needles") when the hot solder dipping process was not been performed.

Shown in Figures 6a and 6b are the plots of the I/O wettability metric as a function of LCCC package. Both cases of non-hot solder dipped and hot solder dipped are shown. The chip capacitor data has also been included in the plot. These latter results serve to benchmark any wettability differences that may have been due to process-related factors such as changes in paste quantity or performance and slight variations in the furnace temperature profiles. Recall that the capacitors were not hot solder dipped. Clearly, when account was taken of those extrinsic factors represented by the chip capacitor data, the differences between the hot solder dipped and non-hot solder dipped joints were similar to those observed for the other two solders (Figures 6c and 6d). Finally, it was noted that, in general, for the non-hot solder dipped LCCC's, a slightly reduced degree of defect prevalence was observed with the "medium sized" U4 and U5 LCCC packages (20 I/O) as compared to the larger LCCC components U1 and U2 (68 I/O and 32 I/O, respectively) and smallest LCCC packages U10 and U11 (16 I/O).

Figure 6 - Graphs of the I/O wettability metric as a function of package configuration and whether or not the LCCC castellations had been hot solder dipped: (a) Sn-Ag-Bi solder, (b) Sn-Pb solder, (c) Sn-Ag solder, and (d) Sn-Ag-Bi-Au solder.

The micrographs in Figures 3 and 4, as well as the data in Figure 6, suggest that the quantity of solder in a "standard" paste deposit (or "brick") was insufficient to accommodate Au contamination caused by the castellation coating. Wettability of the Au coating, per se, was not suspect. Rather, it was presumed that the Au content introduced into the solder resulted in compositional changes that caused premature solidification of the molten alloy under the given process temperatures then in use (termed "constitutional solidification"). The hot solder dipping process provided for both the elimination of Au from the joint as well as an extra measure of solder to fill the solder fillet. The only

recourse to improve the solderability of the non-hot solder dipped LCCC castellations would have been to increase the process temperature.

The discussion of solder joint voiding begins with an examination of the metric values for the baseline Sn-Pb test vehicles; these data are presented in Figure 7a. The magnitude of the metrics indicates that void formation was very minimal with the Sn-Pb solder. Further examination of the data showed that neither the presence of a hot solder dipped coating or the particular configuration of the LCCC or chip capacitor package had a significant impact on void formation. A similar conclusion was drawn with respect to the LCCC and chip capacitor solder joints made with the Sn-Ag-Bi and Sn-Ag-Bi-Au solders.

Finally, the Sn-Ag solder demonstrated the most difficulty with voids, albeit still not of a sufficient magnitude that would jeopardize the functionality of the interconnects. The metric values in Figure 7d show: (1) overall lower mean values; (2) an increased discrepancy between the case of hot solder dipped LCCC castellations and those with the original Au coating; and (3) a high level of scatter in the data.

The observed trends in void formation with the Pb-free solders suggest an increased difficulty with eliminating the air and flux volatiles from the molten solder fillet structure. The inability to remove such gases can be attributed to a reduced flowability exhibited by the Pb-free solders as compared to the performance of the Sn-Pb solder.

As a final observation, it was noted in the case of all three Pb-free solders that the U1 LCCC solder joints were somewhat more prone to void formation than were the other package configurations. Since U1 is the largest LCCC package (68 I/O), the increased propensity for void formation may be due to the local temperatures not reaching sufficiently high values that would permit sufficient volatilization of the flux vehicle prior to flow by the molten solder. This circumstance has been observed when a single thermal schedule must accommodate a wide range of package configurations on the same circuit card; often, the temperature rise of the largest packages was curtailed in an effort to prevent overheating of the smaller configurations (including chip capacitors).

Figure 7 - Plots of the void metric as a function of component and the implementation of a hot solder dipping process on the LCCC castellations: (a) Sn-Pb solder, (b) Sn-Ag-Bi solder, (c) Sn-Ag-Bi-Au solder, and (d) Sn-Ag solder.

The final metric of interest that was compiled from the metallographic cross sections was that of solder damage. Solder damage was defined as the presence of plastic (permanent) deformation and/or cracks in the solder or interfaces. Cracking was not observed in any of the evaluated solder joints. Plastic deformation was not observed in any of the Pb-free solder joint structures, with the exception of a few chip capacitor solder joints made with the Sn-Ag solder. However, damage to the Sn-Pb solder joints was noted; it persisted primarily in the form of grain boundary sliding and phase boundary sliding. The deformation occurred in the solder that filled the gap between the under side of the LCCC

castellation or chip termination and the thick film pad. The source of the deformation was residual stresses generated by the local thermal expansion mismatch between the Sn-Pb solder and the alumina material that comprised both the LCCC package as well as the substrate materials. The deformation effects were likely to have been formed during the cool-down stage of the soldering process.

The damage metric as a function of package configuration for all solders, using the hot solder dipped LCCC castellations, is shown in Figure 8. The Sn-Pb solder damage metric exhibit a significant degree of scatter. This variability was caused by the fact that the extent of damage was dependent upon the size of the gap of the individual solder joint; the smaller the gap, greater was the extent of damage to the solder microstructure.

Figure 8 - Plot of the damage metric as a function of package configuration for all of the solders. The LCCC package data are from the case in which the castellations had received a hot solder dipped coating.

In the case of the non-hot solder dipped castellations, there was no damage present in the Sn-Pb solder microstructure (Damage was also absent from the Pb-free solder joints made to same LCCC castellations). This point is exemplified by the graph in Figure 9 showing the damage metric for Sn-Pb solder joints as a function of package type and whether or not the LCCC castellations had received a hot solder dipped coating to remove the Au layer. The absence of damage in non-hot solder dipped, Sn-Pb solder joints was caused by a strengthening effect arising from dissolved Au and the presence of Au-Sn intermetallic compound particles in the solder microstructure.

Figure 9 - Plot of the damage metric as a function of package configuration for the Sn-Pb solder joint. Data include both cases of the LCCC castellations having, and having not, received the hot solder dipped coating.

The absence of deformation in the stronger, Pb-free solder microstructures bodes well for the service reliability of those joints under thermal mechanical fatigue conditions. Improved thermal mechanical fatigue resistance has been confirmed by aging studies using organic laminate test vehicles[5,6,11,12].

Conclusion

The manufacturability of HMC assemblies using the three Pb-free solder compositions 96.5Sn-3.5Ag, 91.84Sn-3.33Ag-4.83Bi, and 86.85Sn-3.15Ag-5.0Bi-5.0Au was evaluated. Baseline data were provided by test vehicles assembled with 63Sn-37Pb solder. The test vehicle substrate was 96% alumina; the thick film conductor composition was 76Au-21Pt-3Pd (23 μm thick). All test vehicles exhibited excellent registration between the LCCC or chip capacitor package and the thick film solder pads. Improved wettability of LCCC castellations was realized by hot solder dipping the I/Os prior to assembly of the circuit card in order to eliminate the Au coating. The Pb-free solders were slightly more susceptible to void formation, but not to a degree that would

significantly impact joint functionality. Microstructural damage was also absent from the Pb-free solder joints, unlike their Sn-Pb counterparts.

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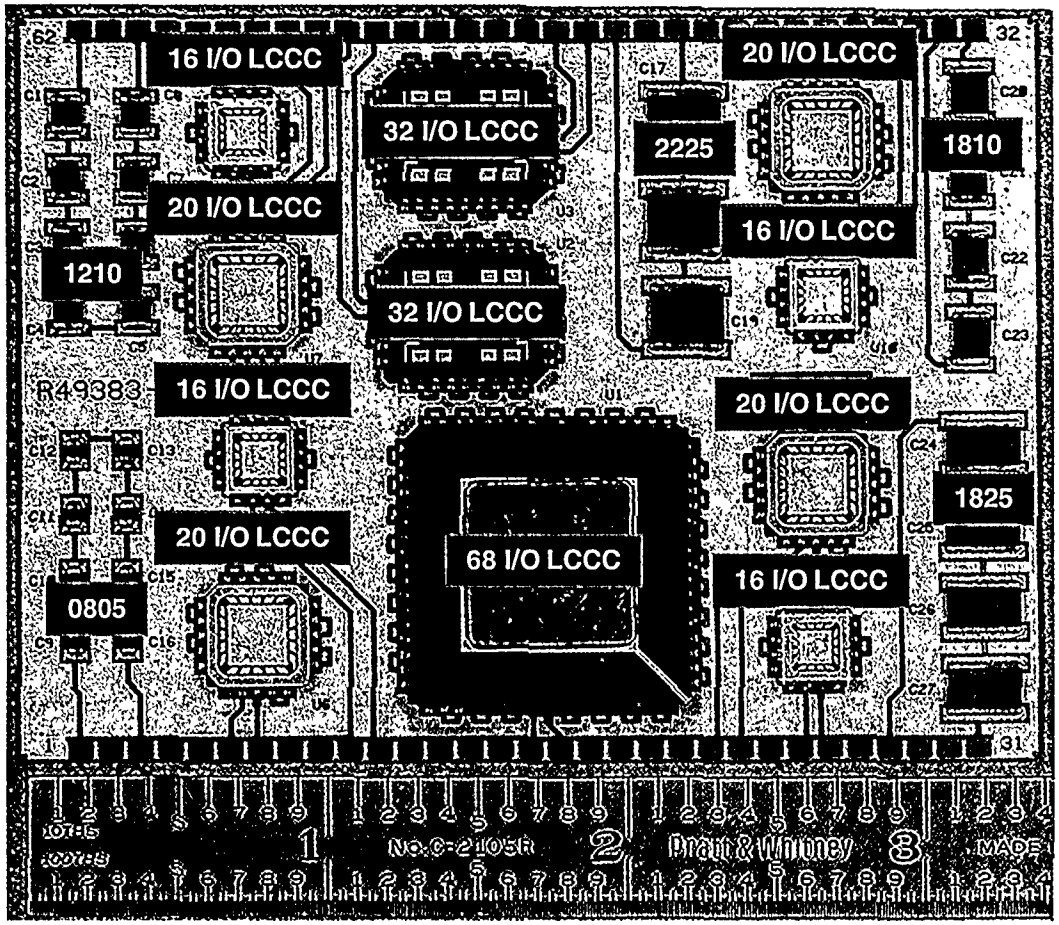

16 I/O LCCC
32 I/O LCCC
20 I/O LCCC
2225
1810
20 I/O LCCC
16 I/O LCCC
1210
32 I/O LCCC
R49383
16 I/O LCCC
20 I/O LCCC
1825
68 I/O LCCC
20 I/O LCCC
16 I/O LCCC
0805
Pratt & Whitney
MADE

Figure 1

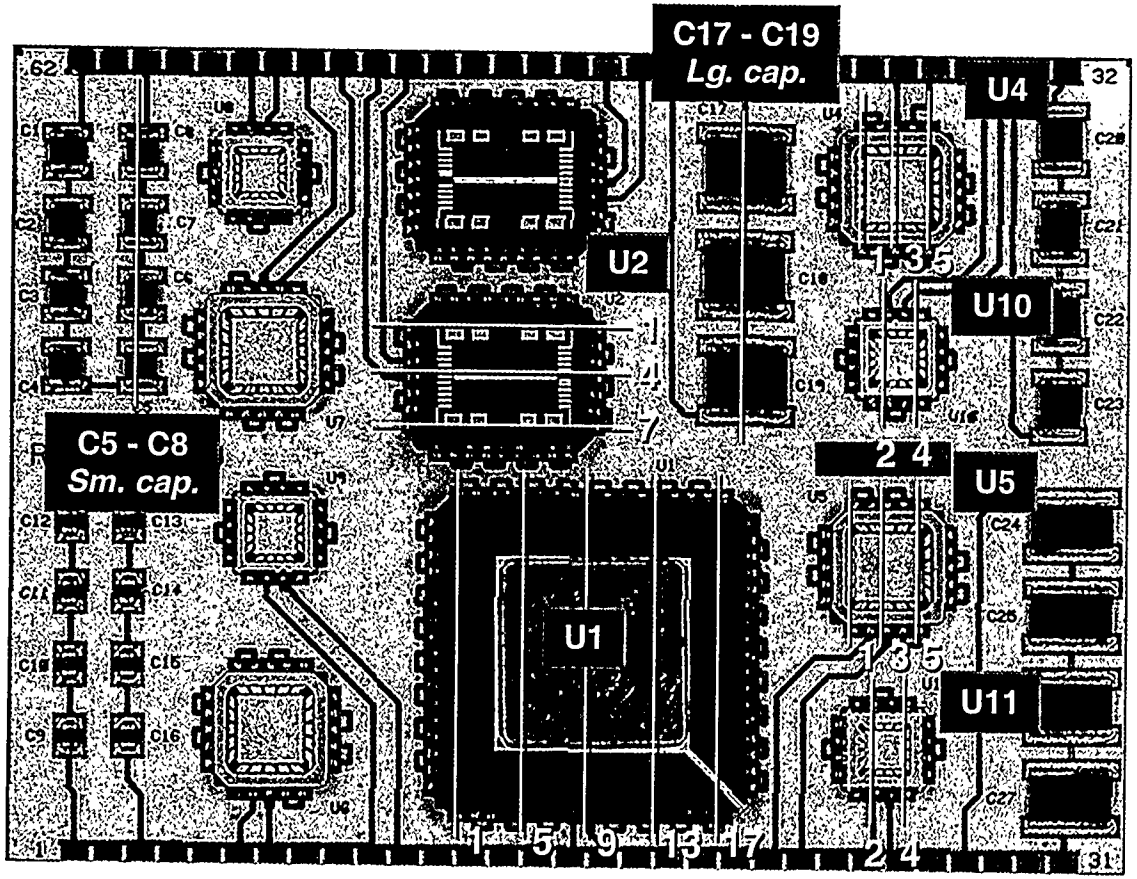


Figure 2

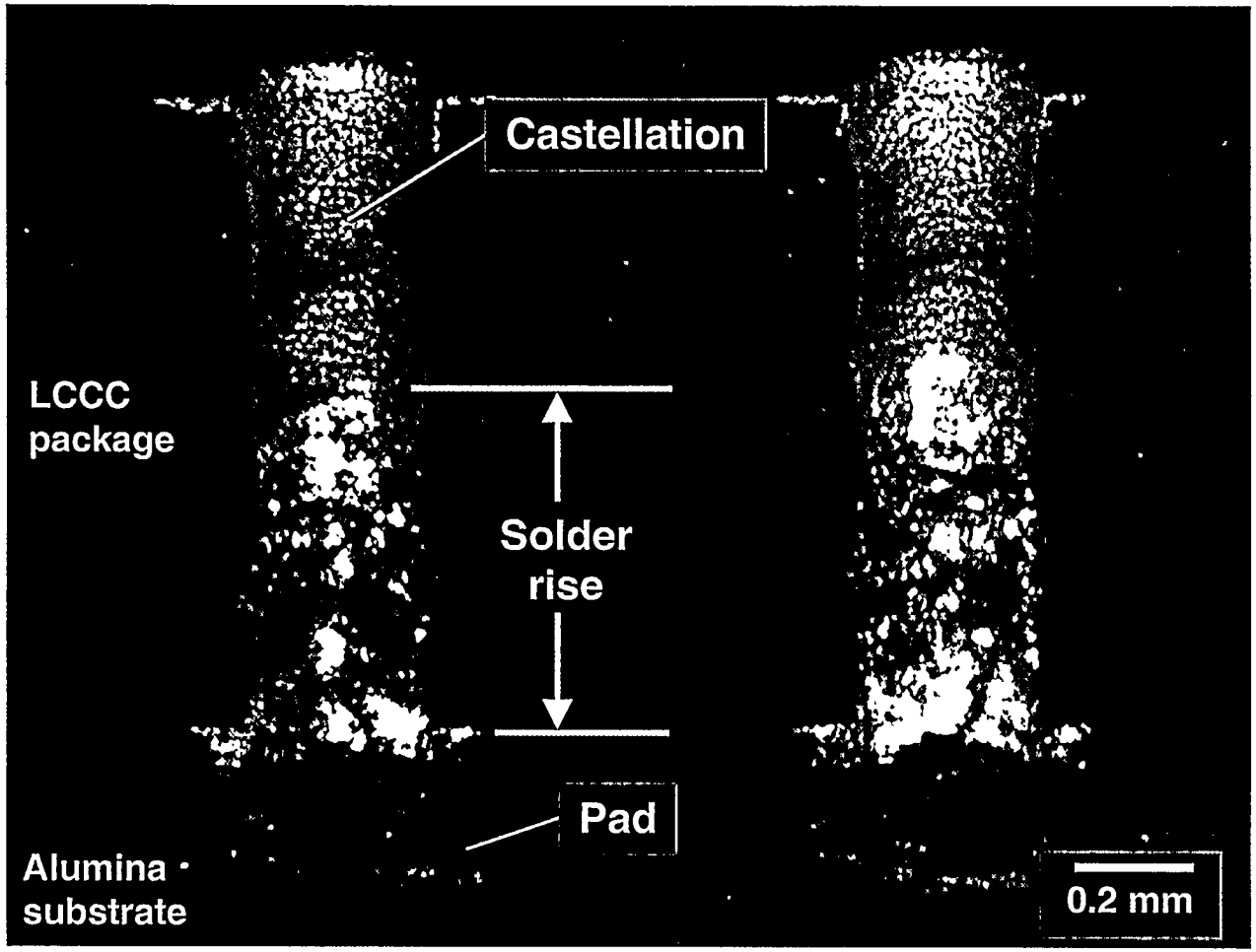

Castellation
LCCC
package
Solder
rise
Pad
Alumina
substrate
0.2 mm

Figure 3a

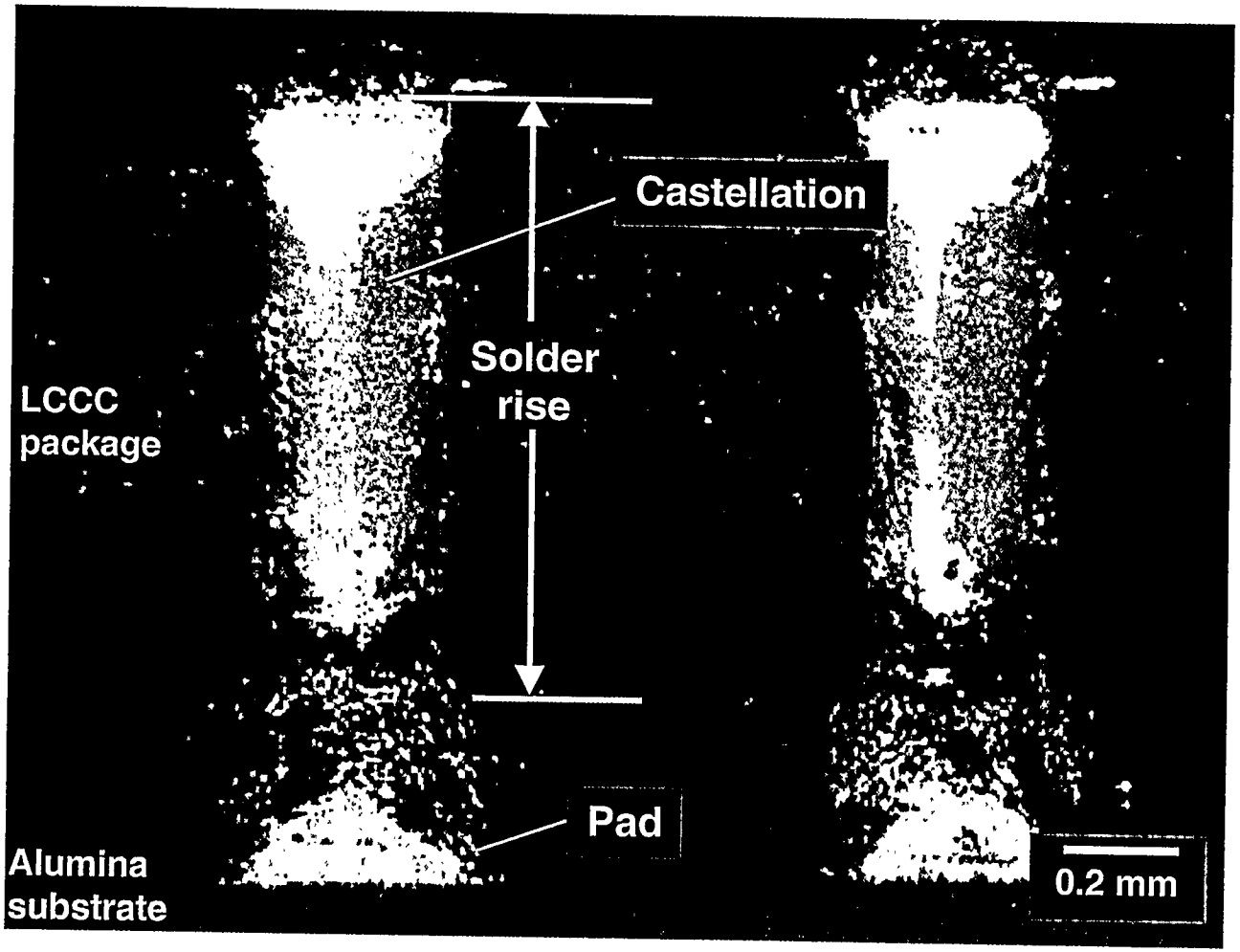

Castellation
Solder rise
LCCC package
Pad
Alumina substrate
0.2 mm

Figure 3b

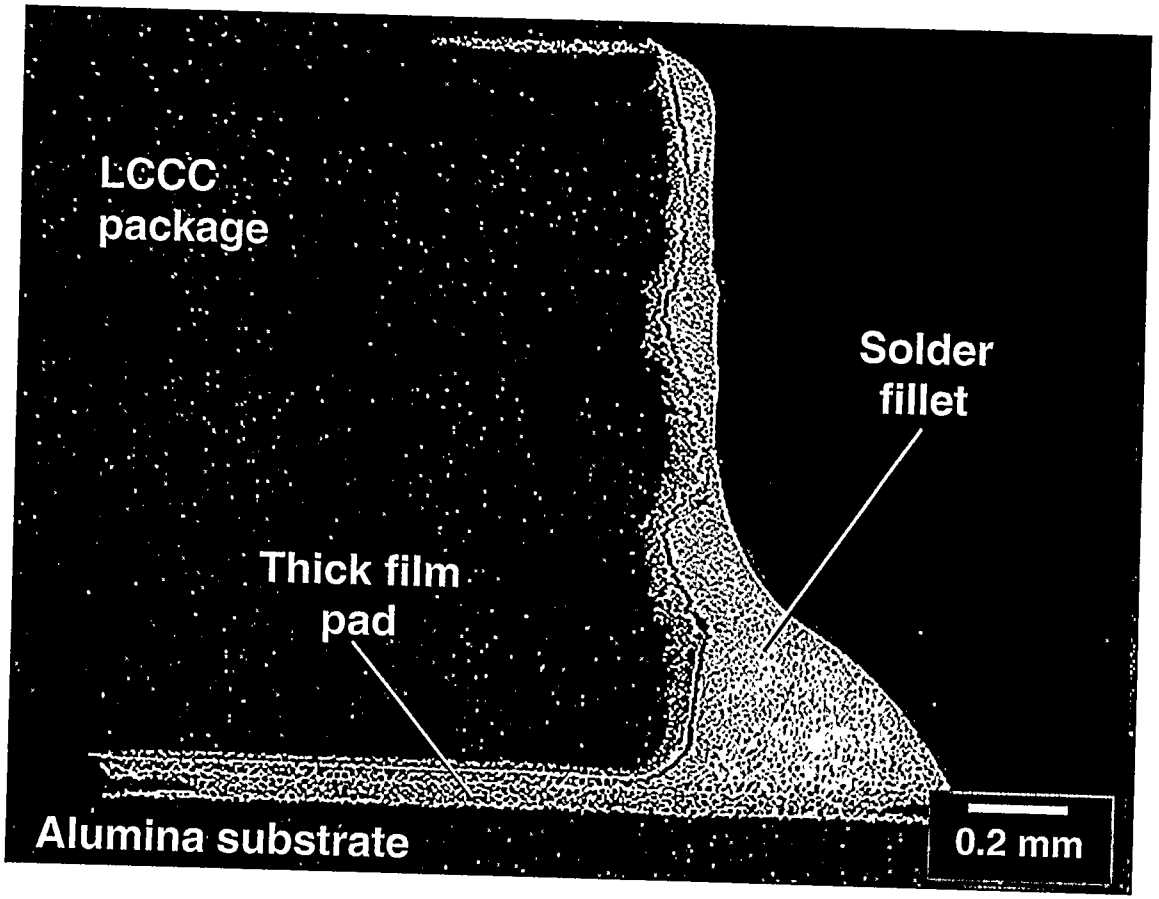

LCCC
package
Solder
fillet
Thick film
pad
Alumina substrate
0.2 mm

Figure 4a

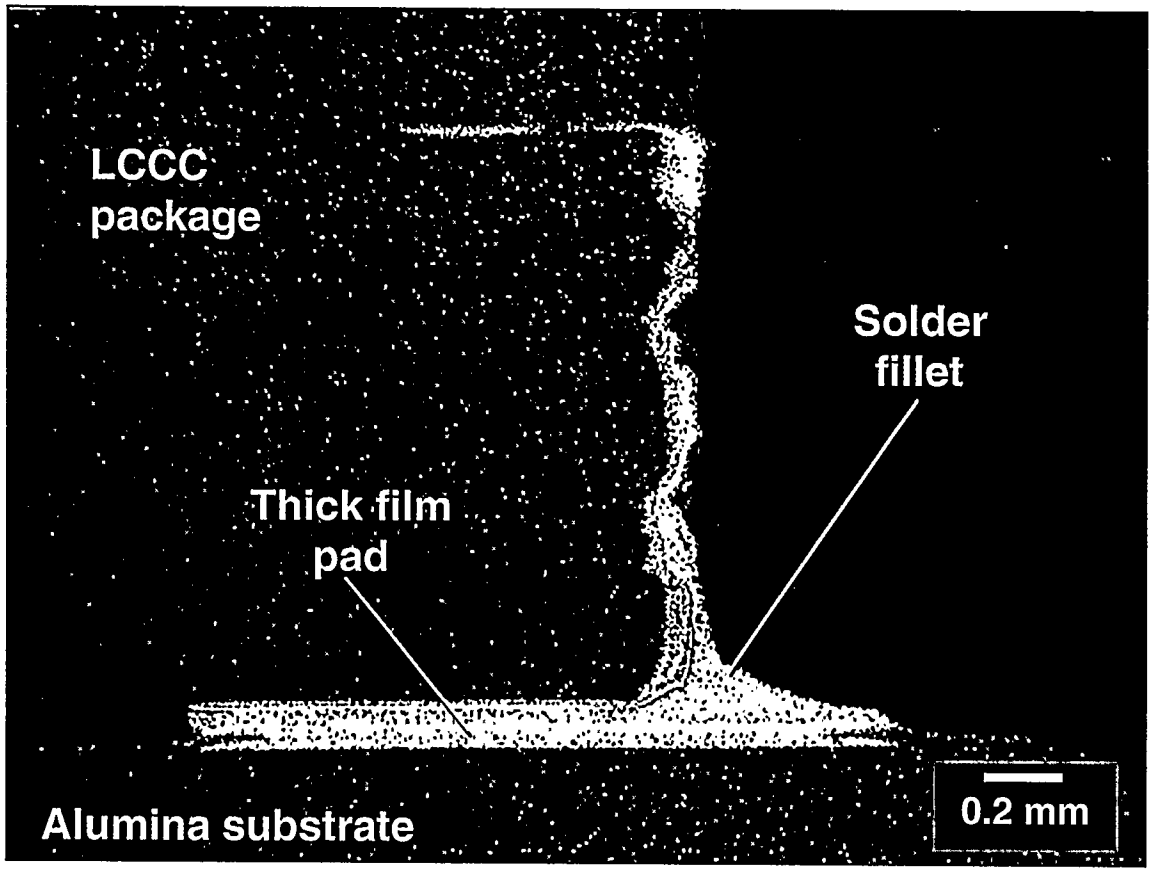

LCCC
package
Solder
fillet
Thick film
pad
Alumina substrate
0.2 mm

Figure 4b

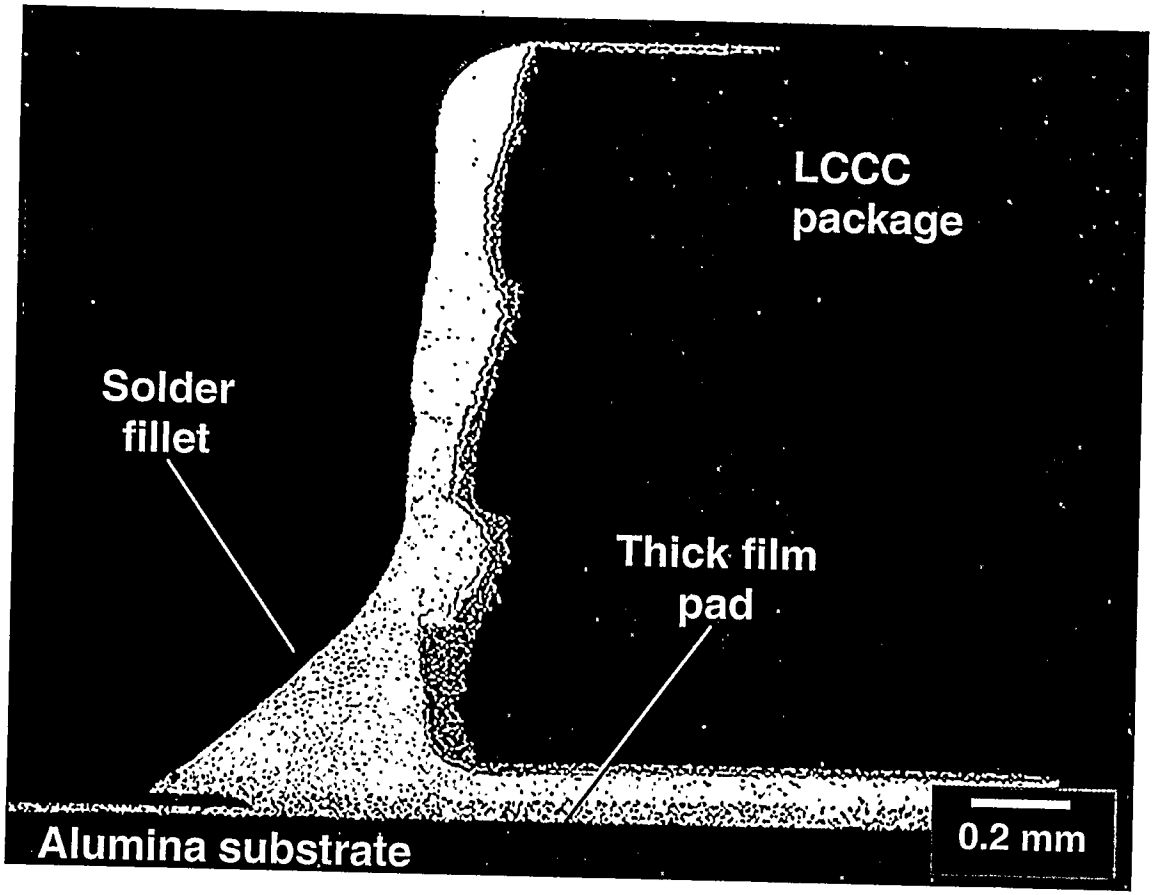

LCCC
package
Solder
fillet
Thick film
pad
Alumina substrate
0.2 mm

Figure 4c

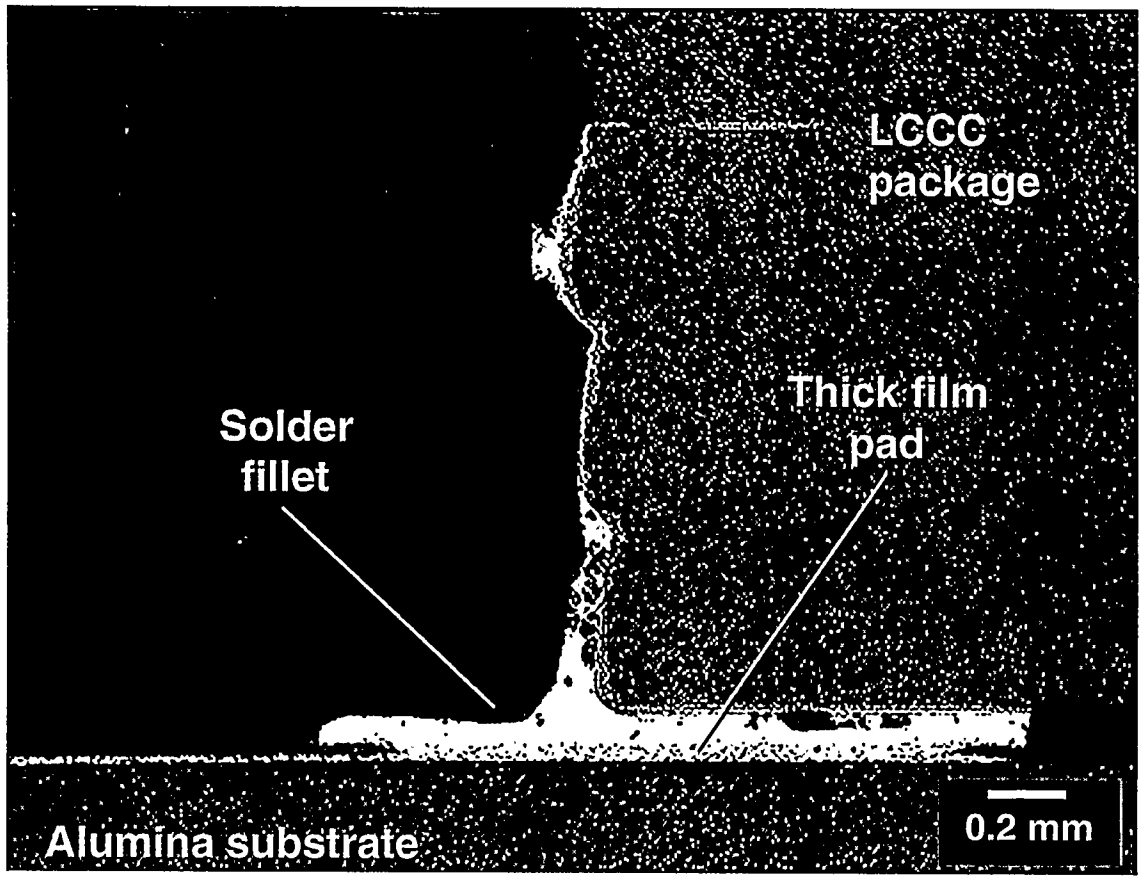

LCCC
package
Thick film
pad
Solder
fillet
Alumina substrate
0.2 mm

Figure 4d

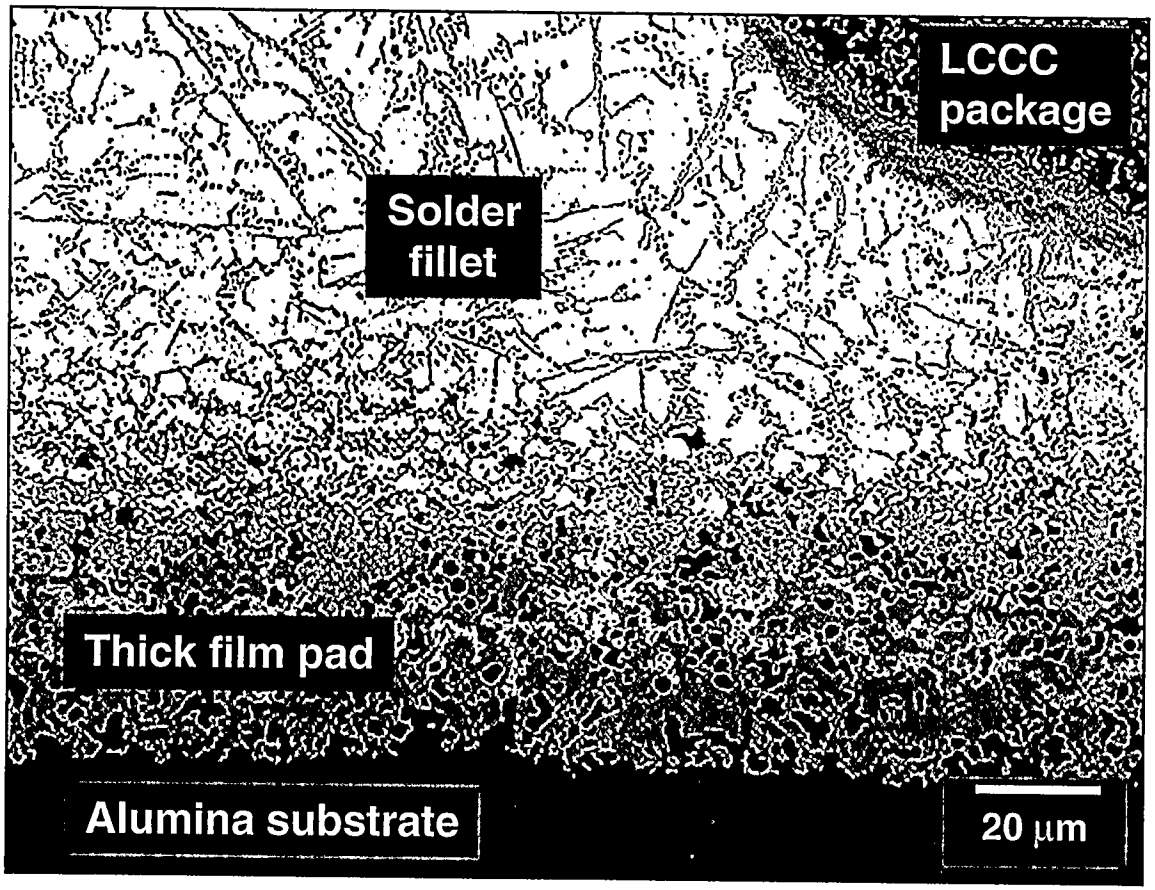

LCCC
package
Solder
fillet
Thick film pad
Alumina substrate
20 μm

Figure 5a

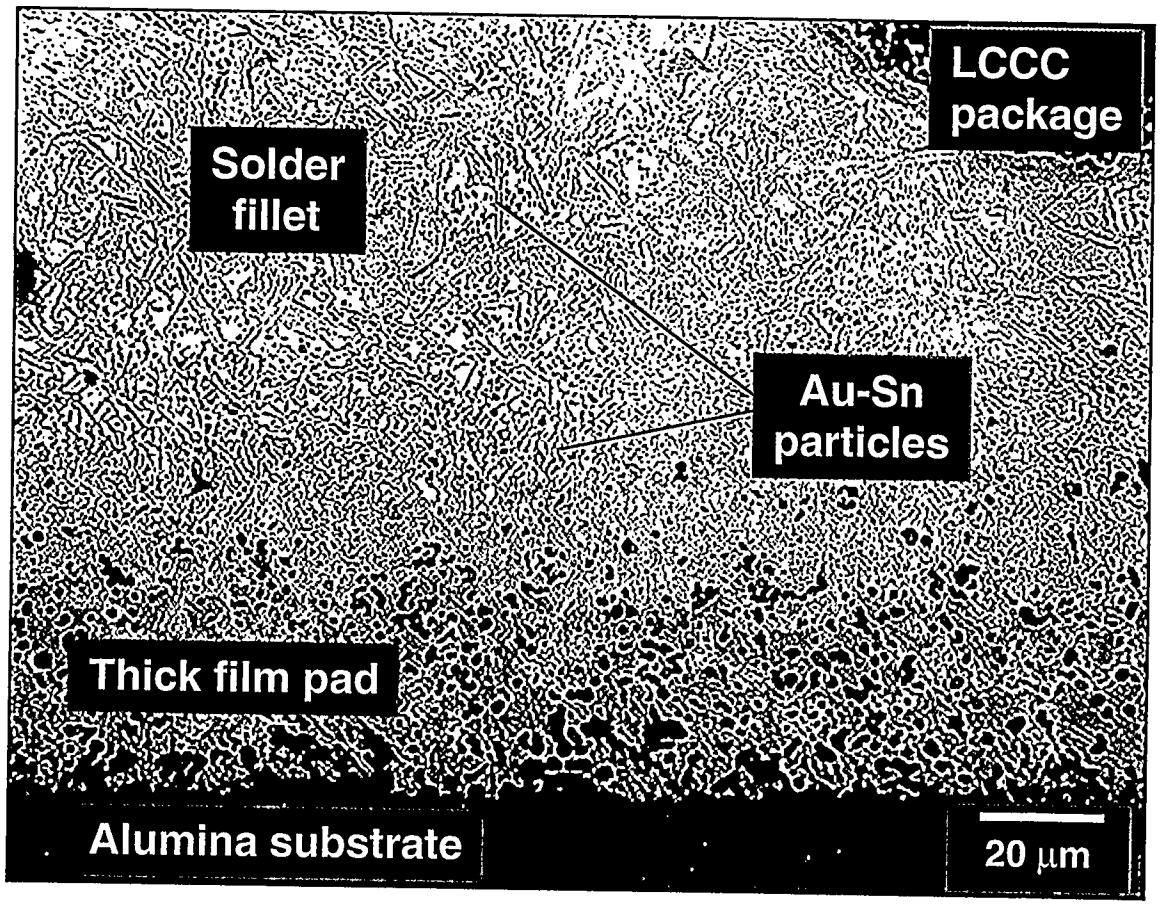

LCCC
package
Solder
fillet
Au-Sn
particles
Thick film pad
Alumina substrate
20 μm

Figure 5b

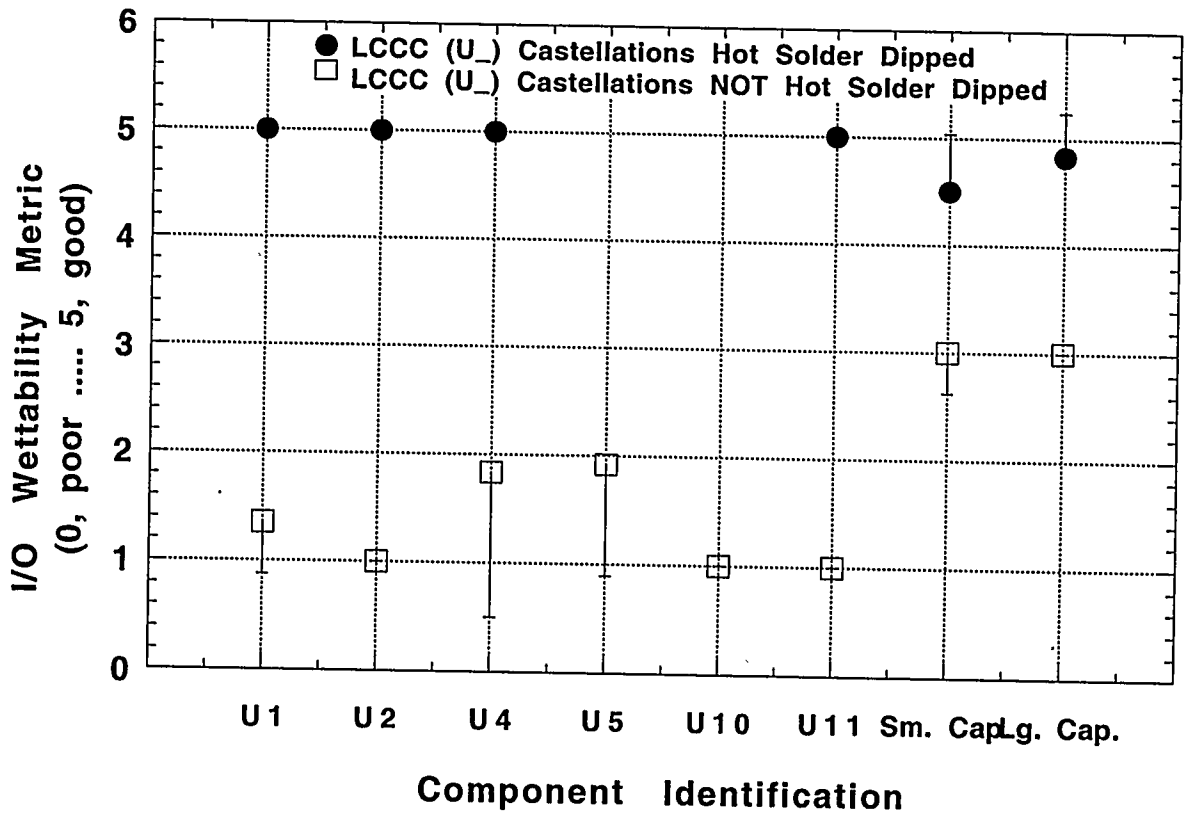

LCCC (U_) Castellations Hot Solder Dipped
LCCC (U_) Castellations NOT Hot Solder Dipped
I/O Wettability Metric
(0, poor ..... 5, good)
0
1
2
3
4
5
6
U1
U2
U4
U5
U10
U11
Sm. Cap
Lg. Cap.
Component Identification

Figure 6a

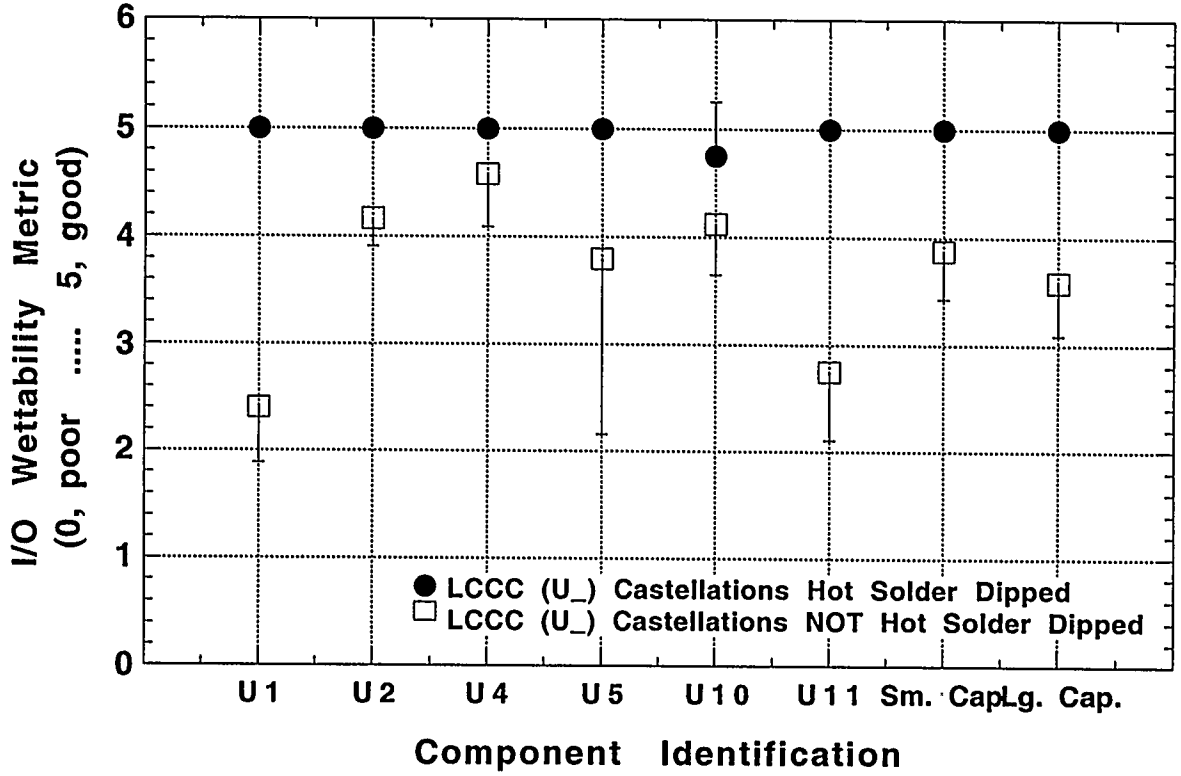

I/O Wettability Metric
(0, poor ..... 5, good)
6
5
4
3
2
1
0
LCCC (U_) Castellations Hot Solder Dipped
LCCC (U_) Castellations NOT Hot Solder Dipped
U1
U2
U4
U5
U10
U11
Sm. Cap
Lg. Cap.
Component Identification

Figure 6b

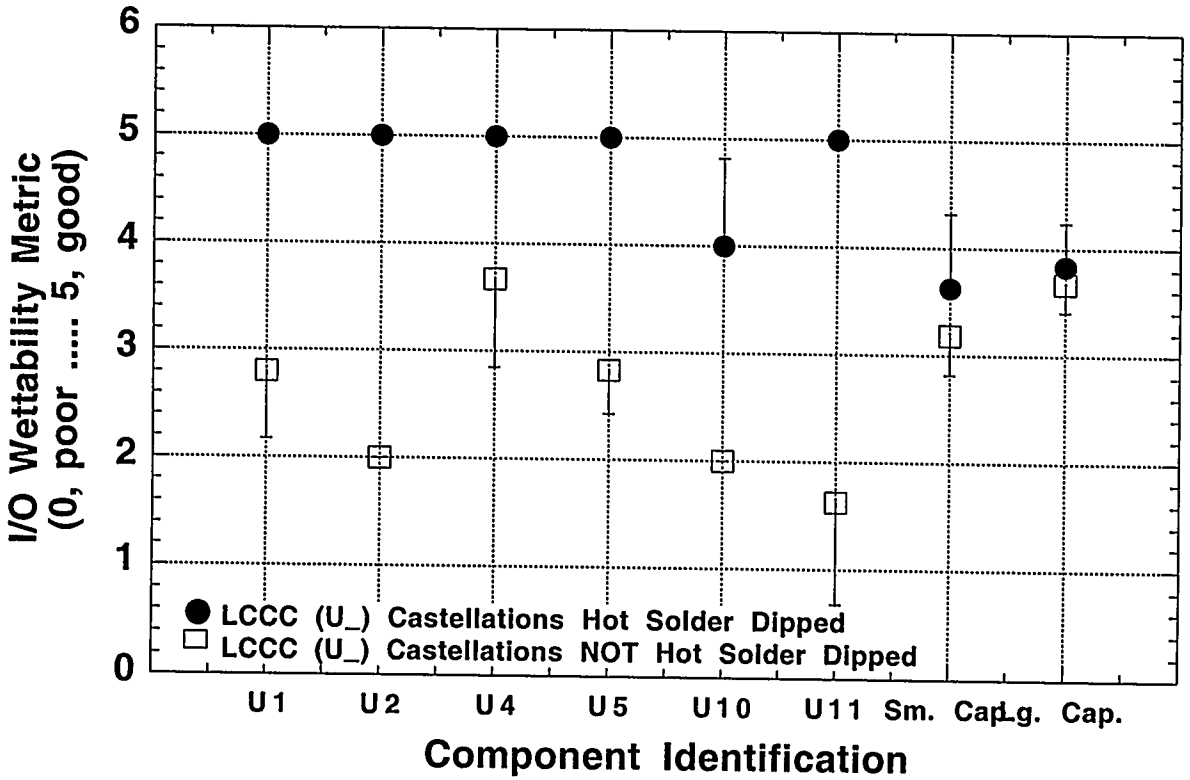

I/O Wettability Metric
(0, poor ..... 5, good)
6
5
4
3
2
1
0
LCCC (U_) Castellations Hot Solder Dipped
LCCC (U_) Castellations NOT Hot Solder Dipped
U1
U2
U4
U5
U10
U11
Sm. Cap.
Lg. Cap.
Component Identification

Figure 6c

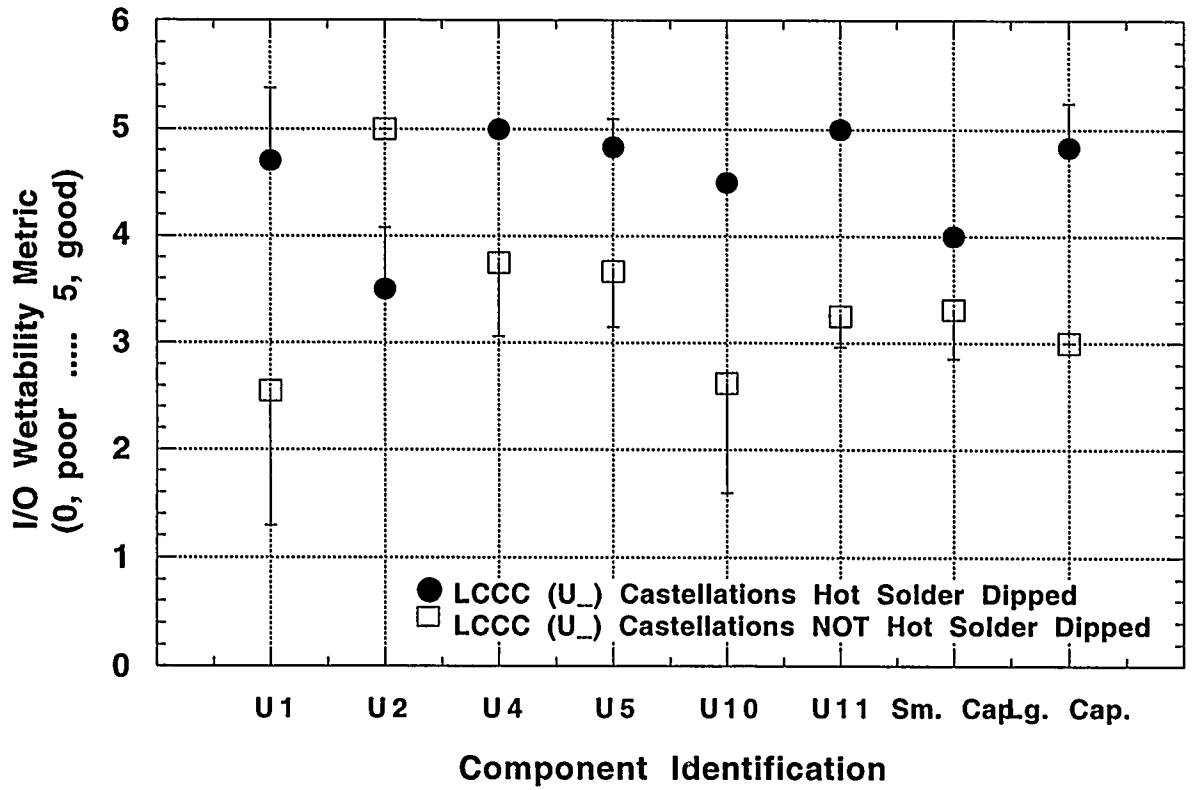
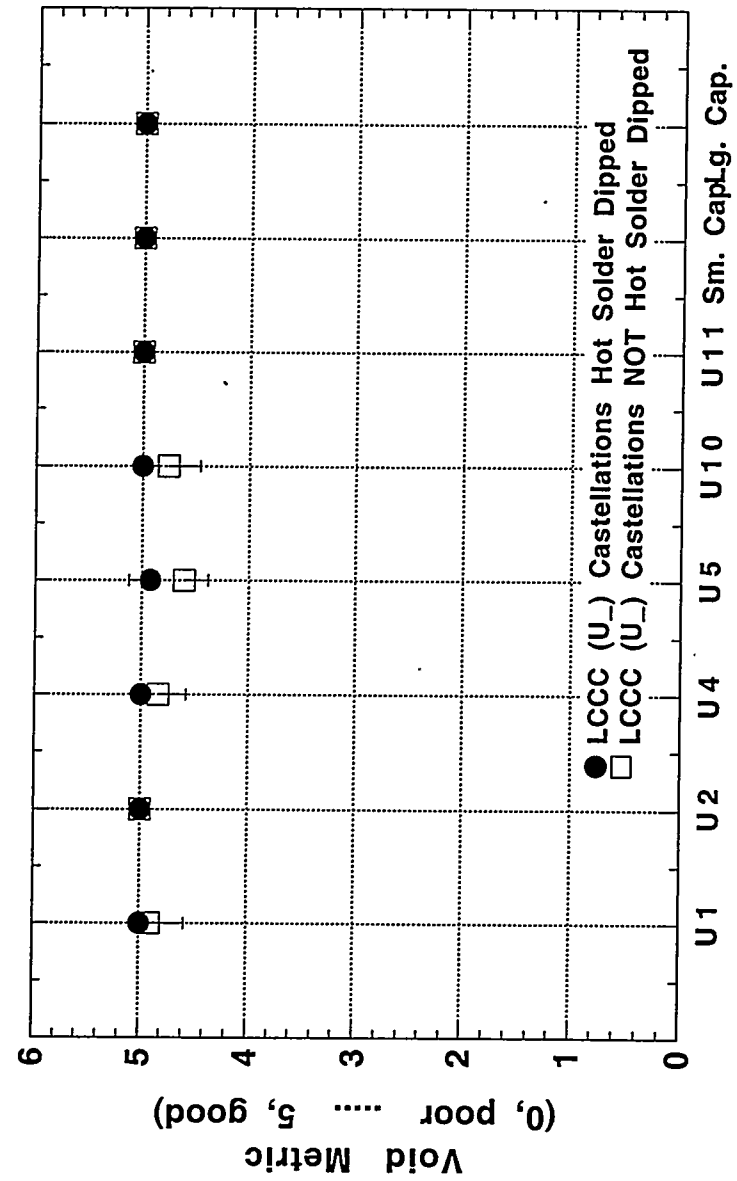

I/O Wettability Metric
(0, poor ..... 5, good)
6
5
4
3
2
1
0
LCCC (U_) Castellations Hot Solder Dipped
LCCC (U_) Castellations NOT Hot Solder Dipped
U1
U2
U4
U5
U10
U11
Sm. Cap.
Lg. Cap.
Component Identification

Figure 6d

Figure 7a


Void Metric
(0, poor ..... 5, good)
0
1
2
3
4
5
6
U1
U2
U4
U5
U10
U11 Sm. Cap
Lg. Cap.
Component Identification
LCCC (U_) Castellations Hot Solder Dipped
LCCC (U_) Castellations NOT Hot Solder Dipped

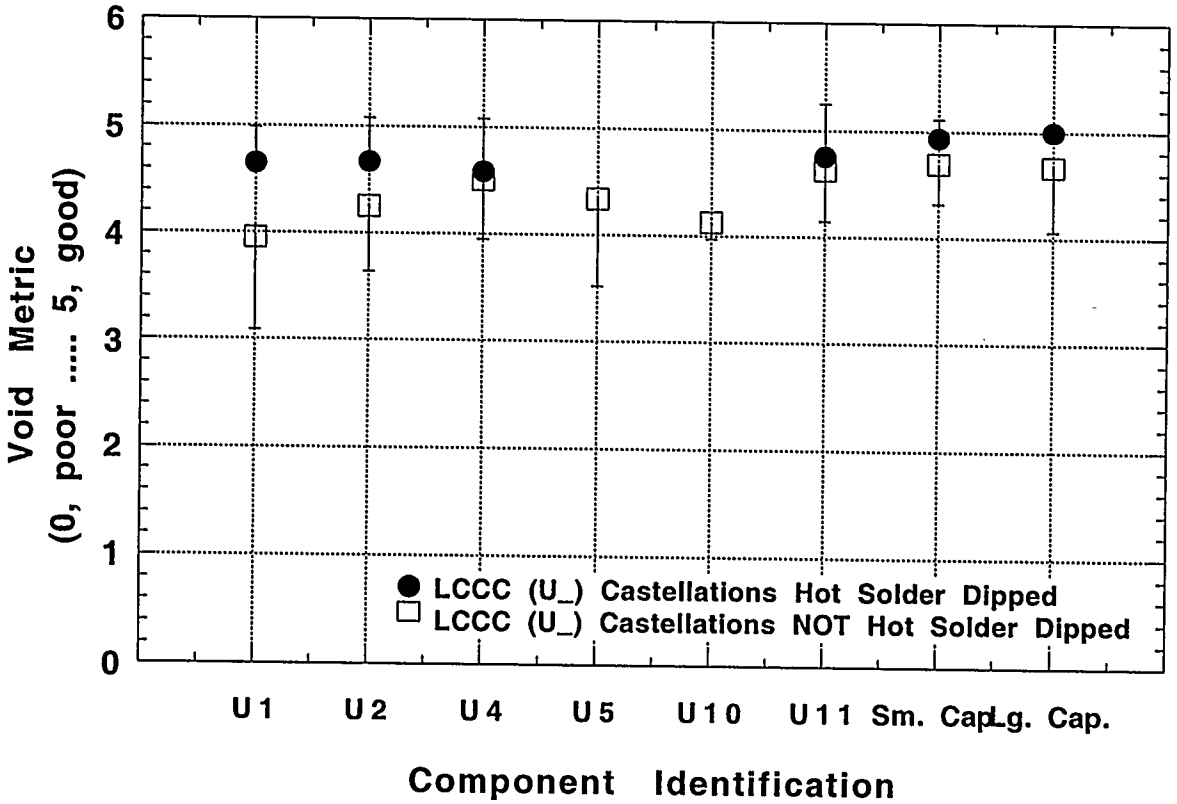

Void Metric
(0, poor ..... 5, good)
6
5
4
3
2
1
0
LCCC (U_) Castellations Hot Solder Dipped
LCCC (U_) Castellations NOT Hot Solder Dipped
U1
U2
U4
U5
U10
U11
Sm. Cap
Lg. Cap.
Component Identification

Figure 7b

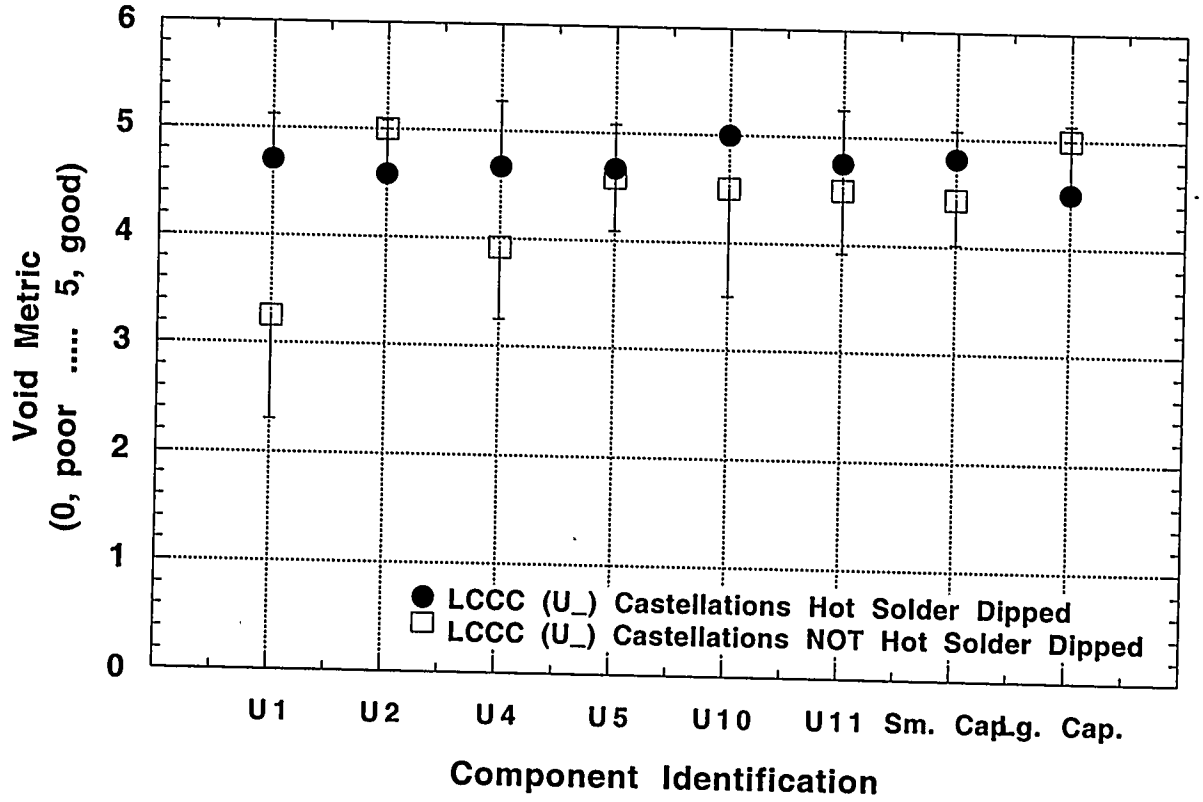

Void Metric
(0, poor ..... 5, good)
6
5
4
3
2
1
0
LCCC (U_) Castellations Hot Solder Dipped
LCCC (U_) Castellations NOT Hot Solder Dipped
U1
U2
U4
U5
U10
U11
Sm. Cap.
Lg. Cap.
Component Identification

Figure 7c

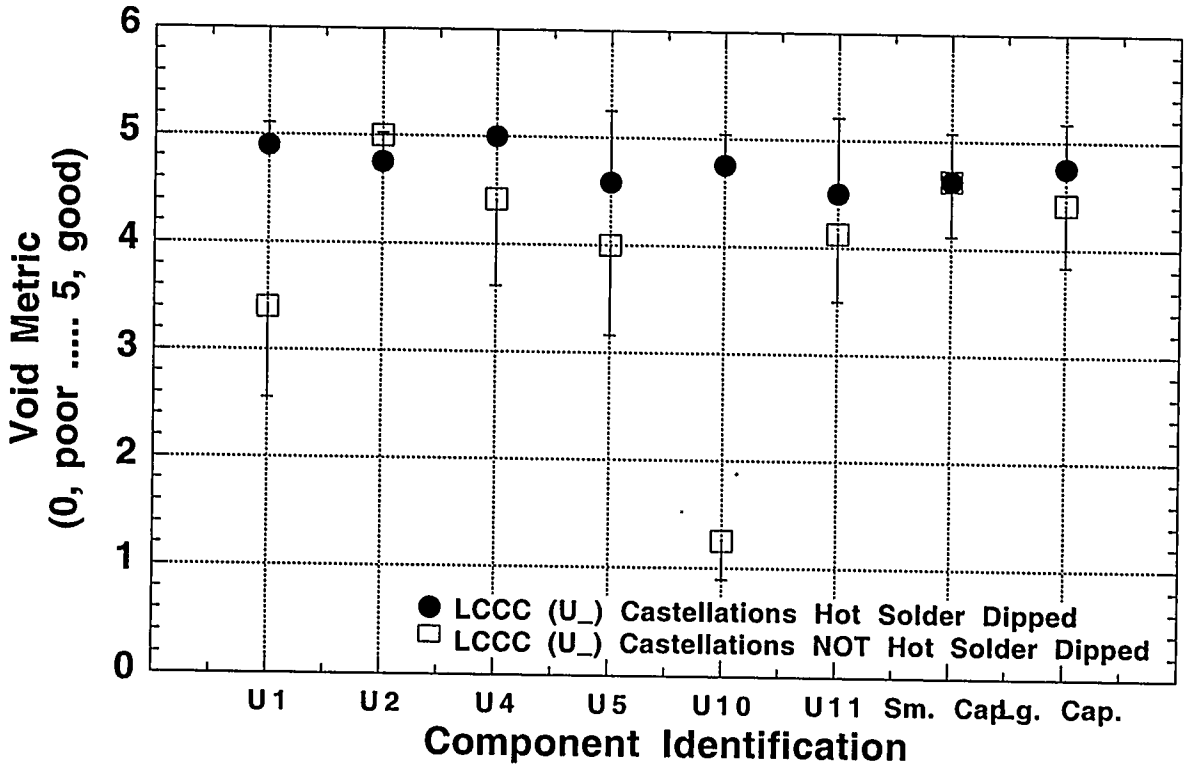

Void Metric
(0, poor ..... 5, good)
6
5
4
3
2
1
0
LCCC (U_) Castellations Hot Solder Dipped
LCCC (U_) Castellations NOT Hot Solder Dipped
U1
U2
U4
U5
U10
U11
Sm. Cap.
Lg. Cap.
Component Identification

Figure 7d

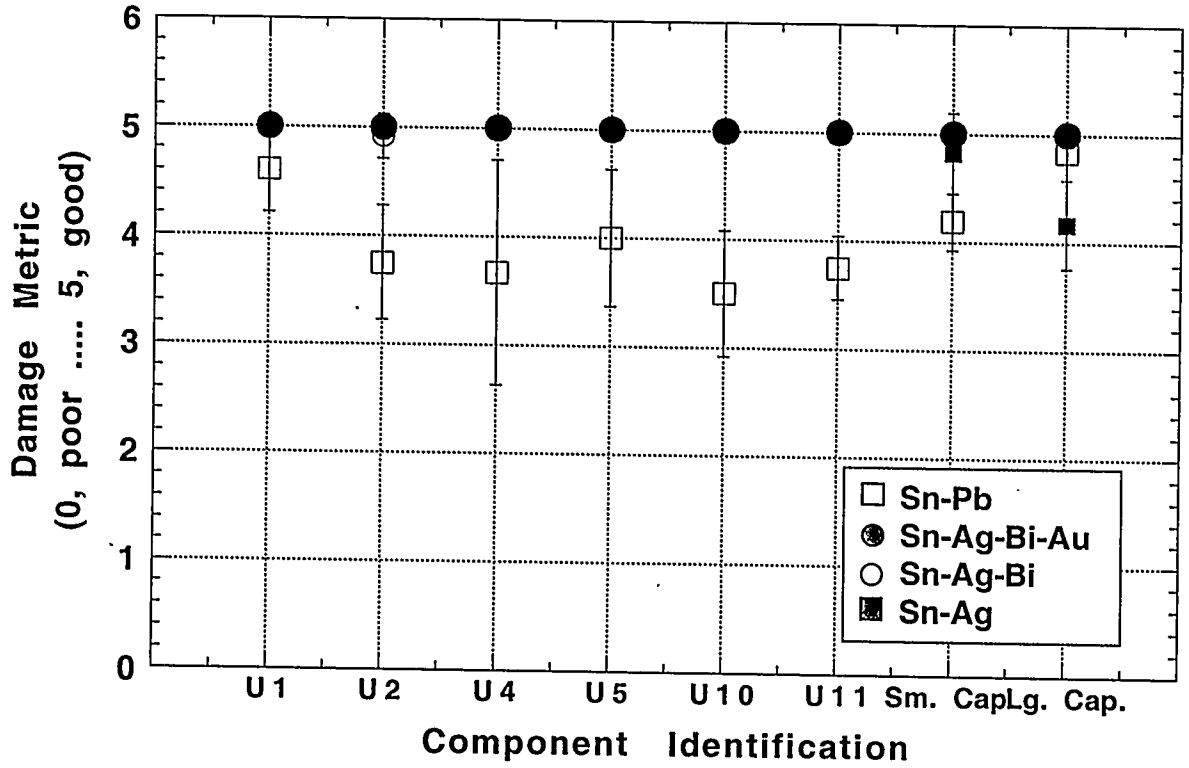

Damage Metric
(0, poor ..... 5, good)
6
5
4
3
2
1
0
U1
U2
U4
U5
U10
U11
Sm. Cap
Lg. Cap.
Component Identification
Sn-Pb
Sn-Ag-Bi-Au
Sn-Ag-Bi
Sn-Ag

Figure 8

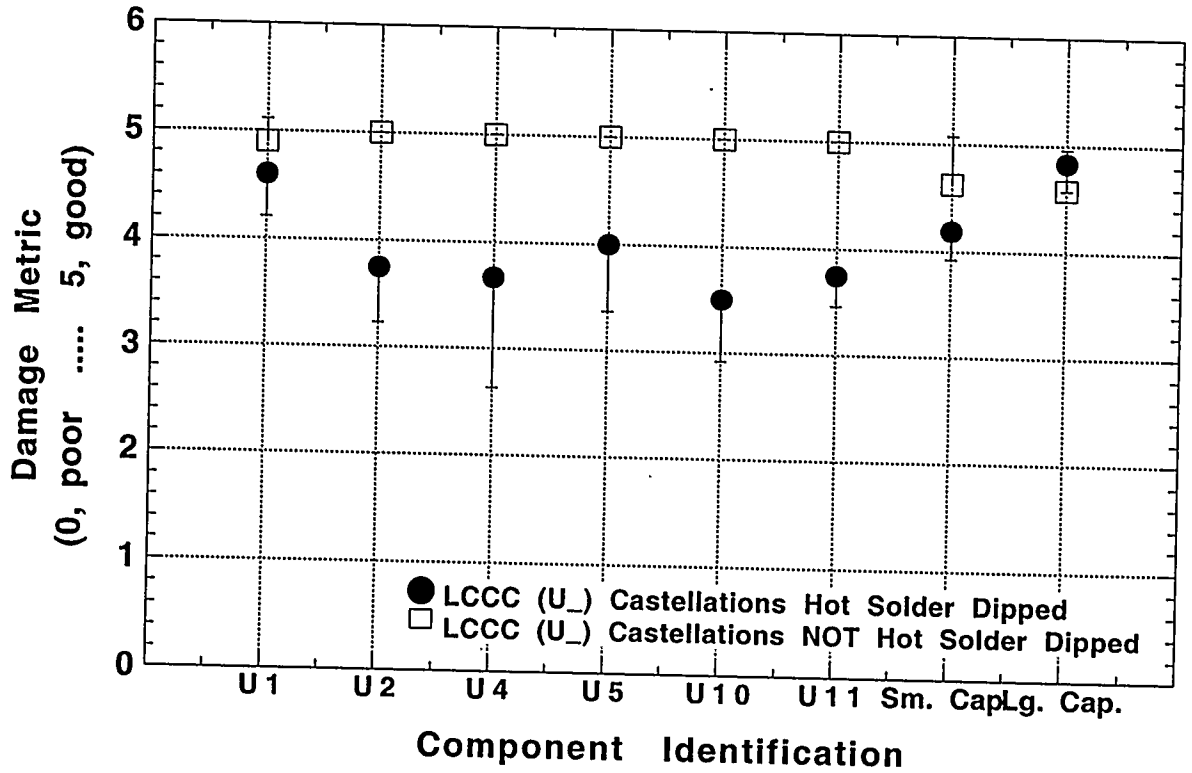

Damage Metric
(0, poor ..... 5, good)
6
5
4
3
2
1
0
LCCC (U_) Castellations Hot Solder Dipped
LCCC (U_) Castellations NOT Hot Solder Dipped
U1
U2
U4
U5
U10
U11
Sm. Cap
Lg. Cap.
Component Identification

Figure 9