EFFECT OF FIRING CONDITIONS ON THICK FILM MICROSTRUCTURE AND SOLDER JOINT STRENGTH FOR LOW-TEMPERATURE, CO-FIRED CERAMIC SUBSTRATES[1]

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ABSTRACT

Low-temperature, co-fired ceramics (LTCC) are the substrate material-of-choice for a growing number of multi-chip module (MCM) applications. Unlike the longer-standing hybrid microcircuit technology based upon alumina substrates, the manufacturability and reliability of thick film solder joints on LTCC substrates have not been widely studied. An investigation was undertaken to fully characterize solder joints on these substrates. A surface mount test vehicle with Daisy chain electrical connections was designed and built with Dupont™ 951 tape. The Dupont™ 4569 thick film ink (Au76-Pt21-Pd3 wt.%) was used to establish the surface conductor pattern. The conductor pattern was fired onto the LTCC substrate in a matrix of processing conditions that included: (1) double versus triple prints, (2) dielectric window versus no window, and (3) three firing temperatures (800°C, 875°C and 950°C). Sn63-Pb37 solder paste with an RMA flux was screen printed onto the circuit boards. The appropriate packages, which included five sizes of chip capacitors and four sizes of leadless ceramic chip carriers, were placed on the circuit boards. The test vehicles were oven reflowed under a N_2 atmosphere. Non-soldered pads were removed from the test vehicles and the porosity of their thick film layers was measured using quantitative image analysis in both the transverse and short transverse directions. A significant dependence on firing temperature was recorded for porosity. The double printed substrates without a dielectric window revealed a thick film porosity of 31.2% at 800°C, 26.2% at 875°C and 20.4% at 950°C. In contrast, the thick film porosity of the triple printed substrates with a dielectric window is 24.1% at 800°C, 23.2% at 875°C and 17.6% at 950°C. These observations were compared with the shear strength of the as-fabricated chip capacitor solder joints to determine the effect of firing conditions on solder joint integrity. The denser films from the higher firing temperatures had correspondingly higher shear strengths. The 0805 chip capacitor had a shear strength of 12.6 ± 1.4 lbs. at 800°C, 13.3 ± 1.9 lbs. at 875°C and 13.6 ± 1.4 lbs. at 950° for the triple printed substrates with a dielectric window. The trend was similar for the larger capacitors; the 1812's exhibiting shear strengths of 20.5 ± 4.8 lbs. at 800°C, 26.2 ± 1.7 lbs. at 875°C and 29.0 ± 0.2 lbs. at 950°C.

INTRODUCTION

Multichip module (MCM) technologies are differentiated from other technologies by their ability to fabricate multilayer interconnection structures that are capable of packaging a higher ratio of silicon area to substrate area than conventional hybrid technologies. A MCM is a package in

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[1] Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed-Martin Company, for the United States Department of Energy, under contract DE-AC04-94AL85000.

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DISCLAIMER

which the silicon area is generally 30 percent or more of the substrate area. Although MCM technologies have some manufacturing limitations, they still have important end uses in the automotive market, consumer, industrial and defense, and telecommunications applications[1]. Demands for more functionality in a smaller space have exceeded the capabilities of hybrid circuits. Therefore, understanding the properties of the materials used to fabricate MCM's can lead to increased packaging density and an ever greater range of applications[2].

Material suppliers continue to improve quality, processability, and reduce costs for low-temperature co-fired ceramic (LTCC) material systems[3]. LTCC ceramics, often referred to as glass/ceramics, are designed to be fired at lower temperatures, in the 850 - 1050°C range. This permits the use of standard thick film materials, such as silver and gold. It also allows the addition of thick film passive components after firing to eliminate the cost of purchasing and mounting passive components[4]. The behavior of interest in the present study is the effect of firing temperature on solderability, porosity and joint strength.

EXPERIMENTAL

The LTCC test vehicle in this evaluation used the Dupont™ 4569 thick film ink with Au76-Pt21-Pd3 (wt.%) metallization. The test vehicle measures 2.60" x 2.60" x 0.042" thick. A completed test vehicle is illustrated below in Fig. 1.

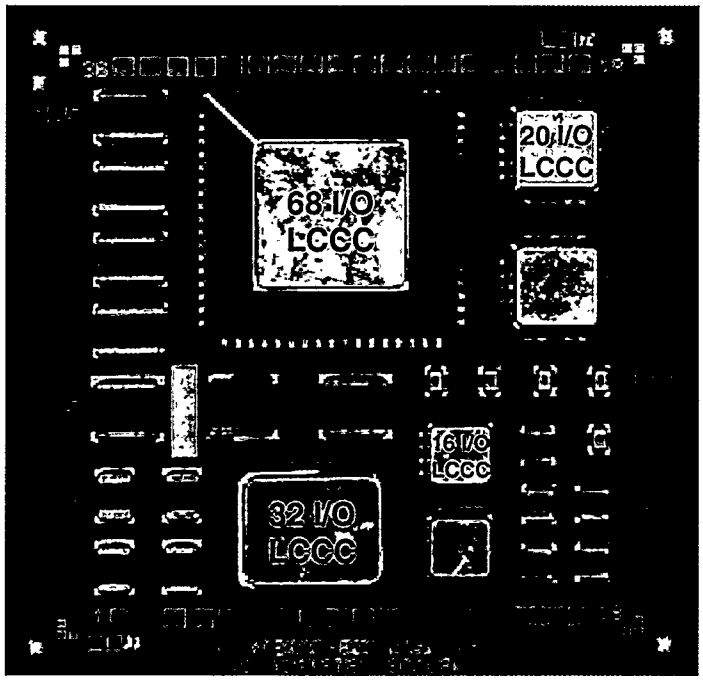


Figure 1. The LTCC test vehicle has 21 chip capacitors and 6 leadless ceramic chip carriers.

The circuit design has a daisy-chained configuration to permit the measurement of electrical continuity during testing. The test components consist of five sizes of dummy chip capacitors (0805, 1210, 1812, 1825 and 2225). The chip capacitors used in this study have 100% Sn terminations. There are also four sizes of leadless ceramic chip carriers (LCCC's). The LCCC's have Au castellations with 16, 20, 32 or 68 input/outputs (I/O's) and a 50 mil pitch.

The reflow soldering operation used to populate the test vehicles involves screen printing the solder paste on to the unpopulated test substrate with a 0.008" thick stencil. Sn63-Pb37 solder paste with an RMA flux was screen printed onto the circuit boards. The components were then placed on the paste. The test vehicles were processed through a five zone IR convective reflow furnace. The part moves across the heat zones at a line speed of 15 in./min. The peak topside temperature of this board was 221°C and the time above the solder melting temperature (183°C) was 1 min. 10 sec. to assure adequate solder reflow.

RESULTS AND DISCUSSION

An initial assessment of the solderability was to evaluate, by image analysis, the percent of the thick film pads that had been wetted by the SnPb solder for each of the processing conditions. Those conditions included three firing temperatures (800, 875 and 950°C), double or triple printing and with or without a dielectric window (DW). The presence of the dielectric window required additional high temperature firing steps. Some of the additional processing steps had a marked effect on how much of the thick film pad was wetted by the solder. Shown below in Fig. 2 are optical images of how processing conditions affect solderability. The thick film pad that was wetted by the solder remained at 100% with and without the dielectric window at 800°C, but decreased slightly from 100% to 96.2% at 875°C and decreased even more from 94.1 to 66.3% at 950°C.

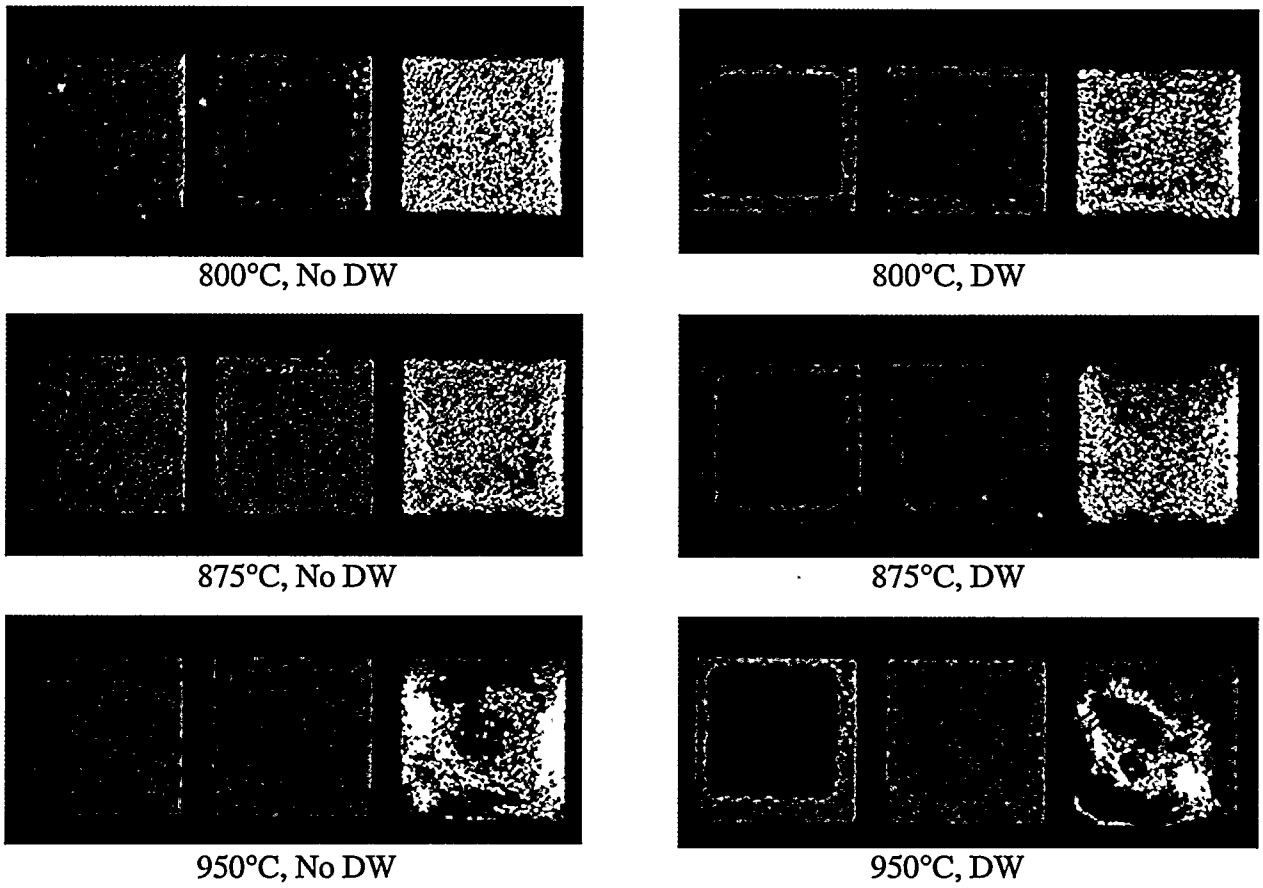
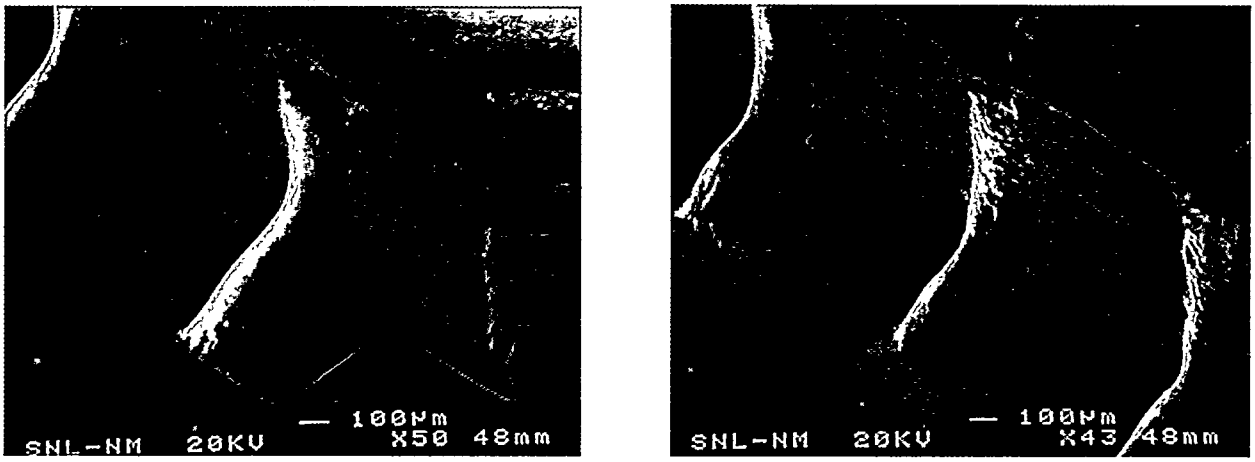


Fig. 2. Optical images of thick film pads illustrating the difference in solderability for the double printed substrates at varying temperatures with and without a dielectric window.

Similar results were noted on the LCCC joint pads. Shown below in Fig. 3a-b is a SEM image of a solder joint on a 20 I/O LCCC fired at (a) 875°C and (b) 950°C without the dielectric window. Note the difference in the joint smoothness, the shape of the solder fillet and the dewetting of the solder pad on the substrate fired at 950°C.



(a) (b)

Figure 3. SEM/backscattered image of solder fillet on substrate fired at (a) 875°C and (b) 950°C without a dielectric window.

Quantitative image analysis was used to assess the porosity of the thick film layers from the test vehicle for each of the above mentioned processing conditions. The thick film pads were metallographically cross-sectioned, mounted and polished. Two edge and two center photos for each of five pads on each board were analyzed. Fig. 4a-f illustrates the SEM/backscattered images of the thick film double and triple printed substrates with the dielectric frame. Note the difference in the microstructure for each of the processing temperatures. The films appear to become denser at higher firing temperatures.

Table 1 illustrates the differences in the thick film porosity for the double and triple printed boards with and without a dielectric window. The porosity of the thick film on the double printed substrates without a dielectric window is 31.2% at 800°C, 26.2% at 875°C and 20.1% at 950°C. In contrast, the porosity of the triple printed substrates, also without the dielectric window, is 26.0% at 800°C, 24.3% at 875°C and 15.0% at 950°C. These data show that the thick film increased in density as the firing temperature was increased. The trend in porosity was not monotonic when the dielectric was added to the process sequence although the general behavior also suggests that a higher firing temperature decreased film porosity.

Mechanical testing was also performed on the chip capacitor solder joints. The boards were laser sectioned without damage to any joints. The board segments were introduced into a load frame with a ram attached to the cross head member of the load frame. At a crosshead speed of 10 mm/min., the ram was used to push the component from the board. The maximum recorded load, plus or minus one standard deviation, was used to designate the strength of the joint. In most cases, the joint strength increased with increased firing temperatures. The 0805 chip capacitors triple printed with a dielectric window had a joint strength of 12.6 ± 0.9 at 800°C, 13.3 ± 1.9 at 875°C and 13.6 ± 1.4 lbs. at 950°C. In contrast, the 0805 chip capacitors triple

printed without a dielectric window had joint strengths of 13.4 ± 1.8 at 800°C, 13.1 ± 0.9 at 875°C and 15.3 ± 0.5 lbs. at 950°C. Similarly, the 1210 capacitors triple printed with a dielectric window have joint strengths of 30.3 ± 2.8 at 800°C, 33.1 ± 3.1 at 875°C and 34.5 ± 5.8 lbs. at 950°C; while those printed without a dielectric window have joint strengths of 35.3 ± 1.9 at 800°C, 37.1 ± 3.7 at 875°C and 37.6 ± 6.2 lbs. at 950°C. The mechanical test data for each of the chip capacitor sizes with the various processing conditions is shown in Fig. 5.

CONCLUSIONS

Quantitative image analysis has been evaluated on prototype surface mount LTCC circuit boards. The overall porosity of the films was reduced after the 800 and 875°C firings when the dielectric was present than in those samples without the dielectric. The difference was less significant after the 950°C firing step between the two cases. This trend indicates that the heat input resulting from the additional firing step required by the dielectric window had the anticipated effect of further densifying the thick film.

ACKNOWLEDGMENTS

The authors would like to acknowledge the efforts of James Gonzales for the screen printing of the solder pastes; Charlie Carter and Alice Kilgo for metallographic sample preparation and Barry Ritchie for his scanning electron microscopy efforts. Ed Lopez reviewed the manuscript.

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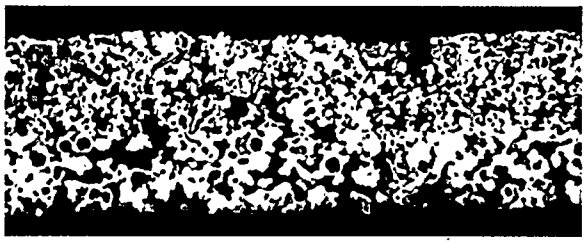
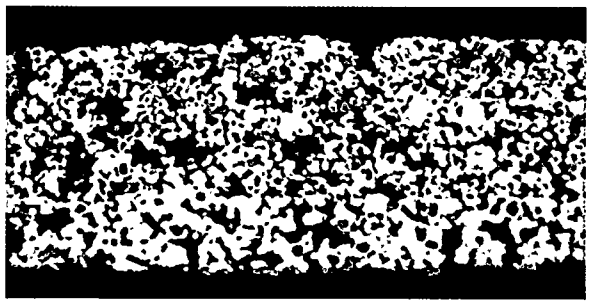
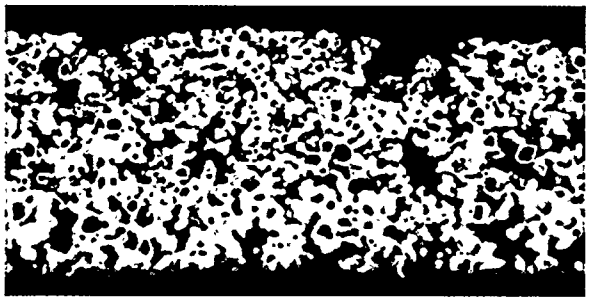


(a) 800°C, 2X, DW



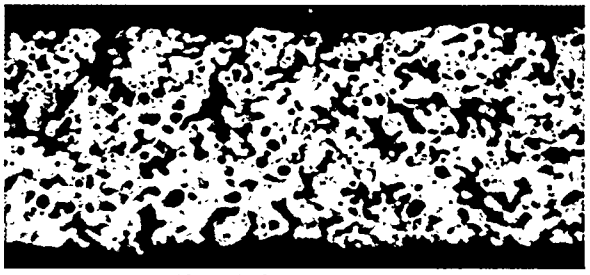
(d) 800°C, 3X, DW

(b) 875°C, 2X, DW



(e) 875°C, 3X, DW

(c) 950°C, 2X, DW



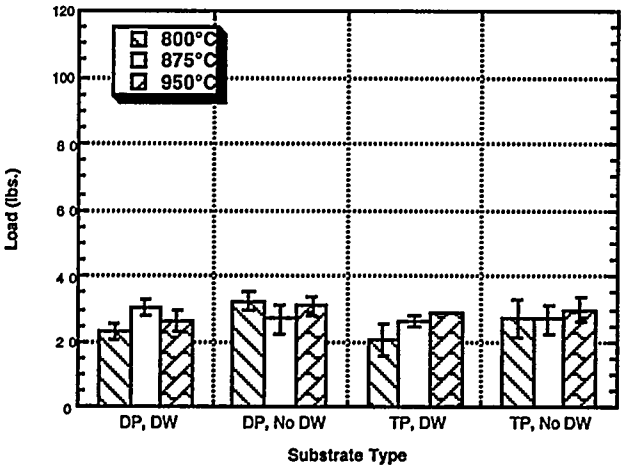
(f) 950°C, 3X, DW

Figure 4. SEM/backscattered cross-section images of the thick film double and triple printed substrates with a dielectric window.

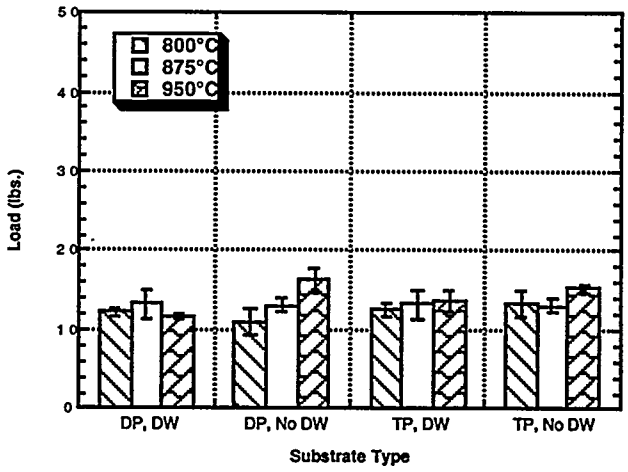
Table 1. Thick Film Porosity for LTCC Boards with and without the Dielectric Window

	Double Printed							
	No Dielectric Window				Dielectric Window			
Firing Temp (°C)	Mean Area	Variance x # of particles	Maximum Area	% Porosity	Mean Area	Variance x # of particles	Maximum Area	% Porosity
800	7.03 E-06	8.56 E-07	3.13 E-04	31.16	6.81 E-06	8.00 E-07	2.59 E-04	26.78
875	9.17 E-06	9.73 E-07	4.83 E-04	26.23	8.13 E-06	7.81 E-07	3.27 E-04	19.66
950	1.07 E-05	5.52 E-.7	3.61 E-04	20.36	7.12 E-06	9.70 E-07	3.13 E-04	23.24

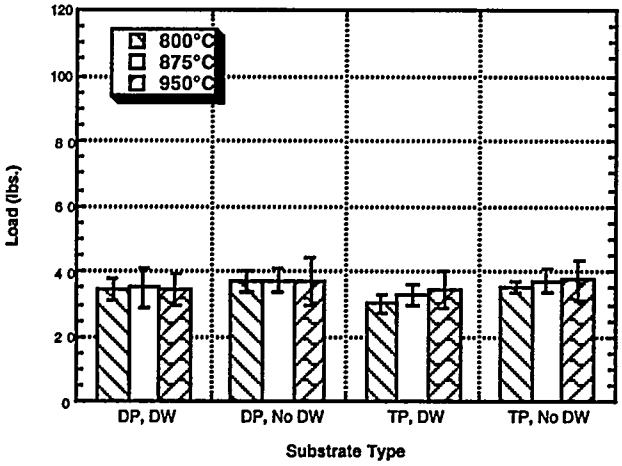
	Triple Printed							
	No Dielectric Window				Dielectric Window			
800	6.06 E-06	6.72 E-07	2.33 E-04	26.02	6.57 E-06	7.67 E-07	2.71 E-04	24.14
875	9.53 E-06	6.86 E-07	2.32 E-04	24.31	9.50 E-06	1.28 E-07	4.55 E-04	23.22
950	6.98 E-06	5.15 E-07	2.99 E-04	14.96	6.62 E-06	8.36 E-07	2.30 E-04	17.64



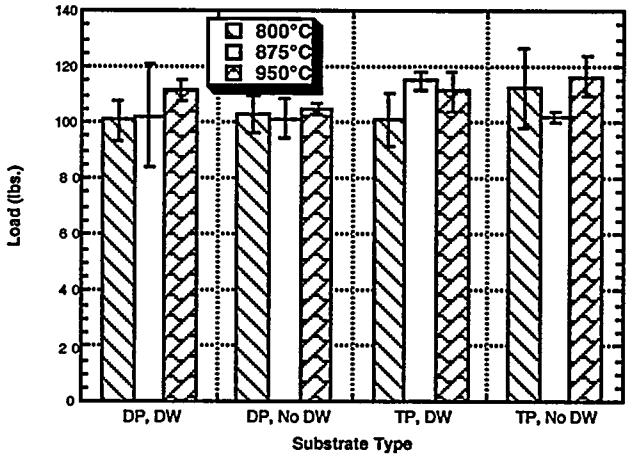
(a) 0805 CC's



(c) 1812 CC's



(b) 1210 CC's



(d) 1825 CC's

Figure 5. Mechanical test data for four types of chip capacitors.