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ENGINEERING CHANGE NOTICE

Page 1 of 21. ECN **613433**Proj.
ECN

2. ECN Category (mark one) Supplemental ☐ Direct Revision ☒ Change ECN ☐ Temporary ☐ Standby ☐ Supersedure ☐ Cancel/Void ☐	3. Originator's Name, Organization, MSIN, and Telephone No. MC TEATS, WTSE, R1-43, 3-4655	3a. USQ Required? ☐ Yes ☒ No	4. Date 5-22-95
	5. Project Title/No./Work Order No. PLC SOFTWARE DOCUMENTATION	6. Bldg./Sys./Fac. No. 242-A/LERF	7. Approval Designator NA
	8. Document Numbers Changed by this ECN (includes sheet no. and rev.) WHC-SD-W105-SWD-001, REV. 0	9. Related ECN No(s). NA	10. Related PO No. NA
11a. Modification Work ☐ Yes (fill out Blk. 11b) ☒ No (NA Blks. 11b, 11c, 11d)	11b. Work Package No. NA	11c. Modification Work Complete NA _____ Cog. Engineer Signature & Date	11d. Restored to Original Condition (Temp. or Standby ECN only) NA _____ Cog. Engineer Signature & Date
12. Description of Change Revise software description document and change title of document. Descriptions reflect replacement of ESTeem with Motorola modems, and C-018 signal termination changes on the LERF PLC.			
13a. Justification (mark one) Criteria Change ☒ Design Improvement ☐ Environmental ☐ Facility Deactivation ☐ As-Found ☐ Facilitate Const ☐ Const. Error/Omission ☐ Design Error/Omission ☐			
13b. Justification Details Project construction for C-018 modified some 242-A Plant equipment. Software was changed to reflect the hardware changes. This ECN modifies the software description document.			
14. Distribution (include name, MSIN, and no. of copies) JF BERGER, R1-43, 1 DS HARING, R1-43, 1 JE GEARY, S5-07, 1 RJ NICKLAS, R1-43, 1 RM PERSIN, R1-43, 1 MC TEATS, R1-43, 1 OSTI, L8-07 2 RECEIVED JUN 19 1995 OSTI RELEASE STAND OFFICIAL RELEASE BY WHC DATE MAY 23 1995 <i>Sta. 4</i>			

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ENGINEERING CHANGE NOTICE						Page 2 of 2		1. ECN (use no. from pg. 1) 613433	
15. Design Verification Required ☒ [X] Yes ☐ [] No		16. Cost Impact ENGINEERING CONSTRUCTION Additional [NA] \$0 Additional [NA] \$0 Savings [NA] \$0 Savings [NA] \$0				17. Schedule Impact (days) Improvement [NA] Delay [NA]			
18. Change Impact Review: Indicate the related documents (other than the engineering documents identified on Side 1) that will be affected by the change described in Block 12. Enter the affected document number in Block 19.									
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Document Number/Revision			Document Number/Revision			Document Number Revision			
20. Approvals									
Signature		Date	Signature		Date				
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Document Number: WHC-SD-W105-SWD-001, Rev. 1

Document Title: 242-A/LERF PROGRAMMABLE LOGIC CONTROLLER LADDER LOGIC

Release Date: 5/23/95

**This document was reviewed following the
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SUPPORTING DOCUMENT

1. Total Pages

5/23/95
4445

2. Title

242-A/LERF PROGRAMMABLE LOGIC CONTROLLER LADDER LOGIC

3. Number

WHC-SD-W105-SWD-001

4. Rev No.

1

5. Key Words

242-A EVAPORATOR, LERF, PLC, LADDER LOGIC

6. Author

Name: MC TEATS

M.C. Teats 5/22/95
Signature

Organization/Charge Code 77310/N1179

7. Abstract

PLCs and modems were installed in the 242-A Evaporator by Project W-105 (LERF) to transmit 6 analog liquid level signals, 6 range alarms based on the analog signals, and 6 leak detection and pump status signals to the 242-A Distributive Control System (DCS) from LERF. Communications between the two facilities are also monitored and alarm on the DCS. Following the Project W-105 completion, the communications and signal mix were modified by Project C-018H (ETF). The current PLC software (including ladder logic and data tables), PLC hardware settings, and modem option settings to transmit the signals and monitor communications are documented and described in this document.

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1.0 INTRODUCTION

1.1 PURPOSE

This document defines and describes the user-generated application software written to transmit digital and analog signals from the Liquid Effluent Retention Facility (LERF) to the 242-A Evaporator Distributed Control System (DCS).

1.2 SCOPE

This document applies to the programming for two Allen-Bradley (A-B) Programmable Logic Controller (PLC) 5/10s and the custom option settings for two Motorola V.3225 modems. The A-B and Motorola equipment is used to fetch 6 analog and 12 digital signals generated at the LERF facility and transmit them to the 242-A Evaporator DCS. This document includes the following information for equipment at the Evaporator and LERF locations:

- Allen-Bradley PLC ladder logic, data tables, and dip switch settings.
- Allen-Bradley 1785-KE communications module dip switch settings.
- Motorola V.3225 modem software settings.

This document will not address 242-A terminations or software.

No attempt will be made to explain the steps needed to use the Allen-Bradley 6200 software.

Specifications for this software are found in WHC-SD-WM-CSRS-011, "242-A and LERF PLC and Modem Software Requirements and Specifications". Software test results are found in document WHC-SD-534-OTR-002, "Operational Test Report for the 242-A Evaporator Operational Testing Program". Software configuration management is documented in WHC-SD-WM-CSCM-021, "242-A Programmable Logic Controller and Modem Software Configuration and Management Plan".

1.3 SYSTEM OVERVIEW

The LERF has six analog and six discrete signals that need to be monitored by the 242-A evaporator. The analog signals represent the liquid levels of the three large basins and three catch basins. The six discrete signals include three catch basin pump states and three catch basin leak detectors.

In addition, seven discrete alarms are generated by the PLCs and transmitted to the evaporator DCS. These include one over-range or under-range alarm for each analog input, for a total of six range alarms that are generated by the LERF PLC. One communication failure alarm is generated by the 242-A PLC.

This system uses two Allen-Bradley PLC-5/10s connected peer to peer via leased line modem. The communication scheme functions as follows:

- 1) The analog and discrete LERF signals are terminated at the LERF PLC in the 242AL-71 instrument building. The 4-20 mA analog signals undergo a 12 bit analog to digital (A/D) conversion and are stored as six 16-bit words in the LERF PLC memory.
- 2) The six discrete signals plus the value of the six analog error bits are stored in one 16-bit word in the LERF PLC memory.
- 3) Every 15 seconds, the 242-A PLC sends a message to the LERF PLC requesting a copy of these seven words.
- 4) The values of these seven words are then transmitted approximately 1 mile via leased line modem to the memory of the 242-A PLC.
- 5) The six words representing the analog signals are converted into six 4-20 mA analog signals at the 242-A PLC analog output module.
- 6) The six 4-20 mA signals are terminated at the 242-A DCS which converts each to a 13-bit number for use within the DCS.
- 7) The one word containing all of the discrete signals is written to a digital output module and sent to 15 discrete terminations on the 242-A DCS.

2.0 HARDWARE

2.1 PLC

Each PLC has one PLC-5/10 processor module, one power supply, one or two 1785-KE communications modules, a number of I/O modules, and one 8-slot I/O chassis. The PLC processor module resides in the left-most slot. The slot adjacent to the processor is occupied by the backplane power supply module.

The PLC modules must never be removed or inserted while the chassis is powered, otherwise damage to the module may occur. Chassis power is removed by setting the power switch on the power supply module to the off position.

Each PLC-5/10 processor module has four status lights, a keyed switch and two Data Highway Plus (DH+) connections. The 3-pin DH+ terminal is used to connect to the 1785-KE communications module. The 7-pin connector is used to connect to a laptop personal computer (PC) running Allen-Bradley PLC 6200 software for programming. Each processor is also equipped with one 1770-XY lithium battery (3.6 V, size AA) for backup power and one 1785-MJ 8K-word Electrically Erasable Programmable Read Only Memory (EEPROM) module for nonvolatile memory backup. The average life of the battery at 77 degrees Fahrenheit is about two years but should be replaced every year.

Slots to the right of the processor are numbered 0 through 7 (left to right). This numbering scheme is used in software addressing. Slot 0 is occupied by the PLC power supply. The other slots are occupied by several different types

of I/O modules. I/O modules may occupy any slot. However, their location must take into account the type of "slot addressing" selected, which is set with the PLC dip switches (see Section 3.1). Software reference to these terminations is by slot and point. (Note that plant instrumentation drawings have a different numbering scheme, which software addressing does not follow, where slots are numbered 1 through 9 (left to right) starting with the processor module.) The location of modules in the two PLC chassis and associated signals are summarized below in Tables 1 and 2.

TABLE 1. LERF PLC MODULE ARRANGEMENT			
SLOT	MODULE	FUNCTION	SIGNALS
LEFT	1785-LT4	PLC 5/10 PROCESSOR	NONE
0	1771-P4S	POWER SUPPLY	NONE
1	1771-IA	120 VAC DISCRETE NON-ISOLATED INPUT	NONE
2	1771-ID	120 VAC DISCRETE ISOLATED INPUT	YS-P-42, YS-P-43, YS-P-44, LDS-BSN42, LDS-BSN43, LDS-BSN44.
3	1771-OA	120 VAC DISCRETE OUTPUT	NONE
4	BLANK	NONE	NONE
5	1785-KE	242-A COMMUNICATIONS MODULE	NONE
6	BLANK	NONE	NONE
7	1771-IFE	4-20 mA ANALOG INPUT, SINGLE-ENDED, EXTERNALLY POWERED	LI-LCH42, LI-BSN42, LI-LCH43, LI-BSN43, LI-LCH44, LI-BSN44.

TABLE 2. 242-A PLC MODULE ARRANGEMENT			
SLOT	MODULE	FUNCTION	SIGNALS
LEFT	1785-LT4	PLC 5/10 PROCESSOR	NONE
0	1771-P4S	POWER SUPPLY	NONE
1	1771-IA	120 VAC DISCRETE NON-ISOLATED INPUT	NONE
2	1771-OAD	120 VAC DISCRETE OUTPUT	YS-P-42, YS-P-43, YS-P-44, YS-PLC-1, LDS-BSN42, LDS-BSN43, LDS-BSN44, LXS-LCH42, LXS-BSN42, LXS-LCH43, LXS-BSN43, LXS-LCH44, LXS-BSN44.
3	1771-OAD	120 VAC DISCRETE OUTPUT	NONE

TABLE 2. 242-A PLC MODULE ARRANGEMENT			
SLOT	MODULE	FUNCTION	SIGNALS
4	1785-KE	SPARE COMMUNICATIONS MODULE	NONE
5	1785-KE	LERF COMMUNICATIONS MODULE	NONE
6	1771-OFE2	4-20 mA ANALOG OUTPUT	LI-LCH44, LI-BSN44
7	1771-OFE2	4-20 mA ANALOG OUTPUT	LI-LCH42, LI-BSN42, LI-LCH43, LI-BSN43

2.2 COMMUNICATION HIGHWAY AND THE 1785-KE MODULE

The peer to peer communication between PLCs is normally 57.6 Kbaud. However, the communication speed used for the Motorola leased line modems is 9600 baud. The speed difference is handled by the 1785-KE DH+ Communications Interface Module which plugs into the PLC backplane.

Although the 1785-KE module is powered from the backplane, it does not communicate with the PLC processor module over the backplane. The communications module must be connected to the 3-pin DH+ terminals on the processor module via Belden 9463 or equivalent two wire shielded cable.

Connection between the 1785-KE module and the modem must be via shielded RS-232-C cable provided by the vendor. Un-shielded cable will pickup radio frequency noise and destroy communications. The cable (A-B catalog number 1770-CP) has a maximum length of 50 feet and is connected to the RS-232-C port on the module.

2.3 HARDWARE ADDRESSES

All equipment is addressed in octal. Addresses for the PLC processor and 1785-KE modules are dip switch selectable (see Section 3.0 for settings). These addresses are shown in the table below.

TABLE 3. HARDWARE ADDRESSES	
MODULE	OCTAL
242-A PLC processor	10
242-A 1785-KE module	11
LERF PLC processor	20
LERF 1785-KE module	21

2.4 LEASED LINE MODEMS

The two Motorola V.3225 modems are 9 watt, externally powered, full duplex modems. A leased phone line is used for communications between the two modems. The RS-232-C cable from the 1785-KE module is plugged into the modem's data terminal equipment (DTE) port. The DTE port, power switch, and leased line phone jack are located on the back panel of the modem.

The front panel has three buttons and six lights. The three buttons are used to select operating options from a menu (see Section 4.1). The front panel lights indicate the status of communications. The lights and their normal status are indicated in the table below.

TABLE 4. MODEM STATUS LIGHTS		
LIGHT	DESCRIPTION	NORMAL STATUS
QM	QUALITY MONITOR - lights when poor quality signal produces bit error rate of 10,000 or greater	Off
CS	CLEAR TO SEND - lights when the modem transmitter is ready to accept data from the terminal (KE module)	On
RS	REQUEST TO SEND - lights when the terminal is ready to send data to the modem	Off
CD	CARRIER DETECT - lights when the received audio carrier signal is detected	On
RD	RECEIVED DATA - lights for a space indicating receive output data activity	Flashes about every 15 seconds
TD	TRANSMIT DATA - lights for a space indicating transmit input data activity	Flashes about every 15 seconds

Under normal conditions, a failure of communications indicated on the 242-A DCS may require turning the modem power switch off, then on. When a modem is turned on, option settings are loaded from nonvolatile memory and any faults clear.

3.0 DIP SWITCH SETTINGS

3.1 PLC PROCESSOR AND CHASSIS

PLC-5/10 processor modules have three dip switch assemblies (SW1, SW2, and SW3) that must be set by the programmer. These assemblies are described below and listed in Table 5. Assemblies SW1, SW2, and SW3 are set such that a toggle pushed to the bottom is ON (closed) and equals "1" in Table 5; a toggle pushed to the top is OFF (open) and equals "0" in Table 5.

SW1: An 8-switch assembly for setting the station address of the processor on the data highway. This is octal 10 and 20 for the 242-A and LERF processors, respectively.

SW2: An 8-switch assembly used for defining adapter mode communication which is not used on this model PLC.

SW3: A 4-switch assembly that connects a terminator across the line when the processor module is an end device on a DH+ or remote I/O link. Both 242-A and LERF processors are end devices on DH+ and remote I/O links.

A fourth dip switch assembly on the chassis backplane behind the processor module must also be set. The backplane dip switch assembly sets output handling when a hardware watchdog timeout occurs, "slot addressing", Electrically Erasable Programmable Read Only Memory (EEPROM) transfer, and RAM memory protection. Both LERF and 242-A PLCs are set for output resetting upon watchdog timeout, 1-slot addressing, EEPROM memory transfer to CMOS RAM at power-up, and RAM memory protection disabled. For this assembly, a switch pressed in at the top is ON (closed) and equals "1" in Table 5; a switch pressed in at the bottom is OFF (open) and equals "0" in Table 5.

Please see the "1785 PLC-5 Family Programmable Controllers - Hardware Installation Manual" (Reference 1) for more information about processor and backplane dip switches and settings.

TABLE 5. PROCESSOR AND CHASSIS DIP SWITCH SETTINGS

PLC	SWITCH SW1	SWITCH SW2	SWITCH SW3	BACKPLANE
242-A PLC	11101100	01111101	1100	00001000
LERF PLC	11110100	01111101	1100	00001000

3.2 1785-KE DH+ COMMUNICATIONS INTERFACE MODULE

The communications module setup is performed with four dip switches. Vendor dip switch documentation for the 1785-KE module is somewhat confusing because UP equals OFF which equals 1. Rather than list settings as "1" and "0", they are defined as "UP" (U) or "DOWN" (D). Dip switch settings for the LERF and 242-A KE modules are described below and listed in Table 6.

- SW1: This 6-switch assembly is used to select RS-232-C link features. The LERF and 242-A 1785-KE modules are set up for full duplex, BCC, no parity, no embedded responses, accept duplicate messages, ignore handshaking signals, and pass through diagnostic commands.
- SW2: This 8-switch assembly sets the node number. The 242-A 1785-KE module address is octal 11. The LERF 1785-KE address is octal 21.
- SW3: This 6-switch assembly sets the DH+ and RS-232-C link communication rates, and local or remote operation. The LERF and 242-A 1785-KE modules are both set for a DH+ speed of 57.6 Kbaud, RS-232-C link speed of 9600 baud, and remote operation.
- SW4: Not used

For more information on module features and set up see the "1785-KE Data Highway Plus Communications Interface Module - User's Manual" (Reference 2).

TABLE 6. KE MODULE DIP SWITCH SETTINGS				
MODULE	SW1	SW2	SW3	SW4
242-A 1785-KE	UUUUUU	DDDD <u>U</u> DDU	DDUDDU	UUUU
LERF 1785-KE	UUUUUU	DDDU <u>U</u> DDU	DDUDDU	UUUU

4.0 SOFTWARE

4.1 LEASED LINE MODEMS

Modems must be set up to be compatible with the 1785-KE module for communication speed and error checking.

There are three buttons on the front panel of each modem. The three buttons are used to select operating options from a menu, which is accessed using the buttons. Appendix E contains the modem option settings. These settings are saved in nonvolatile memory, as should normally be the case, if the programmer so chooses. The settings are loaded from nonvolatile memory when the modem is powered up. Please see the Motorola "Installation and Operation Manual" (Reference 4) for more information on the set up of modem model V.3225.

4.2 PLC PROGRAMMING

Ladder logic for the LERF PLC is found in Appendix A, and Appendix B contains the ladder logic for the 242-A PLC. The data tables for the LERF and 242-A PLCs are found in Appendix C and D, respectively.

All PLC signals are listed in Table 7 and Table 8 by DCS External Point Name (EPN), LERF PLC input termination, data table address, and 242-A PLC output termination. PLC inputs and outputs are in octal. Data table addresses are given in decimal.

TABLE 7. ANALOG SIGNAL ADDRESSES				
EPN	LERF PLC-20 ANALOG INPUT	LERF PLC-20 DATA TABLE ADDRESS	242-A PLC-10 DATA TABLE ADDRESS	242-A PLC-10 ANALOG OUTPUT
LI-LCH42	I:007/0	N7:21	N7:21	O:007/0
LI-BSN42	I:007/1	N7:22	N7:22	O:007/1
LI-LCH43	I:007/2	N7:23	N7:23	O:007/2
LI-BSN43	I:007/3	N7:24	N7:24	O:007/3
LI-LCH44	I:007/4	N7:25	N7:25	O:006/0
LI-BSN44	I:007/5	N7:26	N7:26	O:006/1

TABLE 8. DIGITAL SIGNAL ADDRESSES				
EPN ¹	LERF PLC-20 DISCRETE INPUT	LERF PLC-20 DATA TABLE ADDRESS	242-A PLC-10 DATA TABLE ADDRESS	242-A PLC-10 DISCRETE OUTPUT
YS-P-42	I:002/0	N7:20/0	N7:20/0	O:002/0
YS-P-43	I:002/1	N7:20/1	N7:20/1	O:002/1
YS-P-44	I:002/2	N7:20/2	N7:20/2	O:002/2
YS-PLC-1 ²	-----	-----	N7:20/6	O:002/6
LDS-BSN42	I:002/3	N7:20/7	N7:20/7	O:002/7
LDS-BSN43	I:002/4	N7:20/8	N7:20/8	O:002/10
LDS-BSN44	I:002/5	N7:20/9	N7:20/9	O:002/11
LXS-LCH42	-----	N7:20/10	N7:20/10	O:002/12
LXS-BSN42	-----	N7:20/11	N7:20/11	O:002/13
LXS-LCH43	-----	N7:20/12	N7:20/12	O:002/14
LXS-BSN43	-----	N7:20/13	N7:20/13	O:002/15
LXS-LCH44	-----	N7:20/14	N7:20/14	O:002/16
LXS-BSN44	-----	N7:20/15	N7:20/15	O:002/17

Table 8 Notes:

1. EPNs with the LXS prefix denote signal conditioning errors for the six analog signals.
2. YS-PLC-1 is a discrete communication alarm generated at the 242-A PLC.

4.3 LERF PLC LADDER LOGIC DESCRIPTION

Refer to Appendix A for the LERF ladder logic and Appendix C for a complete bit map of the LERF data table. Please see the "PLC-5 Programming Software - Instruction Set Reference" (Reference 3) for information on control block status bits (EN through RW in the data table).

Rung 2:1:

Block Transfer Write (BTW). This rung contains the commands that configure the 1771-IFE Analog Input Module. A BTW command is executed once on power-up to load scaling and polarity information. Control of the BTW is through the "power-up bit" found on the Block Transfer Read of rung 2:0 (ie: bit N7:40/0). This bit is set on the first scan after the CMOS is loaded from the EEPROM. The BTW has 17 words found in registers N7:0 through N7:16. Words N7:5 through N7:16 define scaling of the analog signals. These values are in Binary Coded Decimal (BCD).

For those not familiar with BCD, 0100 0000 1001 0101 reads 4 0 9 5 in BCD. Signals are scaled to the 12 bit maximum. This means the 4-20 mA signal is scaled from 0 to 4095. Conversion to engineering units is done at the DCS.

Rung 2:0:

Block Transfer Read (BTR). The 4-20 mA signal undergoes an A/D conversion in the 1771-IFE module. The result is stored as 6 words along with 4 diagnostic words at N7:40 in the PLC processor. Bits are set if the analog input current falls below 4 mA or exceeds 20 mA. Word N7:41 contains under-range bits on a channel by channel basis. For example, LI-LCH43 under-range is shown by bit N7:41/2. Word N7:42 is set for over-range on a point by point basis. The BTR occurs when the enable (EN) bit (N7:30/15) is set. The actual count values can be seen by plugging the laptop PC, which is running Allen-Bradley 6200 software, into the processor and looking at the memory map. Testing with a Transmation signal generator showed that 4.000 mA corresponds to 0 counts and 20.000 mA corresponds to 4095 counts. A signal of 20.001 mA corresponds to 4095 counts with an over-bit set in word N7:42. A signal of 3.999 mA corresponds to 0 counts with an under-bit set in word N7:41.

Rung 2:2:

Timer On Delay (TON). Timer T4:0 is set on a 12 second cycle to control a masked move at rung 2:9 and bitwise math at rung 2:10.

Rung 2:9:

Masked Move (MVM). The value of the first three discrete inputs (see Table 8: YS-P-42, YS-P-43, YS-P-44) located at I:002/0 through I:002/2 are copied into bits N7:20/0 through N7:20/2 every 12 seconds. A mask is used to tell the processor which bits of a word to move. Bits are read from right to left with the right-most bit being bit 0. Hence, the mask for this operation is binary 0111, or hexadecimal 7. For more information on masked moves, please see the "PLC-5 Programming Software - Instruction Set Reference" (Reference 3).

Note that the field digital inputs can be monitored at the LERF PLC using a laptop PC running Allen-Bradley 6200 software by viewing the memory map binary values. As with the mask, the signals are found at word I:002 by reading from right to left.

Rung 2:10:

The following occurs ever 12 seconds when timer T4:0 is done:

- Reset (RES) timer T4:0 at rung 2:2.
- A Bitwise Inclusive Or (OR) of words N7:41 and N7:42 representing the six analog over and under-range error bits and place the result in N7:50.
- A Bitwise Exclusive Or (XOR) of N7:50 and 0000 0000 0011 1111 loaded in N7:51. Place results in N7:29. These steps make over and under-range error bits fail-safe.

Rungs 2:11 to 2:13:

On every scan, copy the discrete values of LDS-BSN42, LDS-BSN43, and LDS-BSN44 located at I:002/3 through I:002/5 into N7:20/7 through N7:20/9 (see Table 8). Word N7:20 now contains the value of all discrete signals but none of the analog or communication alarms.

Rungs 2:3 to 2:8:

Move the six analog range alarm bits to N7:20/10 through N7:20/15.

The above operation results in loading of word N7:20 with six discrete values and six analog error bits which will correspond to the discrete outputs of the 242-A PLC.

4.4 242-A PLC LADDER LOGIC DESCRIPTION

At this point in the sequence of data processing, all but one of the discrete signals and all of the analog values have been loaded into the LERF PLC data table. The remaining tasks are for the 242-A PLC to read this data if communications are operating, place a copy in its own memory, generate the one remaining discrete signal (the communications status), and then provide outputs to the DCS.

Refer to Appendix B for the 242-A ladder logic and Appendix D for a complete bit map of the 242-A data table. Please see the "PLC-5 Programming Software - Instruction Set Reference" (Reference 3) for information on control block status bits (EN through RW in the data table).

Rung 2:0:

Timer On Delay (TON). Timer T4:0 has several functions. First, it controls the transfer of data from the LERF PLC to the 242-A PLC by use of its done (DN) bit in rung 2.1 to control the send-message command. Secondly, it controls the moving of data in the memory of the 242-A PLC in rung 2.5. The timer resets every 15 seconds.

Rung 2:1:

Send/Receive Message (MSG). The message is sent every 15 seconds when timer T4:0 times-out. The MSG command copies seven words from N7:20 in the LERF PLC to N7:20 in the 242-A PLC. The message total block size, which can only be viewed on the laptop screen, is 11 words. The control block starts at N7:0.

The MSG command requires the following additional information:

Communication Command:	PLC-5 TYPED READ
PLC-5 data table address:	N7:20
Size in elements:	8
Local/Remote:	Remote
Remote station:	020
Link ID:	00
Remote Link type:	Data Highway
Local Node Address:	11
Destination Data Table Address:	N7:20

Rung 2:2:

Timer On Delay (TON). Timer T4:1 turns on when the MSG command is issued (ie: toggled by N7:0/14, the T4:0 start bit). Timer T4:1 has a 0.01 second (1 tick) time base. The value the timer must reach before its done bit is set is 1500 ticks, or 15 seconds. If communications are successful, the timer will never reach its 15 second limit. If the timer times-out (ie: communications fail), then the alarm bit is set in rung 2.3.

Rung 2:3:

Unlatch (OTU) bit N7:20/6 to off (0) if the enable (EN) bit of timer T4:1 is set and the timer reaches 15 seconds. When the timer reaches 15 seconds its done (DN) bit is set. A zero at bit N7:20/6 indicates communications between the two PLCs has failed. The OTU result is retentive.

Rung 2:4:

Latch (OTL) bit N7:20/6 to on (1) any time the MSG command is completed. A "1" at bit N7:20/6 means communications are working. The OTL result is retentive. Bit N7:20/6 was one of the left-over bits from LERF word N7:20.

Rung 2:5:

The following occurs every 15 seconds when timer T4:0 is done:

- Move (MOV) all 16 bits of word N7:20, which contains the values of the 13 digital signals, to the 1771-OAD discrete output module in slot 2.
- Reset (RES) timer T4:0.
- Copy (COP) four words from N7:21 to N7:31. These four words contain the values of analog signals LI-LCH42, LI-BSN42, LI-LCH43, and LI-BSN43.
- Copy (COP) two words from N7:25 to N7:51. These two words contain the values of analog signals LI-LCH44 and LI-BSN44.

Rung 2:6:

Block Transfer Write (BTW). This rung writes 13 words, including the four analog signals (LI-LCH42, LI-BSN42, LI-LCH43, and LI-BSN43) copied at rung 2:5, to the 1771-OFE2 analog output module in slot 7. The first four words (beginning at N7:31) of the block of 13 words represent the analog signals, and the remaining nine words are unused. The five-word control block begins at N7:45.

Rung 2:7:

Block Transfer Write (BTW). This rung writes 13 words, including the two analog signals (LI-LCH44 and LI-BSN44) copied at rung 2:5, to the 1771-OFE2 analog output module in slot 6. The first two words

(beginning at N7:51) of the block of 13 words represent the analog signals, and the remaining 11 words are unused. The five-word control block begins at N7:65.

Rung 2:8:

Block Transfer Read (BTR). This rung reads from the analog output module in slot 7 what was written to it by rung 2:6 so values can be displayed on a laptop PC running Allen-Bradley 6200 software.

Rung 2:9:

Block Transfer Read (BTR). This rung reads from the analog output module in slot 6 what was written to it by rung 2:7 so values can be displayed on a laptop PC running Allen-Bradley 6200 software.

4.5 RADIX (DATA FORMAT) CONVERSION

For those unfamiliar with counting or converting from one radix to another, this discussion and Appendix F are provided. This may be helpful primarily with understanding or specifying masks. Octal requires three bits to set a value and BCD takes four bits. In binary, bits are numbered from right to left. The right-most bit is bit 0 and has a value of 1 when set. The values of the first four bits are shown below in Table 9.

TABLE 9. BINARY BIT VALUES				
BIT	3	2	1	0
VALUE	8	4	2	1

To convert from binary to hex:

- 1) chop the binary into groups by deleting the four right-most bits, then the four left-most bits
- 2) using Table 9, determine the value of the resulting groups and combine the values

ie: 100000 binary = 100000 , 100000
 = 2 , 0
 = 20 hex

To convert from binary to octal:

- 1) convert the binary to base-8 by chopping the binary into groups each containing three bits
- 2) using Table 9, determine the value of the resulting groups and combine the values

ie: 100000 binary = 100 , 000
 = 4 , 0
 = 40 octal

5.0 REFERENCES

1. Allen-Bradley publication 1785-6.6.1, June 1993, "1785 PLC-5 Family Programmable Controllers - Hardware Installation Manual".
2. Allen-Bradley publication 1785-6.5.2, May 1989, "1785-KE Data Highway Plus Communications Interface Module - User's Manual".
3. Allen-Bradley publication 6200-6.4.11, May 1993, "PLC-5 Programming Software - Instruction Set Reference", Release 4.4.
4. Motorola document number 6 209 5136 13014, April 1993, "Installation and Operation Manual", models V.3225/V.3225L.

APPENDIX A - LERF LADDER LOGIC

Allen-Bradley Company
6200 Series Software
PLC-5 Programming Terminal Software
Release 4.2
Program Listing Report

Processor Name: LERF, Addr: 20
8 May 1995 - 11:25

REPORT OPTIONS

Page Width:	80
Page Length:	66
Graphics Capabilities:	NO
Right Power Rail:	YES
Address Display:	SYMBOL
Address Comments:	YES
Rung Comments:	YES
Output Cross Reference:	NO
Ladder Cross Reference:	ALL
Starting Rung:	2:0
Ending Rung:	999:32767

Rung 2:0

N7:30	+BTR-----+	
+] / [-----	BLOCK TRNSFR READ	+- (EN) -+
15	Rack	00
	Group	7+- (DN)
	Module	0
	Control Block	N7:30+- (ER)
	Data file	N7:40
	Length	10
	Continuous	N

Rung 2:1

N7:40 N7:35	+BTW-----+	
+] [---] / [-----	BLOCK TRNSFR WRITE	+- (EN) -+
0 15	Rack	00
	Group	7+- (DN)
	Module	0
	Control Block	N7:35+- (ER)
	Data file	N7:0
	Length	17
	Continuous	N

Rung 2:2

	+TON-----+	
	TIMER ON DELAY	+- (EN) -+
	Timer	T4:0
	Time base	1.0+- (DN)
	Preset	12
	Accum	10

Rung 2:3

N7:29		N7:20	
+--]	[-----	()--+	
0		10	

Rung 2:4

N7:29		N7:20	
+--]	[-----	()--+	
1		11	

Rung 2:5

N7:29		N7:20	
+--]	[-----	()--+	
2		12	

Rung 2:6

N7:29		N7:20	
+--]	[-----	()--+	
3		13	

Rung 2:7

N7:29		N7:20	
+--]	[-----	()--+	
4		14	

Rung 2:8

N7:29		N7:20	
+--]	[-----	()--+	
5		15	

Rung 2:9

T4:0	+MVM-----+
]/[	+MASKED MOVE++
DN	Source #I:002
	0
	Mask 0007
	Dest N7:20
	-1024

Rung 2:10

T4:0		T4:0
]/[		(RES)
DN		
	+COP-----+	
	++COPY FILE+++	
	Source #N7:44	
	Dest #N7:21	
	Length 6	
	+OR-----+	
	+++BITWISE INCLUS OR+++	
	Source A #N7:41	
	-64	
	Source B #N7:42	
	0	
	Dest #N7:50	
	-64	
	+XOR-----+	
	+++BITWISE EXCLUS OR++	
	Source A #N7:50	
	-64	
	Source B #N7:51	
	63	
	Dest #N7:29	
	-1	

Rung 2:11

I:002	N7:20
+--] [-----	()--+
05	9

Rung 2:12

I:002	N7:20
+--] [-----	()--+
04	8

Rung 2:13

I:002	N7:20
+--] [-----	()--+
03	7

Rung 2:14

+-----[END OF FILE]-----	+-----

APPENDIX B - 242-A LADDER LOGIC

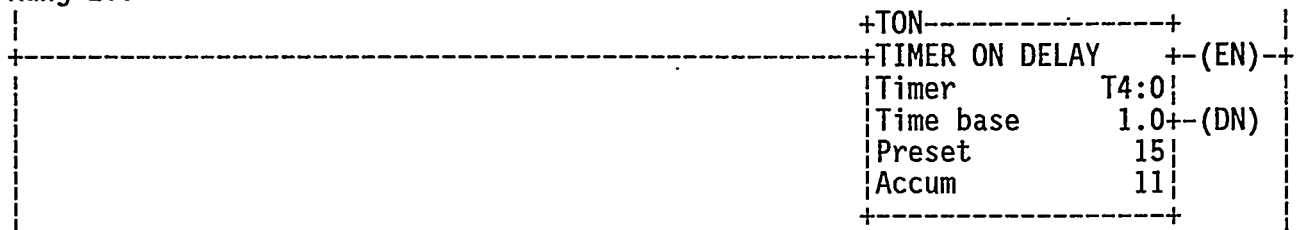
Allen-Bradley Company
6200 Series Software
PLC-5 Programming Terminal Software
Release 4.2
Program Listing Report

Processor Name: 242A, Addr: 10
8 May 1995 - 12:11

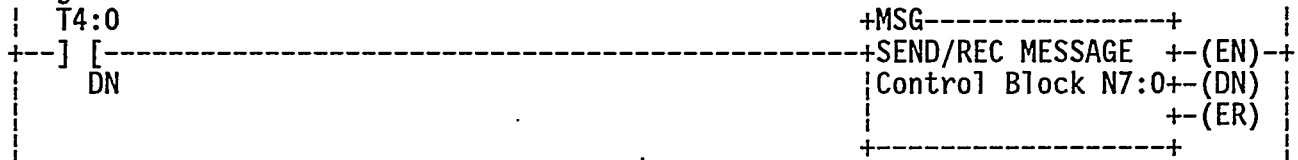
REPORT OPTIONS

Page Width:	80
Page Length:	66
Graphics Capabilities:	NO
Right Power Rail:	YES
Address Display:	SYMBOL
Address Comments:	YES
Rung Comments:	YES
Output Cross Reference:	NO
Ladder Cross Reference:	ALL
Starting Rung:	2:0
Ending Rung:	999:32767

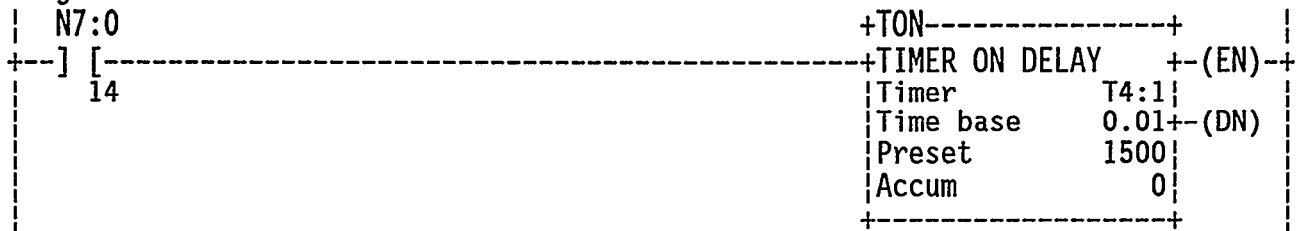
Rung 2:0



Rung 2:1



Rung 2:2



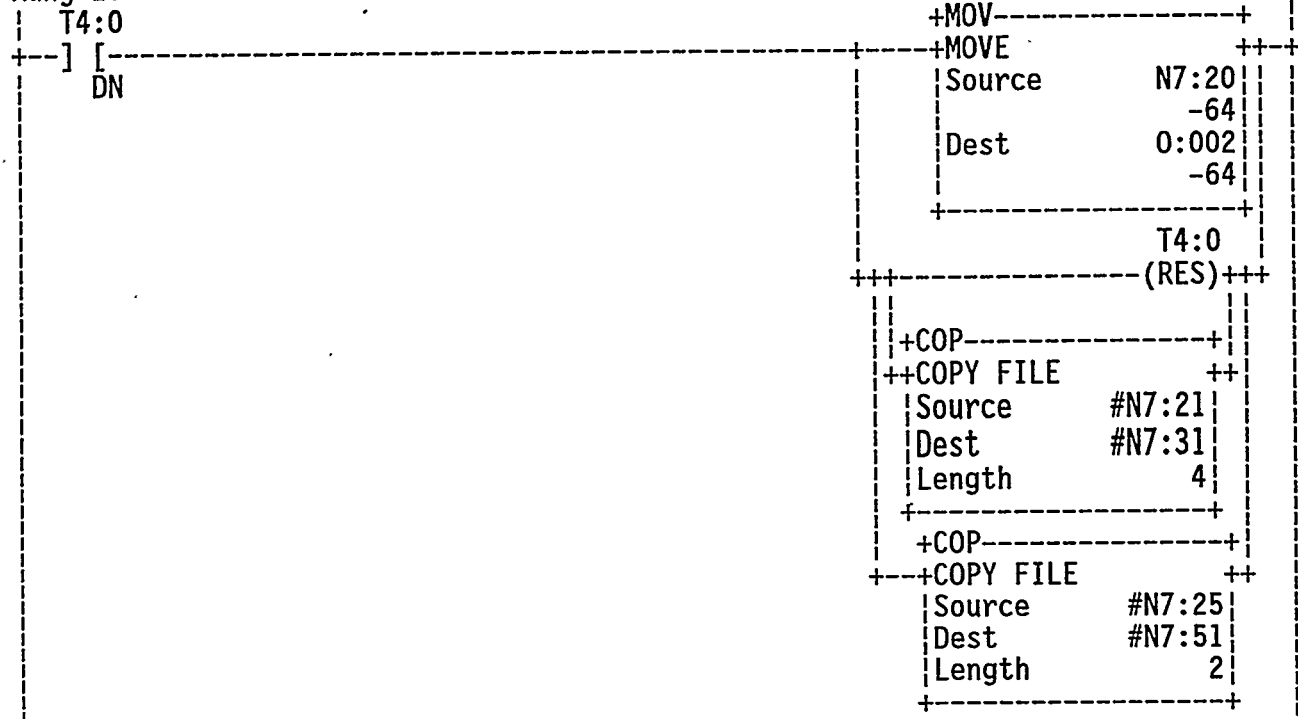
Rung 2:3



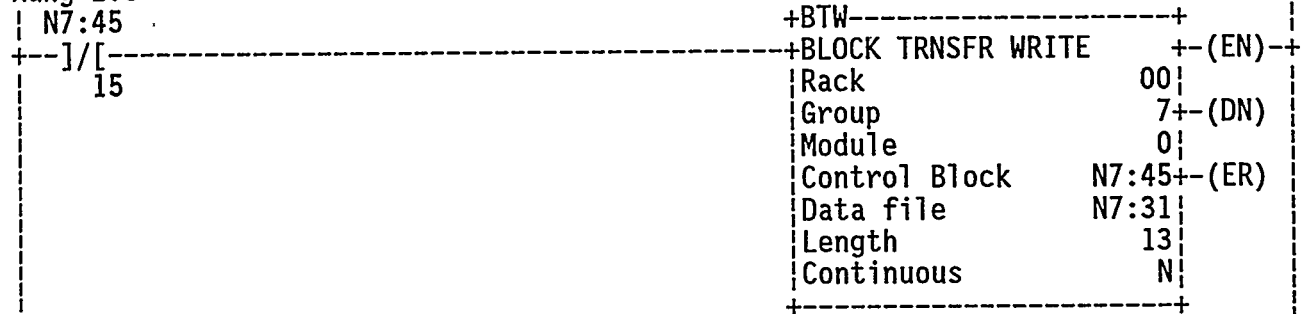
Rung 2:4



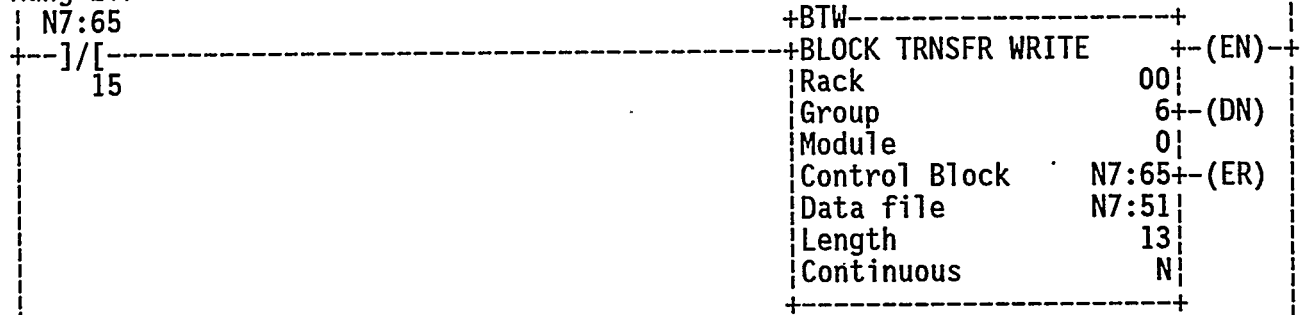
Rung 2:5



Rung 2:6



Rung 2:7



Rung 2:8

N7:70	+BTR-----+	
15	BLOCK TRNSFR READ	+- (EN) -+
	Rack	00
	Group	7+- (DN)
	Module	0
	Control Block	N7:70+- (ER)
	Data file	N7:75
	Length	5
	Continuous	N

Rung 2:9

N7:80	+BTR-----+	
15	BLOCK TRNSFR READ	+- (EN) -+
	Rack	00
	Group	6+- (DN)
	Module	0
	Control Block	N7:80+- (ER)
	Data file	N7:85
	Length	5
	Continuous	N

Rung 2:10

[END OF FILE]		
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APPENDIX C - LERF DATA TABLE

LOCATION	OCTAL																DESCRIPTION
	17	16	15	14	13	12	11	10	7	6	5	4	3	2	1	0	
N7:0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RANGE SELECTION CHANNELS 1-8 RANGE SELECTION CHANNELS 9-16 SAMPLING, FORMAT, INPUT TYPE, FILTER SIGN BITS, MINIMUM SCALING VALUE
N7:1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:2	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	
N7:3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SIGN BITS, MINIMUM SCALING VALUE MINIMUM MAXIMUM MINIMUM MAXIMUM
N7:5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:6	0	1	0	0	0	0	0	0	1	0	0	1	0	1	0	1	
N7:7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:8	0	1	0	0	0	0	0	0	1	0	0	1	0	1	0	1	MINIMUM MAXIMUM MINIMUM MAXIMUM
N7:9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:10	0	1	0	0	0	0	0	0	1	0	0	1	0	1	0	1	
N7:11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:12	0	1	0	0	0	0	0	0	1	0	0	1	0	1	0	1	MINIMUM MAXIMUM MINIMUM MAXIMUM
N7:13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:14	0	1	0	0	0	0	0	0	1	0	0	1	0	1	0	1	
N7:15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:16	0	1	0	0	0	0	0	0	1	0	0	1	0	1	0	1	MINIMUM MAXIMUM MINIMUM MAXIMUM
N7:17	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:18	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:19	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:20	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DIGITAL INPUTS LI-LCH42 LI-BSN42 LI-LCH43 LI-BSN43 LI-LCH44 LI-BSN44
N7:21	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:22	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:23	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:24	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MESSAGE WORDS READ BY 242-A PLC-10 AT RUNG 2:1
N7:25	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:26	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:27	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

BLOCK TRANSFER WRITE
DATA IN LERF PLC-20
AT RUNG 2:1

LERF PLC-20 DATA TABLE (SHEET 1 OF 2)

C:\ERFDAT1.DWG

LOCATION	OCTAL																DESCRIPTION
	17	16	15	14	13	12	11	10	7	6	5	4	3	2	1	0	
N7:28	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESULT OF RUNG 2:10 XOR OF N7:50 AND N7:51
N7:29	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:30	EN	ST	DN	ER	CO	EW	NR	TO	RW	0	0	0	0	0	0	0	
N7:31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CONTROL BLOCK FOR BTR (RUNG 2:0) 5 WORDS FIRST WORD HAS ALL ERROR BITS
N7:33	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:34	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:35	EN	ST	DN	ER	CO	EW	NR	TO	RW	0	0	0	0	0	0	0	
N7:36	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CONTROL BLOCK FOR BTW (RUNG 2:1) 5 WORDS FIRST WORD HAS ALL ERROR BITS
N7:37	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:38	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:39	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:40	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DIAGNOSTICS, BIT 0 IS POWER-UP BIT
N7:41	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:42	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:43	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:44	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	RESULTS OF RUNG 2:0 BLOCK TRANSFER READ INCLUDING ERROR BITS
N7:45	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:46	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:47	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:48	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	RESULT OF RUNG 2:10 INCLUS OR OF N7:41 AND N7:42 RUNG 2:10 XOR MASK FOR N7:50 TRANSFER TO N7:29
N7:49	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:50	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:51	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

LERF PLC-20 DATA TABLE (SHEET 2 OF 2)

(LERFDAT2.DWG)

APPENDIX D - 242-A DATA TABLE

LOCATION	OCTAL																DESCRIPTION
	17	16	15	14	13	12	11	10	7	6	5	4	3	2	1	0	
N7:0	EN	ST	DN	ER	CO	EW	NR	TO	RW	0	0	0	0	0	0	0	CONTROL BLOCK FOR RUNG 2:1 MESSAGE
N7:1	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	1	
N7:2	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	
N7:3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	
N7:4	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	
N7:5	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	
N7:6	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	
N7:7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:8	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	
N7:9	0	0	0	0	0	1	1	1	0	0	0	1	0	1	0	0	
N7:10	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	
N7:11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DIGITAL INPUTS LI-LCH42 LI-BSN42 LI-LCH43 LI-BSN43 LI-LCH44 LI-BSN44 MESSAGE WORDS READ FROM LERF PLC-20 (RUNG 2:1) LI-LCH42 LI-BSN42 LI-LCH43 LI-BSN43 COPY 4 WORDS BEGINNING AT N7:21 (RUNG 2:5) BLOCK TRANSFER WRITE TO GROUP 7 (RUNG 2:6)
N7:13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:15	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	
N7:16	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	
N7:17	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:18	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:19	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:20	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:21	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:22	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:23	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:24	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:25	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:26	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:27	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:28	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BLOCK TRANSFER WRITE TO GROUP 7 (RUNG 2:6)
N7:29	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:30	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:31	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:32	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:33	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:34	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:35	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:36	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:37	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	
N7:38	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:39	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:40	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:41	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	
N7:42	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:43	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	

242-A PLC-10 DATA TABLE (SHEET 1 OF 2)

(242ADAT1.DWG)

LOCATION	OCTAL																DESCRIPTION
	17	16	15	14	13	12	11	10	7	6	5	4	3	2	1	0	
N7:44	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CONTROL BLOCK FOR BTW (RUNG 2:6)
N7:45	EN	ST	DN	ER	CO	EW	NR	TO	RW	0	0	0	0	0	0	0	
N7:46	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:47	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:48	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:49	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LI-LCH44 } COPY LI-BSN44 } 2 WORDS BEGINNING AT N7:25 (RUNG 2:5)
N7:50	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:51	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:52	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:53	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:54	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BLOCK TRANSFER WRITE TO GROUP 6 (RUNG 2:7)
N7:55	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:56	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:57	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	
N7:58	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:59	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	CONTROL BLOCK FOR BTW (RUNG 2:7)
N7:60	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:61	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	
N7:62	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:63	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	
N7:64	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CONTROL BLOCK FOR BTR (RUNG 2:8)
N7:65	EN	ST	DN	ER	CO	EW	NR	TO	RW	0	0	0	0	0	0	0	
N7:66	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:67	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:68	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:69	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LI-LCH42 } BLOCK TRANSFER READ LI-BSN42 } FROM GROUP 7 LI-LCH43 } OUTPUTS (RUNG 2:8) LI-BSN43 }
N7:70	EN	ST	DN	ER	CO	EW	NR	TO	RW	0	0	0	0	0	0	0	
N7:71	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:72	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:73	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:74	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CONTROL BLOCK FOR BTR (RUNG 2:9)
N7:75	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:76	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:77	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:78	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:79	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LI-LCH44 } BLOCK TRANSFER READ LI-BSN44 } FROM GROUP 6 OUTPUTS (RUNG 2:9)
N7:80	EN	ST	DN	ER	CO	EW	NR	TO	RW	0	0	0	0	0	0	0	
N7:81	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:82	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:83	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:84	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LI-LCH44 } BLOCK TRANSFER READ LI-BSN44 } FROM GROUP 6 OUTPUTS (RUNG 2:9)
N7:85	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:86	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
N7:87	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:88	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
N7:89	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

242-A PLC-10 DATA TABLE (SHEET 2 OF 2)

(242ADAT2.DWG)

APPENDIX E - MODEM OPTION SETTINGS

MOTOROLA V.3225 MODEM SETUP

MENU OPTIONS	MODEM SETTINGS ^{1,2}	
	242-A MODEM 20 (MASTER)	LERF MODEM 20 (SLAVE)
MODEM OPTIONS		
DCE RATE	9600 TRELLIS	9600 TRELLIS
FORCED ANS / NORMAL ORIG	NORMAL ORIGINATE	FORCED ANSWER
FAST TRAIN	DISABLED	DISABLED
AUTO RETRAIN	ENABLED	ENABLED
TRANSMIT CLOCK	INTERNAL	INTERNAL
LINE TYPE	LEASED	LEASED
WIRE	4 WIRE	4 WIRE
TX LEVEL	0 dBm	0 dBm
DIAL BACKUP	MANUAL	MANUAL
LOOKBACK TIMER	15 MIN.	15 MIN.
JACK TYPE	RJ11	RJ11
LINE CURRENT DISCONNECT	LONG	LONG
LONG SPACE DISCONNECT	DISABLED	DISABLED
V.32 CLEARDOWN	ENABLED	ENABLED
V.22 GUARD TONE	DISABLED	DISABLED
MNP OPTIONS		
MNP PROTOCOL	DISABLED	DISABLED
DTE SPEED	DTE = DCE	DTE = DCE
MNP FLOW CONTROL	DISABLED	DISABLED
XON/XOFF PASS THROUGH	DISABLED	DISABLED
DATA COMPRESSION	ENABLED	ENABLED
INACTIVITY TIMER	OFF	OFF
MNP BREAK CONTROL	0	0
DTE OPTIONS		
OPERATION	ASYN	ASYN
DTE RATE	9600	9600

MENU OPTIONS	MODEM SETTINGS ^{1,2}	
	242-A MODEM 20 (MASTER)	LERF MODEM 20 (SLAVE)
CHARACTER SIZE	8 BIT	8 BIT
PARITY	NO PARITY	NO PARITY
AT COMMAND SET	DISABLED	DISABLED
DTR RESPONSE	IGNORE	IGNORE
DSR STATE	FORCED HIGH	FORCED HIGH
DCD STATE	NORMAL	NORMAL
CTS STATE	FORCED HIGH	FORCED HIGH
RTS/CTS DELAY	N/A	N/A
DTE FALLBACK	DISABLED	DISABLED
DISCONNECT OPTIONS	RETAINED	RETAINED
TEST OPTIONS		
BILATERAL ANALOG LOOP	ENABLED	DISABLED
BILATERAL DIGITAL LOOP	ENABLED	DISABLED
DTE LOCAL TEST	DISABLED	DISABLED
DTE REMOTE TEST	DISABLED	DISABLED
REMOTE COMMANDED	ENABLED	ENABLED
TEST TIMEOUT	OFF	OFF
DIAL OPTIONS		
DIAL TYPE	TONE	TONE
AUTO-DIAL #	1	1
DIAL TONE	WAIT FOR	WAIT FOR
WAIT DELAY	2 SECONDS	2 SECONDS
PAUSE DELAY	2 SECONDS	2 SECONDS
CALL TIMEOUT	60 SECONDS	30 SECONDS
ANSWER RING #	1	1
801 V.32 TIMEOUT	LONG	LONG
AUTO-CALLBACK	DISABLED	DISABLED
SPEAKER OPTIONS		
VOLUME CONTROL	MEDIUM	MEDIUM

MENU OPTIONS	MODEM SETTINGS ^{1,2}	
	242-A MODEM 20 (MASTER)	LERF MODEM 20 (SLAVE)
SPEAKER CONTROL	ON UNTIL CAR. DETECT	ON UNTIL CAR. DETECT

Option Setting Notes:

1. N/A (not applicable) means not prompted by modem setup procedure.
2. Settings of slave modem that are different from master are in bold text.

APPENDIX F - DATA FORMAT CONVERSIONS

DATA FORMAT CONVERSIONS			
DECIMAL	HEXADECIMAL	OCTAL	BINARY
0	0	0	0000
1	1	1	0001
2	2	2	0010
3	3	3	0011
4	4	4	0100
5	5	5	0101
6	6	6	0110
7	7	7	0111
8	8	10	1000
9	9	11	1001
10	0A	12	1010
11	0B	13	1011
12	0C	14	1100
13	0D	15	1101
14	0E	16	1110
15	0F	17	1111
16	10	20	0001 0000
17	11	21	0001 0001
18	12	22	0001 0010
19	13	23	0001 0011
20	14	24	0001 0100
21	15	25	0001 0101
22	16	26	0001 0110
23	17	27	0001 0111
24	18	30	0001 1000
25	19	31	0001 1001
26	1A	32	0001 1010
27	1B	33	0001 1011
28	1C	34	0001 1100
29	1D	35	0001 1101
30	1E	36	0001 1110

DATA FORMAT CONVERSIONS			
DECIMAL	HEXADECIMAL	OCTAL	BINARY
31	1F	37	0001 1111
32	20	40	0010 0000