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AUTOMATED ARRAY ASSEMBLY TASK
Phase I

Quarterly Report No. 1

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ABSTRACT

Work during this quarter consisted primarily of preparing base line cost estimates for current solar cell processing technologies; preparing an initial design-to-cost goal breakdown; designing and beginning construction of an experimental solar cell module; and initiating the various activities that make up this task. The base line cost estimates show that current solar cell fabrication technology is about an order of magnitude too expensive as compared to the design-to-cost goals. In the area of solar cell fabrication, metallization is shown to be the least cost-effective process element.

The design-to-cost concept is used to measure the overall effectiveness of low-cost silicon solar cell module improvements. The design-to-cost goal is $500 per peak kilowatt in 1985 with an annual production output of 500 megawatts peak power. The key to the Low-Cost Silicon Solar Array Project is the ability to meet this integrated cost goal. The Automated Array Assembly Task is the obvious focal point for assessing the overall success of the program.

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SECTION I
INTRODUCTION

The overall goal of the Array Automated Assembly Task, Phase I, of the Low Cost Silicon Solar Array Project is a comprehensive assessment of the processes, conceptual designs, and new technologies required to achieve, by 1985, annual solar cell array production capability greater than 500 megawatts per year at a cost less than $500 per kilowatt. This goal is being approached from two directions. The first is to build a model or models of the costs involved in the various steps used to fabricate solar cell modules. These costs are being analyzed in terms of present-day capabilities and projected capabilities. Also, new technologies will be fitted to these models to determine the cost ranges for solar cell processing using new or emerging technologies. The second approach is to determine the cost goals for each of the processing steps. The program will then undertake a series of studies that are intended to point the way from exisitng and projected costs to the cost goals. This design-to-cost concept will establish allowable costs for each cell manufacture/array assembly step consistent with the 1985 cost goals.

In the first quarter, cost goals have been determined for the processing steps involved in junction formation, metallization, and antireflection coating, assuming existing technology capabilities in the semiconductor industry. Subsequent effort will be directed toward improving the accuracy of these cost estimates and extending these cost estimates to projected new technologies and new concepts. All first-quarter cost estimates are based on handling standard 7.6 centimeter round slices. As the program progresses, the impact of other shapes and sizes will be evaluated. Initial baseline cost estimates show that at present, metallization of the cell represents the most significant cost barrier using current technologies.

All of the cost-per-watt figures in this report are related to flat cells at a one-sun illumination level. The effect of concentrators would increase the power output per cell or module but would also require an extensive engineering evaluation of the overall impact of increased solar radiation. The design of the cell, module, and array would have to take into account the significant larger thermal effects.

Appendix I presents some specific definitions used throughout this task.

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SECTION II
TECHNICAL DISCUSSION

A. SCOPE

The magnitude of the 500-megawatt-per-peak power goal can be put in perspective in the following manner. At 100 watts per square meter, this represents 5 times 10^6 square meters of silicon solar cells. This might be conceived of as a 12-centimeter wide band of silicon solar cell completely encircling the earth at the equator. The existing installed worldwide capacity of the semiconductor industry can be estimated in the range of 1.4 to 2.3 times 10^5 square meters per year. Thus, the 500-kilowatts-per-year goal represents an output of silicon solar cells 20 to 35 times that of the 1976 worldwide semiconductor industry.

The $500-per-peak kilowatt cost goal at 100-watt output per square meter gives a $50 per square meter selling price for silicon solar modules. Semiconductor devices cost $4,000 to $10,000 per square meter to process, excluding yield considerations. Admittedly, semiconductor device processing is 3 to 10 times more complex than solar cell processing, but conventional semiconductor process techniques are obviously at least an order of magnitude too expensive to apply to solar cell module fabrication. A step-by-step evaluation of the processes required to fabricate a silicon solar cell module should lead to an identification of the critical cost elements at each step and point the way to the developments required to reduce these costs to levels consistent with the Automated Array Assembly Task of the Low-Cost Silicon Solar Array (LSSA) Project.

Using the design-to-cost concept, all of the elements required in the fabrication of a solar module can be assigned cost goals. Each process or technology used in the fabrication can then be compared against the cost goals assigned to that element of the module, and a solar cell module fabrication scheme can be built that utilizes elements whose costs are consistent with the program goals.

B. APPROACH

During the first quarter, a baseline process for N on P solar cells has been outlined. Initial baseline cost estimates for this process have been developed using conventional semiconductor processing techniques, equipment, and throughput rates. A few alternate processes have also been evaluated in terms of cost. The areas of poly-silicon, single-crystal silicon, and shaped silicon substrates have not been evaluated because these areas are treated specifically under other tasks in the Low-Cost Silicon Solar Array project. Inputs from these programs will be used in the future in

developing both the impact of alternate shapes on the process and on the overall cost figures. Module assembly and encapsulation costs have not been addressed in this quarter. These areas will be evaluated as more experience with module assembly is gained.

An initial design-to-cost analysis has been made to give approximate ranges for allowable costs for each element of the module assembly process. These costs will be continually reevaluated as a better understanding is developed of the costs involved on each element. These initial design-to-cost goals are very instructive in pointing out the magnitude of the task in meeting the cost goals of the LSSA Project.

C. SOLAR CELL PROCESSING

1. General

A generalized solar cell module process flow is shown in Figure 1. Starting from raw materials, polycrystalline silicon is generated, then converted into single crystal silicon; the single-crystal silicon is shaped into forms used in the solar cell manufacture. In the manufacturing process for solar cells, first a junction is formed, metallization is applied to the front and to the back of the silicon solar cell, an antireflection coating is applied to the front of the silicon cell, and then several cells are mounted on a module board and encapsulated on the board to form the module assembly. Process Control test points and final tests are conducted at various places in the process consistent with process control, costs and yield. This quarterly report will primarily treat those elements in the solar cell module flow that are enclosed within the dashed line in Figure 1. The elements in the process flow that precede the dashed line are being separately addressed by other tasks in the LSSA Project. Inputs derived from these tasks will be incorporated into later reports, under this task.

Both N on P and P on N solar cells can be fabricated using essentially identical processes. The baseline analysis carried out in this quarterly report is focused primarily on the N on P solar cell process.

2. N on P Solar Cell Process

A baseline process for fabrication on N on P solar cells has been outlined, and process has been initiated using hexagonal substrates, laser scribed from 7.6 centimeter diameter slices. This baseline solar cell process is given below.

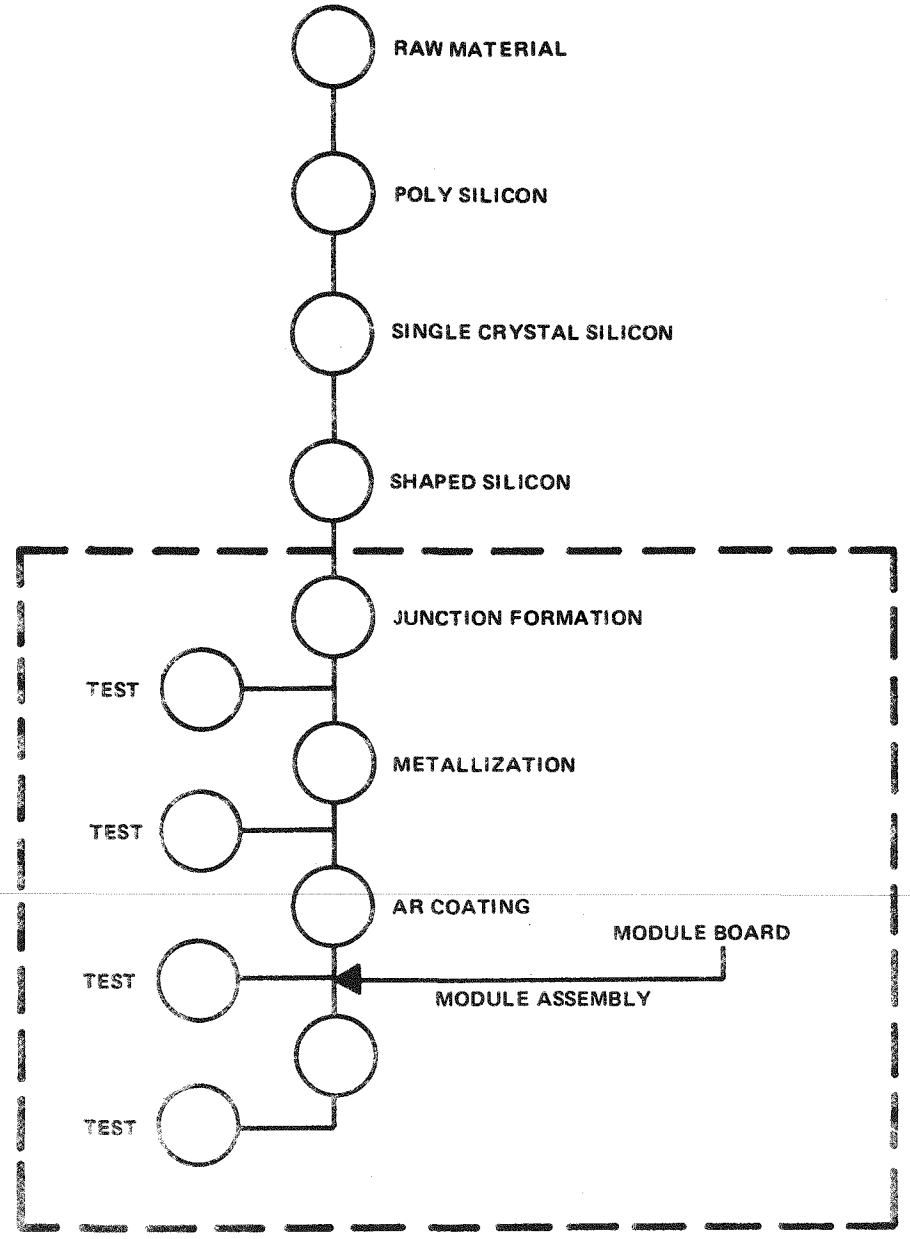


Figure 1. Generalized Solar Cell Module Process Flow

1. Substrate
   - Type: p
   - Dopant: boron
   - Resistivity: 0.8-1.2 ohm-cm
   - Orientation: (111)

2. N+ Deposition
   - Cleanup
     - Deposition
       - Temperature: 900° C (slow push, pull)
       - Source: $POCl_3$
       - Junction Depth: 0.4 μm
       - Sheet Resistivity: 50-60 ohms/square

3. Remove Backside N+
   - Coat, bake, expose frontside
   - Coat, bake, mask, expose backside
   - Develop
   - Planar etch

4. Backside Metal
   - Cleanup
   - Evaporate aluminum
   - Define metal pattern
   - Sinter
   - Evaporate titanium – copper
   - Define metal pattern
   - Anneal

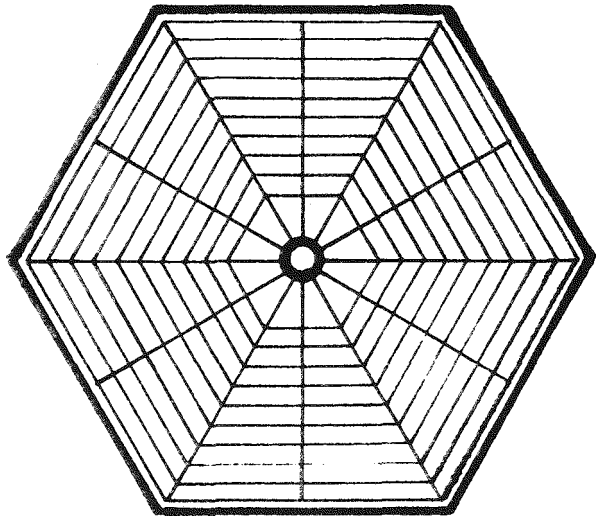
5. Frontside Metal
   - Cleanup
   - Evaporate titanium – copper
   - Define metal
   - Anneal

6. Solder Dip Cell

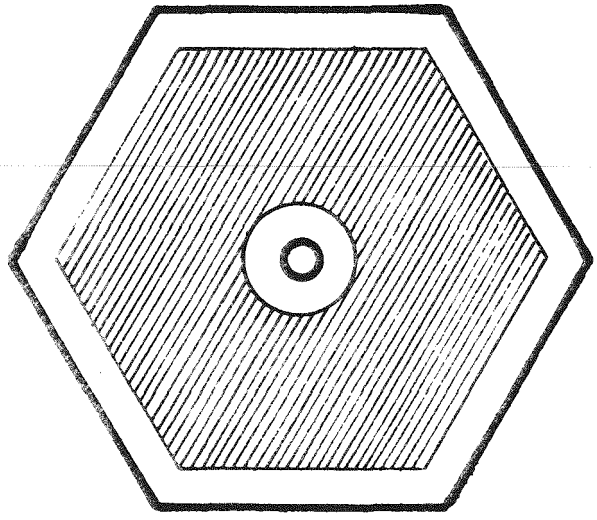
7. Cleanup

8. Antireflection Coating

Figure 2 shows the frontside and backside metallization patterns. The hexagonal cell has a center hole which is used to connect the frontside grid contacts to the printed circuit board.



FRONTSIDE GRID PATTERN



BACKSIDE METALLIZATION

Figure 2. Hexagonal Cell Metallizations

Approximately 25 slices have been processed through diffusion at this time. The processing outlined above will be used to establish baseline processing costs with which to compare alternatives. It is recognized that the process described is expensive but it is believed representative of current industry solar cell processing.

a. Junction Formation

The baseline process utilizes open-tube diffusion furnaces. Spin-on polymer dopants and ion implantation will be examined next with regard to costs and automation approaches.

b. Metallization

A survey of metallization options was begun. The primary option other than that outlined in the process is electroless nickel followed by anodic or electroless plating for subsequent solder dipping. Masks to accomplish the metallizations of Figure 2 were designed and fabricated during February. The frontside grid pattern in Figure 2 covers approximately 7% of the front surface.

c. Solder-Dip

Specific solder-dip techniques have not been outlined yet. The primary options will be solder wave processes or solder plating processes. Both techniques are currently in use in the semiconductor industry. Initial cost figures have not been developed for solder-dip procedures.

d. Antireflection Coating

Several alternate antireflection coating techniques are being considered. These include conventional evaporation techniques used on optical systems, a simplified conventional technique that would use less expensive capital equipment and a spin-on technique similar to the spin-on polymer dopant process.

3. Testing

This activity is just beginning at the end of the first quarter. A survey of published literature discussing test approaches was begun. The amount and degree of in-process testing that can and must be applied in the solar cell module process will be evaluated on a cost-return basis. Obviously, enough testing must be included to ensure adequate in-process control at all phases of the process. The overall cost goals of the program limit the amount of testing that can be incorporated. Therefore, test frequency and test complexity will be balanced against test costs as the program proceeds.

D. MODULE DESIGN STUDY

A number of factors go into the choice of a suitable standard module. This study assumes a rectangular shape for the module recognizing that an improvement could be made in module packing density with irregular shaped edges. The key factors that have been considered in the choice of an optimum size module are size, board utilization, and assembly yields. Each of these factors is recognized to be dependent upon the others.

1. Size

The size of an optimum module will be governed by several factors. Among these, are intended usage, ability to handle large flat pieces without excessive breakage or damage, and final array configuration. Very small module sizes could be inefficient in the amount of handling required while very large module sizes would be very difficult to handle in terms of assembly, breakage, shipping, and testing. For the purposes of this study, an optimum module will be on the order of 50 centimeters on the side, such that four modules could be readily assembled into a 1-square-meter array.

2. Board Utilization

The efficiency of an assembled module will be a direct function of the efficiency of the individual solar cells mounted on the module and the fractions of the module board occupied by active solar cells. This fraction is referred to as "board utilization." Board utilization will be a function both of the packing density of the individual cells on the board and the shape of the individual solar cells mounted on the board. To a first approximation, the efficiency of the board will be the product of the conversion efficiency of the individual cells times the board utilization factor.

Figure 3 is a plot of board utilization as a function of separation of the individual cells on the board. Plots are shown for square, hexagonal, and circular cells. Separation is expressed as a ratio t/D where t is the spacing between the cells at the point of closest approach and D is the major diameter for circles and hexagons or an edge for squares. Rectangles would be treated the same as squares. For cells with D greater than or equal to 7.5 centimeters, typical t over D values, would be 0.03 to 0.05. The curves shown on the graph represent the board utilization assuming close packing for each figure and for circles and hexagons, the end of each row would be occupied by a half cell. The bands shown for the circular and hexagonal shapes represent the board utilization factor as a function of the size of the array with array dimensions indicated on the graph. The upper limit of 10.5 by 10 cells is larger than the recommended 50 centimeter on-a-side board.

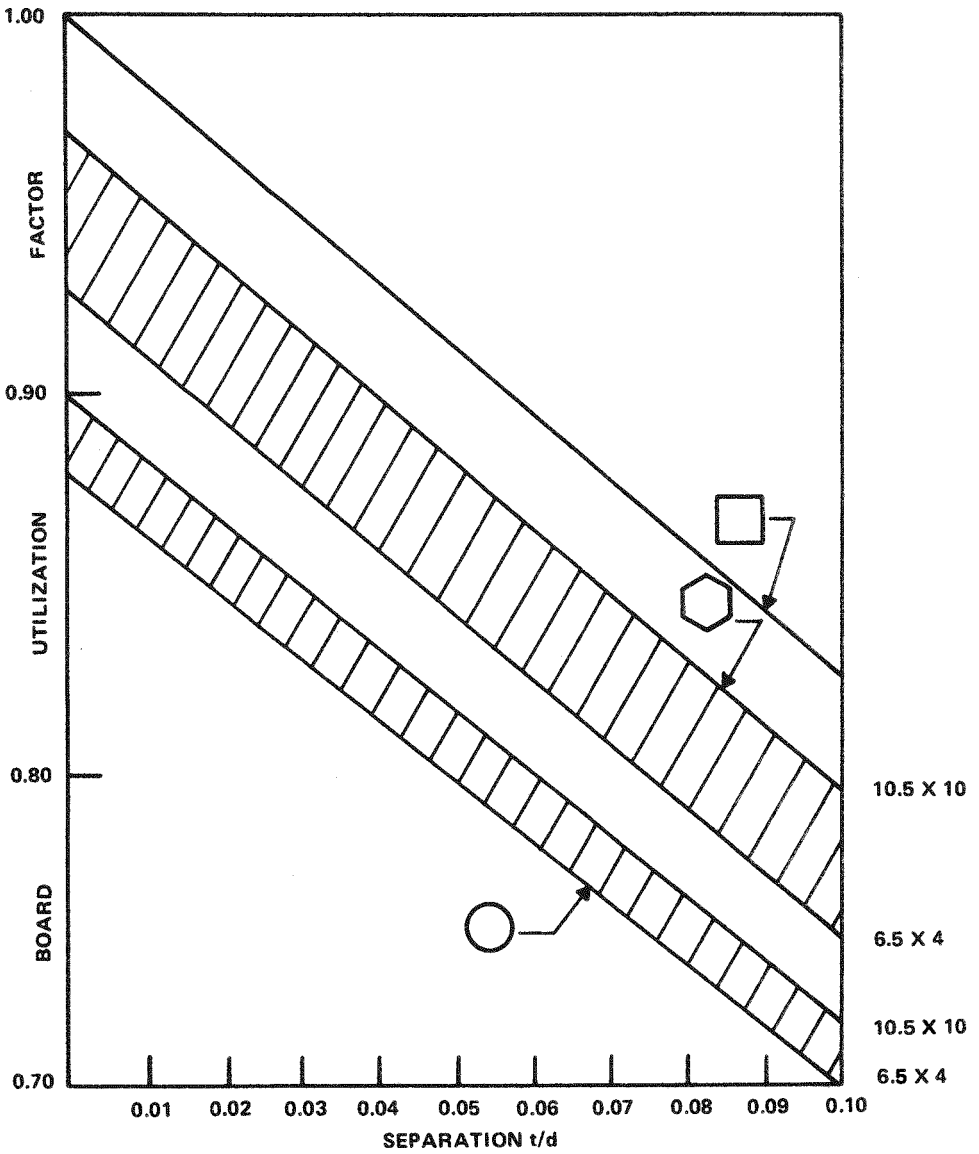


Figure 3. Board Utilization as a Function of Cell Separation

As seen in Figure 3, squares give the highest board utilization factor and circles the lowest. On this basis alone, square cells would be favored; however, other considerations, such as the cost of shaped silicon, the ease of processing different shapes, and the availability of single-crystal silicon in the various shapes could definitely change this choice. Using today's most advanced technology, circular shapes are far and away the cheapest and most readily available. If hexagons or squares were cut from circles, the loss of single-crystal material would not compensate for the better board utilization factor. The vast majority of solar cell modules available on the market today use circular silicon material.

Using the board utilization factors shown in Figure 3 to achieve a module efficiency greater than or equal to 10%, individual cells would have to have efficiencies of 12 to 14%.

3. Assembly Yield

At this point in time, a good experience history is not available to accurately define a correlation factor between good tested solar cells and the yield of assembled panels. It is obvious, however, that this correlation factor must be very high if panels of any size are to be developed. Assuming no other yield losses, the yield of good assembled modules is given by the relationship in equation (1).

$$(CF)^N = Y_M \tag{1}$$

where

CF = correlation factor

N = number of solar cells on module

Y_M = module yield

Using equation (1), if the correlation factor is 99%, that is, if 99% of the good tested solar cells are still good after module assembly, a module containing 40 cells will have a final test yield of 67%. This is obviously unacceptable from a cost and production viewpoint. This same 40-cell module with a correlation factor of 99.9% would have a module yield of 96%. The importance of this correlation factor in determining module yield will dictate, to a large extent, the amount of testing that must be done at the finished cell level to ensure a very high correlation factor.

Many other factors will affect module assembly yield. Among these are methods of attachment of the cell to the module board, contact systems to the front and back surfaces of the solar cell, encapsulation, and mechanical handling of the cells and the module boards.

4. Module Design

The cell module depicted in Figure 4 was designed. This module utilizes the 7.6-centimeter hexagonal cells being fabricated under the cell design activity. The 24 cells per module should produce 10 watts at a voltage up to 14 volts. Based on the external board dimensions, this wattage would represent 76 watts per square meter. However, this power density is only 8% efficient from a total area basis. To meet the 10% efficiency goal, both cell efficiency must be improved and the board utilization factor must be increased. In the case of the hexagonal cell module, as in Figure 4, packing density can be improved through reducing the board over-hangs and by placing half cells at the end of each row.

Figure 5 shows the circuit board metallization pattern for the 10-watt module. The large copper donuts will contact the backside cell metallization in Figure 2. The cell frontside grid pattern will be connected through the circuit board to broad copper stripes on the backside of the circuit board. These stripes are shown by dashed lines in Figure 5. Each horizontal row of six cells in Figure 4 is connected in series. Either circular or hexagonal cells can be attached to the board. The backside-to-frontside grid metallization connection stud can be brought through the board at any location from the center of the solar cell to the outside edge of the solar cell, depending upon the placement of the copper stud.

For the first few modules, the solar cells will be attached to the circuit board with conductive epoxy. Cost and ease of assembly point to furnace soldering as the best assembly approach, but experience in soldering large silicon devices indicates a high probability of cell breakage for the 7.6-centimeter cells. Experiments will be conducted later in this program on soldering the cells to the circuit board. The circuit board artwork is complete, and work is in progress on circuit board fabrication. Standard G-10, 0.16-centimeter thick metallized circuit board material will be used in these modules. It is anticipated that the first modules will be assembled early in the second quarter.

A number of cost obstacles are apparent. For instance, G-10 circuit board runs about $10 per square meter at present, and typical encapsulation plastics will run about $10 to $13 per square meter, which indicates the total cost on the order of $0.23 per watt for packaging in the module. Obviously, this cost is too high and innovative approaches are required to achieve a reasonable cost to package the cells.

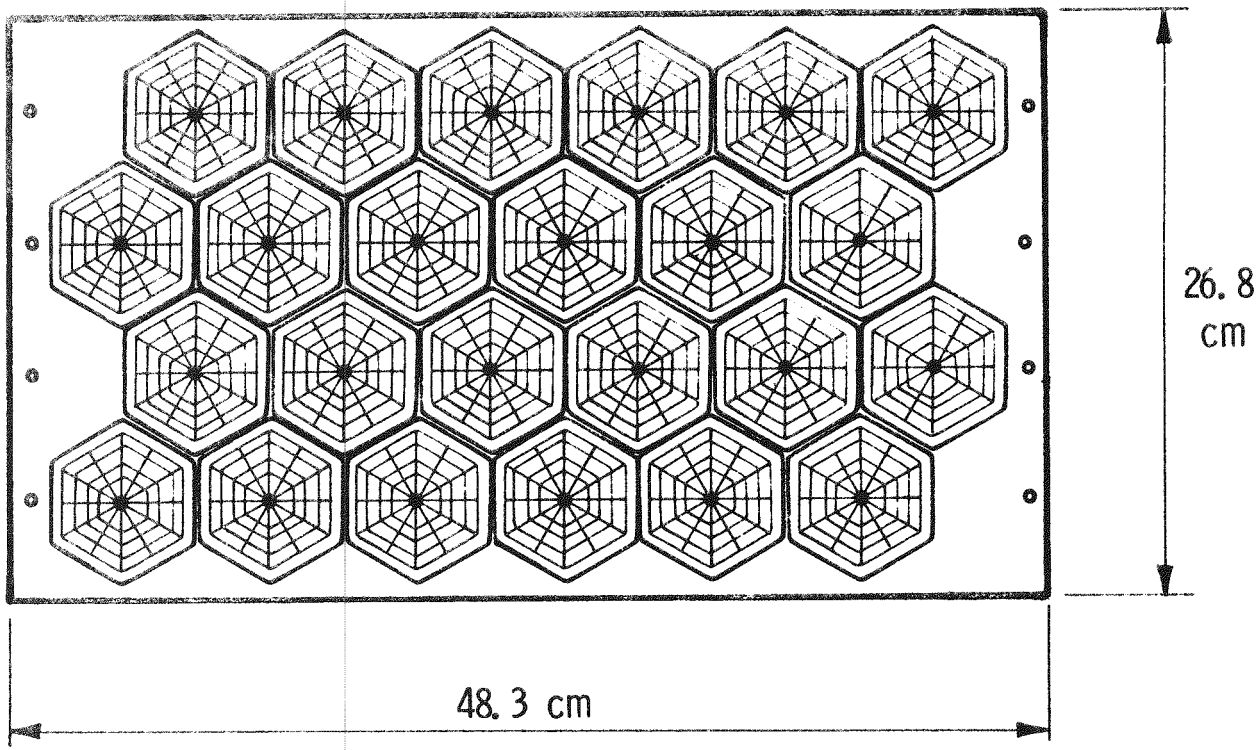


Figure 4. Ten-Watt Solar Cell Module

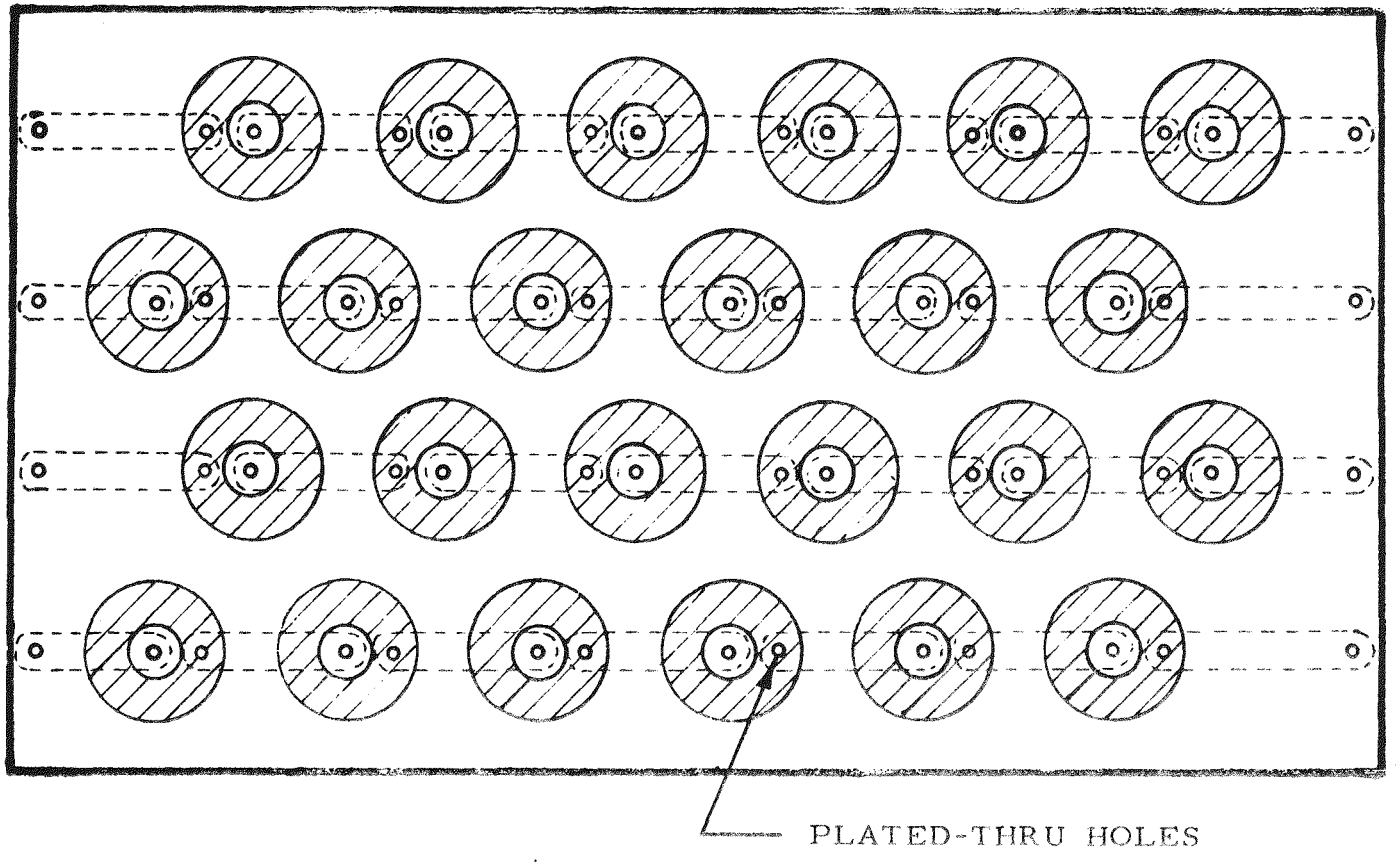


Figure 5. Ten-Watt Module Circuit Board Metallization

E. ECONOMIC EVALUATION

The baseline cost figures have been developed for standard solar cell processing technologies that are existent in the industry today. These baseline cost figures are intended to show manufacturing cost ranges for high-volume operations and are not intended as definitive cost figures in the industry today.

1. Assumptions

Baseline cost estimates were made assuming standard labor rates; defined overhead rates; a defined work year; a defined equipment utilization factor, which allows for maintenance, repair and normal down time; consumed material costs; and 7-year straight-line depreciation on all identified capital equipment. Figure 6 gives the values of these factors that were used in the following baseline cost calculations. No allowances were made for processing yield either at individual steps or accumulative through the full process; instead, these figures are intended to be used to compare various progress alternates in a first approximation. From this comparison, process alternates can be ranked in order of the more promising alternates, and those which have excessive material, labor or depreciation costs.

LABOR RATE:	$3.50/HOUR
OVERHEAD RATE:	50% OF LABOR
WORK YEAR:	24 HOURS/DAY 5 DAYS/WEEK 50 WEEKS/YEAR
EQUIPMENT UTILIZATION:	80%
MATERIAL:	ALL MATERIAL CONSUMED IN OPERATION WITH NO RECOVERY
DEPRECIATION:	7 YEAR STRAIGHT LINE NO ALLOWANCE FOR INTEREST

Figure 6. Base Line Cost Estimate Assumptions

2. Baseline Costs

Baseline cost estimates were made for several junction formation, metallization, and antireflection coating techniques. Throughput rates are those claimed for standard manufacturing equipment in the semiconductor industry. For these calculations, no assumptions of innovative automation or innovative processing were taken into account. Material costs, in general, assume semiconductor-grade materials and no allowance has been made for recovery of spent solvent or metals. Costs have been calculated for 7.6-centimeter round cells because most of the equipment available today in the semiconductor industry is built to accommodate this physical shape and size. A 7.6-centimeter round cell at 10% efficiency should produce approximately 1/2-watt power. It is not intended that these numbers could be scaled directly to give a cost per watt, but rather that these numbers are used to compare processes. Appendix II gives the details of the labor and depreciation costs.

From an inspection of Figure 7, in the area of junction formation, it is apparent that polymer doping is the most cost-effective method of forming a junction and conventional open-tube diffusion is the least cost effective. The polymer doping process is also the least capital intensive while the ion implant process is the most capital intensive. The open-tube diffusion process is also the most material intensive of the three. This is a by-product of the fact that open-tube diffusion forms a junction on both sides of the slice simultaneously, and the backside junction must subsequently be removed.

While none of the junction formation technologies shown in Figure 7 would meet the cost goals of the LSSA Project, none of the above technologies presents an insurmountable barrier. Automation techniques and innovative changes in these processes could reduce the cost per unit silicon substrate, probably by a factor of 10 or more.

Conventional metallization approaches, as represented by the process shown in Figure 7, present an apparently insurmountable cost barrier. Material and labor are both excessive and do not appear to be capable of being reduced to acceptable levels using conventional subtractive metallization methods. A more detailed breakdown of the metallization costs by discrete operation is shown in Figure 7. From this, it can be seen that the cost per any one element such as aluminum backside deposition is not excessive, but the complexity of the overall operation, requiring deposition and removal of aluminum followed by deposition of titanium copper and removal of titanium copper from both the front and the back, builds up an unacceptable cost structure. From this, it can be concluded that subtractive metal processing, that is, deposition of the metal, followed by a photoresist patterning and etching operation will not be cost effective for solar cells.

	M	L	O	MLO	Depr.	Total	
Junction Formation							
Open Tube	0.27	0.101	0.051	0.422	0.0153	0.4373	
Ion Implant	0.0639	0.1074	0.0538	0.2251	0.0693	0.2944	
Polymer Doping	0.0540	0.0519	0.0260	0.1319	0.0101	0.1420	
Metallization							
Al-back, Ti-Cu Front and Back	0.239	1.344	0.673	2.256			
Al-backside-dep.	0.010	0.140	0.070	0.220			
Al-removal	0.073	0.175	0.088	0.336			
Ti-Cu dep/side	0.005	0.213	0.107	0.325			
Ti-Cu removal/side	0.073	0.301	0.151	0.525			
PIMDEP	0.0176	0.0538	0.0269	0.0983	0.0784	0.1767	
AR Coating							
Conventional Evaporation	0.050	0.048	0.024	0.122	0.082	0.204	
Conventional-Simple	0.050	0.024	0.012	0.086	0.012	0.098	
Spin-On	0.005	0.0066	0.0033	0.0149	0.0019	0.0168	

Figure 7. Base Line Solar Cell Processing Costs

As an alternate to subtractive processing, one must consider the various additive methods of metallization, that is, methods whereby the metal is only deposited in the desired location and no excess metal is applied. Various methods of additive metallization are known in the industry. Among these are: electroless nickel and copper plating, electrolytic plating upon sensitized surfaces, screen printing, and finally, photo-impeded-metal-deposition (PIMDEP). As an example, a preliminary baseline cost estimate for the PIMDEP process is shown in Figure 7. This process utilizes electroless nickel plating and electroless copper plating. Significant development activity would have to be carried out to make this PIMDEP process useful for solar cell fabrication.

Three potential processes for antireflection coating have been considered, conventional evaporation, as practiced in the optical coating industry, a simplified version of conventional evaporation, using less complicated and expensive evaporators and a spin-on technique using silicon containing polymers. From an inspection of Figure 7, it is apparent that the spin-on technique is by far the most favorable. It is not known at this time, however, how well a spin-on technique could be controlled in terms of both of refractive index and thickness. However, with the cost advantage that appears to be available from these baseline calculations, one might trade off efficiency of the antireflection coating against cost with this large a cost advantage. Further experimentation in this area must be carried out before a clear decision can be made.

From this baseline cost estimate, one could project that in large volume, 7.6-centimeter round solar cells could be manufactured at a processing cost for open-tube diffusion, aluminum/titanium-copper metallization and conventional evaporation AR coating for a minimum of approximately $2.80 a slice, excluding the cost of the shaped silicon substrate and the cost of the module assembly and testing. Note that these figures do not include any allowances for yield losses or for profit. The challenge, therefore, is to reduce these costs by approximately two orders of magnitude.

3. Design to Cost

The design-to-cost concept starts by determining a selling price that the marketplace will accept. From this selling price, individual process elements are assigned fractions of this final cost goal. One should keep in mind that the selling price must include a reasonable level of profit to allow industry to participate in the business and must also include accumulated yield factors through the whole process. Testing costs must be included in the cost of each element of the process.

Figure 8 gives a first estimate of the design-to-cost goals for the various process elements that make up a solar cell module. These goals are the part of the final selling price, not the cost of each processing element. Obviously, if one element of the overall process can be achieved at a cost lower

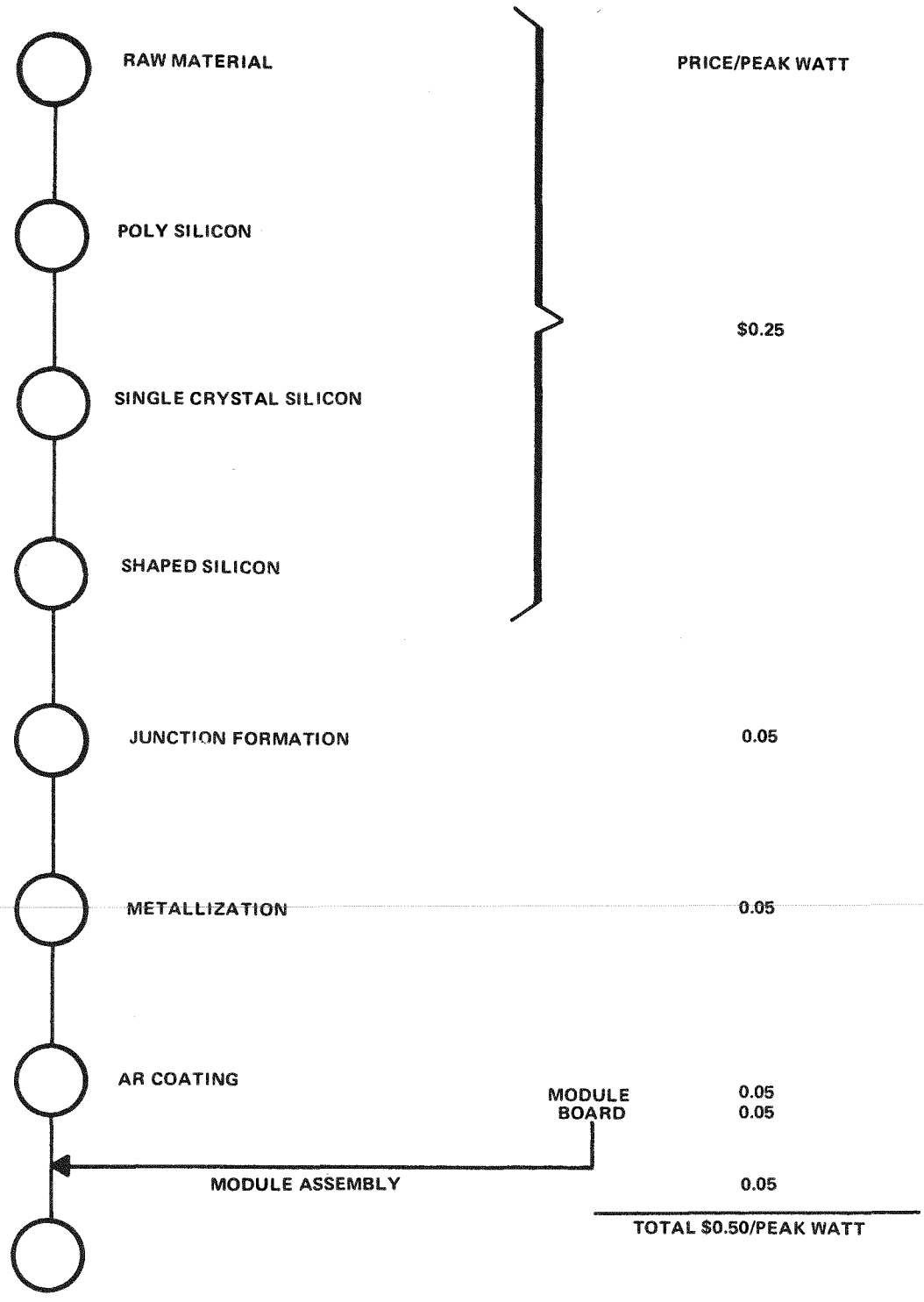


Figure 8. Design-to-Cost Goals

than the assigned cost goal, the extra cost can be allocated among the other elements in the overall process. The total cost goal of $0.50-per-peak-watt is the goal of the LSSA Project.

The cost-per-watt as a function of year is shown in Figure 9. The key to this figure is the overall height of the bar at each year, not the size of the individual components within the bar. It must be clearly understood that the success or failure of the program will be measured in the dollars-per-watt selling price of solar cell modules, not in the cost incurred for the individual elements that go into the module. It must also be understood that the intermediate goals shown for the years 1977 and 1979 must be measured in terms of the dollars-per-watt at a module level only.

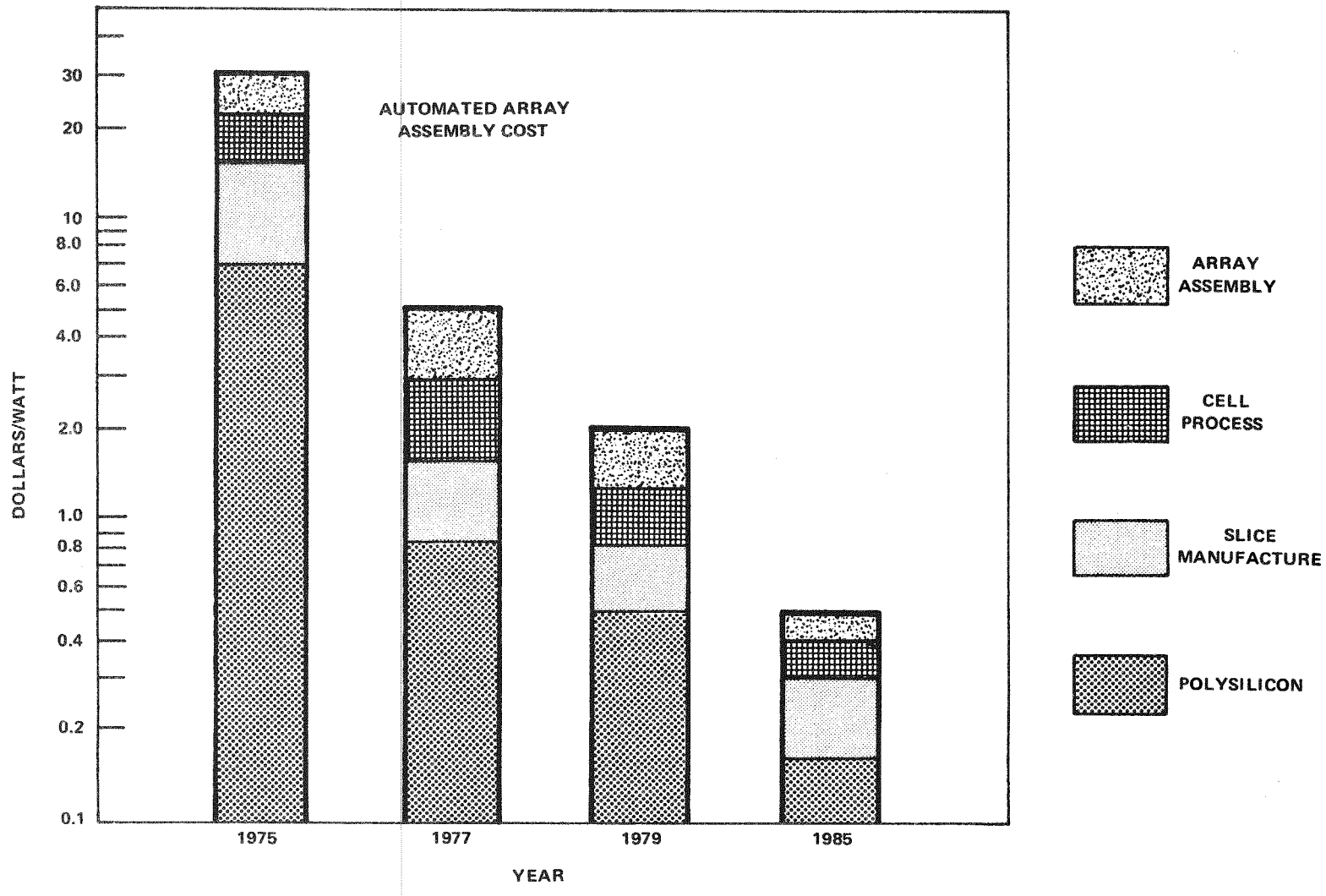


Figure 9. Cost Elements in LSSD Project Cost Goals

SECTION III
CONCLUSIONS

The key to successful execution of the Low-Cost Silicon Solar Array Project is the attainment of the $500-per-peak-kilowatt load cost. This goal can only be met by successfully integrating all of the elements required to fabricate the solar cell modules in a cost-effective manner. Progress must be measured on an overall module cost basis from year to year.

A baseline cost estimate from the process elements involved in solar cell fabrication has shown that none of the existing semiconductor techniques presently in use in solar cell manufacture will meet the required design-to-cost goals. The most formidable cost barrier is the one at metallization. Other elements in the solar cell processing area are within an order of magnitude of meeting design-to-cost goals.

In general, it can be concluded that all processes should be additive toward the final goal of module assembly. Little or no cost can be incurred in subtractive processes such as metal deposition followed by metal removal.

It is obvious that baseline cost projections, while useful in pointing the direction for future development, do not in themselves answer all of the technical questions involved in the manufacture of solar cells. The lowest cost process in terms of silicon area processed may not be the most cost effective in terms of dollars per peak watt.

SECTION IV
RECOMMENDATIONS

The Automated Array Assembly task will continue to refine baseline cost projections for the most promising cost-effective process elements. The impact of automation will be assessed in terms of material, labor, overhead, and depreciation costs.

As cost data is available from the other tasks in the LSSA Project, the overall impact of this cost data in terms of design-to-cost goals must be measured. All projected cost figures from the various tasks in the project should be on a time scale that is compatible with the 1985 large volume production goals. Wherever possible, technical risk factors should also be included.

SECTION V
NEW TECHNOLOGY

No new technology has been developed under this task during this quarter.

SECTION VI
PROGRESS SUMMARY

The progress on each of the activities in this task is shown in Figure 10. The overall task is on schedule.

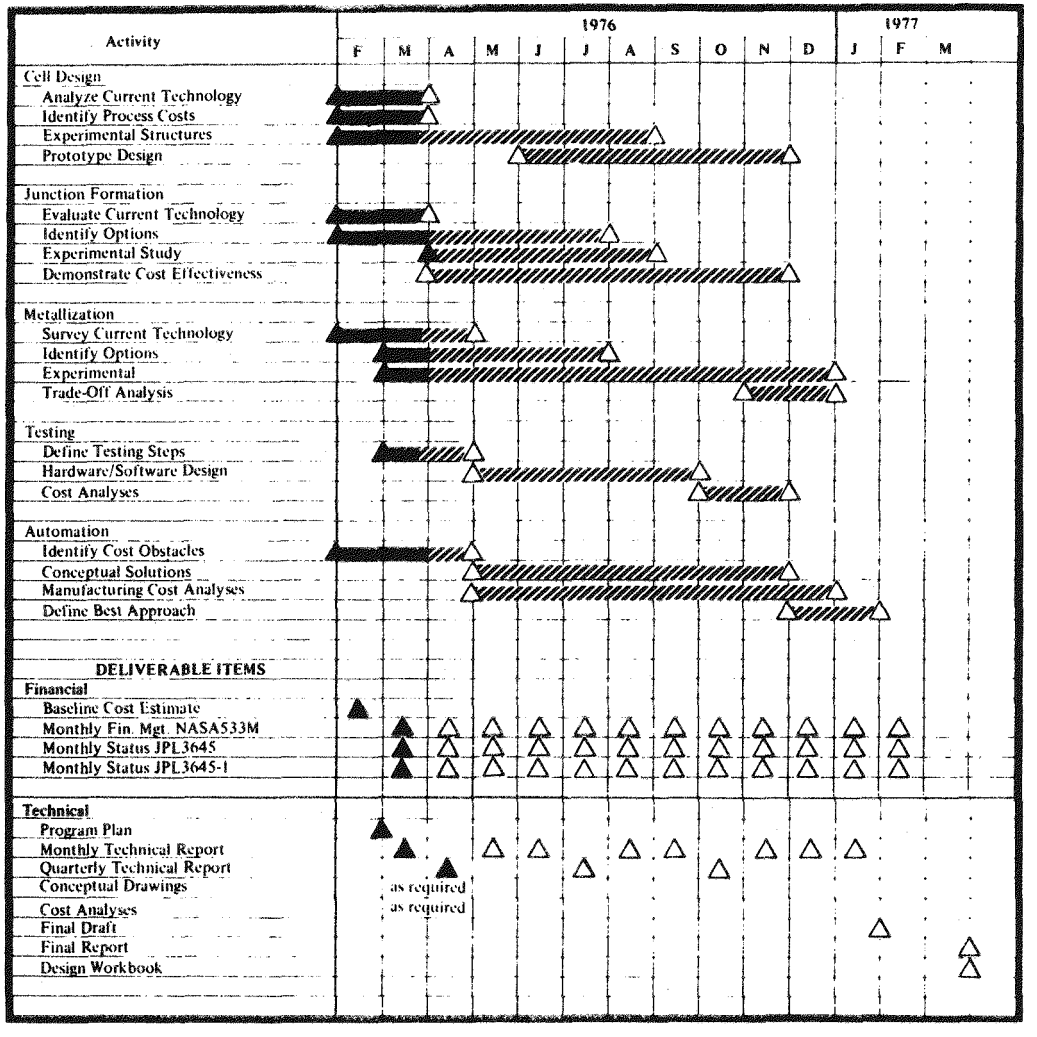


Figure 10. Activity Milestone Chart

APPENDIX I
SPECIFIC DEFINITIONS

In all reports on this task the following definitions will be used:

Cell – a single silicon photovoltaic device that may be assembled into a larger module.

Module – the smallest collection of cells assembled into a unit that is encapsulated.

Panel – a collection of modules that functions as a unit.

Array – a power generating system made up of panels or modules.

APPENDIX II
LABOR AND DEPRECIATION COSTS

The labor cost per 7.6-centimeter cell [equation (3)] was calculated from machine or equipment annual throughput rates assuming a utilization factor of 80% [equation (1)], operator hours/year [equation (2)] and operator pay rate.

$$\text{Annual Throughput/Machine} = \text{(Machine throughput/hour) (24 hours/day) X (5 days/week) (50 weeks/yr) (0.80)} \quad (1)$$

$$\text{Operator hours/year} = \text{(Number of operators/machine) (24 hours/day) X (5 days/week) (50 weeks/yr)} \quad (2)$$

$$\text{Labor Cost/7.6-cm cell} = \frac{\text{(Operator hours/year) (Operator pay/hour)}}{\text{(Annual throughput/machine)}} \quad (3)$$

This assumes a standard 5-day week, three shift operation. The utilization factor allows for holidays, machine failure, and repair and maintenance. Machine throughput rates for 7.6-centimeter round cells were used, since the standard wafer size in the semiconductor industry is 7.6-centimeter.

Depreciation was calculated using initial cost of the equipment divided by seven times (7-year life)the annual throughput/machine [equation (4)] with no allowance for interest on the intial cost.

$$\text{Depreciation/7.6-cm cell} = \frac{\text{Initial Capital Cost}}{\text{7 X Annual Throughput/Machine}} \quad (4)$$

Depreciation over 7 years at 9% interest on the declining balance would be increased by a factor of 1.391 over the no-interest value.