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AUTOMATED ARRAY ASSEMBLY TASK
PHASE I

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The JPL Low-Cost Silicon Solar Array Project is funded by ERDA and forms part of the ERDA Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays.

ABSTRACT

Work during this quarter consisted of preparing design-to-cost goals for each element of the solar cell module fabrication; testing process technologies and forecasted process capabilities against the design-to-goal goals; ranking competing process technologies where enough data is present; fabricating sample solar cells to test process feasibility; initiating device characterization and modeling efforts; and using the device characterization-modeling data to point the way toward improved solar cell characteristics. Design-to-cost concepts are used to model an idealized solar cell factory.

In the area of junction formation, simultaneous N^+-P^+ diffusion from polymer dopant sources appears to be the best choice for low-cost fabrication. In the area of metallization, a clear choice cannot be made. Significant cost reduction could be made in the short-term by using continuous vacuum deposition techniques if a large enough market were available to warrant the use of high throughput machines. The lowest cost metallization option is screen printing of base metals but technical feasibility has not been demonstrated. Module substrates and encapsulation present a formidable cost barrier in solar cell module fabrication.

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SECTION I
INTRODUCTION

The overall goal of the Array Automated Assembly Task, Phase I, of the Low-Cost Silicon Solar Array Project is a comprehensive assessment of the processes, conceptual designs, and new technologies required to achieve, by 1985, annual solar cell array production capability greater than 500 megawatts per year at a cost less than $500 per kilowatt. This goal is being approached from two directions. The first is to build a model or models of the costs involved in the various steps used to fabricate solar cell modules. These costs are being analyzed in terms of present-day capabilities and projected capabilities. Also, new technologies will be fitted to these models to determine the cost ranges for solar cell processing using new or emerging technologies. The second approach is to determine the cost goals for each of the processing steps. The program will then undertake a series of studies that are intended to point the way from existing and projected costs to the cost goals. This design-to-cost concept will establish allowable costs for each cell manufacture/array assembly step consistent with the 1985 cost goals.

During the second quarter, design-to-cost goals have been assigned to each process element in the solar cell module fabrication process. An initial model description of a solar cell module factory was introduced. Junction formation and metallization technologies were evaluated and the direction of further effort in these areas was identified. Device characterization and modeling was introduced as a tool to direct improvements in solar cell processing.

All of the cost-per-watt figures in this report are related to flat cells at a one-sun illumination level. The effect of concentrators would increase the power output per cell or module but would also require an extensive engineering evaluation of the overall impact of increased solar radiation. The design of the cell, module, and array would have to take into account the significant larger thermal effects.

SECTION II
TECHNICAL DISCUSSION

A. SCOPE

The goal of the LSSA project is to reach a $500 per peak kilowatt cost at a volume of 500 megawatts per year by 1985. The present cost of solar cell modules is in the neighborhood of $20 per peak watt. This 40X cost reduction is to be achieved by across-the-board cost reductions in all areas of solar cell module fabrication.

The specific areas of interest in this task are to point the direction to appropriate cost reductions in solar cell fabrication, module assembly and encapsulation. Tasks 1 and 2 of the LSSA project are directed toward producing low-cost solar-grade polysilicon and low-cost silicon sheet respectively. Cost goals for these areas are included in this study.

Using the design-to-cost concept, all of the elements required in the fabrication of a solar photovoltaic module can be assigned cost goals. Each process or technology used in the fabrication can then be compared against the cost goals assigned to that element of the module fabrication, and a solar cell module fabrication scheme can be assembled that utilizes elements whose costs are consistent with the project goals.

B. APPROACH

During this quarter, design-to-cost goals have been refined and cost goals have been assigned to each process element in the fabrication of solar cell modules. Junction formation technologies have been evaluated and ranked in terms of projected costs and technical feasibility. Metallization technologies have been evaluated but a ranking is premature.

Device characterization and modeling has been introduced as a tool to point the way toward improved solar cell processing and as a guide to testing.

The areas of polysilicon, single crystal silicon, and shaped silicon substrates have not been addressed because these areas are treated specifically under other tasks in the LSSA project. Inputs from these tasks will be used in the future as data becomes available.

C. DESIGN-TO-COST CONCEPT

One of the key uses of the design-to-cost concept is to allocate portions of the total cost to the various process elements so that each process element can be tested against its individual cost goal. In this fashion, key cost barriers can be identified for individual consideration. This evaluation then points the way to the required technical innovation for cost reduction.

The allocation of the total cost to the individual process elements is not an exact science and must be weighed by known factors and engineering judgment. The cost allocations for solar cell module fabrication used in this analysis were arrived at in this fashion. Since solar cell manufacture is a material intensive process, up to 50% of the total cost is allocated to silicon sheet fabrication. Junction formation, metallization, and antireflection (AR) coating are each allocated 10% of the total cost. Module substrate, assembly, and encapsulation are allocated 20% of the total cost. Testing costs must be included with the process element where testing is used and does not represent a separate cost element in this analysis.

The cost goal of the LSSA project is \$500/kW peak power in 1985. An intermediate goal of \$2000/kW peak power can be assigned to the 1980-81 time period.

Manufacturing costs for solar cell modules are a function of the number of units and the area of modules processed and can be related to a cost per watt as shown in equation (1)

$$\text{cost/meter}^2 = (\text{cost/watt})\,(\text{solar flux})\,(\text{conversion efficiency}) \qquad (1)$$

where conversion efficiency = η_M = conversion efficiency of the module. The cost/watt is the project goal of \$500/watt and the solar flux at the earth's surface is taken as 1.00 kW/m^2. Figure 1 is a plot of cost/meter^2 versus conversion efficiency. The left ordinate is scaled to a cost/watt goal of \$500/watt and the right ordinate is scaled to the intermediate cost/watt goal of \$2000/watt.

The allowed cost/meter^2 can be readily read for any given module efficiency, e.g., at $\eta_M = 0.10$ cost/meter^2 = \$50 in 1985. Using the above allocated percentages of the total cost, the data in Table 1 is obtained.

The cost of the solar cell manufacture is related to module cost allocation by using the board utilization factor shown graphically in Figure 2. Using a utilization factor of 0.85 for circles or hexagons, the process element costs for cell manufacture given in Table 2 are obtained. The process element costs are for solar cells with a cell efficiency (η) of 11.8% obtained by dividing the module efficiency by the board utilization as in equation (2)

$$\eta = \frac{\eta_M}{\text{B.U.}} \qquad (2)$$

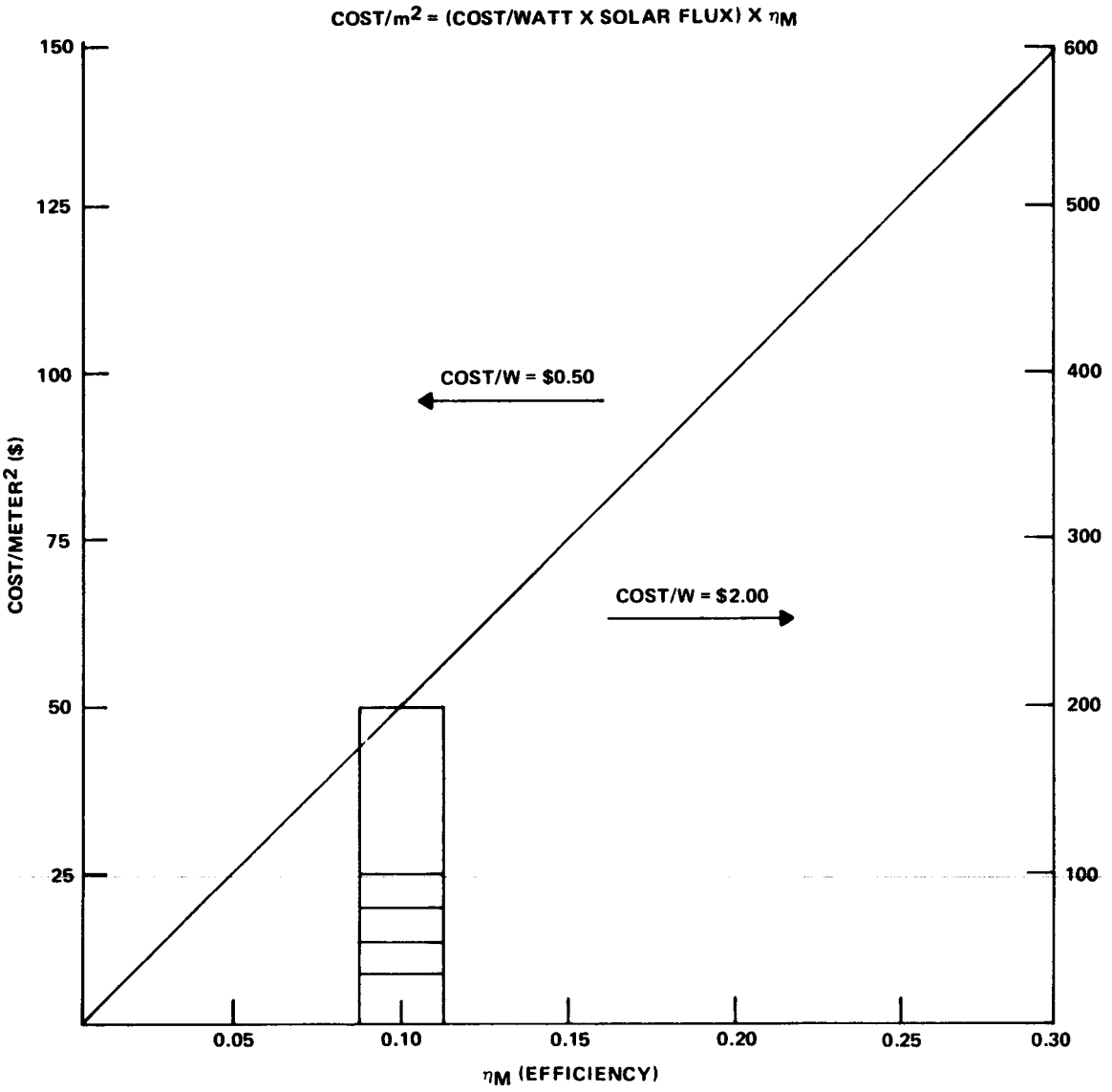

Figure 1. Cost/Unit Area versus Module Efficiency

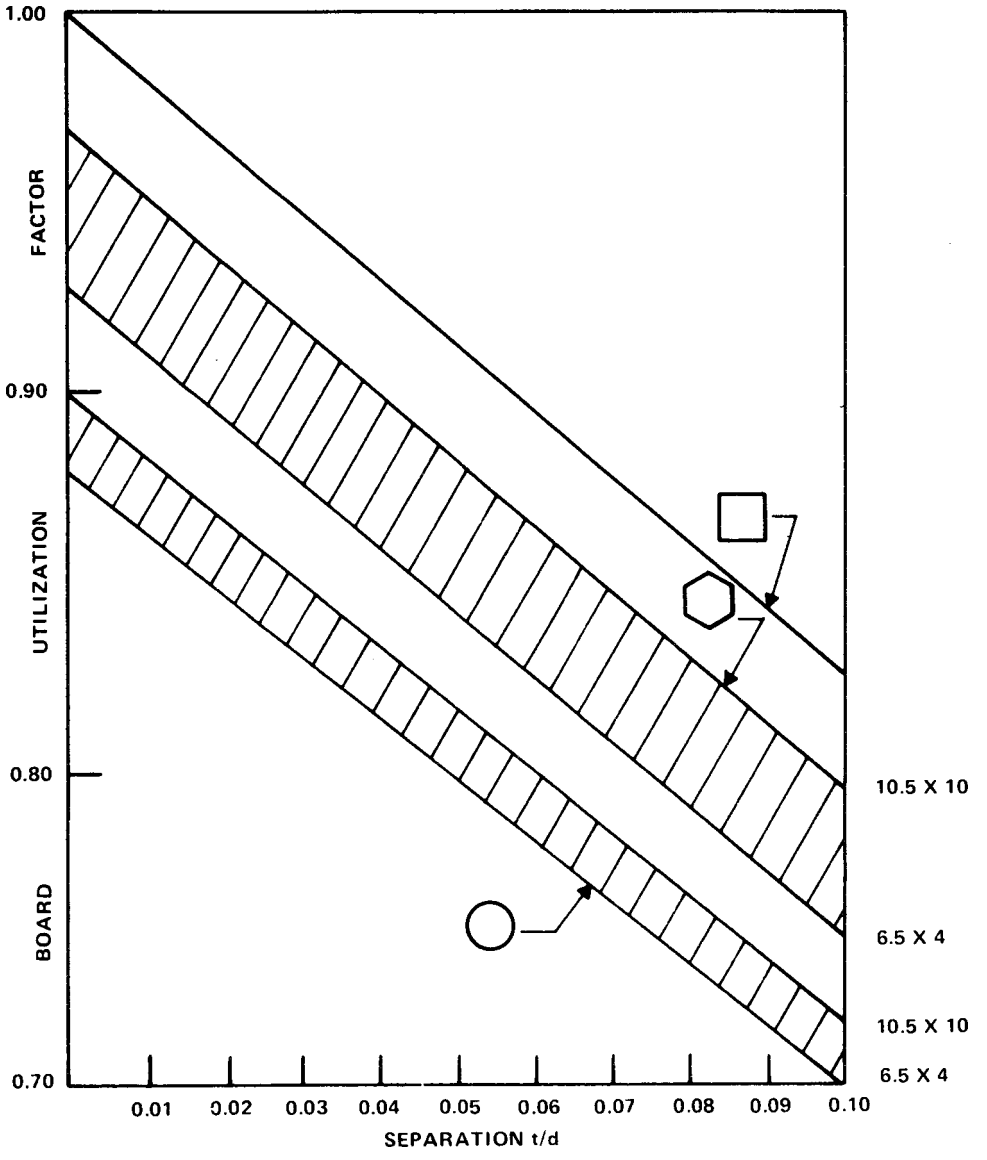

Figure 2. Board Utilization as a Function of Cell Separation

Table 1. Design-To-Cost Allocation
Cost/Meter^2 (module)

Si sheet	$25
Junction formation	$ 5
Metallization	$ 5
AR coating	$ 5
Module assembly and encapsulation	$10
Total	$50

Solar cell efficiencies greater than 11.8% would allow corresponding larger cost/meter allocations than those shown in Tables 1 and 2. Single crystal silicon solar cell efficiencies of 15% to 18% in the early 1980s appear to be a reasonable extrapolation from existing technology. Using board utilization of 0.85, this gives an allowable module manufacturing cost per square meter of $64 to $76 to meet the 1985 cost goal of $500/watt peak power.

This analysis can now be used to assess the compatibility of various approaches for each of the module fabrication process elements to the overall cost goal and initial technical confidence (or risk) factors can be assigned. For example the Si sheet cost goal of $29.41/m^2 for a 10% efficient module compares favorably with the $30/m^2 projection for a semicontinuous Czochralski process.[1] A cell efficiency of 11.8% should be readily achieved leading to a high confidence factor (0.9) that this Si sheet process is compatible with the overall module goal. Other Si sheet processes that had comparable cost projections but lower confidence factors would be higher risk options.

This analysis can also be used to define some limiting criteria (keeping in mind the assumptions included in the analysis). Each process element has a lower limiting value that is finite at any point in time. If it is assumed that the allocated costs for junction formation, metallization, AR coating, and module assembly and encapsulation shown in Table 1 are at the limiting value for 1985, then the cost of the Si sheet is the only cost that varies with module efficiency. Inspection of Figure 1 shows that at $\eta_M = 0.05$, the allowed cost allocation for Si sheet is zero. Therefore, Si sheet processes that inherently yield modules of less than 5% efficiency are unacceptable, and for module efficiencies greater than 5%, a cost allowance derived from Figure 1 must be met, e.g., at $\eta_M = 0.08$, the allowed cost for Si sheet = $15/m^2 (module) or with a board utilization of 0.85, allowed cost for Si sheet = $17.65/m^2 (cell).

Another trend that can be derived from this analysis is that cost per area is a function of module efficiency, therefore higher conversion efficiency processes allow higher cost processing. For example, a solar cell fabrication process that yields a value for $\eta = 0.18$ at a board utilization of 0.85 gives $\eta_M = 0.18 \times 0.85 = 0.153$, this gives an allowable module fabrication cost of $76.50.

1. Samuel N. Rea, *Large Area Czochralski Silicon* (Dallas, Texas: Texas Instruments Incorporated) JPL Contract 954475, Quarterly Technical Report (June 1976), ERDA/JPL-954475-76/1.

Table 2. Design-To-Cost Goals for Solar Cell Manufacture
Cost/Meter^2 (cell)

Si sheet	$29.41
Junction formation	5.88
Metallization	5.88
AR coating	5.88
Total	$47.05

In summary, the analysis of module efficiency (η_M), cell efficiency (η), board utilization, cost per watt and allowable cost per unit area allow one to test each of the module fabrication process elements, prioritize various options for each process element, and evaluate overall module fabrication processes. As more data and projections become available, optimum processes can be identified.

D. LABOR AND CAPITAL COST MODELING

Direct labor and capital cost for any operation can be calculated from the following parameters:

Operator Hours/Year = OHPY = (work hours/day) (work days/week) (work weeks/year)

Annual Throughput/Machine = ATPM = (machine throughput/hour) (work hours/day) (work days/week) X (work weeks/year) (utilization factor)

$$\text{Annual Capital Recovery} = \text{ACR} = (\text{capital cost})(\text{interest rate}) \times \left[1 + \frac{1}{(1+R)^N - 1}\right]$$

where

R = interest rate

N = number of years

$$\text{Capital Recovery Factor} = \text{CRF} = (\text{interest rate}) \left[1 + \frac{1}{(I+R)^N - 1}\right]$$

Solar cells will be manufactured in units that will then be assembled into modules. The labor cost per unit (cell), for direct labor, is given in equation (3).

$$\text{Labor Cost/Unit} = \text{LCPU} = \frac{\text{OHPY}}{\text{ATPM}} \times (\text{operator pay/hour}) \times \text{OPM} \qquad (3)$$

where

OPM = (number of operators/machine)

Labor cost per unit is independent of the number of hours worked per year.

Depreciation cost per unit is given in equation (4).

$$\text{Depreciation Cost/Unit} = \text{DCPU} = \frac{\text{ACR}}{\text{ATPM}} \tag{4}$$

Combining equations (3) and (4), an allowable capital cost as a function of DCPU and LCPU [equation (5)] can be derived:

$$\text{Capital Cost} = \text{CC} = \frac{\text{DCPU}}{\text{LCPU}} \text{ X } \frac{\text{OHPY X OPPH}}{\text{CRF}} \text{ X OPM} \tag{5}$$

where OPPH = operator pay/ hour.

CRF, OHPY, and operator pay/hour are definable terms that can be evaluated as follows:

CRF (7 yr life, 9% interest) = 0.1987/year

OHPY = (24 hour/day) (7 day/week) (50 week/year)

= 8400 hour/year

Operator pay/hour = $3.50/hour

Then:

$$\text{Capital Cost} = 147962 \text{ X } \frac{\text{DCPU}}{\text{LCPU}} \text{ X OPM}$$

or

$$\text{Capital Cost/OPM} = 147962 \text{ X } \frac{\text{DCPU}}{\text{LCPU}} \tag{6}$$

Using these relationships and the design-to-cost goals in Table 2, a set of boundary conditions for a solar cell factory that meets the $500/kW peak power goal can be described.

OPM can be defined as the equipment run by one operator, i.e., OPM = 1, and one square meter of solar cells, independent of the shape or size of the individual cells, is a unit and the utilization factor is 0.80 (allowing 20% of the time for equipment down time, R&M, etc.) (Table 3).

Table 3. ATPM and LCPU as a Function of Machine Throughput/Hour

Machine Throughput/Hour m^2/hour	ATPM m^2/year	LCPU $/$m^2$
1.00	6,720	4.375
2.00	13,440	2.188
3.00	20,160	1.458
4.00	26,880	1.094
5.00	33,660	0.875
6.00	40,320	0.729
7.00	47,040	0.625
8.00	53,760	0.547
9.00	60,480	0.486
10.00	67,200	0.4375

The cost associated with processing one unit is the sum of material, labor, overhead, and depreciation in equation (7).

$$CPU = MPU + LCPU + OH + DCPU \tag{7}$$

where

CPU = cost per unit

MPU = material consumed per unit

OH = overhead associated with LCPU

If OH = LCPU, where 50% of the OH is labor associated and 50% is allocated to cover supervisory wages, management costs, building cleaning and maintenance, then equation (7) reduces to:

$$CPU = MPU + LCPU + LCPU + DCPU$$

$$= MPU + 2\ LCPU + DCPU$$

Using the design-to-cost goals in Table 2 and assigning a value of 25% of CPU to MPU, total allowable labor and depreciation costs to a process element in solar cell manufacture, such as metallization can be defined.

$$\$5.88 = 0.25\ (\$5.88) + 2\ LCPU + DCPU$$

$$\$4.41 = 2\ LCPU + DCPU$$

Substituting this into equation (6)

$$\text{Capital Cost} = \frac{147962 \times 4.41}{LCPU} - 295924 \tag{8}$$

or

$$\text{Capital Cost} = \frac{147962 \text{ X } 2 \text{ X DCPU}}{4.41 - \text{DCPU}} \tag{9}$$

or

$$\text{Capital Cost} = \frac{147962 \text{ X } 4.41}{4.375} \text{ MTPH} - 295924 \tag{10}$$

These equations are plotted in Figures 3, 4, and 5. One interesting observation that is shown in Figure 5 is that for a given set of assumptions, there is a threshold throughput rate below which no capital expenditure will meet the cost goal. Above this threshold, the allowed capital cost is a linear function of the machine throughput rate. For the set of assumptions used in this analysis the threshold limit for machine throughput is 2 square meters per hour.

The allowed DCPU as a function of MTPH can also be derived from equation (4). This relationship is given in equation (11).

$$\text{DCPU} = \frac{\text{ACR}}{\text{MTPH (work hours/day) (work days/week) (work weeks/year) (utilization factor)}} \tag{11}$$

$$= \frac{\text{ACR}}{\text{MTPH X } 6720}$$

for 7-year depreciation and 9% interest rate ACR = 0.19869 X Capital Cost

$$\text{DCPU} = \frac{\text{Capital Cost}}{\text{MTPH}} \text{ X } \frac{0.19869}{6720}$$

and substituting equation (10):

$$\text{DCPU} = \frac{149145.69 \text{ MTPH} - 295924}{\text{MTPH}} \text{ X } \left(\frac{0.19869}{6720}\right)$$

$$= 4.4098 - \frac{8.7496}{\text{MTPH}}$$

DCPU versus MTPH is plotted in Figure 6.

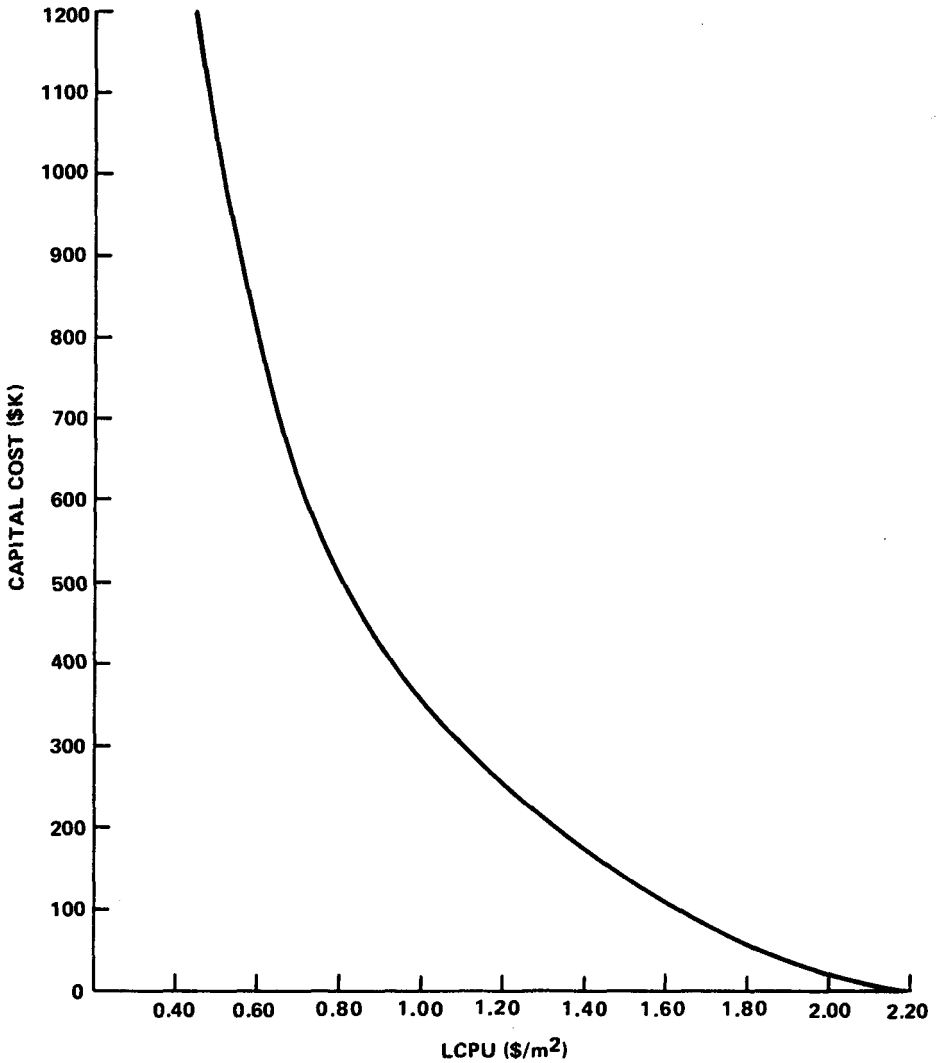

Figure 3. Capital Cost versus LCPU

Similarly, the allowed LCPU can be expressed as a function of MTPH, equation (12) and given in Table 3.

$$\text{LCPU} = \frac{\text{OPPH X OPM}}{\text{MTPH X Utilization Factor}} \qquad (12)$$

$$= \frac{4.375}{\text{MTPH}}$$

Equation (12) is plotted in Figure 7.

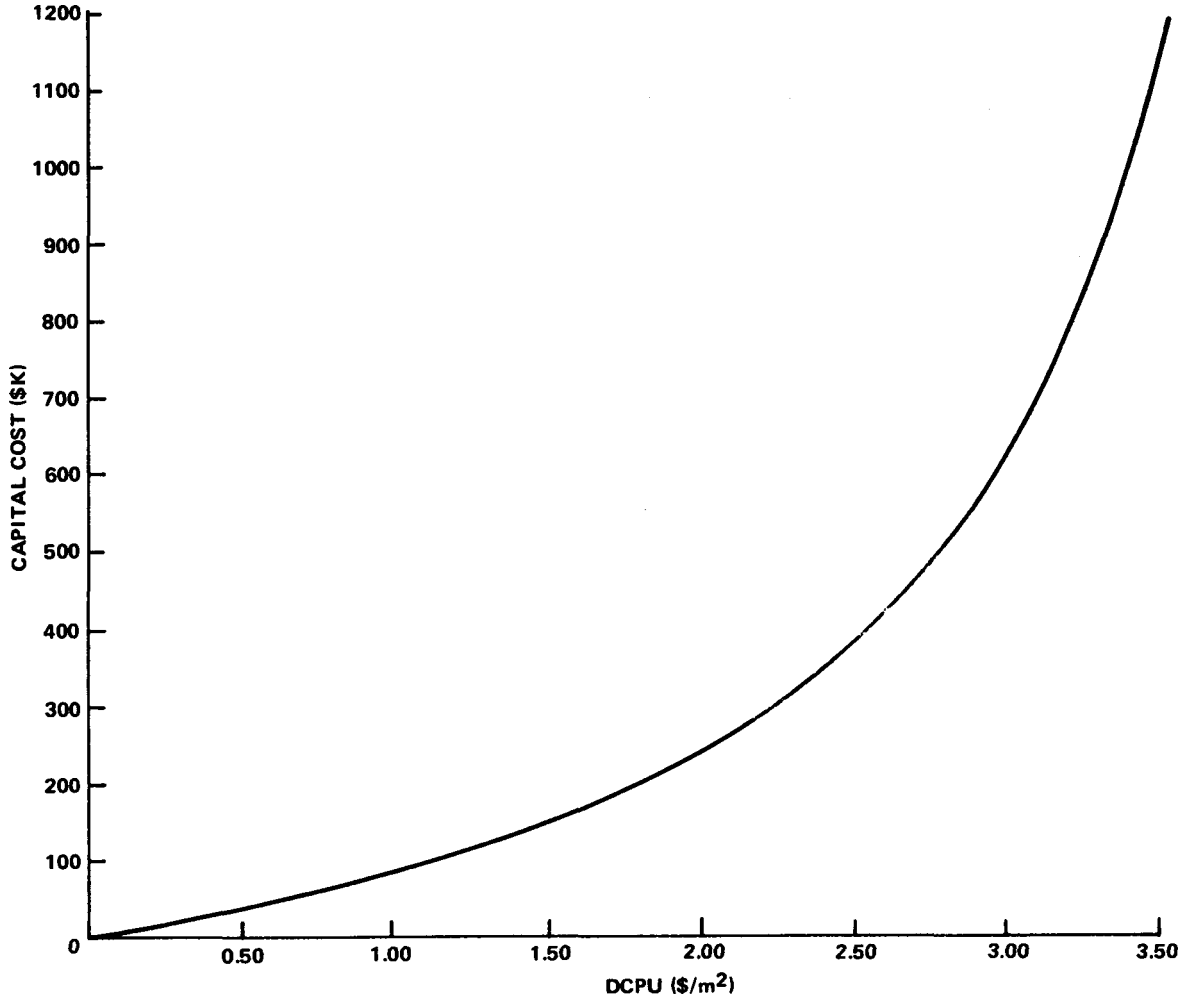

Figure 4. Capital Cost versus DCPU

The key parameter in this analysis is MTPH. For the values used in this design-to-cost simulation, a MTPH threshold of 2 m^2 per hour exists before any capital or depreciation cost can be tolerated. This leads to a description of a model metallization system that will meet the program goals. Table 4 describes this model system.

Any of the parameters in a design-to-cost model can be varied according to engineering judgment within the constraint of the total cost. The most impactive change would be to improve the module efficiency and thereby generate more available cost dollars per square meter.

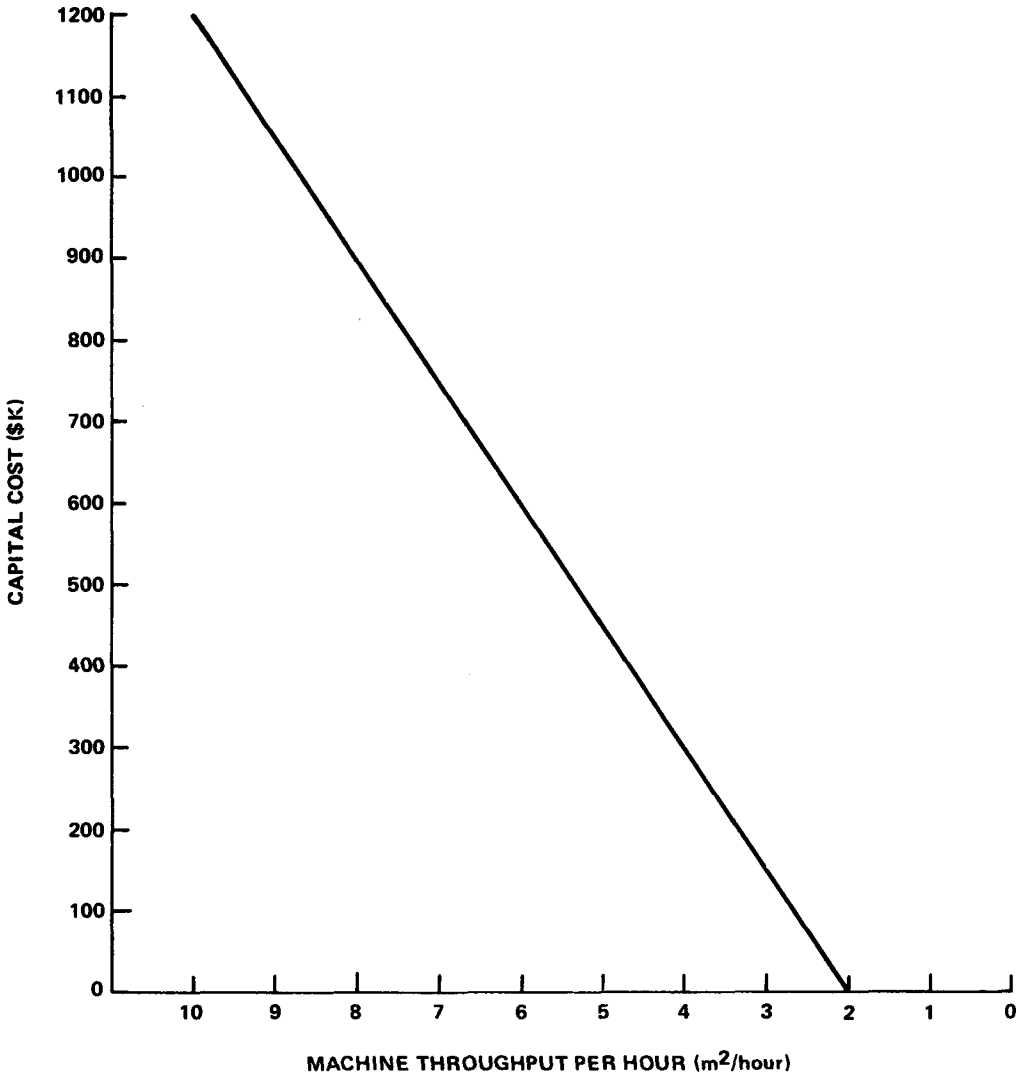

Figure 5. Capital Cost versus Machine Throughput

For purposes of comparison, one can relate square meters of cell to 10.16-cm (4.00 inch) diameter round cells. The area of a 10.16 cm diameter round cell is 81.07 cm^2. This corresponds to 123.4 cells/m^2. Therefore the threshold value of 2 m^2/hour is equivalent to a throughput of 246.7 round cells (10.16-cm diameter) per hour. Table 5 gives the CC, LCPU and DCPU for a metallization module as a function of slice (10.16-cm diameter round cells) throughput per hour.

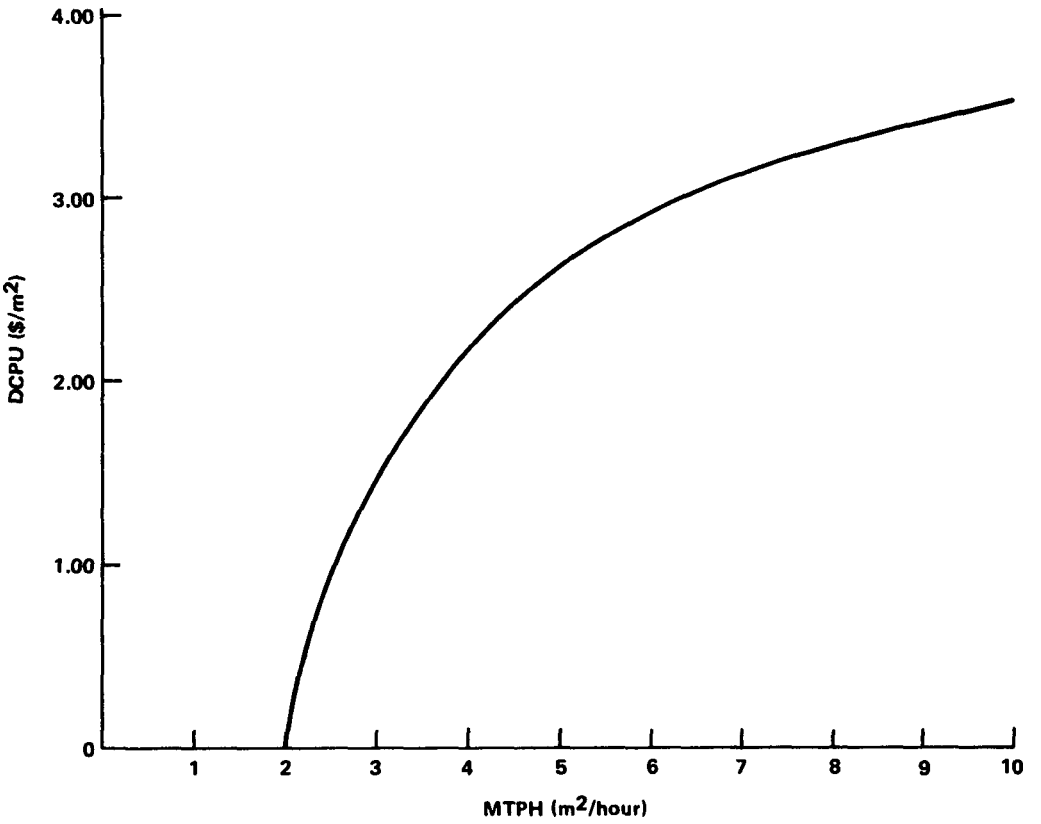

Figure 6. DCPU as a Function of MTPH

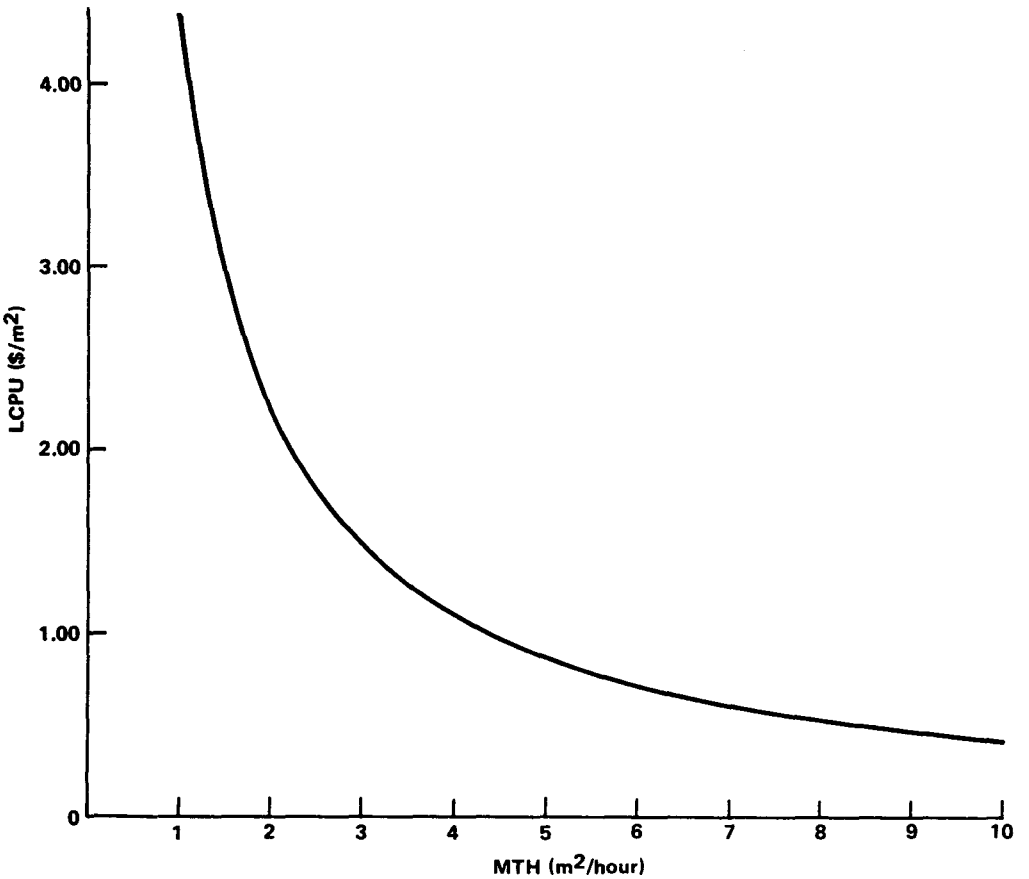

Figure 7. LCPU versus MTH

Table 4. Model Metallization System

OPM	1 technician
OPPH	$3.50/hour
OH	100% of OPPH
CPU	$5.88/$m^2$
MPU	$1.47/$m^2$
MTPH	>2 m^2/hour
LCPU	See Figure 7
DCPU	See Figure 6
CC	See Figure 5
Work Year	50 weeks 7 days/week 24 hours/day

Table 5. LCPU, DCPU and CC as a Function of Machine Throughput (10.16 cm diameter slices/hour)

Machine Throughput/Hour (10.16 cm diameter slices)	LCPU $/slice	DCPU $/slice	CC $K
200	.0219	(Below Threshold)	
250	.0175	.0005	2
300	.0146	.0064	65
350	.0125	.0106	125
400	.0109	.0137	185
450	.0097	.0161	245
500	.0088	.0180	305

E. JUNCTION FORMATION

Three types of junction formation techniques have been considered: open-tube diffusion, ion implantation, and polymer dopant. These have been evaluated in terms of potential to meet cost objectives and technical feasibility. At this time, these are ranked in the following order.

1. Polymer Dopant

The polymers can be applied by spin-on techniques, similar to photoresist, or by screen painting techniques. The polymer can be applied to one side of the silicon wafer and polymer dopants of opposite conductivity type can be applied to opposite sides to form the collecting junction and the back side contact in successive operations. After baking, the dopants can be diffused simultaneously, thereby eliminating the need for a separate back-side alloy procedure. Diffusion can be run in conventional diffusion furnaces or continuous diffusion furnaces could be designed for higher productivity rates. Initial evaluation indicates that acceptable solar cell efficiencies (>10%, AMI) can be achieved. With improved polymer formulations, the residual polymer dopant film after diffusion may form an acceptable AR coating. Arsenic (As), phosphorus (P) and boron (B) are available as dopants allowing the fabrication of N on P or P on N cells.

Semiautomatic spin-on equipment is available today (as used for photoresist application) and open-tube diffusion furnace modules are available today. A five-track spin-on module applying polymer dopant at a rate of 60 seconds/wafer/track would coat 300 wafers (one side) per hour. Two five-track machines would coat 300 wafers (both sides, opposite conductivity type) per hour. One operator could handle two machines. Capital cost would be in the range of $70K. As calculated from equation (3), the labor cost per wafer (10.16-cm diameter) would be $0.01458 and depreciation cost calculated from equation (4) (24 hour day, 7 day week, 50 week year, 0.80 utilization factor) would be $0.00690 per wafer.

A three-tube diffusion module, run by one operator, processing 300 wafers per hour would have a capital cost in the range of $30K. The labor cost would be the same as above, $0.01458/wafer and the depreciation cost would be $0.00296 per wafer. The total LCPU for this operation would be $0.02916 and DCPU would be 0.00986.

Polymer dopant costs could be within a factor of 2 of model cost goals, see Table 5, and acceptable solar cell fabrication is highly probable. The main technical disadvantages of the polymer dopant process are possible overlap of the N^+ and P^+ regions at the wafer edge, and spin-on techniques are best suited to round wafers and may cause uniformity problems with other shapes. Screen print techniques do not have this form factor problem.

2. Ion Implantation

Ion Implantation (II) is widely used in the Semiconductor industry. The main economic factor limiting the use of II in the Semiconductor industry is machine throughput rate which is a function of ion beam current, total dose, and mechanical handling and beam scan time. The primary applications of II in the Semiconductor industry are V_{TX} adjust for metal-oxide-semiconductor (MOS) devices and semiconductor integrated circuit resistors where the total doses are less than 1×10^{14} ions/cm^2. Figure 8 is a plot of slices per hour versus total dose assuming a 10-second mechanical handling and a 10-second ion beam scan time where the total dose is not the limiting factor. Curves are shown for 30×10^{-6} and 300×10^{-6} ampere beam currents (commercially available machines). The maximum MTPH is 180 3-inch (7.6 cm) slices per hour for a machine that costs ≈$100K. This gives a LCPU of $0.02431 per 7.6-cm slice and DCPU of $0.01643 per 7.6-cm slice. In the mechanical handling-scan limited region, 10.16-cm slices could be run at the same rate.

For solar cell junction formation, a total dose of 1×10^{15} ions/cm^2 would be required to give a diffused region of 100 Ω/□ at a depth of 0.3 micrometers. From inspection of Figure 8, ion beam currents below 300×10^{-6} ampere give throughput rates <100 slices per hour. Even at 3000×10^{-6} ampere ion beam current (see broken line in Figure 8) throughput is <300 slices per hour, assuming mechanical handling and scan can be accomplished in 12 seconds. The junction must be annealed after implant to remove damage and an anneal operation would be comparable to the polymer dopant diffusion facility – 300 slices/hour, one operator, $30K capital.

From the above, LCPU for implantation would be $0.07292 (7.6-cm wafer) at 300×10^{-6} ampere beam current and $0.01750 (7.6-cm wafer) at 3000×10^{-6} ampere beam current. With a total capital cost of ≈$125K for a 300×10^{-6} ampere machine, DCPU is $0.06160 and at $175K for a 3000×10^{-6} ampere machine, DCPU is $0.02070. Since total dose is area dependent,

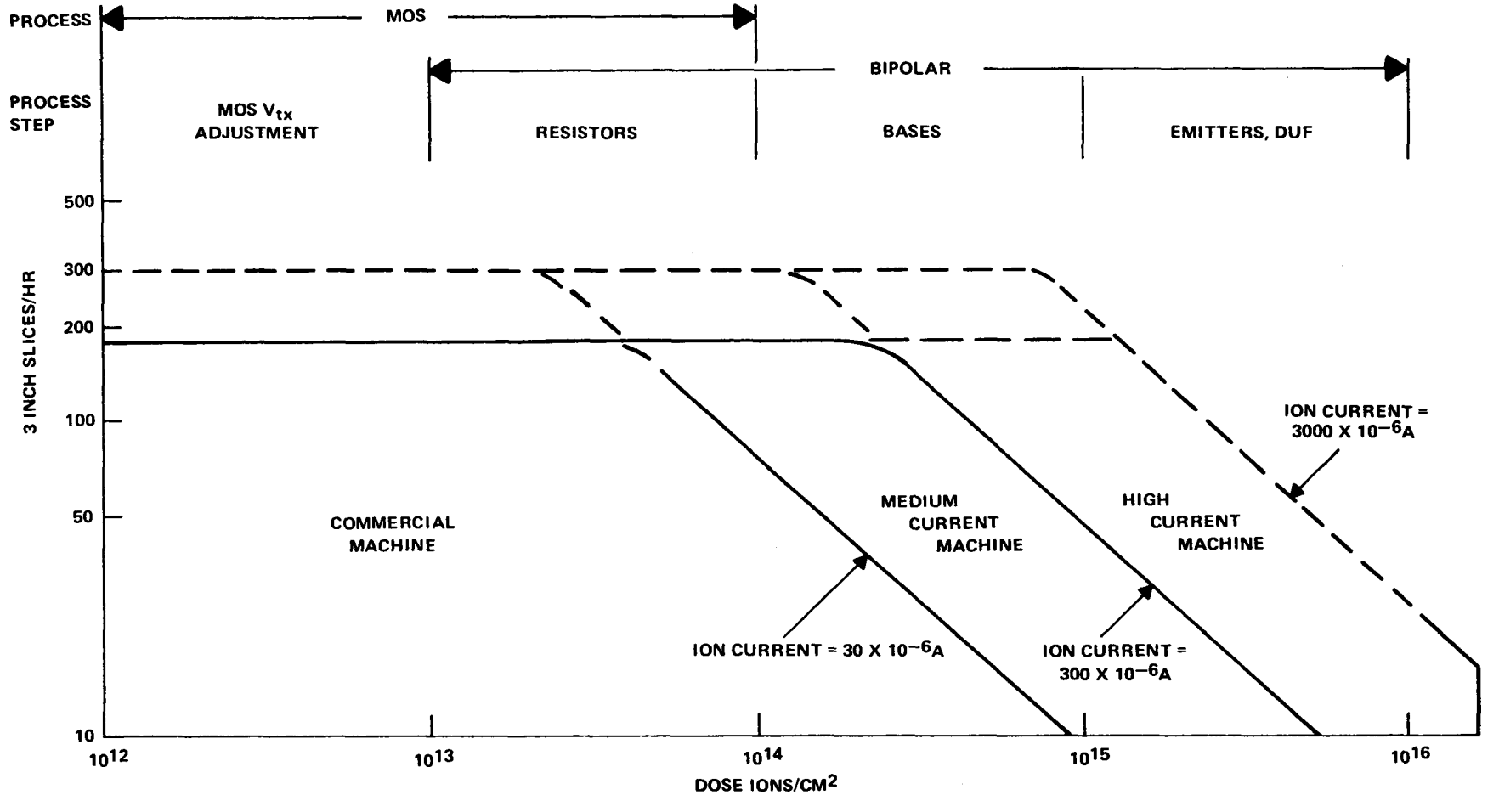

Figure 8. Ion Implantation Slice Throughput versus Dose Level

throughput rates and costs would have to be scaled according to relative area for 10.16-cm wafers. The scaling factor is Area (10.16 cm)/Area (7.6 cm) = 1.7778. Therefore, LCPU and DCPU would increase by this factor for the larger wafers. Costs for the anneal operation would not be area dependent and would be: LCPU = $0.01458 and DCPU = $0.00296.

The key to making II meet the cost objectives is a major breakthrough in ion beam current to the 10-30 X 10^{-3} ampere range coupled with major improvements in the mechanical handling-scan time. Shorter scan times or large-area unscanned ion beams must achieve acceptable implant uniformity across the solar cell area. Solar cells with conversion efficiency as high as 10% AMO, SiOx AR coating have been demonstrated.[2] Higher efficiencies may be possible if the residual damage can be removed during anneal.

II is not affected by silicon substrate shape and separate implants of opposite conductivity type could be applied to opposite sides of the silicon wafer (sheet). As with polymer dopant, the N^+ and P^+ doped areas could overlap at the wafer edge.

3. Open-Tube Diffusion

Conventional open-tube diffusion techniques are not as suitable for low-cost solar cell fabrication as the above techniques because of the inherent requirement for back-side removal after diffusion. The deposition diffusion cycle would generate labor and depreciate costs about 50% greater than the polymer dopant diffusion step, e.g., LCPU = $0.02187 and DCPU = $0.00444. Back-side removal would be material and labor intensive using standard wet chemical techniques – protect front side, etch back side through junction, remove front side protection. The maximum throughput rates per hour per operator would be in the range of 50-100. Capital cost would be approximately $30K. LCPU would range from $0.04375 to $0.08750 and DCPU would range from $0.00887 to $0.01774.

From a technical feasibility viewpoint, the best silicon solar cells fabricated to date, and most of the cells fabricated to date, have used open-tube diffusion techniques. The probability that solar cells with conversion efficiency greater than 12% can be fabricated is very high.

Table 6 summarizes the estimated LCPU and DCPU for present technology and projected technology (next five years) for the above junction formation techniques. Table 6 also includes comments on key advantages and disadvantages.

2. A. R. Kirkpatrick and J. A. Minnucci, *Development of Methods and Procedures for High Rate Low Energy Expenditure Fabrication of Solar Cells*, Quarterly Progress Report No. 1, JPL Contract 954289 (January 1976).

Table 6. High-Volume LCPU and DCPU Possible with Present Technology and Projected for Next 5 Years for Junction Formation Technologies

Technique	LCPU $/wafer	DCPU $/wafer	Advantages(+)/Disadvantages(−)
Polymer Dopant			+ Simultaneous N^+-P^+ diffusion
Current	0.02916	0.00986	−N^+-P^+ overlap at edge
Projected	0.01500	0.00600	−Uniformity problem with shapes other than round
Ion Implant			+ Simultaneous N^+-P^+ diffusion
Current	0.14422	0.03407	+ Any shape
Projected	0.04569	0.02366	−Throughput rate − beam current −N^+-P^+ overlap at edge
Open Tube			
Current	0.10937	0.02218	+ Very well defined technology
Projected	0.06562	0.01331	−Requires backside removal −Can't do simultaneous N^+-P^+

In summary, of the available junction formation technologies, polymer dopant offers the most favorable high-volume cost picture and open-tube diffusion offers the least favorable high-volume cost picture. Improvement of the projected cost for ion implantation would require development of machines with ion beam currents significantly greater than 3×10^{-3} ampere with good uniformity coupled with mechanical handling-scan time significantly less than 12 seconds per 10.16-cm wafer. These improvements do not appear probable within the next five years.

F. METALLIZATION

1. Choice of Metal System

An ideal metallization system for silicon solar cells should meet or approach the following characteristics:

a. Low contact resistance

b. High conductivity

c. Compatibility with interconnect system

d. Resistance to corrosion

e. Low electrochemical activity

f. Good adhesion to silicon

g. Compatibility with device structure

h. Metallurgical stability

i. Low cost

For process simplicity, a single metal system would be preferred, however no single metal is known to meet all of the above criteria. For silicon integrated circuits, aluminum affords the best overall choice. However for solar cell applications, Al is not a good choice because of its alloy penetration qualities (shallow solar cell junctions, ≈0.2-0.3 micrometer, are susceptible to alloy penetration), and difficulties in making high current contacts to the interconnect system.

Solar cell manufacturers have historically used multiple metal systems, Ti-Ag, Ti-Pd-Ag or similar combinations. The conductivity and solderability of the Ag outer layer being coupled with the adhesion and low contact resistance of Ti. The Ti-Ag system is typically applied by vacuum evaporation through a mask stencil in a batch operation. The process is costly both from a material cost (Pd and Ag) and from the high labor cost of batch processing.

The optimum choice will probably be a base metal (for low cost) that has high conductivity, possibly coupled with a more active metal for good contact resistance and adhesion. If good contact resistance and adhesion can be obtained with an inexpensive base metal, a single metal system may be feasible.

2. Specific Contact Resistance

Initial tests using electroless nickel on solar cells demonstrate the need for a basic contact resistance test pattern. A specific contact resistance (R_C) test pattern has been designed. The pattern consists of parallel metal stripes, 0.127-mm wide, with lengths of 1.27 mm, 2.54 mm, and 5.08 mm spaced on 1.27-mm, 2.54-mm, and 5.08-mm centers. The spacing provides one square between adjacent parallel stripes. This technique for measuring contact resistance is adapted from the technique of Shockley.[3] This technique should provide an accuracy of approximately ±30% in the value of R_C. This accuracy should be more than adequate to evaluate the feasibility of using various metal contact systems.

Initial specific contact resistance measurements were made on evaporated Ti-Pd-Ag contacts on diffused N^+ (phosphorus, 100 Ω/□) and P^+ (boron, 100 Ω/□) layers. R_C values in the range $1\text{-}10 \times 10^{-2}$ Ω-cm^2 were obtained. This value would lead to a series resistance component of

3. W. Shockley, *Research and Investigation of Inverse Epitaxial UHF Power Transistor*, Final Technical Report No. AL-TDR-64-207, Air Force Atomic Laboratory, Air Force Systems Command, Wright-Patterson Air Force Base, Ohio (September 1964.

4-40 X 10^{-3} Ω for the metal-semiconductor contact resistance. Sintering at 450°C for 10 minutes in N_2 did not improve the R_C. An acceptable metallization for solar cells should contribute less than 1 X 10^{-3} Ω contact resistance. This experiment will be repeated to verify the result and establish a baseline.

Specific contact resistance measurements will be run on electroless nickel contacts and screen printed copper next month.

3. Vacuum Deposited Contacts

The most widely used metallization system used for the front side of solar cells is the Ti-Ag or Ti-Pd-Ag system. The metal layers are deposited by evaporation either through a mask stencil or patterned after evaporation. The Ti is reputed to make good ohmic contact with the diffused layer and provide good adhesion to the silicon surface. Initial evaluation of the specific contact resistance (see above) indicates that contact resistance may be a problem if the surface impurity concentration is not high enough.

From a cost evaluation, patterning after deposition is an excessively costly operation and is not compatible with the low-cost silicon solar cell goals. Therefore evaporation followed by photolithographic patterning will not be further evaluated.

Evaporation or sputtering through a mask stencil must be considered as a low-cost option. Machines are available on the market or in development for continuous metal deposition. These machines are typically in modular form so that one or more metals may be deposited from adjacent modules. Throughput rates of 400 7.62-cm round (or hexagonal or square) wafers per hour are feasible in the near future. Since vacuum deposition is an area-dependent operation, this throughput rate would convert to 225 10.16-cm diameter wafers per hour. A modular machine of this throughput would cost in the range of $250,000 to $400,000, exclusive of the mask stencil carriers and alignment fixtures. The throughput of a machine of this type would approach the parameters of a model metallization system, see Tables 4 and 5 within a factor of 2 or 3. Using a Ti-Cu metallization system, 0.2 micrometer Ti and 5 micrometer Cu, the material cost (<$0.50/$m^2$) would be acceptable even though >95% of the deposited material would not be utilized on the produced solar cells (50% of deposited metal is not on wafer area and 10% of wafer is contact metallization). Cost variables have not been evaluated for mask stencil inventory, cleaning, material recovery, or alignment fixtures. While continuous vacuum deposition appears to offer a substantial improvement in cost over batch processing, it does not appear to be capable of meeting the LSSA goals within the next five years without substantial improvements in throughput rate.

The cost improvements that could be realized from a machine of this description would require a market that could utilize the output of this system. Minimum DCPU would require maximum output. At a 24-hour day, 7-day week, 50-week year and 80% utilization, this system would metallize $\approx 1.5 \times 10^6$ 10.16-cm diameter wafers, front and back sides. With a 12% conversion efficiency at AMI, this would represent $\approx 1.5 \times 10^6$ W peak power for one system.

At present vacuum deposition, either evaporation or sputtering will remain the method of choice until a lower cost metallization system is demonstrated.

4. Screen Printed Contacts

Screen printing of conductive material from pastes is a very attractive option for metallization. Throughput is not a function of printed area, up to the screen size limitation of the machine. Very high throughput rates, $\approx$1000 pieces (e.g., 10.16-cm wafers) per hour are feasible with semiautomatic equipment at a capital cost in the neighborhood of $100,000. Typical line widths of 0.025 cm (0.010 inch) and 0.013 cm (0.005 inch) are readily obtained. A lower limit of 0.008 cm (0.003 inch) is typical. Typical metal thicknesses are in the range of 15 to 20 micrometers. Conductivity of the printed and fired metal films is less than that of evaporated films but total resistance is acceptable with the 15-20 micrometer films. Within reasonable limits, surface finish is not a problem – thick films are used on unglazed ceramics. The process is additive, i.e., metal paste is only printed in areas where it will be used and firing temperatures ($<750°C$) are usually low enough to be compatible with semiconductor processing.

Historically only noble or seminoble metals (Au, Pt, Pd, Ag) have been used. The material costs are very high for these precious metals, >$100 per ounce of paste or >$25 per m^2 on solar cells. Recently base metal pastes, Cu and Ni, have become available.[4] Projected costs in high volume are in the $5-$10 per ounce range, giving a material cost of $1.25 to $2.50 per m^2 on solar cells. The lower part of this range fits the model metallization system in Table 4. LCPU and DCPU are well within the bounds of the model metallization system.

Technically this metallization scheme has not been demonstrated on solar cells or other semiconductor devices. Several key characteristics, notably contact resistance, adhesion to silicon and compatibility with the device structure must be demonstrated before these metal systems could be utilized.

Initial evaluation of screened on base metal will begin next quarter.

4. Cermalloy, Cermet Division of Bala Electronics Corp., West Conshohocken, PA.

5. Electroless Plating

Electroless nickel (Ni) plating has been used in the Semiconductor industry for many years. The process is additive and inexpensive. Ni plates have been used to make ohmic contact to both N^+ and P^+ diffused layers. Several key questions are unanswered at this time, among these are: what is the specific contact resistance to N^+ and P^+ layers as used on solar cells; can high conductivity and good adhesion be achieved; are sintered Ni contacts compatible with shallow junctions used in solar cell devices; and can electroless contacts be patterned during plating.

A survey of the literature on electroless metal contacts has begun. Initial results will be reported next quarter.

6. Other Contacts

Other types of contacts are being surveyed. The most attractive candidate is transparent metal oxide conductors, e.g., SnO_2 and In_2O_3. An initial evaluation indicates that acceptable conductivity is not readily achievable and no data is available that would indicate that good ohmic contact can be made between silicon and metal oxide conductors. Contact from the metal oxides to the interconnect system would also be a problem. For these reasons, no further work is planned on metal oxide systems.

7. Summary

At this time the most attractive metallization system from a low-cost standpoint is screen printed base metals. Several key technical questions remain before feasibility can be demonstrated.

From a functional standpoint, vacuum deposited Ti-Ag systems give the best performance. High-volume cost projections indicate a substantial cost reduction could be achieved using continuous deposition machines. These projections require a market of several megawatts per year. Even at this rate the LSSA project goals appear to be beyond the capability of projected vacuum deposition machines.

G. ANTIREFLECTION COATING

No detailed work has been done in this area this quarter. Deposition techniques used for junction formation and metallization, e.g., spin-on polymers, screen printing, and vacuum deposition, would be applicable.

H. SOLAR CELL FABRICATION

Experimental cells are being processed using the process outlined in the first quarterly report. The front-side and back-side metallization patterns are shown in Figure 2 of the first quarterly report. Twenty-five hexagonal cells, laser scribed from 7.6-cm round slices with holes cavitroned in the center, were processed to metallization. Twenty of the 25 cells were lost to breakage that was traced to microcracks originating at the cavitroned center hole. The remaining five cells are on hold at metallization.

A second group of 25 hexagonal cells without center holes laser scribed from 7.6-cm round slices were processed in five cell lots. One lot of five cells was finished using two different metallization schemes for the front-side metallization. One group (three cells) used a standard Ti-Pd-Ag evaporated contact. These cells exhibit $V_{OC} = 0.62$ V and $I_{SC} = 1.15$ A ($J_{SC} = 30.7$ mA/cm^2). The efficiency is in the range of 8-9% (without antireflection coating) due to poor fill factor. This is most probably caused by high series resistance and nonoptimum metallization pattern. A typical current-voltage plot on a hexagonal cell is shown in Figure 9.

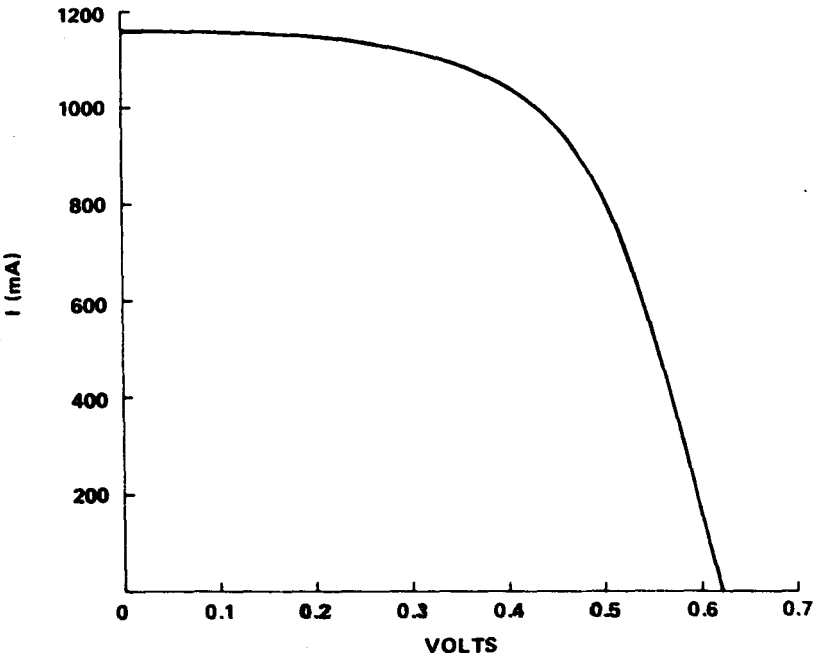

Figure 9. I-V Characteristics of 7.6-cm Experimental Solar Cell

The second group (two cells) from this same lot was completed using electroless nickel for front-side metallization. The electroless nickel pattern was uniform but the contact resistance was very high, even after a 590°C sinter. The photoresponse of these cells was very poor ($J_{SC} \approx 7$ mA/cm^2). Further work will be required to define suitable conditions for using electroless nickel contacts on solar cells.

A baseline process for spin-on polymer dopant has been defined that utilizes simultaneous N^+ (arsenic) and P^+ (boron) diffusion for a N^+PP^+ solar cell process. Simple 2-cm X 2-cm cells were fabricated in 8-microsecond lifetime material. These cells exhibit $V_{OC} = 0.55$ V and $I_{SC} = 60\text{-}80$ mA ($J_{SC} = 15\text{-}20$ mA/cm^2).

Sample solar cells, 7.6-cm hexagonal, N^+-P-P^+, were fabricated using simultaneous N^+-P^+ diffusion from polymer dopant sources. Evaporated Ti-Pd-Ag contacts were used on front and back sides. The hexagonal shape was laser scribed from round wafers after fabrication. Before laser scribing, the reverse diode characteristics showed high leakage indicating that the N^+ and P^+ areas overlapped at the wafer edges. After laser scribing, the reverse diode characteristic was acceptable. At AMO conditions, the $V_{OC} = 0.52$ V, and $I_{SC} = 700$ mA ($J_{SC} \cong 18$ mA/cm^2) with a fill factor $\cong 0.6$. The poor conversion efficiency is attributed to high series resistance, low shunt resistance, and excessive recombination. The experiment will be repeated to verify this result.

Forward volt-ampere characteristics of the hexagonal solar cell were measured with no illumination in order to determine the cause of the low fill factor observed. A power supply and ammeter were connected to the center contact of the cell. The voltage across the cells measured with a digital voltmeter connected to a second probe. This probe contacted the cell at the outer edge to minimize series resistance drops.

A linear plot of the I-V characteristics at low voltages (Figure 10) indicates a shunt resistance of about 71 ohms. A semilog plot of measured current vs voltage is shown in Figure 11. Also plotted is the difference between the total current and the shunt component of current. In the range of 0.15 volt to 0.5 volt, the difference current is of the form

$$I_X \propto \exp(qV/4KT)$$

For voltages between 0.5 and 0.55 volt, the current approaches the form

$$I_D \propto \exp(qV/KT)$$

Series resistance drop obscures the I-V characteristics of the junction for voltages greater than 0.55 volt (currents greater than 0.1 amp).

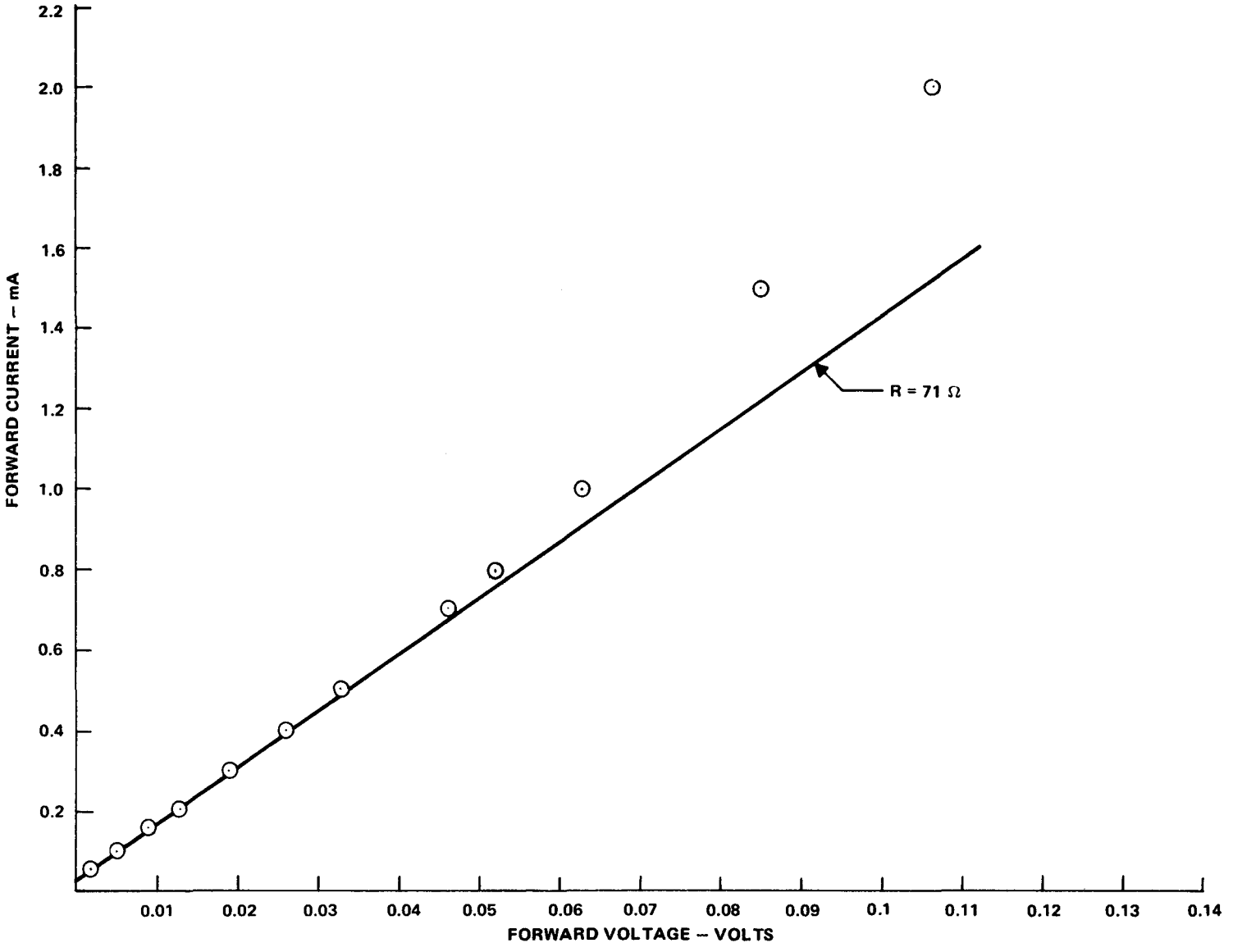

Figure 10. Forward Unilluminated Characteristics of Solar Cell at Low Voltage

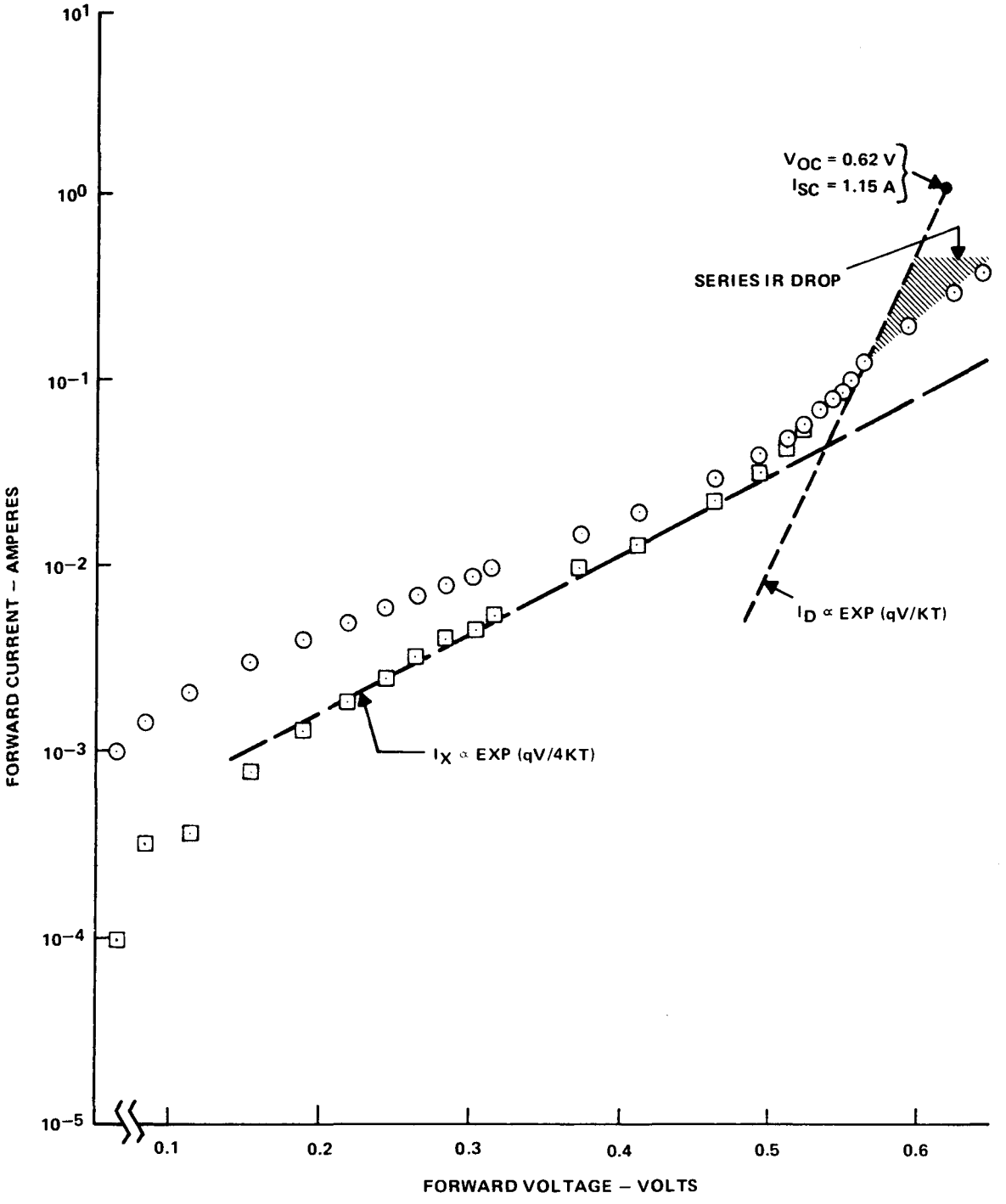

Figure 11. Forward Unilluminated Characteristics of Solar Cell

A circuit model which represents the I-V characteristics of Figure 11 is shown in Figure 12. The current, I_D, is the diffusion current of the ideal junction; I_X accounts for the excess component of current observed. It is shown in another section that this model simulates the characteristics observed under illumination. The current component

$$I_X \propto \exp(qV/4KT)$$

is probably due to recombination in a channel at the junction periphery.

The hexagonal cell discussed here was fabricated with an unpassivated junction; the cross section is shown diagrammatically in Figure 13. The unpassivated junction as well as damage at the edges of the cell could account for a high value of recombination current as observed.

An experiment has been designed to identify the source of the excess current. An experimental lot will be fabricated which contains both unpassivated cells and planar cells with passivated junctions. Comparison of the volt-ampere characteristics for the two cell types should indicate whether the excess current originates in the active junction or at the junction periphery. Additionally, junction cleanup techniques will be investigated.

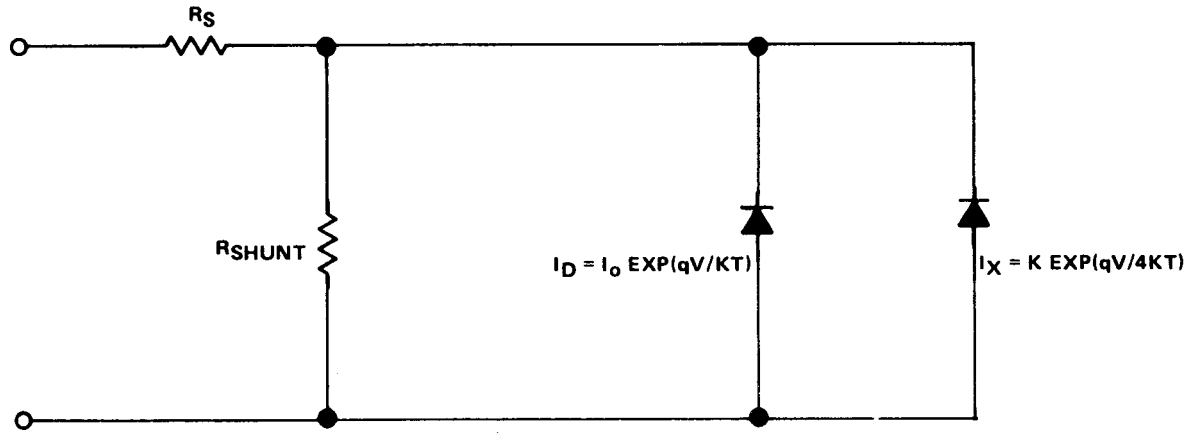

Figure 12. Model for Unilluminated Solar Cell with Excess Current Component

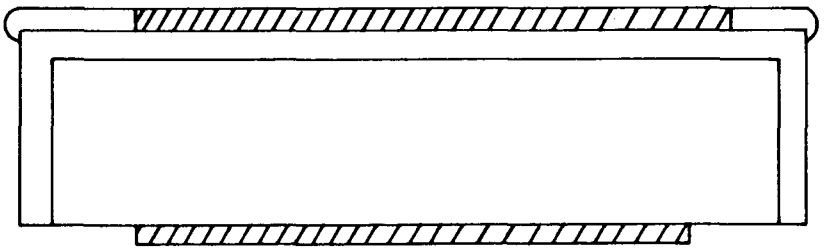

Figure 13. Experimental Structure for Solar Cell

I. SOLAR CELL MODELING

A computer model of a solar cell and a model of a 16-cell module have been developed. The model output and schematic for a simple cell are shown in Figure 14. The solar cell characteristics assumed for the model are $V_{OC} = 0.55$ V and $I_{SC} = 1.272$ A with an internal resistance of 0.015 ohm. With an optimum load of 0.38 ohm, the series-parallel module would deliver 8.79 W at 4.81 A and 1.83 V if all cells are identical. Figure 15 is a schematic of the balanced array module. The I-V curve for the balanced array module is shown in Figure 16. A computer run with cell 11 generating no photocurrent, $R_L = 0.38$ ohm predicts that the module should deliver 5.52 W at 3.81 A and 1.27 V. With 25% of the module inoperative (one series leg of the 4 X 4 cell module), the 3 X 4 portion of the module delivers only 63% of the original power. The 37% power loss due to a 25% loss of active cells is caused by the nonoptimum load conditions for the effective 3 X 4 module. The optimum load resistance for the damaged module would be 0.51 ohm. Figure 17 shows the model schematic for the array with cell 11 inoperative.

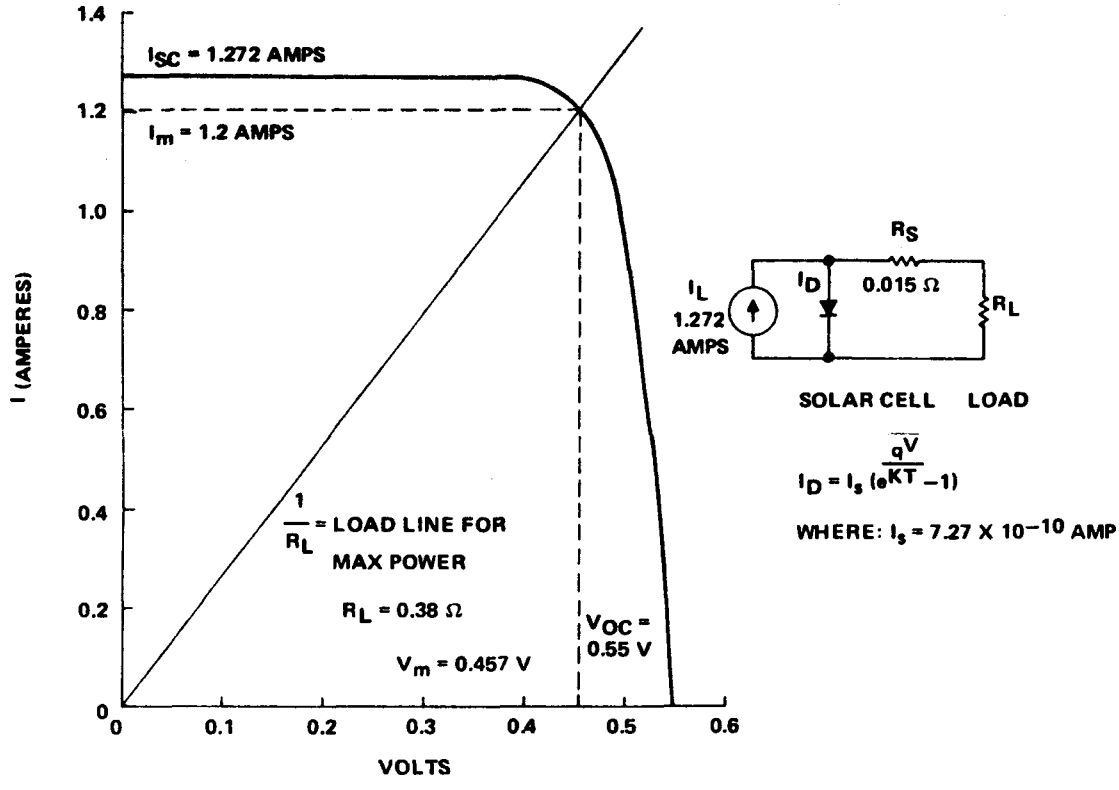

Figure 14. I-V Curve of Computer Modeled 7.6-cm Solar Cell

J. MODULE MODELING

Two failure mechanisms have been investigated to date. One cell of the 4 X 4 module model was selected as the failing cell and one of its parameters varied from 0 to 120% nominal value.

The first parameter varied was light generated current. A graph of normalized power output versus I_L of one cell is shown in Figure 18.

The second parameter varied was open circuit voltage. A graph of normalized power output as V_{OC} is varied as shown in Figure 19. A module schematic is shown in Figures 15 and 17. From Figures 18 and 19, a variation of ±10% in V_{OC} or I_{SC} of one cell of a 16-cell module would cause less than a 2% variation in module output power. A variation of ±20% in one cell would cause less than a 5% variation in module output. Further testing of the module model will continue.

K. SOLAR CELL CHARACTERIZATION

An operating solar cell has been constructed and the I-V characteristic plotted. Work is continuing in an attempt to fit the simple computer model to this actual I-V curve. It is hoped that in so doing, a better understanding of the types and magnitudes of cell defects can be obtained.

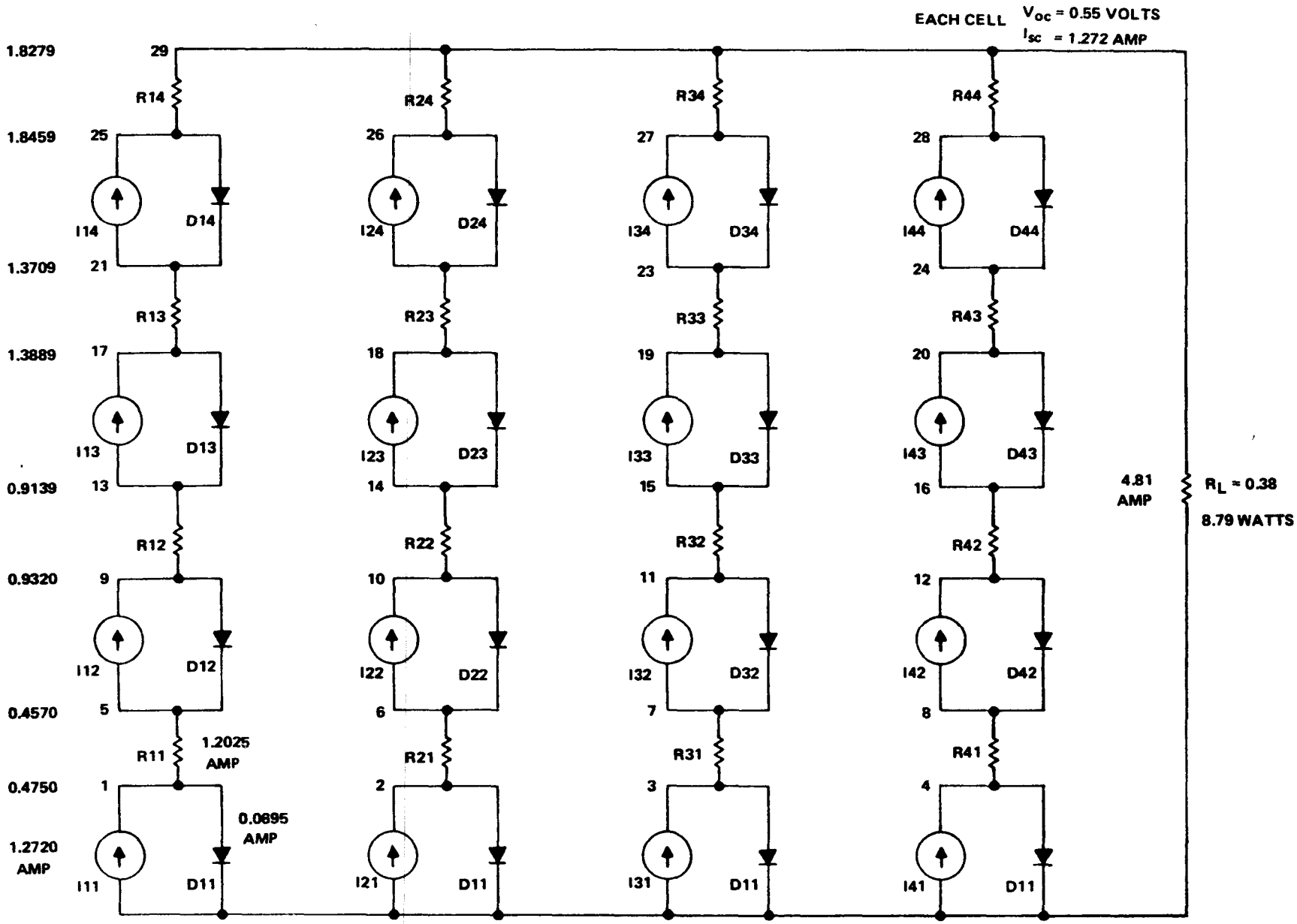

Figure 15. Solar Cell Module Model with Balanced Cells

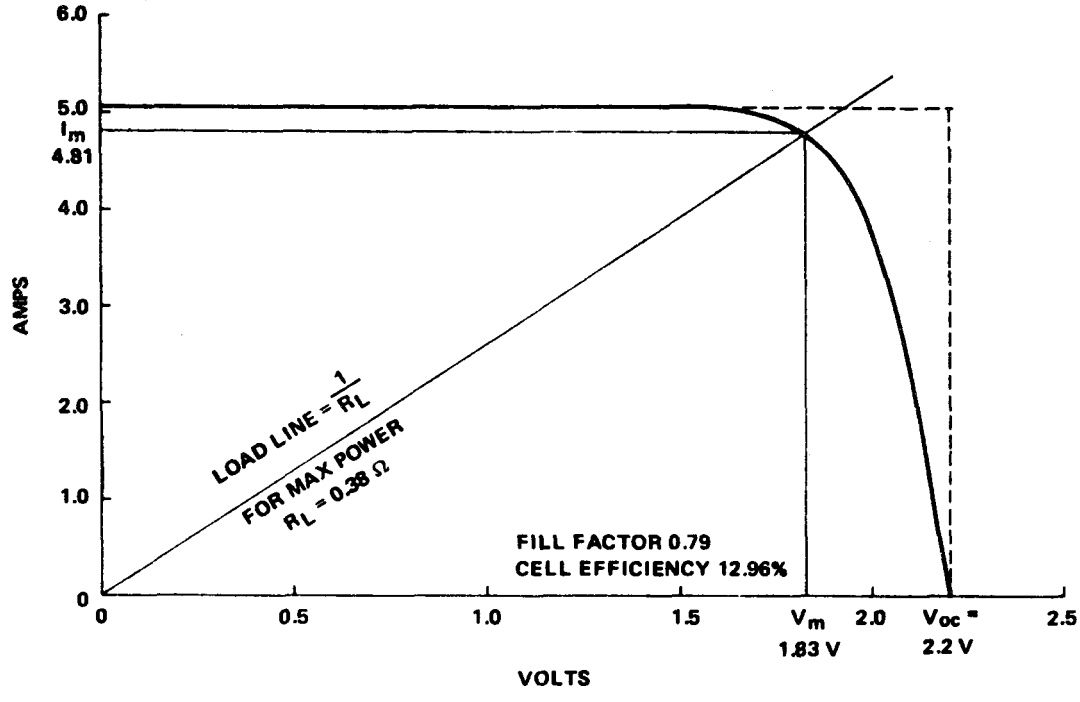

Figure 16. Solar Cell Module I-V Curve from Computer Model

After numerous trials, the "best fit" to date has been obtained using the model shown in Figure 20.

Figure 21 is a "best fit" of the actual I-V characteristics using the "best fit" model in Figure 20. The low fill factor of the actual cell is attributed to the higher series resistance, $R_S = 0.08\ \Omega$ and the I'_D component of recombination and shunt resistance. The value of n = 4 in the exponential term indicates a significant deviation from ideal junction characteristics.

L. AUTOMATION

A mock-up of a 10 W solar cell module has been fabricated.

An initial survey of circuit board materials as substrates for module assembly indicates that all commonly used materials are too expensive, $>\$20/m^2$. A search has begun to identify other options.

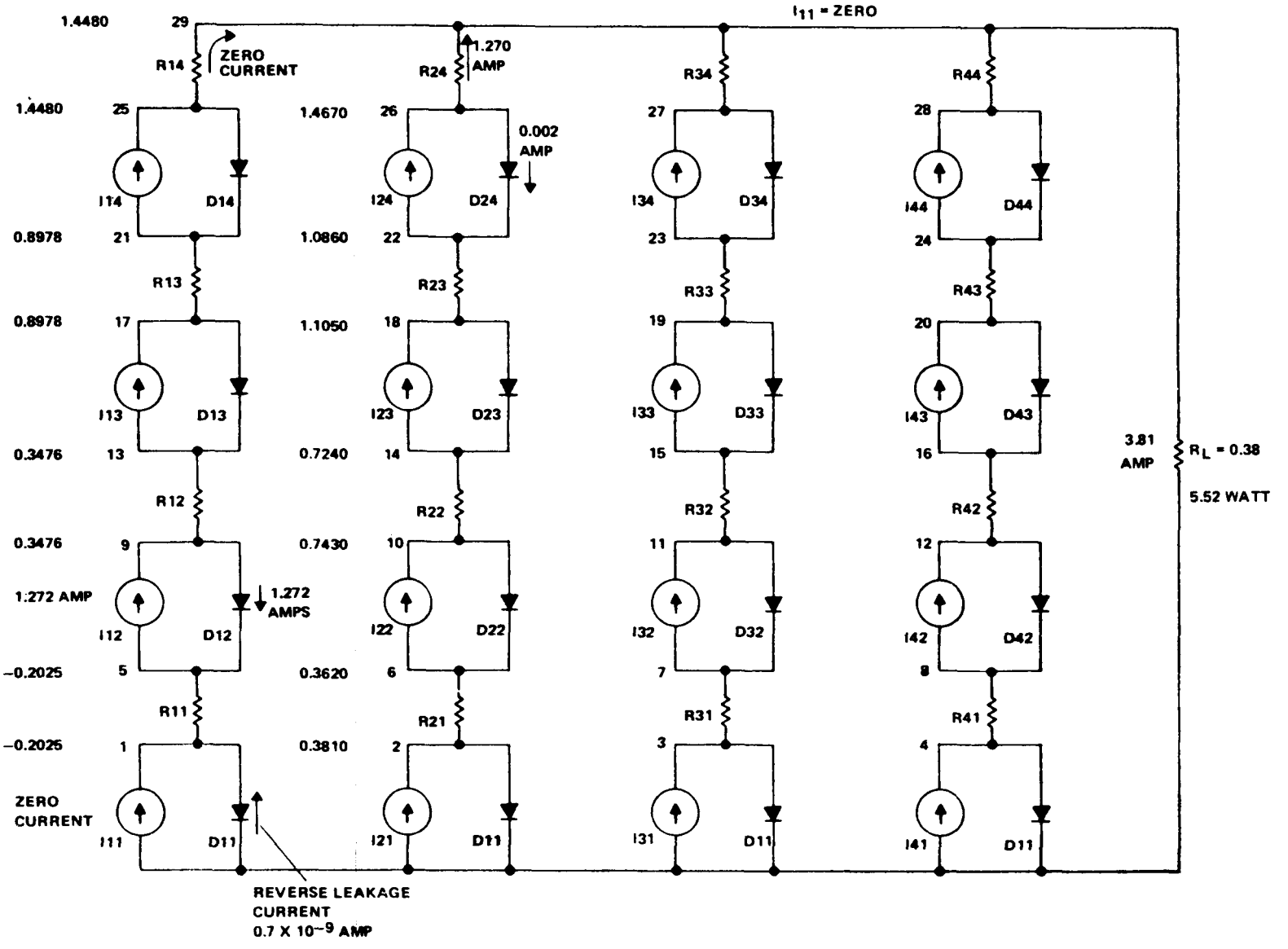

Figure 17. Solar Cell Module Model with One Inoperative Cell

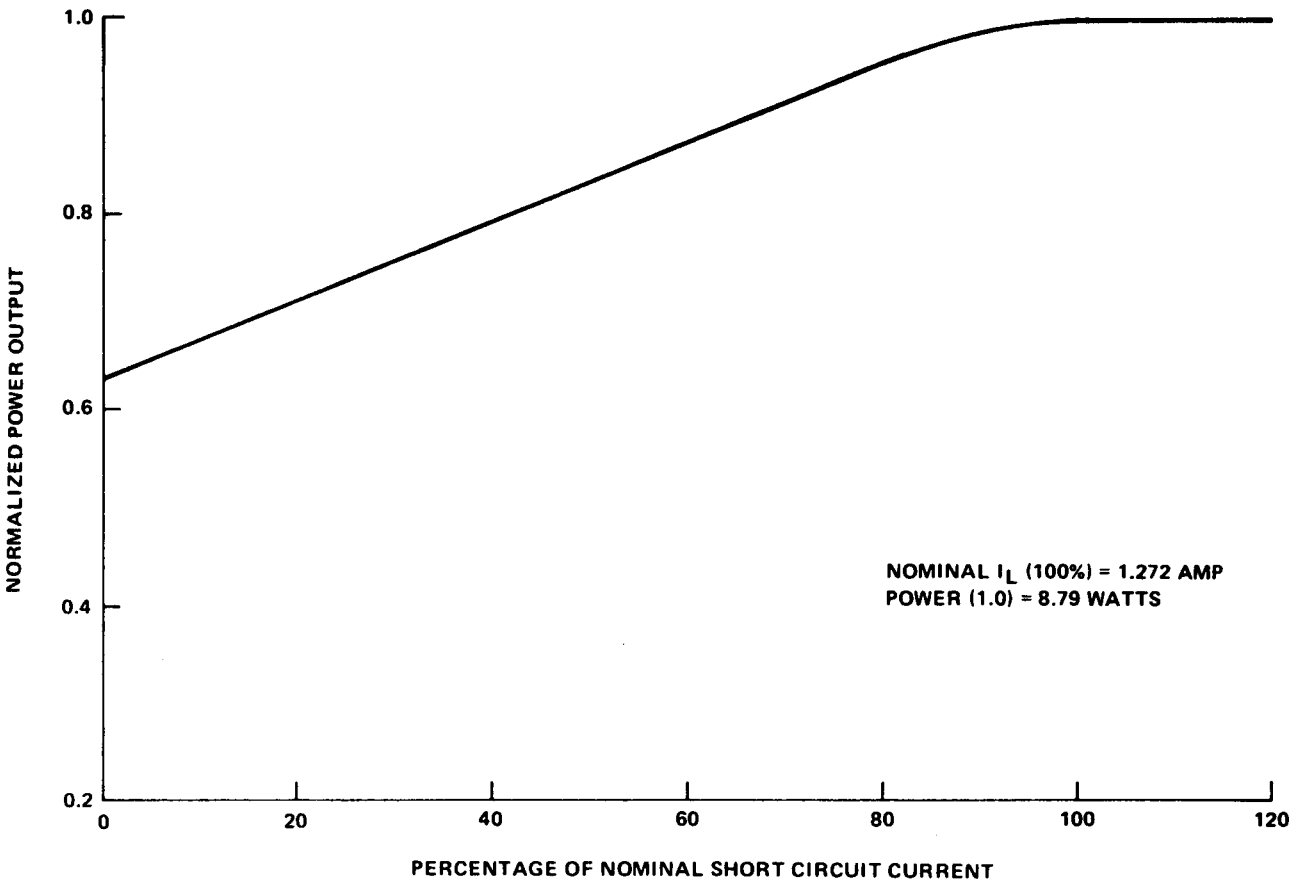

Figure 18. Normalized Power Output of 16-Cell Module as I_L of One Cell Varies

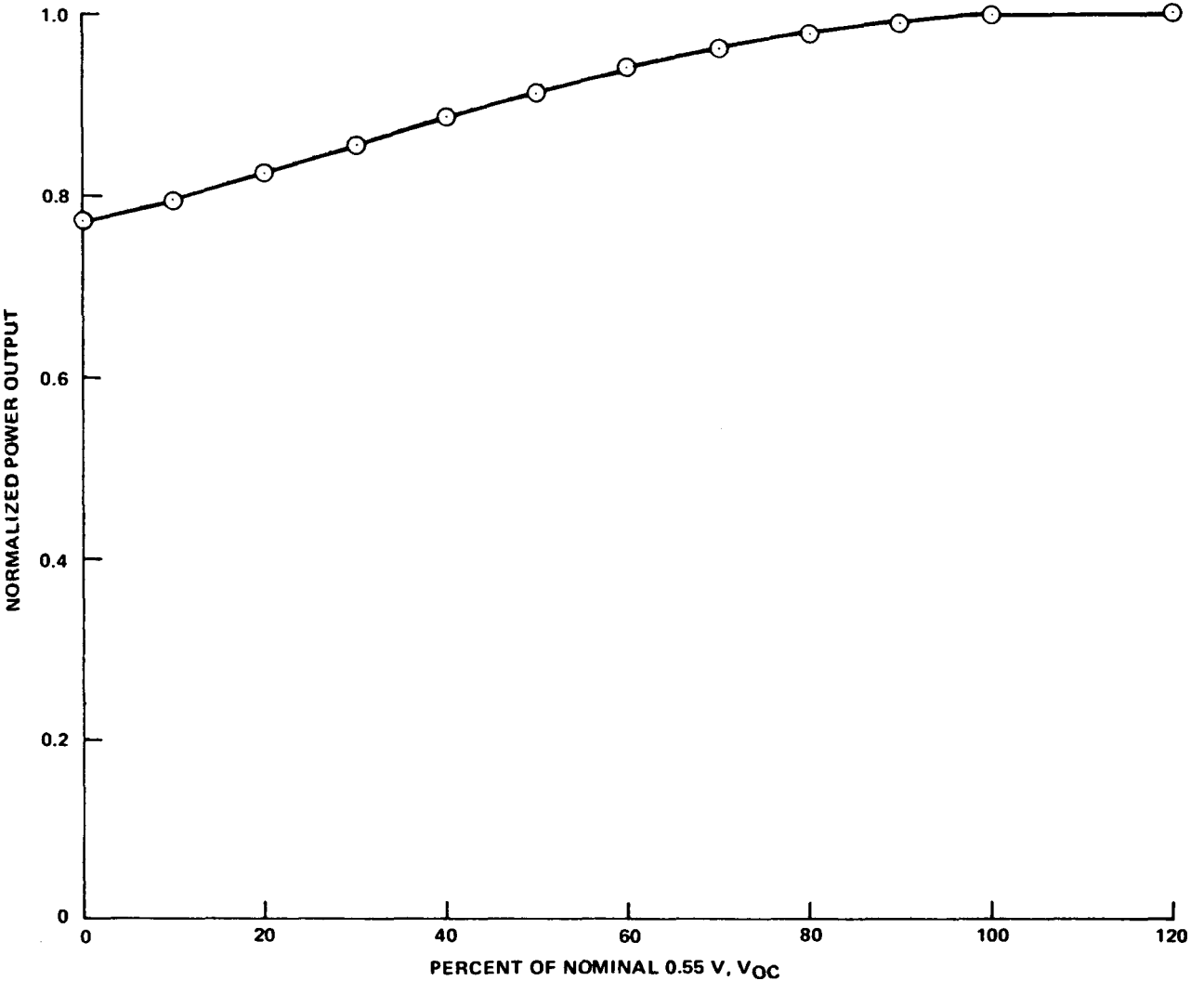

Figure 19. Sixteen-Cell Module V_{OC} of One Cell Varying

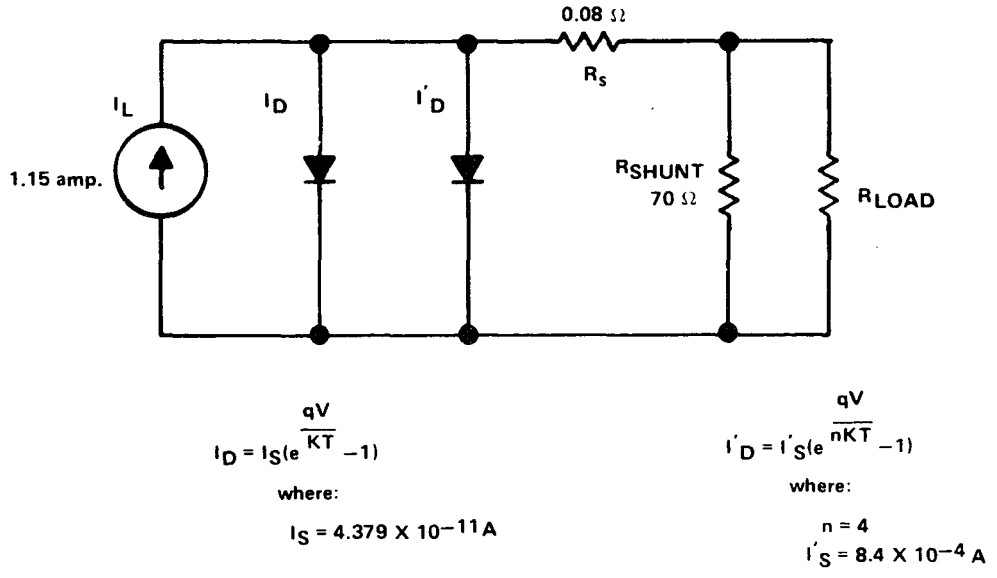

Figure 20. "Best Fit" Model of Actual Solar Cell Characteristics

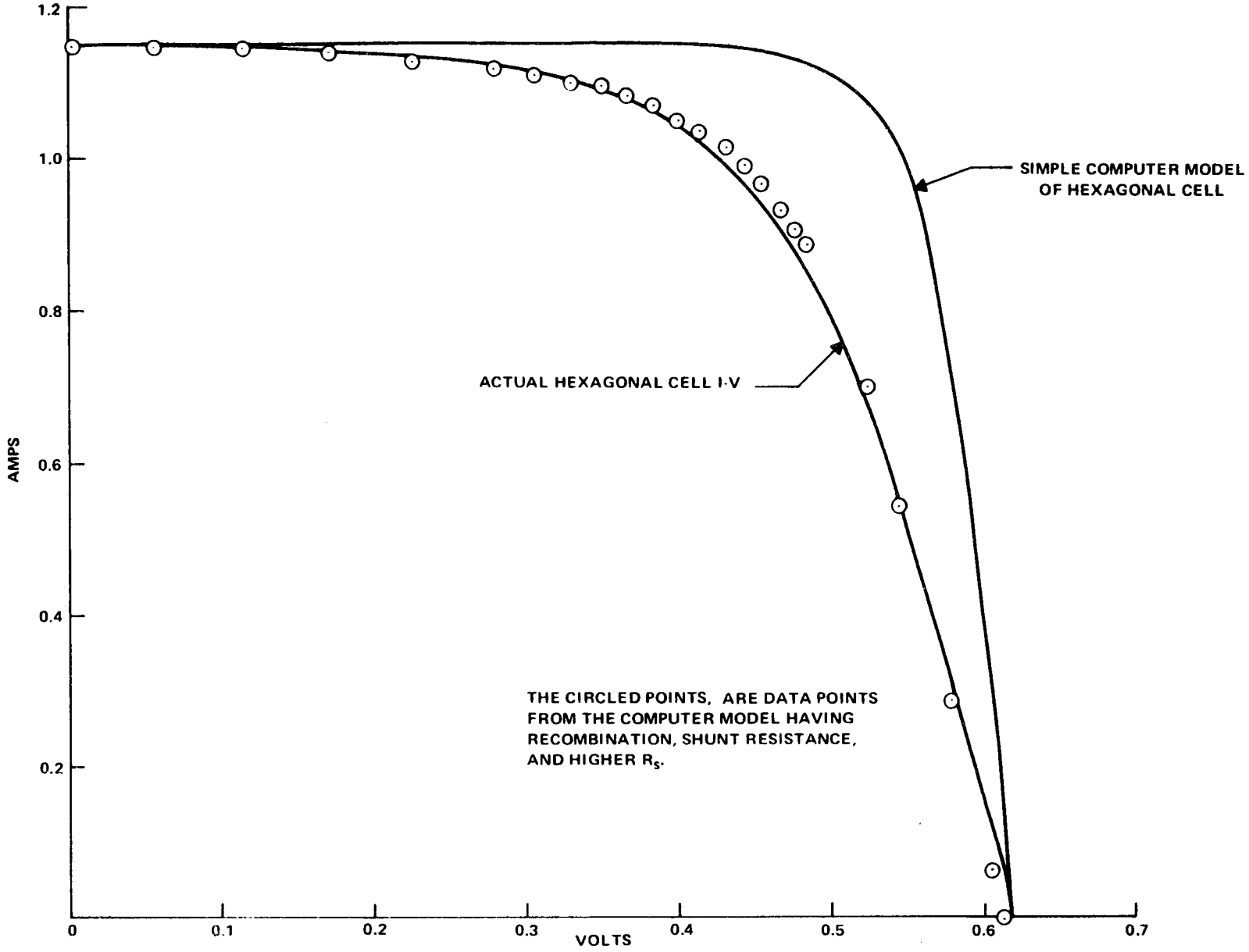

Figure 21. I-V Characteristics of Hexagonal Cells

SECTION III
CONCLUSIONS AND RECOMMENDATIONS

Design-to-cost analysis demonstrates that module conversion efficiency is a key parameter in determining cost per unit area of solar cell modules. Low efficiency processes will have to meet low cost per unit area goals. Cell processing, substrate and encapsulation costs present a potentially insurmountable barrier to low-cost, low-efficiency silicon sheet processes.

Individual process elements can be assigned cost goals and a model description of a solar cell factory can be defined. Feasibility and compatibility must be demonstrated before a factory process can be defined.

Simultaneous P^+-N^+ diffusion from polymer dopant sources appears to be the most attractive approach to junction formation. Higher conversion efficiency processing must be defined.

Low-cost metallization is still a significant cost barrier. Continuous vacuum deposition represents a short-term cost reduction but the short-term market is not large enough to support the investment at this time. Screen printed base metals may be the most attractive low-cost metal option if technical feasibility can be demonstrated.

Device characterization coupled with modeling is a very useful tool to improve solar cell characteristics. Further work needs to be done in this area.

Assembly and encapsulation of modules represents the most severe cost barrier in the LSSA project.

SECTION IV
NEW TECHNOLOGY

No new technology has been developed under this task during this quarter.

SECTION V
PROGRESS SUMMARY

The progress on each of the activities in this task is shown in Figure 22. The overall task is on schedule.

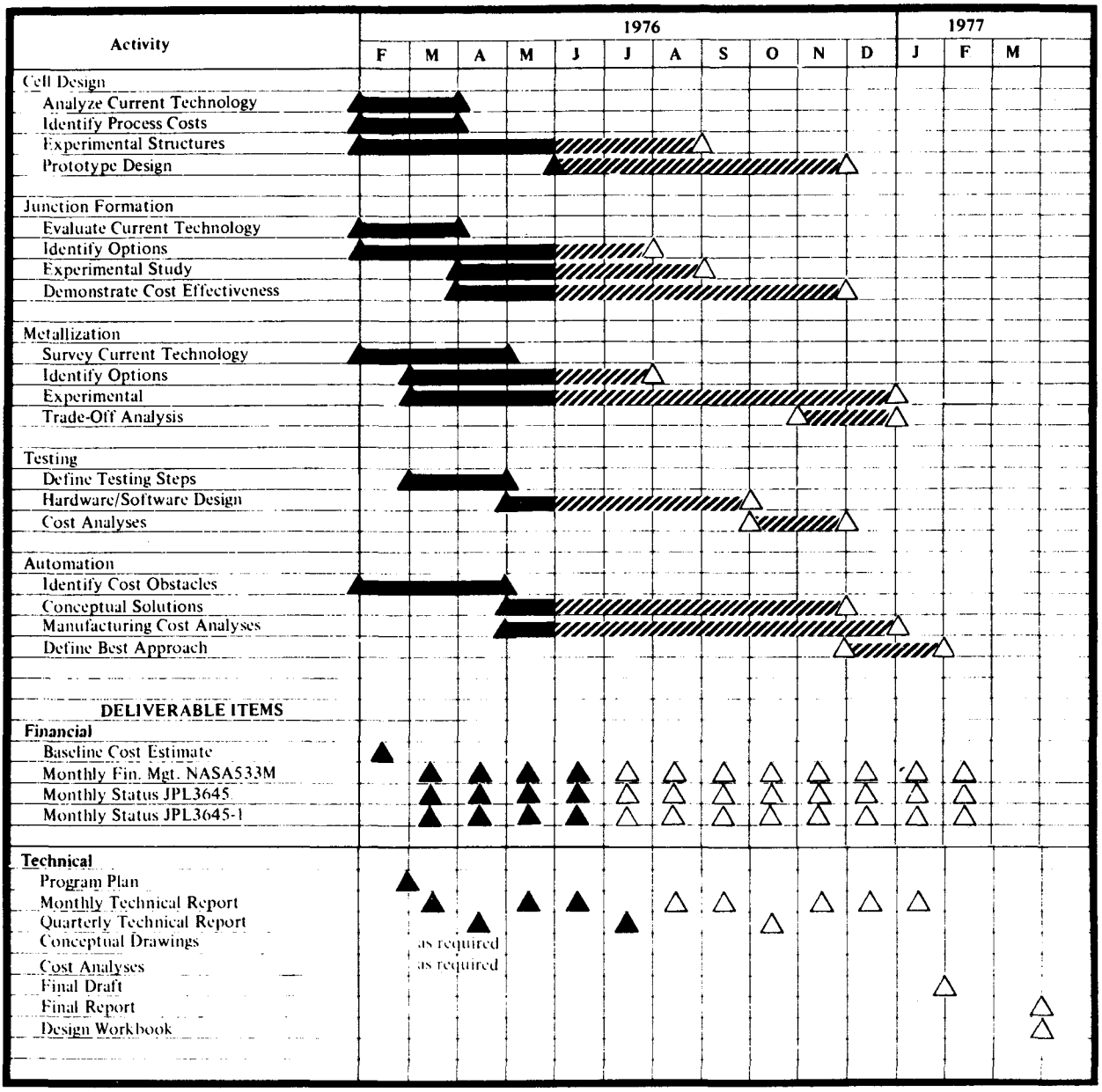

Figure 22. Work Plan Status