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MASTER

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ABSTRACT

A thin film technique developed for the SLL Micro Actuator in which both gold and aluminum can be incorporated on sapphire or fine grained alumina substrates in a two-level metallization system is described. Tungsten is used as a lateral transition metal permitting electrical contact between the gold and aluminum without the two metals coming in physical contact. Silicon dioxide serves as an insulator between the tungsten and aluminum for crossover purposes, and vias through the silicon dioxide permit interconnections where desired. Tungsten-gold is the first level conductor except at crossovers where tungsten only is used and aluminum is the second level conductor. Sheet resistances of the two levels can be as low as 0.01 ohm/square. Line widths and spaces as small as 0.025 mm can be attained. A second layer of silicon dioxide is deposited over the metallization and opened for all gold and aluminum bonding areas. The metallization system permits effective interconnection of a mixture of devices having both gold and aluminum terminations without creating undesirable gold-aluminum interfaces.

Processing temperatures up to 400°C can be tolerated for short times without effect on bondability, conductor, and insulator characteristics, thus permitting silicon-gold eutectic die attachment, component soldering, and higher temperatures during gold lead bonding. Tests conducted on special test pattern circuits indicate good stability over the temperature range -55°C to +150°C. Aging studies indicate no degradation in characteristics in tests of 500 hours duration at 150°C.

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TABLE OF CONTENTS

INTRODUCTION

A thin film hybrid microcircuit metallization system was developed and feasibility established for the SLL Micro Actuator which required the interconnection of a mixture of semiconductor devices (MOS and bipolar) with both gold and aluminum terminations as well as passive components (chip resistors and monolithic capacitors). Eutectic die attach and soldering of components was desired for thermal dissipation reasons. The necessity for processing temperatures as high as 370°C for die attach, soldering, and bonding during assembly and rework made it desirable to avoid gold-aluminum wire bonds at the devices or substrates, thus eliminating the controversial Au-Al intermetallic problem.[1] Extreme miniaturization and circuit complexity requirements led to a two-level metallization system with crossovers and the capability of mounting some devices and components directly over the metallization.

The metallization system developed meets many of the universal characteristics and requirements desired in a hybrid microcircuit including:

1. Extreme miniaturization.
2. Fine line and space resolution.
3. Monometallic wire, beam lead, ribbon and lead frame bonding capability (i.e., Au-Au and Al-Al).
4. Eutectic die attachment capability (i.e., Au-Si and Al-Ge).
5. Solder device and component attachment compatibility (i.e., Au-Sn, Pb-Sn, and Pb-In).
6. Mounting of devices over the metallization.
7. Two-level metallization for crossovers (necessary for interconnecting bipolar, MOS, and CMOS integrated circuits).
8. Process compatibility and viability (capable of withstanding temperature, etchant compatibility, equipment availability, etc.).

The metallization system is based on W-Au/SiO_2/Al/SiO_2. The first two layers of W-Au are sequentially sputtered films photodefined to form Au conductors and bonding areas, W crossunders, and transition areas for contacting Al. A SiO_2

insulating layer is next sputtered and photodefined to open windows to the Au bonding areas and vias for the W-Al transition areas. An aluminum layer is evaporated and photodefined to form Al conductors, crossovers ($W-SiO_2-Al$), and bonding areas. A final layer of SiO_2 is sputtered and photodefined to open windows to the Au and Al bonding areas; otherwise it covers the complete circuitry and permits mounting of components directly over the circuitry. Gold and aluminum are always physically separated on the substrate but can be electrically connected by the tungsten transition layer (see Figs. 1 and 2). Monometallic (Au-Au and Al-Al) wire bonding is then possible. Substrate materials found to be suitable were polished sapphire and fine grained alumina ceramic.

In order to develop the processing techniques, characterize, and determine feasibility of the metallization system, several different test circuits were designed, fabricated, and tested. Throughout the investigation it was assumed that the presence of aluminum-terminated devices would require hermetic packaging, and, therefore, effects of moisture and corrosive environments were not considered.

Covered in order are: 1) Micro Actuator requirements, 2) Design considerations and developmental approach, 3) Processing, 4) Test and evaluation results, and 5) Discussion and conclusions. Design rules for the technology are included as Appendix I. Background information on multi-level hybrid circuit techniques considered for this application is in Appendix II.

Details of the metallization procedures and processes are brief here but are covered in considerable depth in a companion report.[2] Those interested in this aspect are referred to it.

SLL MICRO ACTUATOR HYBRID CIRCUIT REQUIREMENTS

The circuit design, device component choice, and package configuration was the responsibility of Department 8180. Therefore, the functional aspects of the circuit will not be discussed except to say that analog, digital, memory, and output circuit functions were required. In the first iteration, the circuitry was divided into four substrates which in turn were to be mounted on a metal plate assembly with connectors for input and output at each end (see Fig. 3).

A summary of the device and component types, mounting, and bonding criteria for each substrate and for the complete circuitry is shown in Table I. It may be noted that the preponderance of wire bonds on the devices is to aluminum bonding pads. Considering the dimensions of the substrates, the density of interconnections and bonding areas is quite high.

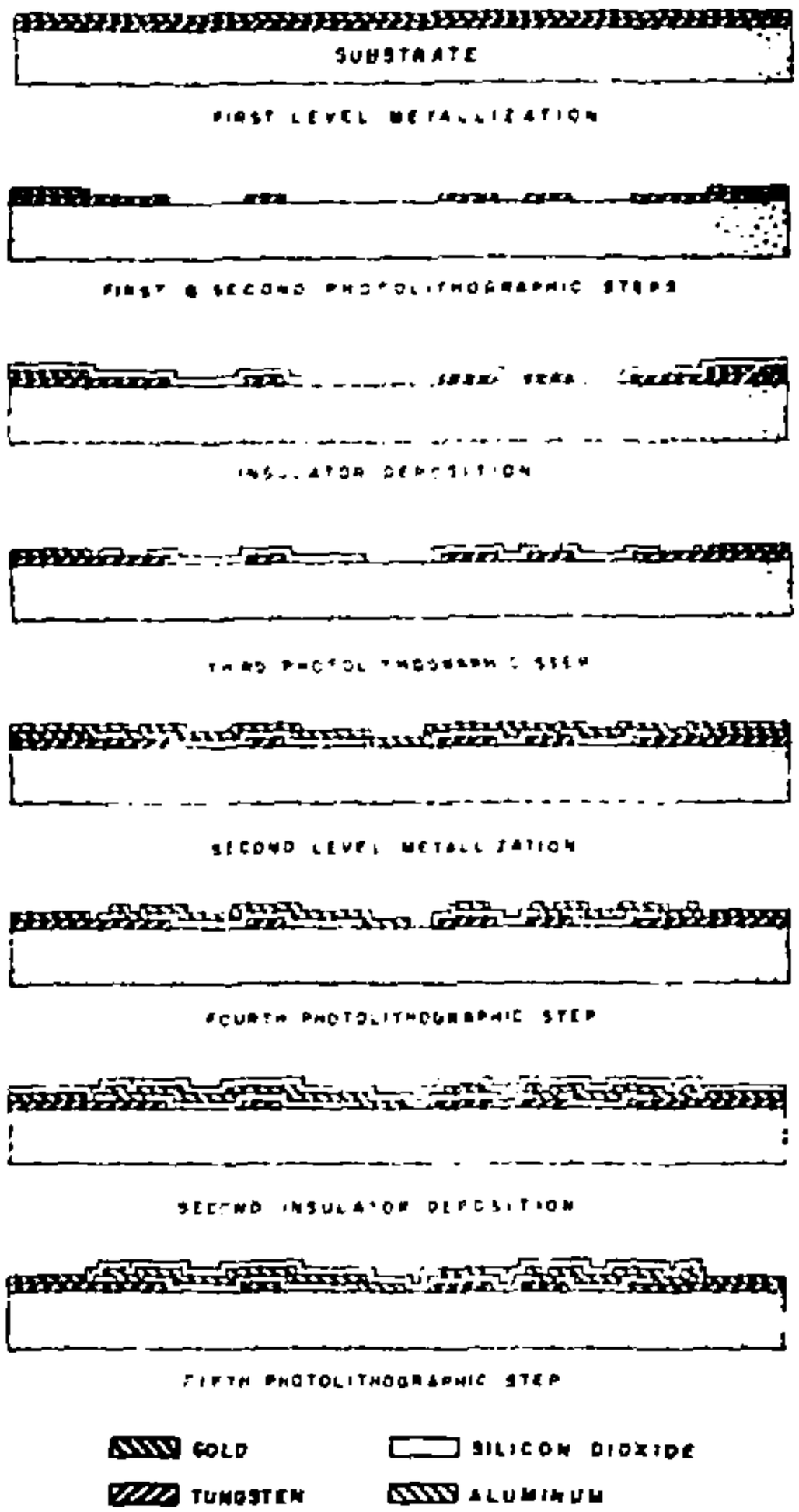
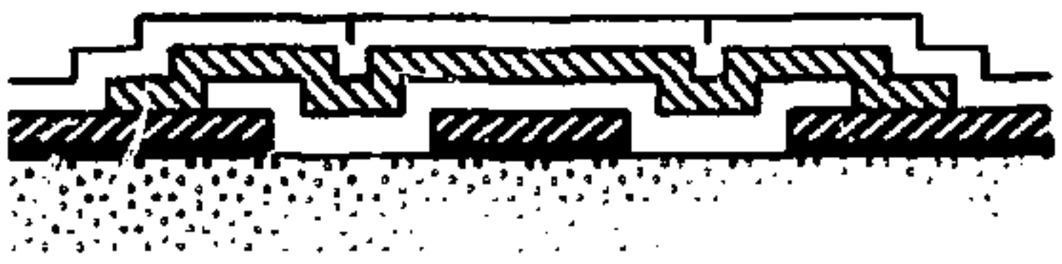
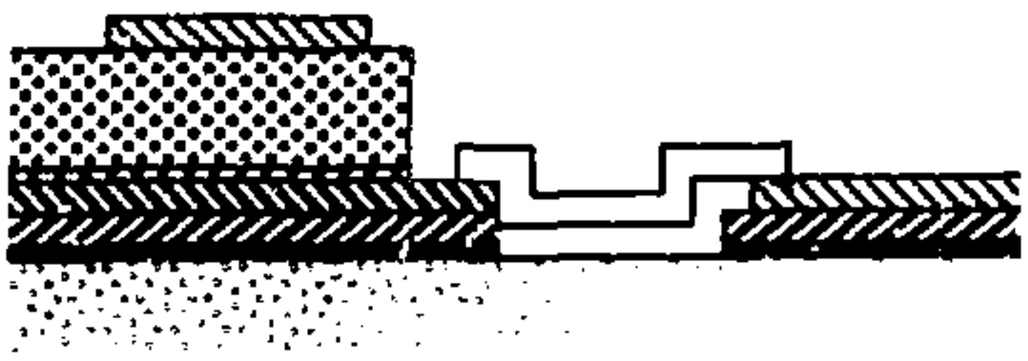


Fig. 1. Metallization deposition and definition sequence.

(a) An Au-W-Al transition with a W-SiO_2-Al crossover, Au and Al conductors and bonding pads.



(b) A typical W-SiO_2-Al crossover.



(c) Die attachment for Al-Al wire bonding.

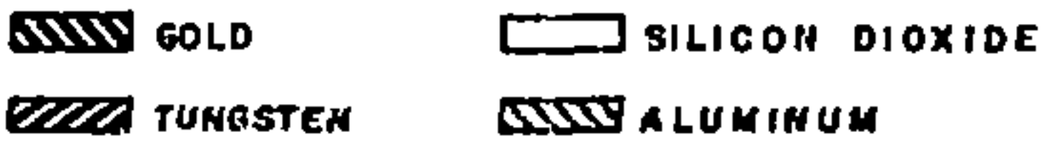
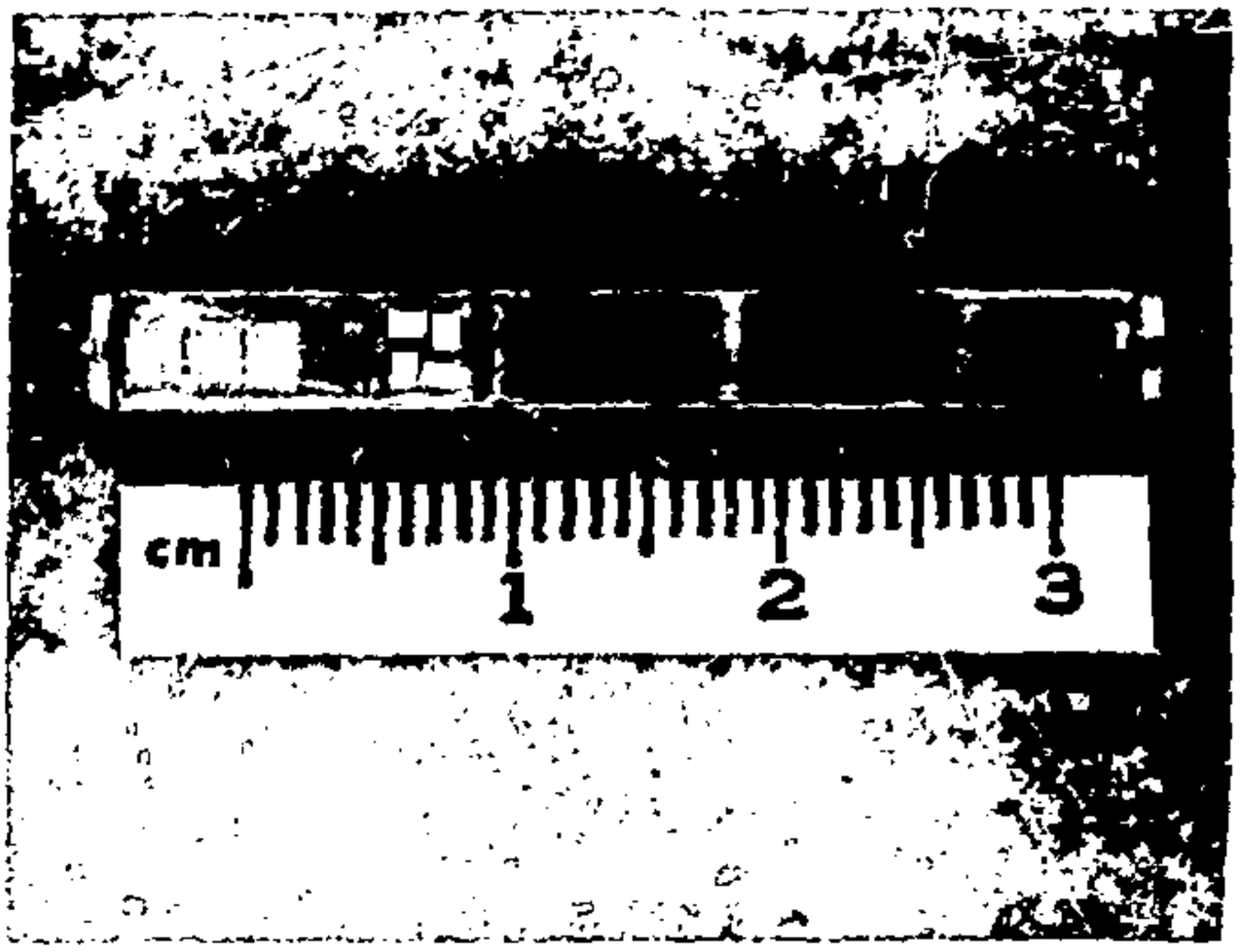
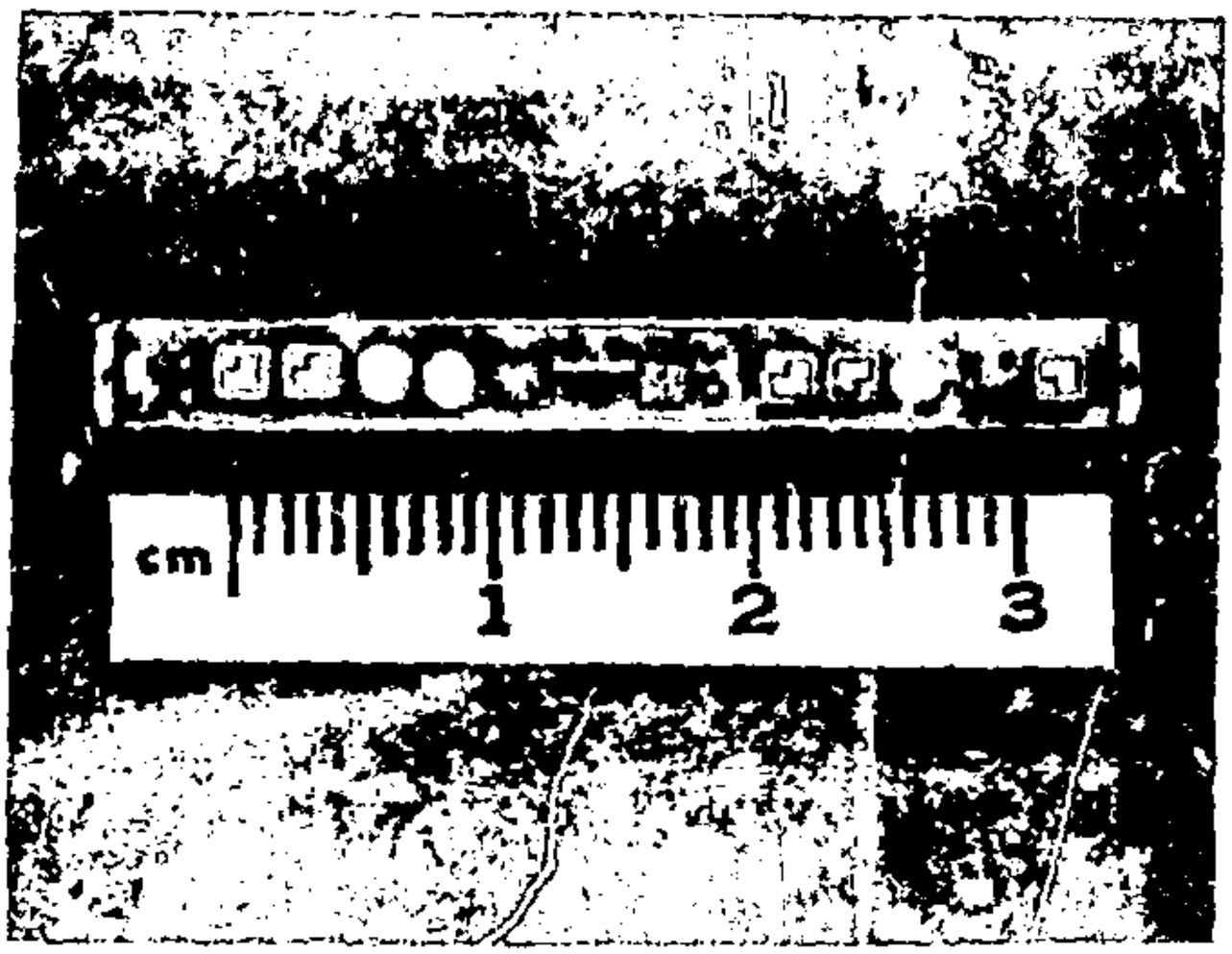


Fig. 2. Typical metallization structures and details.



(a) Top View



(b) Bottom View

Fig. 3. Mockup of Micro Actuator hybrid circuits.

TABLE 1

DEVICES, COMPONENTS AND SUBSTRATE FEATURES

	SUBSTRATE NO.				
Devices	1	2	3	4	Total
IC's (MOS & Bipolar)	3	1	2	0	6
Transistors	0	1	2	5	8
Diodes & Zeners	0	1	5	1	7
Electro-Optic	0	3	0	0	3
Capacitors	0	4	0	0	4
Resistors	0	7	7	4	18

	SUBSTRATE NO.				
Feature	1	2	3	4	Total
Al Bonding Pads	101	36	59	22	213
Au Bonding Pads*	13	32	7	8	60
Die Attach Pads	0	1	7	6	14
Solder Pads	0	8	0	0	8
Resin Pads	3	4	9	4	20
Vias	2	21	16	8	47
Crossovers	14	30	7	8	59
Length, mm	22.66	16.21	24.59	14.27	-
Width, mm	4.191	4.191	3.810	3.810	-
Thickness, mm	0.381	0.381	0.381	0.381	-
Area, mm^2	94.84	67.74	93.55	54.19	310.96

* Includes output pads and die attach pads

A

Environmental requirements were not severe but required consideration. The following general criteria were expected:

Temperature Range	-55°C to +125°C
Maximum Voltage	41 volts
Maximum Power	1.2 watts
Shelf Life	15 years
Operation Time	Intermittent
No. of Operations	Undefined but limited
Packaging	Hermetically sealed
Size	Configuration & package size fixed

Reliability was a prime consideration and must be high since redundancy was not planned. The circuit was to be operated only intermittently; therefore, long-term electrochemical and electromigration problems are mitigated. The package was to be hermetically sealed, which, if properly done, should eliminate humidity and corrosion problems.

From a hybrid circuit metallization viewpoint, the following general requirements are applicable:

1. Small size, thin substrates.
2. Good thermal conductivity; heat generated is in excess of 1 watt when operated.
3. Multilivel metallization with crossovers and interconnecting vias between levels of metallization.
4. Conductors, crossovers, and vias must be insulated since some devices will be attached with adhesive over the metallization.
5. Line widths and spacings must approach 0.025 mm (1 mil) in places.
6. Electrical conductivity of at least one of the metal levels must be high.
7. Dielectric strength and insulation resistance of the insulating material must be stable and adequate.
8. The metallization must be compatible with both aluminum and gold wire bonding.
9. The substrate and metallization should be compatible with gold eutectic die attach and soldering techniques and withstand the temperatures (up to 370°C) involved.

10. The metallization must be versatile to accomodate the diversity of circuitry (analog, digital, etc.), devices, and components.
11. The hybrid technique must be flexible to accommodate the inevitable circuit changes and should, from an economic viewpoint, have wider usage than the present application.
12. Fabrication techniques must be viable from a manufacturing viewpoint and projected yields must be reasonable.

The rather stringent requirements are brought about primarily by the small size and geometrical requirements of the package and the diversity of device and component types necessary to perform the desired circuit function. Present hybrid circuit techniques, such as used in the MCCS project based on single level metallization, were obviously inadequate.

DESIGN CONSIDERATIONS AND DEVELOPMENTAL APPROACH

In this section we consider the requirements in terms of techniques and outline the development approach followed. The important requirements are listed below:

Substrates

Size - As shown in Fig. 3 and Table 1.
Thickness - 0.38 mm max.
Separation Technique - Preferably laser scribing.
Smoothness - $25.4 + 10^{-6}$ mm max.
Camber - 0.001 mm/mm max.
Thermal Conductivity - Reasonably high.
Mechanical Strength - Equivalent to alumina.
Process Compatibility - Deposition, etchant compatibility.

Resolution

Minimum Line Width - 0.0508 mm (2 mils).
Minimum Spacing - 0.0254 mm (1 mil).
Minimum Via Width - 0.0508 mm (2 mils).
Registration - 0.02 mm overall.

Metallization

Conductivity - 0.04 - 0.04 ohms/square max.
Adhesion - Excellent from -55°C to +400°C.
Stress - Sufficiently low from -55°C to +400°C.

Thermal Expansion - Matched to substrate if possible.

Etchability and Etchant Compatibility - Required.

Bondability - Au-Au and Al-Al.

Solderability - Pb-In (50-50 wt. %).

Die Attach Capability - Au Si or Au Ge eutectics.

Stability - Over the temperature range -55°C to +200°C.

Insulator (Dielectric)

Dielectric Strength - Adequate for ~ 50 v.

Permittivity - Preferably below 4 ϵ_o.

Leakage Current - Low nanoampere range.

Compatibility - With metal system and substrate.

Stability - Over the temperature range -55°C to +200°C.

Thermal Expansion and Stress - low and matched.

Adhesion - Excellent to metal system and substrate.

Various multilayer metallization and interconnection techniques developed for hybrid microcircuits and semiconductor devices were investigated for this project. A brief discussion of the various techniques and their applicability may be found in Appendix II. They basically fall into five categories:

1. Multilayer Metallized Ceramic
2. Thick Film
3. Thin Film
4. Thick/Thin Film Combinations
5. Metallized Plastic

In each category, there are many variations and adaptations for specific applications.

Development Approach

In attempting to choose the optimum technology, a necessary step was to evaluate the requirements in terms of the options open to us. In Table 2 we have listed some of the requirements and compared them with the hybrid circuit techniques which have merit for this application (discussed in Appendix II). The listing is not all inclusive but is indicative that two techniques have the best chance of success, namely:

TABLE 2

APPLICABLE HYBRID CIRCUIT TECHNOLOGY OPTIONS

MULTILAYER TECHNIQUE*	SUBST. SIZE	SUBST. THICKNESS	LINE WIDTH & SPACING	Au-Au BONDING	Al-Al BONDING	DIE ATTACH	SOLDERABLE	BEAM LEAD BONDING	CONDUCTANCE	INTERLAYER CAPACITANCE	CROSSOVER DIEL. STRENGTH	COMP. DENSITY	COMP. COMPATIBILITY	REGISTRATION
MULTILAYER CERAMIC	N	N	N	Y	N	Y	Y	Y	Y	N	Y	Y	M	M
THICK FILM														
a) Screened	N	M	N	Y	N	Y	Y	Y	Y	N	Y	N	N	M
b) Photodefined	M	M	M	Y	N	Y	Y	Y	Y	M	Y	Y	N	Y
c) Photodefined & Smooth Subst.	Y	M	Y	Y	N	Y	Y	Y	Y	M	Y	Y	N	Y
THIN FILM														
a) Three Level (2 metal level)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
b) Beam Crossover	Y	Y	Y	Y	N	Y	Y	Y	Y	Y	Y	N	N	Y
c) Silicon Substrate	Y	Y	Y	N	Y	N	N	M	M	M	Y	Y	N	M
METALLIZED PLASTIC (Includes STD & BLIP)	Y	Y	Y	Y	N	M	M	M	Y	M	Y	Y	N	N
THIN/THICK FILM														
a) Screened Thick Film and Thin Film	N	Y	N	Y	M	Y	Y	Y	Y	M	Y	M	Y	M
b) Photodefined Thick Film and Thin Film	Y	Y	Y	Y	M	Y	Y	Y	Y	M	Y	Y	Y	M

* See Appendix I for Details

Legend: N = No, M - Maybe, Y = Yes

1. Thin film, three layer (2 metal levels).

2. Thick film, three or more layers, photodefined.

Both techniques require smooth substrates and photolithographic techniques to meet the resolution requirements.

The desirability of a monometallic wire bonding system then required gold-gold and aluminum-aluminum bonding capability. Since there were no proven aluminum thick film pastes at the time (one has recently been marketed but not evaluated), such a scheme was not possible with thick film techniques. With thin film, these criteria then require both aluminum and gold metallization. With two thin film metal layers this is possible.

Thin film techniques were chosen for the development for other reasons as well, however. First, thin film techniques have been in use at Sandia. Second, thin film deposition equipment and photolithographic techniques were available whereas thick film had not been completely developed for multilevel work. Third, thin film materials and techniques were better understood than thick film. Fourth, it is difficult to photodefine thick films with fritted conductors. Fifth, based on trends in the semiconductor industry and future hybrid requirements, thin film techniques offer at least an order of magnitude improvement in resolution, and resultant reduction in size over thick film techniques.

Specific material choices were made and included the following:

Substrates · Fine grained alumina (MRC superstrate or equivalent) and polished sapphire were used successfully. Dielectric strength and leakage current characteristics of the SiO_2 layer was much better on the polished sapphire because of the smooth surface. For the application being considered, extreme miniaturization and fine line resolution were necessary, justifying the more costly polished sapphire.

Metallization - The requirements for monometallic bonding and two-level metallization lead immediately to the choice of gold and aluminum for the two conductors and bonding layers. These two metals permit the use of established techniques for thermocompression (Au-Au) and ultrasonic (Al-Al) wire bonding to interconnect devices with gold and aluminum terminations respectively. The gold layer also serves as a base for eutectic die attach, gold ribbon, and beam lead bonding. Both metals have good conductivity and can be readily deposited in thin film form.

Physical separation of the gold and aluminum was accomplished by using tungsten as a lateral transition layer which underlies both the gold and aluminum. The lateral transition permits wide Au-Al separation (i.e., ≥ 0.025 mm or 1 mil)

and, except for a small amount of surface migration, effectively eliminates any diffusion problem. Tungsten simplifies the crossover design in that it can be used as the crossunder conductor with aluminum as the crossover conductor (i.e., W-SiO_2-Al). Tungsten also serves as an effective solder stop.

Both tungsten and molybdenum were evaluated for the transition layer for several reasons: 1) Good thermal expansion match with Al_2O_3, 2) Excellent adherence to Al_2O_3, 3) Metallurgical compatibility with gold and aluminum, 4) Adherence of SiO_2, and 5) Previous use on semiconductor devices.[3,4] Tungsten proved superior in adherence qualities, electrical stability with SiO_2, and etchant compatibility in preliminary studies; and, therefore, Mo was not investigated further.

Insulating Layers - SiO_2 proved to be an effective and etch compatible insulating layer for the crossover insulation. It has a low dielectric constant and high dielectic strength, as well as a low thermal expansion coefficient. It is widely used with aluminum on semiconductors.[5,6] RF sputtering from a SiO_2 target was chosen over other methods of deposition (i.e., reactive sputtering, CVD and evaporation) because of process simplicity and equipment availability. In thicknesses of approximately 1 μm, SiO_2 proved to have adequate dielectric strength and insulation resistance especially on metallized sapphire substrates for the 41 volt design requirement.

The second layer of SiO_2 permits epoxy or silicone attachment of devices and components over the conducting layers, crossovers, and resistors for miniaturization reasons. It also serves as an abrasion resistant layer during handling and as a solder stop during component attachment. Silicon dioxide becomes somewhat conductive over gold areas after 370°C processing temperatures because of Au-SiO_2 reaction.

PROCESSING

General - Discussion here is brief and is limited to metallization procedures. Die attach, soldering, bonding, and packaging procedures are omitted. The processes described are those which were convenient and successful in development. Some may be cumbersome from a production viewpoint, such as sputtering of relatively thick gold layers. Processes and procedures are covered in more depth in another report.[2] The processing sequence used is shown in Table 3.

Test Patterns - Four different test patterns as shown in Figs. 4 through 7 were designed for evaluation of the metallization system.

Table 3

DEVELOPMENT PROCESSING STEPS

Substrate Cleaning

↓

Tungsten Deposition

↓

Gold Deposition

↓

Gold - Tungsten Photolithography

↓

First SiO_2 Deposition

↓

First SiO_2 Photolithography

↓

Aluminum Deposition

↓

Aluminum Photolithography

↓

Second SiO_2 Deposition

↓

Second SiO_2 Photolithography

↓

Test and Evaluation

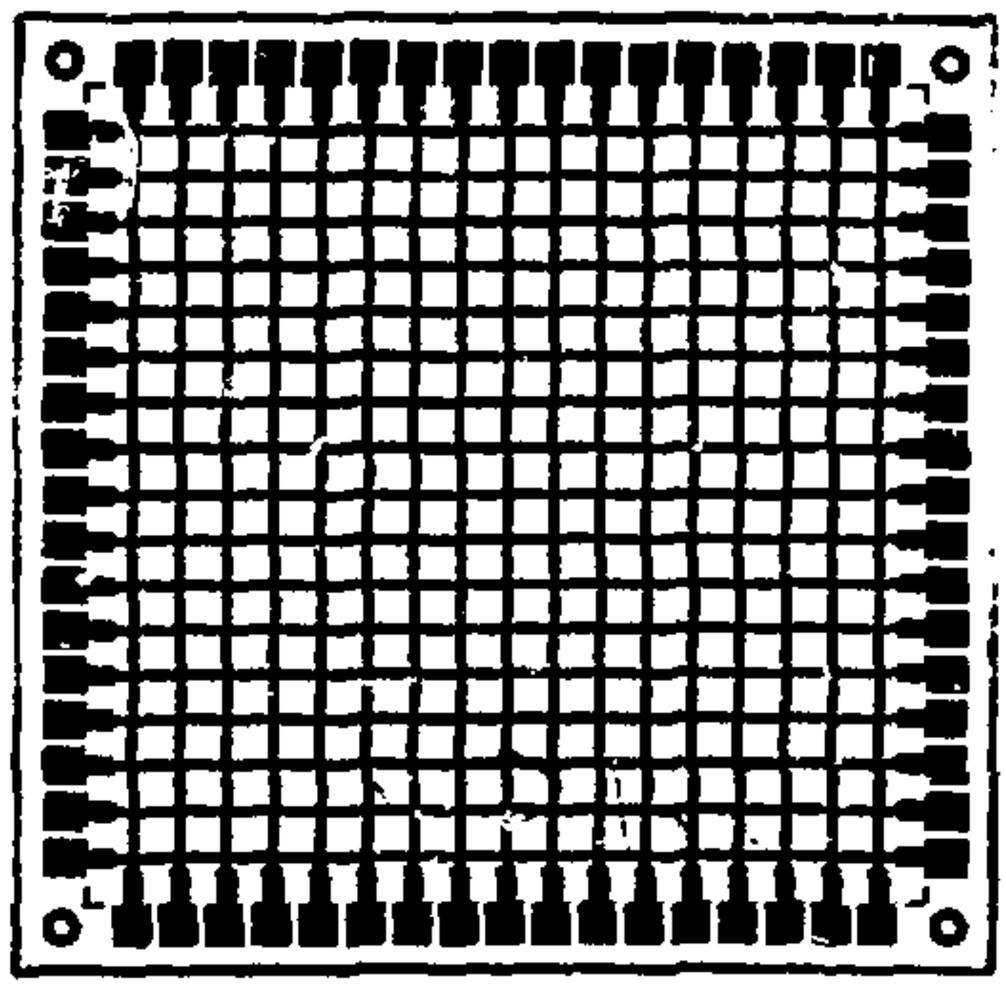


Fig. 4. Screenwire test pattern - Crossed, 0.254 mm wide, tungsten and aluminum conductors with gold terminations. There are 17 lines of each metal separated by the insulating layer, nine vias (Aℓ-W) interconnections, and 280 crossovers (W-SiO_2-Aℓ). Substrate size: 2.54 × 2.54 cm.

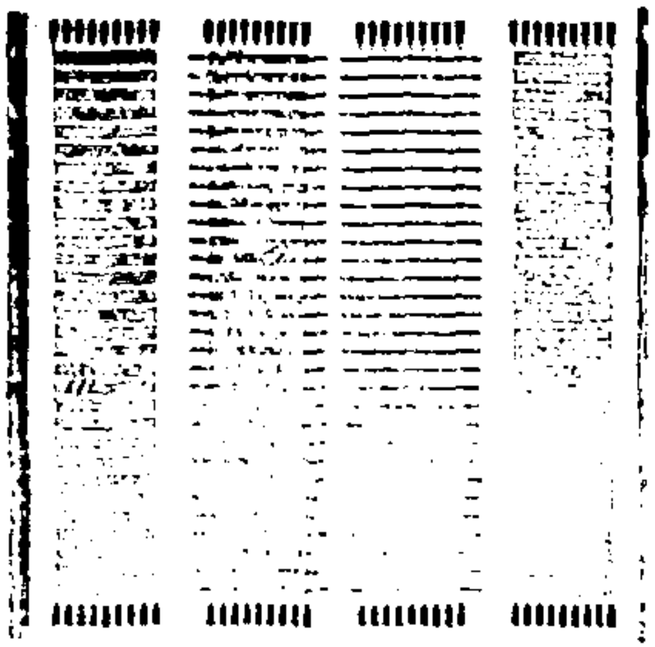


Fig. 5. Fine line test pattern - The first configuration consists of 9 tungsten conductors varying in width from 0.0762 to 0.0254 mm. Silicon dioxide covers the conductors and an array of 0.0762 mm wide aluminum segments are superimposed over the conductors but insulated from them. The next two configurations consist of 0.0762 mm and 0.0254 mm wide tungsten and aluminum line segments respectively joined by vias and crossing over 0.127 mm tungsten strips. The last configuration is similar to the second but without crossovers. Substrate size: 2.54 x 2.54 cm.

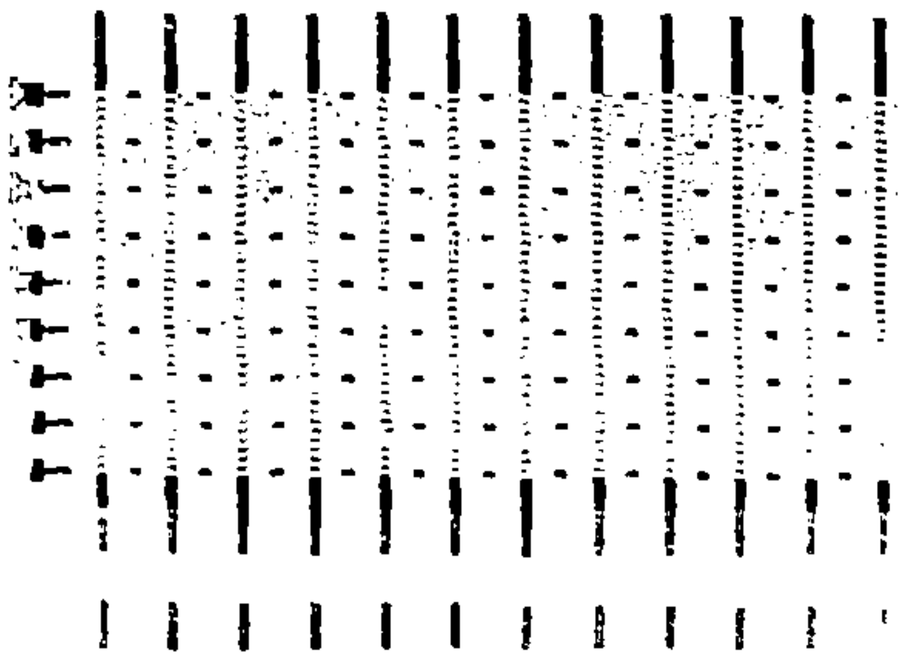


Fig. 5a. Section of fine line test pattern.

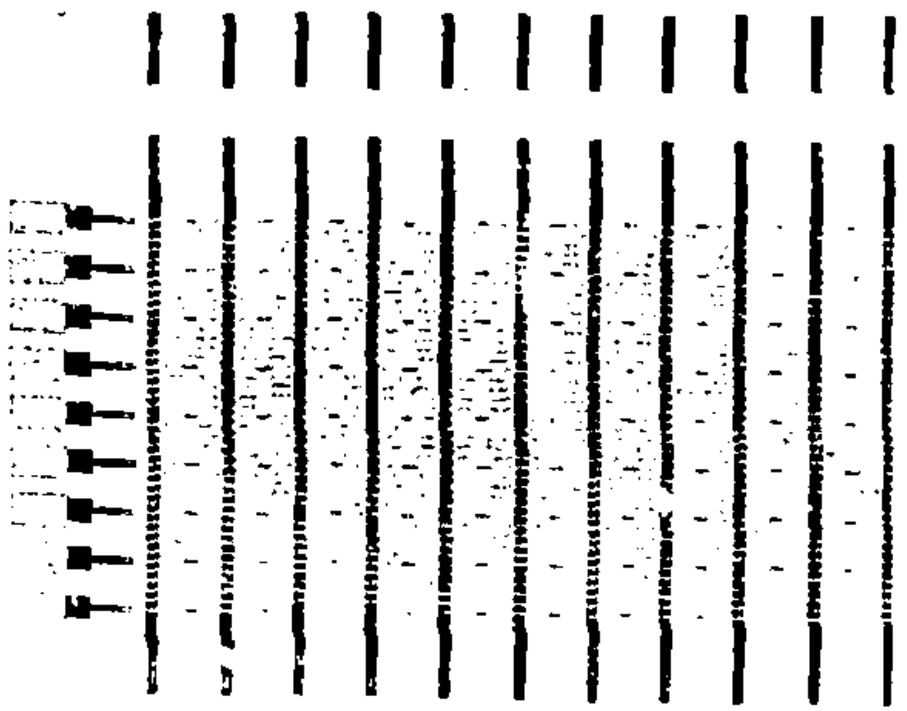


Fig. 5b. Section of fine line pattern.

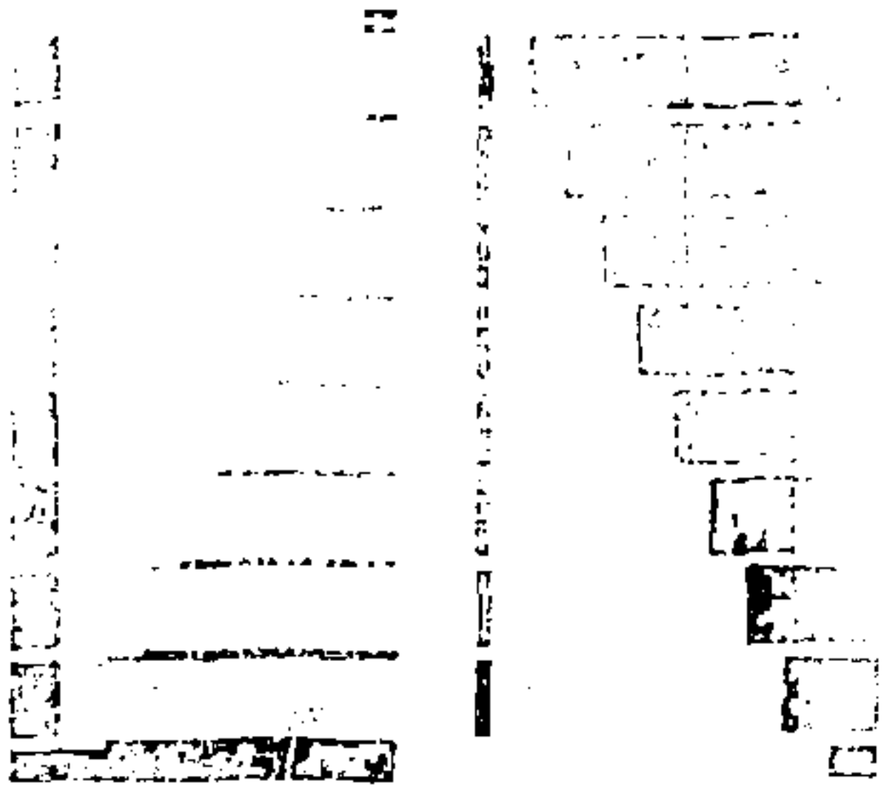


Fig. 6. Dielectric test pattern - 16 capacitors ($W\text{-}SiO_2\text{-}Al$) varying in area from 2.25 to .18 cm^2. The pattern is symmetrical but definition reversed on each half. Substrate size: 2.54 x 2.54 cm.

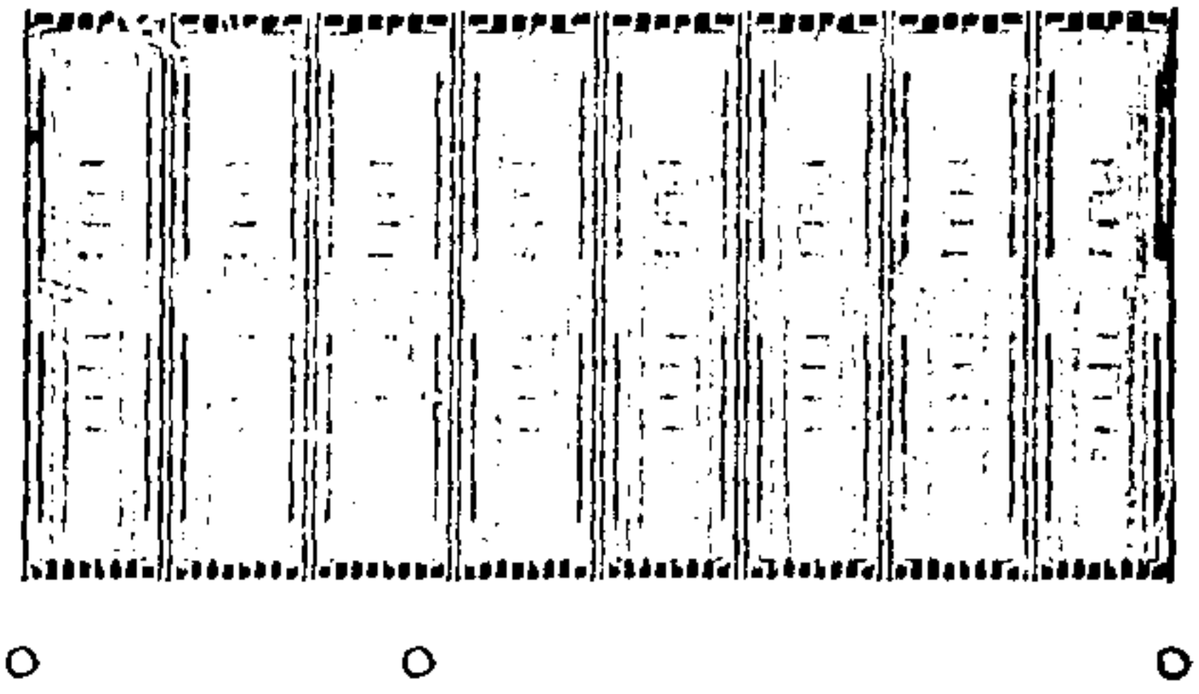


Fig. 7. Test circuit pattern - a circuit designed to simulate the interconnection of two MOS devices with 0.102 mm aluminum bonding pads on 0.203 mm centers. There are eight individual circuits on a sapphire substrate 2.54 x 3.81 cm in size. A blowup of a section is also shown.

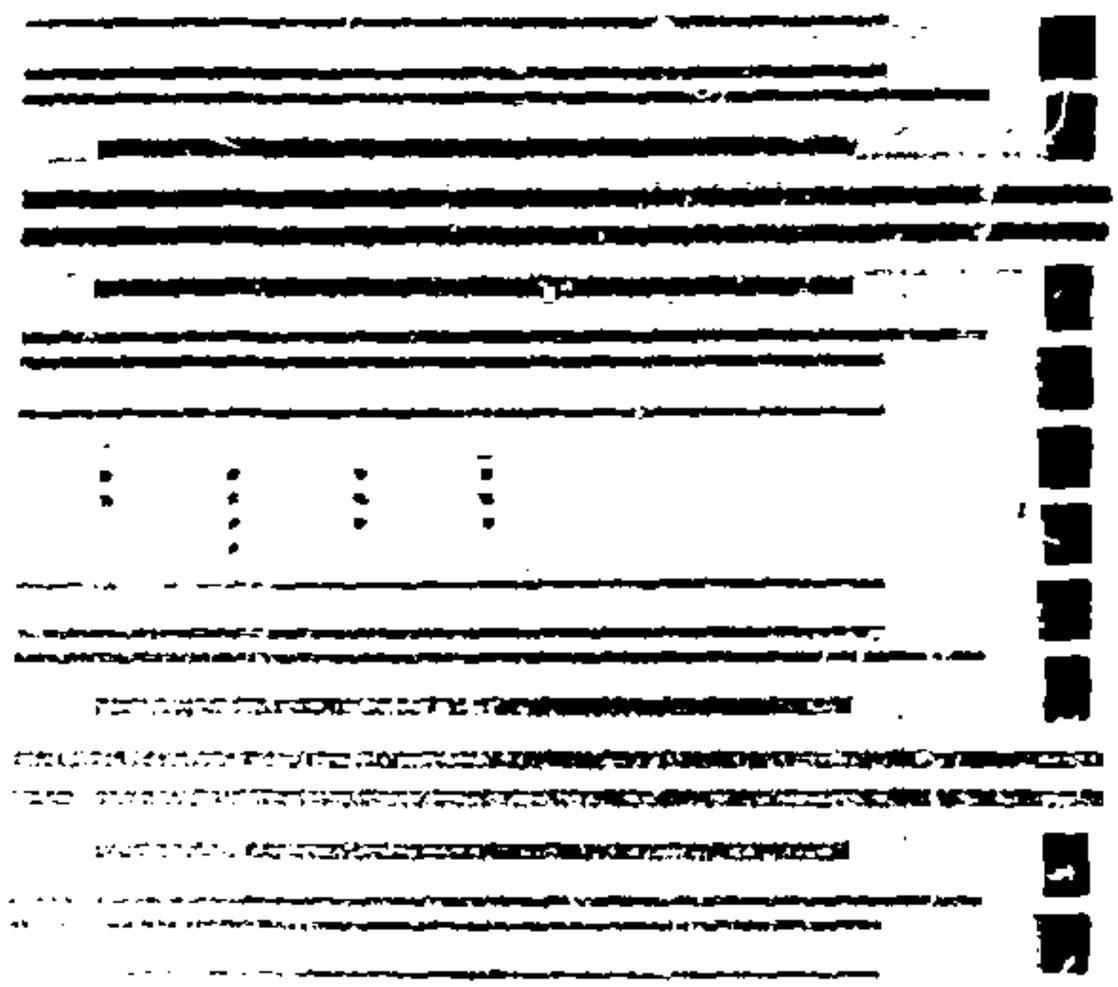


Fig. 7a. Section of test circuit pattern.

Mask Fabrication - Conventional emulsion masks (5.08 x 5.08 cm) were made from 20X masters. The following mask levels are required:

1. Gold definition (bonding pads and conductors).
2. Tungsten definition (W-Au conductors, crossunders, and W-Al transitions).
3. First insulator definition (vias and bonding pad openings).
4. Aluminum definition (W-Al transitions, conductors, and bonding pads).
5. Second insulator (bonding pads, die attach, and solder areas).

Substrate Cleaning - Substrates were cleaned by ultrasonic washing in trichloroethylene, acetone, detergent (Igepal CO-710), and deionized water and then rinsed in hot cascading deionized water and blown dry with nitrogen. These steps were followed by an air fire at 900°C for one hour. The cleaned substrates were stored in a glass container in a clean bench for a maximum of three days before use.

Metal and Insulator Deposition - Tungsten and gold were dc sputtered in sequence without breaking vacuum using a custom built multi-target sputtering module. RF sputtering was used for the SiO_2 deposition from SiO_2 target. The vacuum systems were Sergent Welch, 3102 Turbo molecular type. The sputtering parameters are shown in Table 4.

Aluminum was deposited using electron beam evaporation. After pumpdown, the substrates were outgassed at 300°C for one hour. Substrate temperature was kept below 125°C during actual deposition. After outgassing the charge, deposition was maintained at a nominal 45 Å/sec using an automatic power controller. Pressure was maintained below 2×10^{-7} Torr during deposition. The vacuum system was a 6 inch NRC diffusion type with liquid nitrogen baffling.

Photolithography - All photoresist applications, exposure, development, and baking was done in class 100 facilities with yellow lighting. Kodak 747 Micro Neg (negative photoresist) was used successfully, but filtering and double coating by spinning was found necessary to minimize pinholes.

A Preco model 650 alignment and exposure system was used for pattern alignment and exposure. Photoresist procedures were in accordance with the manufacturer's recommendations. After resist removal, substrates were cleaned in trichloroethylene, acetone, deionized water, and isopropyl alcohol and blown dry with nitrogen.

Etchants, concentrations, and temperatures used successfully for the various layers are shown in Table 5. After etching, all substrates were immediately rinsed in deionized water. Etching parameters, once established, were closely adhered to during development. Some undercutting was desirable in the etching steps to provide sloped contours for good film coverage and dielectric strength of the insulating

Table 4

Sputtering Parameters for Tungsten, Gold, and Silicon Dioxide

Parameter	Tungsten	Gold	Silicon Dioxide
Target Diameter, cm	15.24	15.24	2..32
Target-Anode Spacing, cm	6.35	6.35	7.6
Substrate Temperature, °C	3..	3..	25
Argon Pressure, μm Hg	3.	30	6
Argon Flow Rate, SCCM*	2..	2..	65
Nitrogen Flow Rate, SCCM*	--	--	--
Sputtering Voltage, KVDC	4.5	3.5	--
Sputtering Power, W(RF)	--	--	500
Deposition Rate, Å/min.	165	33.	115

*SCCM - Standard Cubic Centimeters per Second corrected for Argon & Nitrogen

TABLE 5

ETCHANTS

A. Etchants, Concentrations, and Temperature

Layer	Etchant	Concentration	Temperature
Au	$KI + I_2 + H_2O$	1N	39°C
W	$K_3Fe(CN)_6 + Na_2B_4C_7 + H_2O$	5:0.25:100*	40°C
SiO_2	$HF + NH_4F$	1:7*	25°C
Al	$H_3PO_4 + HNO_3 + CH_3COOH + H_2O$	85:5:5:5**	45°C
Au_xAl_y	$KI + I_2 + H_2O$	as above	39°C

*By Weight **By Volume

B. Etchant Compatibility

Etchant For	Effect On Material Being Etched					
	Al_2O_3	Au	W	SiO_2	Al	SiO_2
Au	n	a	n	n	s(2)	n
W	r	n	a	n	x	n
SiO_2	n	n	n	a	s(2)	a
Al	n	n(1)	n	n	a	n
$AuAl_x$	n	a	n	n	s	n

n = nil, a = attacks, s = slight attack

Notes: 1. No effect in a 3 hour test at 48°C.

2. See text.

layers. It was also noted that if the substrate temperature was greater than ~ 125°C during the aluminum deposition, some Au-Al intermetallic formation was encountered at the Au-Al interface which could not be removed by the aluminum etchant. A short (few second) dip in KI + I_2 removed the alloy but required photoresist protection for any exposed aluminum since the gold etchant attacks aluminum. A slight pitting of aluminum caused by the second SiC_2 etch step was noted. Otherwise, excellent etchant compatibility was achieved and is summarized in Table 5.

Complete resist removal and cleanliness before the next deposition was found to be imperative.

TEST AND EVALUATION

General - Testing and evaluation was carried on concurrently with process development, and modifications introduced as difficulties arose. The test patterns were generally used for photolithographic, environmental, and electrical testing. A brief summary of some of the experimental tests and investigations is covered here.

Substrates used in the experiments were: 1) Single crystal sapphire, 25.4 mm (1 in.) finish, C axis parallel to the surface, 0.381 mm thick, and 2) Fine grained alumina (MRC Superstrate) 0.381 mm thick.

Metallization Studies - Good adhesion, low stress, good electrical conductivity, and minimal reaction up to temperatures of 370°C were desired characteristics of the metal layers. The W-Au system does not form any intermediate phases up to the boiling point of Au.[7] The W-Au system has been investigated by others as semiconductor metallization and is superior to Cr-Au or Ti-Au as far as diffusion and resultant resistivity changes at high temperatures in both air and vacuum up to 650°C are concerned.[8] No diffusion information could be found on the W-Al system, however. Therefore, air aging tests were conducted at 400°C on substrates coated with W-Au and W-Al and compared with Cr-Au. The results of sheet resistance measurements are shown in Figs. 8 and 9 and indicate no significant changes for the W-Au or W-Al system compared to the Cr-Au system which is known to exhibit considerable Cr diffusion through the Au at high temperatures. Auger analyses after aging showed no detectable W on the surface of the W-Au or W-Al samples. The slight increases in sheet resistance of the W-Al samples after 20 hours at 400°C is attributed in part to surface oxidation. Scanning electron microscope (SEM) photographs of fracture cross sections did show a slight hint of alloying at the W-Al interface after aging.

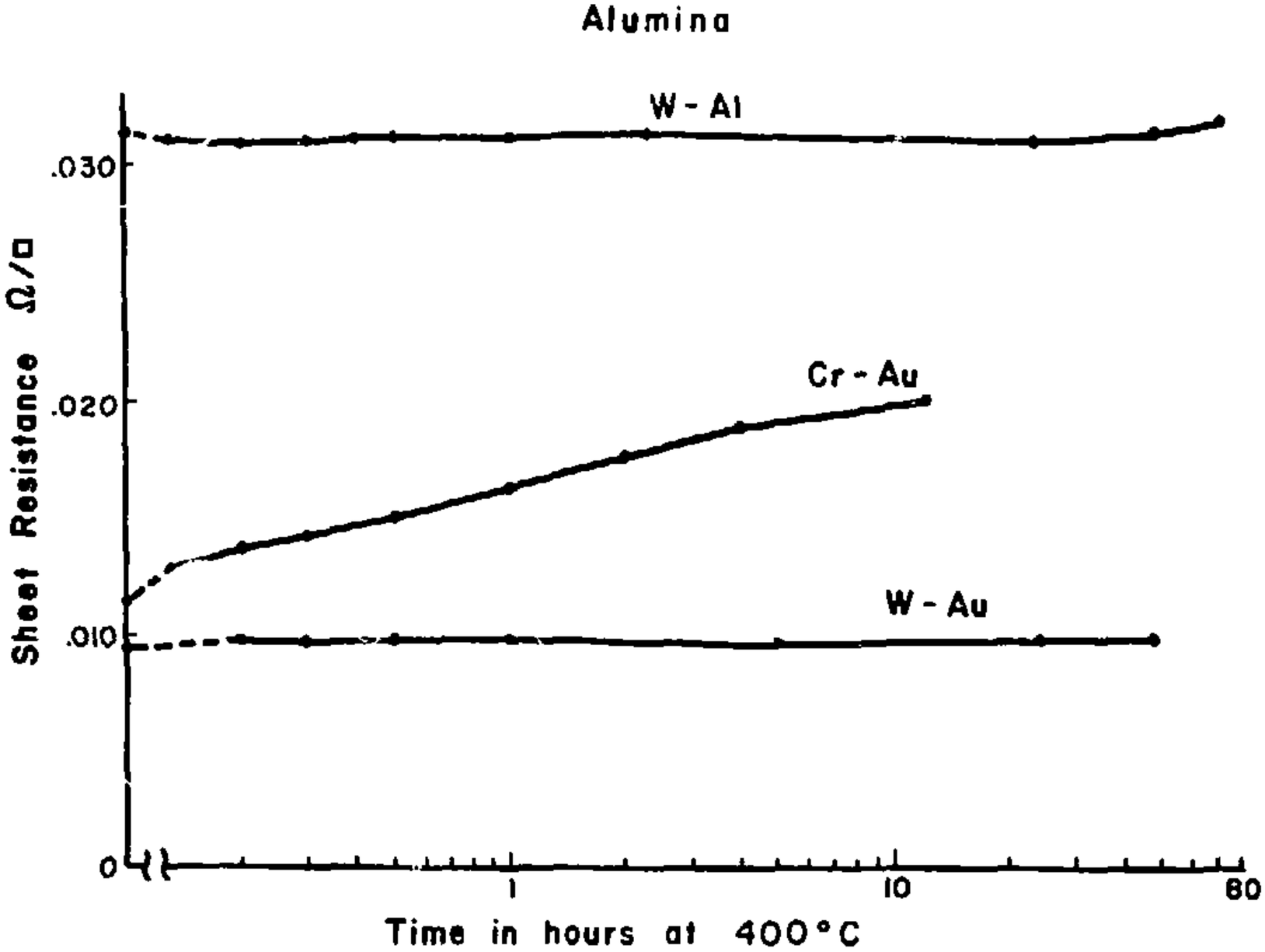


Fig. 8. 400°C aging studies on tungsten-aluminum, tungsten-gold and chromium-gold on alumina.

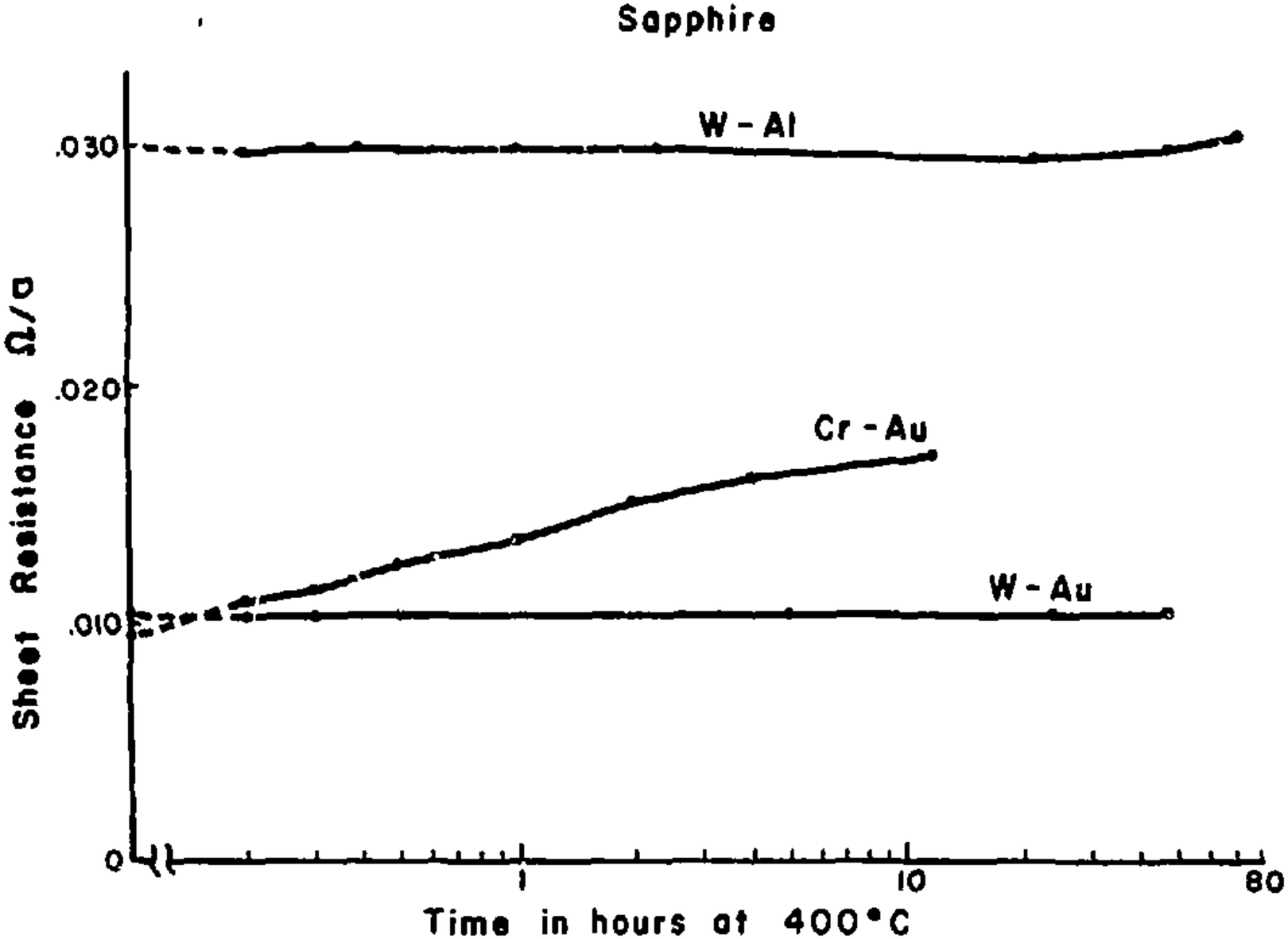


Fig. 4. 400°C aging studies on tungsten-aluminum, tungsten-gold and chromium-gold on sapphire.

If true, it is considered insignificant for the short processing times required at 370°C for eutectic die attachment.

The tungsten layer in thicknesses of ~ 1 μm is a densely packed columnar structure of medium feature size (~ 1000 Å) with density of ~ 95% that of the bulk value. The resistivity ranged from 30-38 μohm-cm for films up to 3 μm thick which is 6 to 7 times the bulk value of 5.6 μohm-cm. This is a limitation of the dc sputtering technique used. Reported values obtained by others are 20-30 μohm-cm using RF bias sputtering[9] and 8-20 μohm-cm using triode sputtering.[10]

Adhesion of the tungsten in thicknesses of 0.03 to 3 μm to both sapphire and alumina was found to be excellent. It was not necessary to use a Ti adherence layer or Ti-W alloy as others have when depositing W on SiO_2.[11] The adhesion of Au to W was also found to be excellent and is attributed to the immediate sequential sputter deposition of W-Au. Adhesion (and indirectly stress) of all films was initially checked using the adhesive tape test and temperature shock from -196°C to +200°C with 10-15 sec dwell at room ambient for 10 cycles. Temperature aging and cycling tests as well as Au and Al bonding studies will be reported on later. The composite W-Au/SiO_2/Al/SiO_2 (thicknesses: 1.0, 2.0, 1.0, 1.0 μm, respectively) withstood adhesion testing without lifting, crazing, or cracking.

Resistivity of the gold and aluminum films was well within +10% of bulk values (2.46 and 2.77 μohm-cm, respectively). SEM analyses indicated rather large feature size: ~ 10,000 Å for Au and ~ 5,000 Å for Al.

SiO_2 Insulator Studies - The RF sputtered SiO_2 insulator film used as the dielectric for the crossover structures (i.e. W-SiO_2-Al) was evaluated for dielectric and physical properties. The dielectric test pattern was used with three thicknesses of SiO_2 on sapphire substrates. The pattern consists of 16 capacitors per substrate, varying in area from 2.25 to 18 mm^2. The results are shown in Table 6 and Fig. 10. The yield figures refer to capacitors on the dielectric test pattern and not to the much smaller crossovers on the fine line pattern. Yield on crossovers will be discussed later. Sputtering from an SiO_2 target generally produces films which are somewhat oxygen deficient. The dielectric constant, density, and dielectric strength obtained, however, are quite close to what would be expected from good SiO_2 films.

Aging Studies - Test circuits using the screen wire and fine line test patterns (Figs. 4 and 5) were fabricated and tested. The top insulator (SiO_2) was left off in order to permit probe tests directly on the metallization. Two groups of samples using both fine grained alumina and sapphire substrates were fabricated. Group I

Table 6

Properties of RF Sputtered SiO_2 Films

PROPERTY	FILM THICKNESS Å		
	4250	9300	13,700
Capacitance, (pF/mm^2)	85	35	24
Dielectric Constant,	3.72	3.72	3.72
Dissipation Factor. (%)	<0.01	<0.01	<0.01
Capacitor Yield, (%)	21	34	44
Density, (g/cm^3)	--	--	2.22
Breakdown Voltage			
W-SiO_2-Aℓ, Ave. (V)	140	518	--
W-SiO_2-Aℓ, σ (V)	31	68	--
Dielectric Strength			
W-SiO_2-Aℓ, Ave. (V/cm)	3.3×10^6	5.6×10^6	--

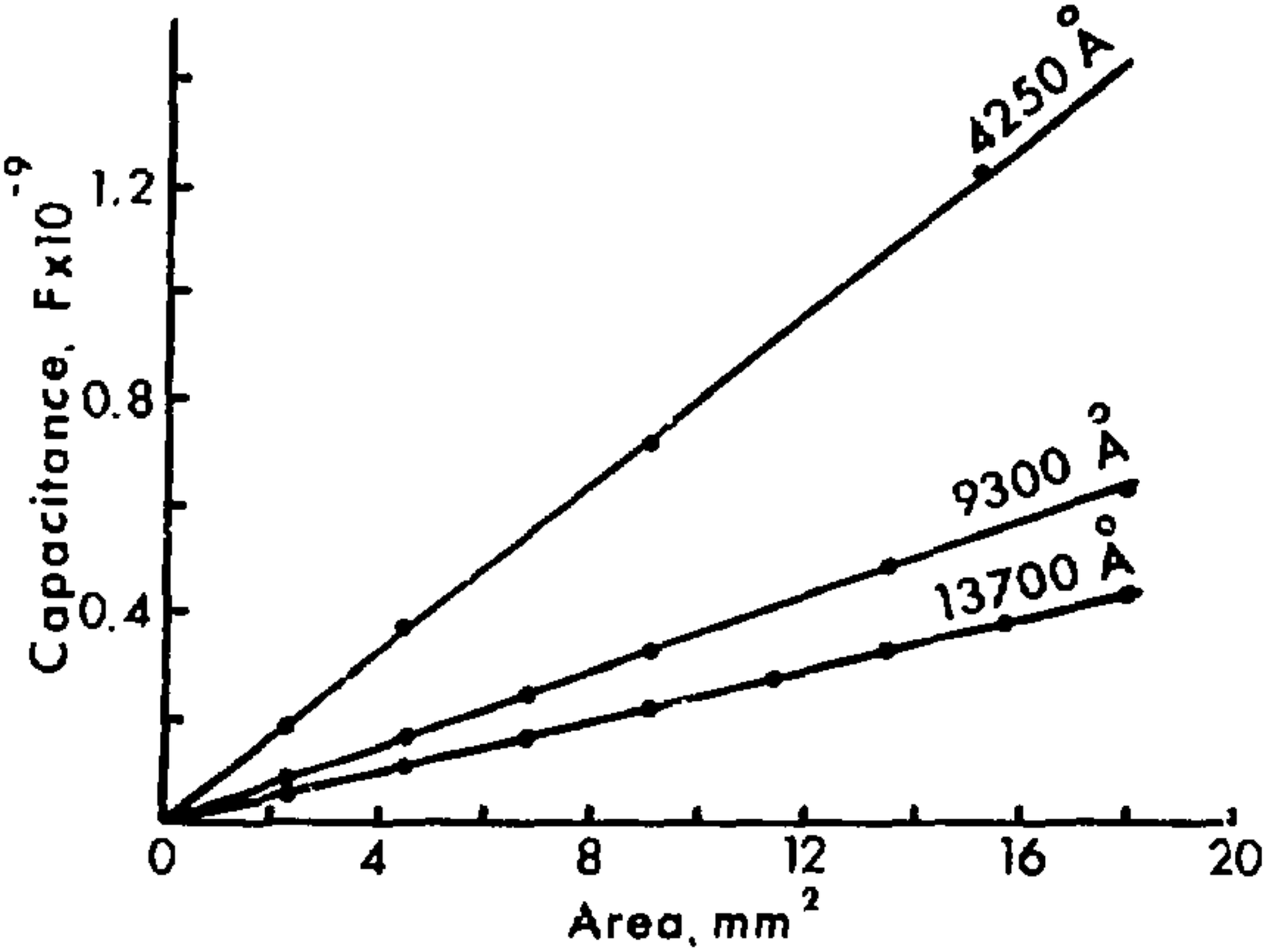


Fig. 10. Capacitance measurements on dielectric test pattern for three thicknesses of silicon dioxide.

was typical of film thicknesses used in the investigation of the metallization scheme. Here the first insulating layer of SiO_2 was approximately as thick as the tungsten layer. Group II was similar except that the SiO_2 layer was approximately one-half as thick as the first tungsten layer.

Before subjecting the samples to temperature cycling and aging tests, initial measurements of electrical parameters were made including:

1. Leakage Current of the W-SiO_2-Al crossovers on the fine line pattern on all groups. The crossover area was 0.127 mm (W) by 0.0762 mm (Al). The applied voltage varied from 25 to 100 VDC depending on the film thickness and substrate. Leakage current was difficult to measure below 1 nA because of instrumentation noise and pickup; therefore, values below 1 nA were not recorded.
2. Crossover Breakdown Voltage of a statistical quantity of the same crossovers referred to in 1 above. The voltage was ramped at ~ 15 V/sec. The current was limited by a 10,000 ohm resistor. This was a destructive test.
3. Via Continuity of the 0.0762 mm wide W-Al conductor links on the fine line pattern by measuring the resistance from termination to termination. There were 61 W-Al interfaces (i.e., vias) in each line, each being 0.0762 mm square.
4. Conductor Resistance of the 0.254 mm wide W and Al conductor lines on Group I and II samples was measured from termination to termination on the screenwire pattern. There were 17 crossovers (0.254 mm square on each line.
5. Contact Resistance of the 0.254 mm square vias (W-Al transitions) was measured on both groups using the screenwire pattern. A crossed contact (four point) method was used with 0.01 ADC applied between two terminals and the resulting voltage measured with a high impedance voltmeter across the opposing terminations. The voltage was reversed to check for non-ohmic behavior and the average of the two readings recorded. No significant non-ohmic behavior was noted.

After the initial measurements of the electrical parameters, the Group I samples were subjected to 110 temperature cycles -55°C to +150°C with approximately 5 minutes between temperature extremes. The electrical parameters were measured at the end of 10 and 110 cycles. The same samples along with Group II samples were then subjected to 500 hours at +150°C with electrical measurements made at the end of 10, 110, and 500 hours, Group I sapphire fine line pattern samples were then

subjected to 10 minutes at 400°C for the final test after which electrical parameters were again measured. All electrical measurements were made at room ambient conditions. The substrates were not packaged or sealed during testing.

Summaries of the aging test results are shown in Tables , through 11 and in Figs. 11, 12, and 13. In all cases, sapphire samples performed better than ceramic because of the smoother surface. The rougher surfaced ceramic substrates had to be subjected to a lower voltage during leakage current measurements. Average crossover breakdown voltage measurements were 1.5 to 2.5 times higher on sapphire than on ceramic. Group I samples fared better than Group II samples on leakage current and breakdown voltage because of the thicker first SiO_2 insulating layer. This is indicative that the insulating layer should be made thick enough to maintain an adequate margin on breakdown voltage and suggests that the layer should be as thick as or thicker than the tungsten crossunder in order to adequately cover the tungsten line edges where the SiO_2 is thinnest. Crossover yield was good. There were only 2 and 3 shorts out of 1230 tested for Group I sapphire and alumina respectively (see Table 7). While precautions for dust control were taken in photolithography, SiO_2 deposition was done outside clean room facilities. The shorts noted were readily identified under the microscope as pinholes in the SiO_2 layer. Voltage breakdown strength and leakage current of Group I sapphire samples were considered adequate for the application. The results on Group I alumina samples were considered good but indicative that thicker insulation or a lower operating voltage would be desirable.

Bondability - Various tests were conducted to determine the bondability of the gold and aluminum metallizations. One-mil aluminum and gold wires were bonded to the Al and W-Au metallization respectively and pull strengths at ~ 45° measured. Gold plated 0.381 mm wide standard lead frames were bonded to Au metallization and pulled to 90°. The number of tests was not large but indicative of good bondability of both the aluminum and gold surfaces. The results are briefly summarized in Table 12. Die attach to gold using Au-Si preforms at 370°C was successful on the few samples tested. Soldering using Pb-In solder was also investigated briefly. The gold layer wets readily, and, if care is not exercised, Au-Si and Pb-In spread rapidly on the surface. To stop this, the gold bonding areas can be limited in size with the underlying tungsten or the SiO_2 layers acting as a solder barrier.

Table 7

Crossover* Leakage Current, nA @ 25°C

Group & Metallization	Value	Initial	Temp. Cycling -55°C to +150°C Post 110 Cycles	Temp. Aging at +150°C Post 500 Hrs.	+400°C Post 10 Min.
I. Sapphire	No. Tested	1230	123	123	123
W ~1 μm	Voltage	100	100	100	100
Au ~2 μm	No. Shorts	2	0	0	0
SiO_2 ~1 μm	No. 1-5 nA	0	0	3	6
Al ~1 μm					
I. Ceramic	No. Tested	1230	123	123	
Same	Voltage	100	100	100	
as	No. Shorts	3	2	0	NT
Above	No. 1-5 nA	54	6	1	
II. Sapphire	No. Tested	861		123	
W ~1 μm	Voltage	50		50	
Au ~2 μm	No. Shorts	1	NT	0	NT
SiO_2 ~0.5 μm	No. 1-5 nA	1		0	
Al ~1.0 μm					
II. Ceramic	No. Tested	1148		123	
Same	Voltage	25		25	
as II	No. Shorts	12	NT	1	NT
Above	No. 1-5 nA	30		1	

* W-SiO_2-Al crossovers; size: W = 0.127 mm, Al = 0.0762 mm, (fine line pattern).
NT - Not Tested

Table 8

Crossover* Breakdown Voltage, V @ 25°C

Group & Metallization		Initial	Temp. Cycling -55°C to +150°C Post 110 Cycles	Temp Aging at 150°C Post 500 Hrs.	400°C Post 10 Min.
I. Sapphire	No. Tested	70	69	96	96
	Min.	326	378	280	289
	Max.	655	648	635	601
	Avg.	518	549	533	512
	σ	68	67	74	62
I. Ceramic	No. Tested	96	93	96	
	Min.	112	143	107	
	Max.	302	277	274	NT
	Avg.	231	229	222	
	σ	34	27	34	
II. Sapphire	No. Tested	95		91	
	Min.	91		104	NT
	Max.	211	NT	188	
	Avg.	140		141	
	σ	31		19	
II. Ceramic	No. Tested	94		96	
	Min.	43		45	
	Max.	151	NT	116	NT
	Avg.	75		83	
	σ	15		17	

* W-SiO_2-Al crossovers, size: W = 0.127 mm, Al = 0.762 mm (fine line pattern).
** See Table 7 for metallization thickness
NT - Not Tested

Table 9

Via* Continuity, ohms @ 25°C

Group & Metallization**	Value	Initial	Temp. Cycling -55°C to +150°C Post 110 Hrs.	Temp. Aging at 150°C Post 500 Hrs.	400°C Post 10 Min.
I. Sapphire	No. lines	8	8	8	8
	Min.	39.8	40.2	40.2	40.4
	Max.	42.1	42.8	42.1	48.4
	Avg.	40.7	41.0	40.9	41.4
I. Ceramic	No. lines	7	7	7	
	Min.	45.2	45.6	45.7	
	Max.	49.7	51.3	53.2	NT
	Avg.	46.7	47.3	48.1	
II. Sapphire	No. lines	7	7	3	
	Min.	66.1	61.6	68.0	
	Max.	118.1	100.4	80.2	NT
	Avg.	70.8	72.8	75.3	
II. Ceramic	No. lines	7	7	8	
	Min.	47.0	47.5	47.4	
	Max.	54.3	60.8	54.9	NT
	Avg.	50.6	51.6	50.8	

* W-Al transitions on Group I & II, 61 per line, 0.0762 mm square.
** See Table 7 for metallization thicknesses.
NT - Not Tested.

Table 10

Conductor* Resistance, ohms @ 25°C

Group & Metallization**	Value	Initial	Temp. Cycling -55°C to +150°C Post 110 Cycles	Temp. Aging at +150°C Post 500 Hrs.	400°C Post 10 Min.
I. Sapphire Al Lines	No.	17	17	17	17
	Min.	4.5	4.4	4.5	4.5
	Max.	4.9	5.0	4.9	5.1
	Avg.	4.6	4.6	4.7	4.7
	σ	0.1	0.2	0.1	0.2
I. Ceramic Al Lines	No.	17	17	15	NT
	Min.	5.4	5.4	5.6	
	Max.	8.2	7.3	7.5	
	Avg.	6.0	6.0	6.1	
	σ	0.6	0.5	0.5	
II. Sapphire W Lines	No.	17	17	16	NT
	Min.	31.1	31.2	31.3	
	Max.	32.2	32.2	34.3	
	Avg.	31.6	31.8	32.3	
	σ	0.3	0.3	0.8	
II. Ceramic W Lines	No.	17	17	17	NT
	Min.	33.8	33.8	36.6	
	Max.	40.2	40.4	40.6	
	Avg.	37.8	37.9	38.1	
	σ	1.6	1.8	1.7	

* Conductor width, 0.254 mm, (Screenwire pattern). Second SiO_2 layer omitted.
** See Table 7 for metallization thickness.
NT - Not Tested.

Table 11

Contact Resistance*, (milliohms)

Group Metallization**	Value	Initial	Temp. Cycling -55°C to +150°C Post 110 Cycles	Temp. Aging at +150°C Post 500 Hrs.
I. Sapphire W-Al	No.	9	9	9
	Min.	6.6	5.6	5.6
	Max.	11.9	11.9	11.9
	Avg.	9.5	9.2	9.1
I. Ceramic W-Al	No.	8	9	8
	Min.	12.4	12.5	12.3
	Max.	16.8	17.0	17.0
	Avg.	13.7	13.6	13.5

* 0.254 mm square contacts, (Screenwire pattern).
** See Table 7 for metallization thicknesses.
NT - Not Tested.

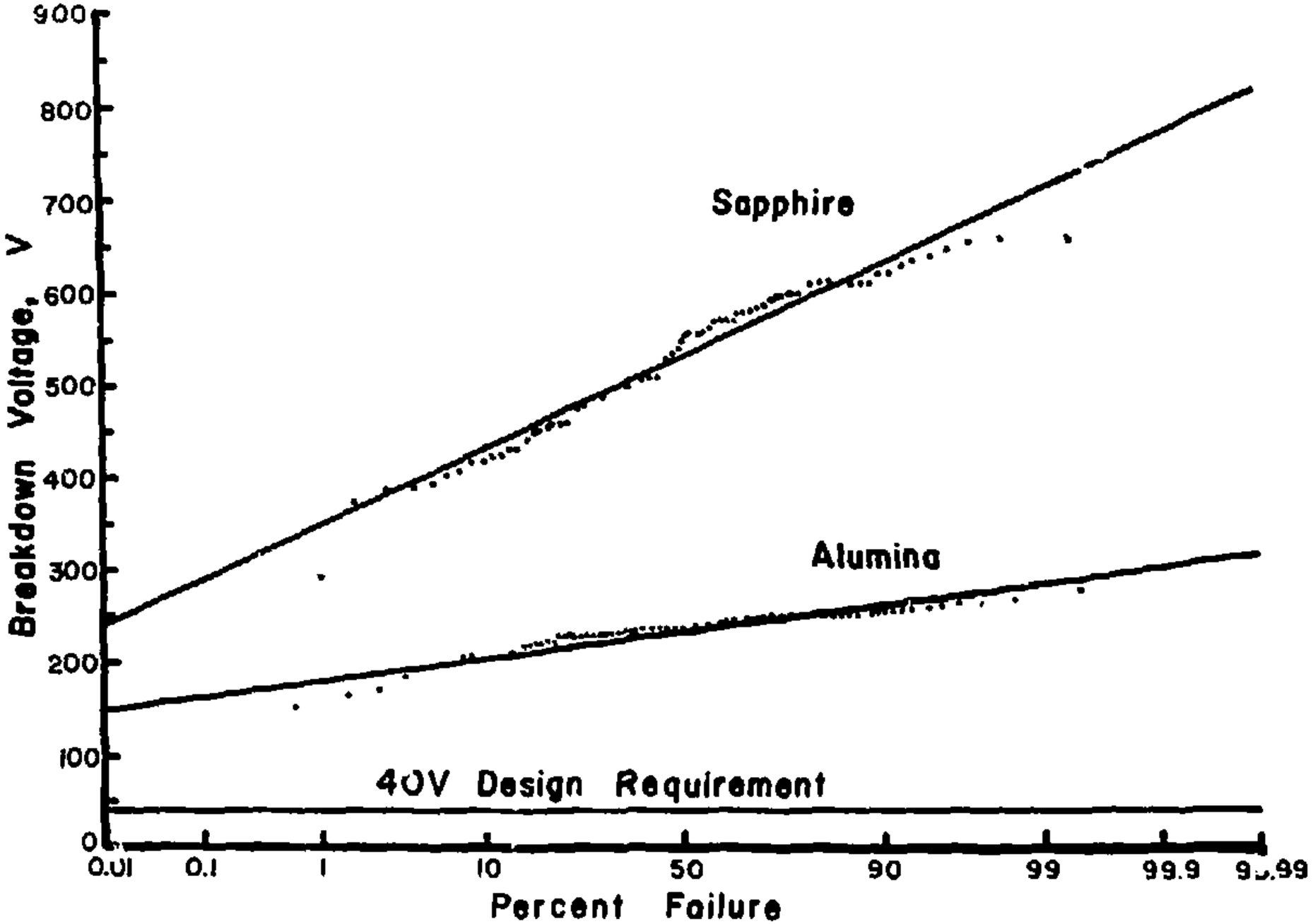


Fig. 11. Probability plot of typical voltage breakdown characteristics of Group I crossovers (fine line pattern) on sapphire and alumina.

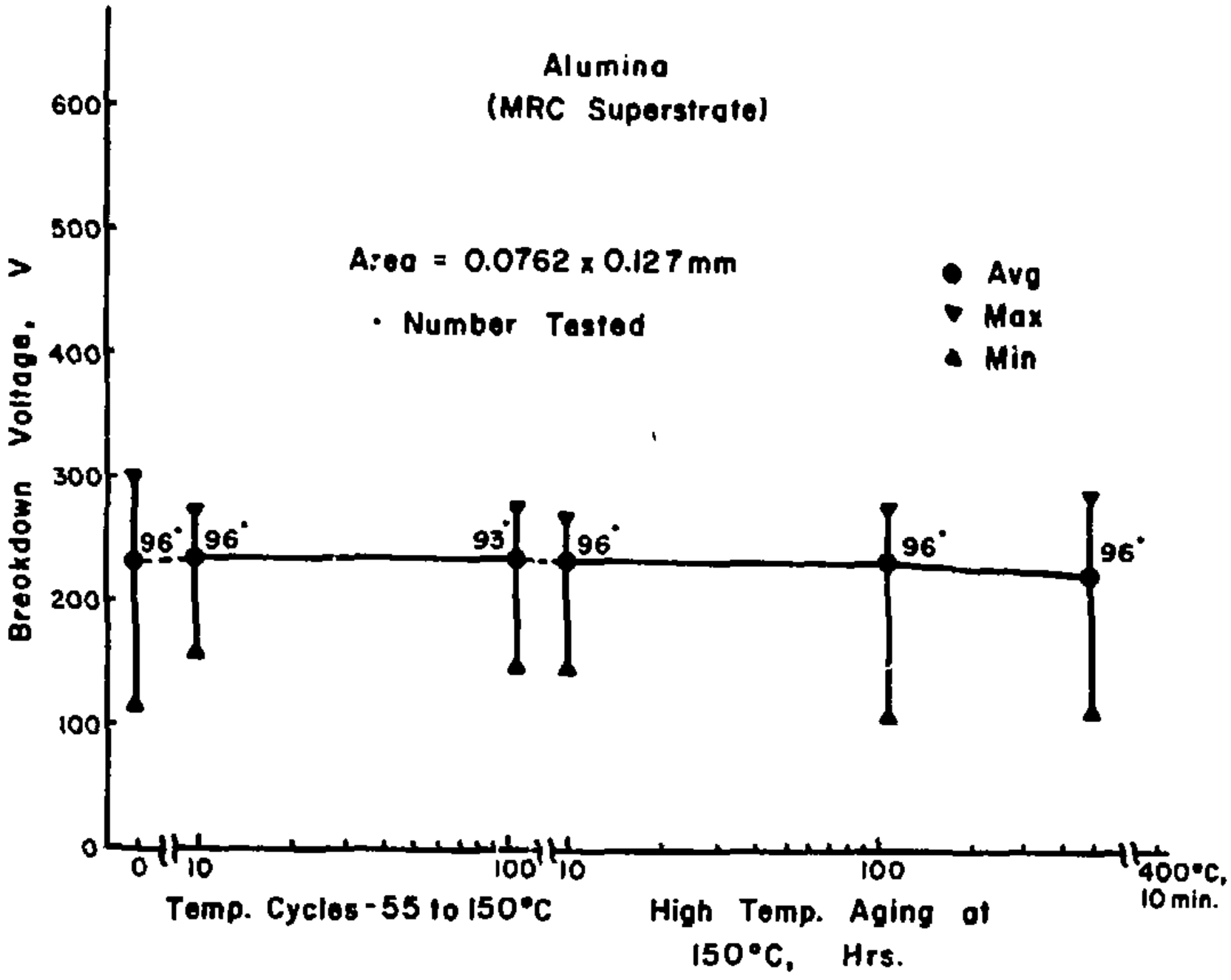


Fig. 12. Voltage breakdown on Group I crossovers on alumina.

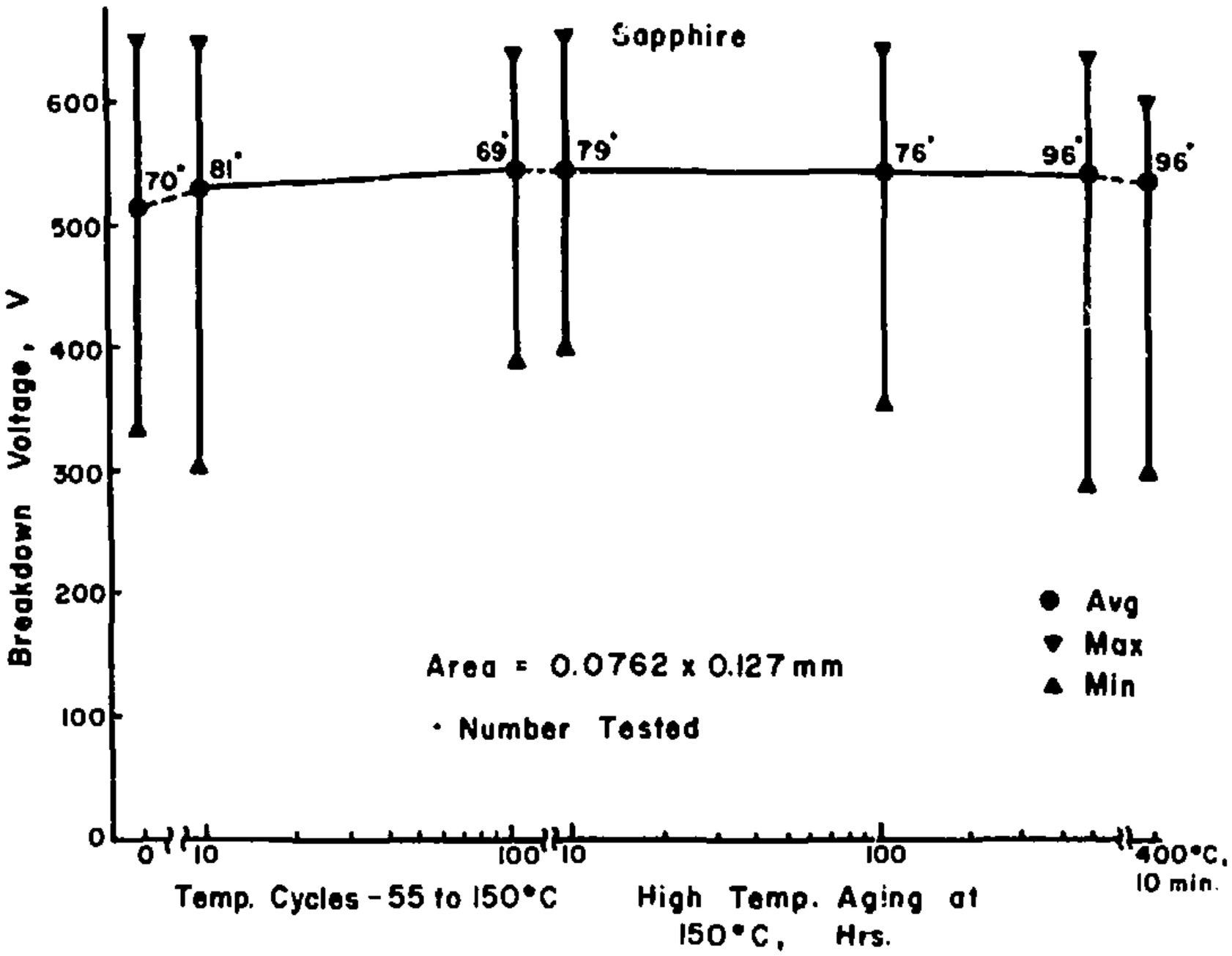


Fig. 13. Voltage breakdown on Group I crossovers on sapphire.

Table 12

Bond Pull Tests
(Sapphire Substrates)

Parameter	Au-Au Wire	Au-Au Lead Frame	Al-Al Wire
Preconditioning*	300°C, 2 hrs.	30 °C, 2 hrs.	400°C, 10 min.
Bonding Method	Thermocompression	Thermocompression	Ultrasonic
Gold Thickness	2.3 µm	2.7 µm	--
Aluminum Thickness	--	--	3.93 µm
Lead Size	0.0254 mm	0.381 mm wide	0.0254 mm
Substrates Temperature	150°C	UNK	RT
Tool Temperature	150°C	UNK	RT
Force	0.130 Kg	UNK	UNK
Number Pulled	22	27	24
Minimum	4.1×10^{-2} N	10.7 N	6×10^{-2} N
Maximum	7.3×10^{-2} N	14.7 N	9×10^{-2} N
Average	5.7×10^{-2} N	12.2 N	7.5×10^{-2} N

Note: All failures were lead rupture type

*Previous air ambient temperature history

DISCUSSION & CONCLUSIONS

The results of the evaluation and aging studies show that the metallization system can withstand processing temperatures up to 370°C for eutectic die attach (Au-Ge at 356°C and Au-Si at 363°C), soldering, beam lead bonding, etc. The operational temperature can be -55°C to +125°C with no apparent problems. Crossover yield was good (less than 0.3% shorts) and can be improved with better process control. Alternate tungsten deposition techniques (i.e., triode sputtering) could result in lower resistivity of that layer.

Thin film techniques for crossovers and interconnects based on a deposited metal-insulator-metal system have been developed and used in hybrid circuits and on semiconductor devices since the early 1960's.[12,13] Recent LSI semiconductor developments have forced the development of two and three level thin film, high resolution metallization systems on semiconductor devices. There are several good reviews of the advantages, limitations, and reliability of different systems[14-17] and at least one general review on materials and processes.[18] The techniques reported on here represent the combination of many semiconductor techniques (i.e., the five level mask system, finer lines and spaces, and batch fabrication on one substrate) with hybrid techniques (i.e., thin film deposition, device attachment, and packaging).

The feasibility of using gold and aluminum metallization in a two-level, thin film hybrid metallization system without gold-aluminum interfaces and meeting the requirements of the SIL Micro Actuator has been demonstrated. The degree of miniaturization possible, the high temperature processing capability, and the bonding and attachment versatility affords the hybrid circuit designer a means of attaching and interconnecting a heterogeneous mixture of MOS and bipolar devices, as well as passive devices heretofore impossible.

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Appendix I

Preliminary Layout Rules

Substrates

a) 25.4 x 38.1 x 0.38 mm (1" x 1½ x 0.015") Sapphire

b) 25.4 x 38.1 x 0.38 mm (1" x 1½ x 0.015") Al_2O_3 (MRC Superstrate)

Mask Levels

1. Gold conductors, bonding pad, and die down areas (for gold-gold bonding and eutectic bonding).
2. Tungsten lower metallization. (Crossovers and vias).
3. Insulator (SiO_x) openings for all gold bonding pads, eutectic bonding areas, vias, and bonding pads where tungsten-aluminum is desired.
4. Aluminum top metallization for all top conductors, over vias, and bonding pads over glass and those over tungsten.
5. Top insulator openings - required for all bonding pads (gold and aluminum), terminations, test points, if any, and eutectic bonding areas.

General Layout Rules

1. Minimize all crossover areas, i.e., aluminum over tungsten with insulator in between. Crossover should not exceed 0.254 x 0.254 mm (10 x 10 mils or 100 square mils).
2. Maximize all gold-tungsten, tungsten and aluminum metallization areas.
3. Gold-tungsten conductors are permissible in areas where conductive components are to be adhesive bonded to substrate. The areas should be covered with SiO_2 layers.
4. Maintain a minimum 0.0508 mm (2 mil) spacing between lines on the same level; where necessary, 0.0254 mm (1 mil) spacing is permissible for short distances, i.e., between bonding pads and when necessary to obtain suitable via widths.
5. Maintain a minimum 0.0254 mm (1 mil) lateral spacing between first and second level metallization except in the areas where crossovers and vias are desired.

6. Metal lines should be 0.0508 mm (2 mils) or greater in width (see 2 above).
7. If possible, keep crossover areas to a 0.106 x 0.106 mm (4 x 4 mil) maximum format.
8. Gold-tungsten metallization sheet resistance will be less than 0.03 ohms/ square.
9. Tungsten metallization sheet resistance will be less than 0.4 ohms/ square.
10. Aluminum metallization sheet resistance will be less than 0.04 ohms/ square.
11. Keep metallization 0.127 mm (5 mils) away from edge of the substrate.
12. Gold to aluminum transistions shall be separated by a minimum of a 0.0508 mm (2 mil) wide strip of tungsten. Maintain this minimum wherever possible to reduce resistance.
13. Bonding pads for aluminum wire should be at least 0.1016 x 0.1016 mm (4 x 4 mils) in area, (maximize area consistent with 4, 5, and 20).
14. Bonding pads for gold wire should be at least 0.1016 x 0.1016 mm (4 x 4 mils) in area (maintain a minimum of 0.0508 mm (2 mils) clearance around pad for squashout. Maximize area consistent with 4, 5, and 20).
15. Bonding pads for gold ribbon should be at least 0.2032 x 0.1016 mm (8 x 4 mils) in area for 0.127 mm (5 mils) wide gold ribbon.
16. Bonding pads 0.1524 mm (6 mils) square minimum must be provided for all beams of any beam lead device. Center of pads shall be 0.003" from the edge of the die.
17. Adjacent bonding pads on the substrate shall have a minimum center spacing of 0.2032 mm (8 mils) with a minimum of 0.0508 mm (2 mils) separation.
18. Glass openings for bonding pads and eutectic die down areas should be designed to be .0254 mm (1 mil) in from the underlying metal.
19. If necessary, tungsten conductors may run under insulated aluminum bonding pads.
20. Maximize bonding pad areas wherever possible.
21. Allow a minimum of 0.381 mm (15 mils) from edge of chip to center of bonding pad for chip to substrate wire bond (ref. 14 and 15).
22. Fine wires should be held to a maximum length of 1.524 mm (60 mils).

23. Where possible, provision will be made for redundant bonding to chip capacitors.
24. If more than 1 wire (aluminum or gold) is connected to a bonding pad, the pad should be at least 0.1016 x 0.2032 mm (4 x 8 mils) in size for 2 wires, for example.
25. Maximize via openings wherever possible.
26. The first SiO_2 layers should cover all tungsten and tungsten-gold areas except via openings and aluminum and gold bonding pad areas.
27. Via width (SiO_2 opening) should be at least 0.0508 mm (2 mils).
28. Via length (SiO_2 opening) should be at least 0.1016 mm (4 mils).
29. Via width (SiO_2 opening) should be 0.0254 mm (1 mil) in from the underlying tungsten metal.
30. Aluminum metallization overlapping the via opening should be 0.0254 mm (1 mil) minimum greater on all sides.
31. The second SiO_2 layer should cover the entire substrate except for aluminum and gold bonding pad areas.

Appendix II

Background on High Density Multilevel Hybrid Circuit Techniques

The SLL Micro Actuator requirements were an example of circuit variety, complexity, and extreme miniaturization. Various methods have been developed over the years for fabricating complex hybrid microcircuits. We here describe and comment on several multilevel techniques which typify the present state of the art and what were considered for this application

Multilayer Ceramic - A ceramic slip (generally alumina) is cast in thin "green" sheets by a doctor blading process. The sheets are cut to size, via holes are punched, and metal and metal posts are screened on the sheets in the desired pattern to form the conductors and interlevel via connections. The individually coated sheets are then laminated and the top layer metallization screened on. The assembly is then fired, sintering the layers together and resulting in a monolithic multilevel structure.[1-4] There are several variations, such as metallizing the top layer with thick film techniques after firing, the use of glass layers, and various metal combinations. IBM has done considerable work using this technique, making it compatible with their "solder bump" semiconductor devices. Line widths and spacings are typical of screened thick film techniques with 0.127 mm possible; however, 0.200-0.254 mm are more desirable.

This technique has merit for volume production but requires specially made devices and access to rather sophisticated ceramic fabrication facilities. Alignment and delamination are problem areas. For this application, aside from device availability, it appeared that the resulting substrate thickness would be too great, tooling charges too high, and resolution during the lamination process on such small substrates a problem. Inevitable changes in circuit configuration and/or size would result in costly tooling changes.

Multilevel Thick Film Techniques - Thick film multilevel circuits based on the patterned screening and firing of successive conductive, insulating, and resistive inks or pastes on alumina ceramic are quite versatile and widely used methods of fabricating hybrid circuits. In the conventional process, screens (generally 200-325 mesh stainless steel) are covered with a photosensitive layer of

material and exposed with ultraviolet light using a photographic image of the desired pattern. Development then washes away openings in the layer as desired. The screen is then placed in a screen printer, and the pastes are forced through the screen openings and onto the substrate in the desired pattern with a squeegee. The coated substrate is then fired in a belt furnace. The next pattern is then screened on and the substrate is again fired. The steps of screening and firing are repeated until the desired layered pattern is complete. Dielectric layers are usually double coatings to cover defects.[5-9]

Considerable improvement in thick film processes, tools, and techniques has been accomplished in recent years. Screen design has been improved; 325 mesh, 40 percent opening stainless steel is now rather common.[10-12] Screen emulsions have been improved,[13] and etched metal rather than screen has also been used to enhance definition.[14] The inks or pastes used have undergone considerable evolution.[15] Fritless gold conductor inks have brought about improvements in bonding and line definition. Crystallizable dielectrics have been developed to permit firing of subsequent layers without softening the previous layer.[16] Many different paste materials and substrate properties have been developed and evaluated for multilayer thick film processes.[17-21]

The resolution capabilities of thick film screened materials have been evaluated, and experience seems to indicate that a ratio of 2.5 to 1 is desirable for centerline spacing to line width. About the best resolution attained has been 0.101 mm lines on 0.254 mm centers. More desirable from a production and yield viewpoint is 0.152 mm lines on 0.381 mm centers. Using these line widths and openings, one study on line segments up to 12.7 mm long on 50.8 mm square substrates indicated that the number of good lines (no opens or bridges) ranged from 81 percent on the latter to 13 percent on the former.[22] Thus, yield falls off drastically as the line width and spacing is reduced.

Several methods of overcoming the line resolution and spacing limitations inherent in the screen printing technique have evolved. One method is the use of photolithographic techniques as in thin film technology. The conductive and/or dielectric inks are screened on over the entire substrate without patterning and then fired. Photoresist and subtractive etching techniques are then used to define the pattern before the next layer is screened on and fired. The screen coating, firing, and photoresist steps are repeated until the circuit is complete. Line widths and spacings of 0.102 mm and matching 0.102 mm vias with reasonable yields are claimed. It was found, however, that the 96 percent alumina substrates

classically used in thick film circuitry were too rough and had to be ground and polished to obtain such resolution.[23,24]

Another thick film technique that may have possibilities for high density multilayer circuits is based on photoprintable thick film pastes introduced by DuPont under the trade name of FODEL. Both gold conductor and crystallizable dielectric type pastes are available and are claimed to be compatible. The pastes are dispersions of particulate metals and/or inorganic oxides in a photosensitive vehicle. They may be considered as filled negative acting photoresists which polymerize under the influence of ultraviolet light. In use, the layers are screened on over the entire substrate and then exposed through a photographic mask to the ultraviolet light. Development in a suitable solvent then washes away the unexposed material, leaving the desired pattern. This is then fired, and the process is then repeated for the next layer. Two and three level metallization patterns have been made with 0.0508 mm line widths, 0.0762 mm spaces, and 0.127 mm vias claimed as practical for the two-level system.[25-27] Other than the development work at DuPont, application data is lacking. Experiments here were not encouraging.

The number of metal levels incorporated in production of thick film hybrids ranges from 1 to greater than 5 with increasing difficulty as the number of levels increases. Adhesion problems, dielectric softening during firing, pinholes, and open and shorts seemed to be the major problems in one study on circuits with up to 5 metal levels on rather large substrates. Thick film resistors have been incorporated in multilevel circuits but are generally put down last on an open area of the alumina substrate which has not previously been coated. This is because the substrate material and underlying layer material influences the electrical properties of the resistor and also because laser or abrasive trimming techniques are necessary.

Thin Film Multilevel Techniques - The discussion will be limited to those techniques which afford a crossover and interconnection capability between metal layers. While thin film hybrid circuits have been produced using a variety of techniques, multilevel thin film hybrid circuits have not been widely used. However, if one looks to the semiconductor LSI (Large Scale Integration) advances, particularly in the MOS (Metal-Oxide-Semiconductor) area, two-level metallization is quite common and well developed. In fact, doped silicon channels in the silicon chip itself often serve as the third conductor level. In the hybrid area, however, circuits are generally made using single level metallization which includes thin film resistors and occasionally thin film capacitors. The practical techniques of

industrial and military significance have been limited to NiCr, Cr, Ta_2N, and Cr-SiO resistors and SiO, SiO_2, and Ta_2O_5 capacitors with gold or aluminum metallization.[29,30] Crossovers, with few exceptions, are minimized by careful circuit layout, utilizing capacitor counter electrodes, and, when necessary, are made by utilizing bonding gold or aluminum wire (or ribbon).

One method for providing crossovers on hybrids that has gained favor is an adaption of the so-called Lepselter beam crossovers first used on silicon integrated circuits.[31] They are made by depositing copper over photodefined thin film circuit metallization, etching holes through the copper for the beam pillars, and then electroplating gold through a patterned coating of photoresist to fabricate the gold beams and pillars. The copper is then etched away, leaving the gold beam 0.0254 mm thick supported by its pillars suspended over the desired metallization lines beneath. (See Fig. 1A.) Widths as small as 0.127 mm and spans as long as 2.16 mm have been made.[32] A variation which overcomes the problem of beam sag and potential shorting is to deposit a layer of zirconium over the circuit before plating the copper. After the copper etching step, the zirconium is oxidized to zirconium oxide (ZrO_2), thus covering the circuitry including the area under the beams with an insulating dielectric, thus avoiding the shorting problem.[33] The use of ZrO_2 is not compatible with tantalum nitride resistors because of the high temperature required to oxidize the zirconium. Despite the complexity of the processing, hybrid circuits using beam crossovers have been made by Bell/Western,[34] RCA,[35] and others.

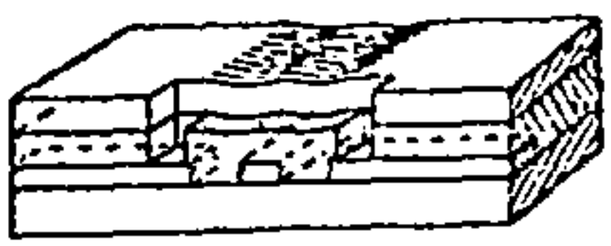
Another method is to incorporate necessary crossovers in a metallized beam lead silicon chip termed a "crossover chip" and then bond it in place.[36] The advantage over ribbons or wires is that the device can be attached at the same time as the regular beam lead devices using the same equipment, and complex crossovers can be made.

Thin film systems for crossovers and interconnects based on a deposited metal-insulator metal system have been used since the early 1960's in hybrid circuits.[37] The most common technique is the use of aluminum or gold conductors separated by a layer of SiO or SiO_2. Deposition techniques for the metal layers is generally done by evaporation or sputtering; for the SiO or SiO_2, RF sputtering and chemical vapor deposition (CVD) techniques have been employed. Rather high interconnect densities were reported in one hybrid application where the first metal layer was a Cr-Cu-Cr sandwich deposited by evaporation. The insulator was CVD deposited SiO_2. The top metal layer was evaporated Cr-Au followed by

Substrate with Au conductors defined.

Plated with Cu (~ 1 mil).

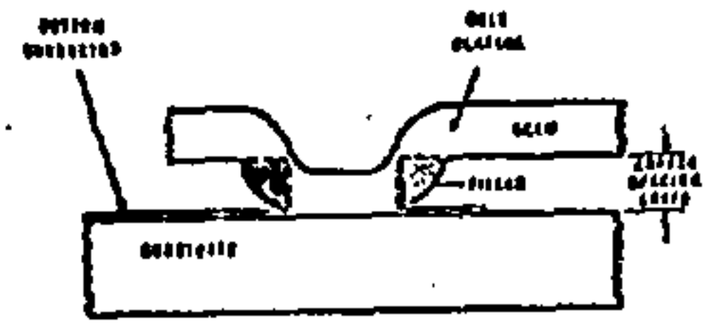
Support columns defined in photoresist.



Crossover span defined in photoresist.

Gold plated into exposed areas.

Photoresist removed and Cr etched away.



Appearance in cross section.

Fig. 1A. Lepselter Air Bridge Crossover Technique.

electroplated gold. Minimum line widths and spacing were 0.102 cm and 0.050 cm, respectively. Crossovers were typically 0.106 cm square. Vias were as small as 0.153 cm square. Substrates were 10 mil thick alumina polished to a surface finish of at least 54 nm. Thin film resistors were not incorporated.[38] There are other examples of thin film multilevel hybrids, but the literature is not nearly as prolific as that on thick film techniques.

In the semiconductor integrated circuit industry, considerable work has been done on thin film multilayer techniques. The [illegible]e of active devices within the silicon, compounded with the greater number of devices in a chip, have made the development of compatible multilevel thin film metallization systems for interconnecting the devices imperative. These LSI applications have forced the development to the point where two-level metallization is quite common. There are several good reviews on the advantages, limitations, and reliability of different systems[39-44] and at least one general review of the materials and processing techniques being used.[45] Many materials have been exploited to fabricate multilevel interconnects on LSI devices. Some are shown below:

Metals	Insulators
Al	SiO_2
Al-Si	SiO_2 (phosphorous doped)
Al-Cu	SiO_2 (boron doped)
Mo	Si_3N_4
Mo-Au-Mo	Al_2O_3
W	Various glass compositions
W-Au-W	Polyamide
PtSi-Ti-Pt-Ti	
PtSi-Ti-Pd-Ti	
Ti/W-Au-Ti/W	

In general, the choice of metals and insulators is stringent when on or over silicon because of impurity diffusion and charge storage problems. In addition, ohmic contact to the silicon is a prime requisite. Most multilevel systems on semiconductors today use evaporated aluminum layers doped with Cu and/or Si to minimize electromigration[46] and SiO_2 doped with phosphorus to minimize interfacial charge storage. Notable exceptions are polycrystalline silicon defined in the silicon itself as a conductive layer, anodized Al for interlevel insulation, and the beam

crossover technique previously described. Minimum line widths are in the vicinity of 0.0025 cm with spacings of 0.013 cm. Minimum via size is in the vicinity of 0.013 cm. Two metal layers and a polycrystalline silicon conductive layer separated by SiO_2 are common. Recently, a 5 level system using Al and polyamide insulation was reported.[47]

One reliability study on a Al-SiO_2-Al system on silicon indicated a very reasonable failure rate on crossovers and vias. Temperatures of 150°C for 1000 hours indicated a failure rate of one crossover in 12,000 and temperature cycling from -65°C to 150°C for 500 cycles resulted in a failure rate (shorts) of 1 in 13,200. No increase in via resistance was noted. Crossover size was 0.0013 cm square.[48]

There is something to be learned from the semiconductor industry in multilayer techniques. First, they are accustomed to complex batch processing techniques involving a large number of well understood procedures and repetitive steps and sophisticated equipment. Second, they process a quantity of devices in one wafer. Third, in contrast to most passive component and even hybrid substrate manufacturing philosophy, they are willing to accept comparatively low yields. As the complexity of metallized substrates increases, their philosophy may be the only viable option.

Other Multilayer Techniques - Several other techniques for hybrid multilayer metallization with interconnecting bias and crossovers are worthy of mention. The first is the STD (Semiconductor Thermoplastic Dielectric) process developed at GE as a means of mounting and interconnecting transistor and integrated circuit chips on a substrate without the conventional wire bonds. In the original version of the process shown in Fig. 2A, thin film NiCr and gold are first deposited on a substrate and photodefined for resistors and lower level interconnections. Mesas or pillars for interlevel connections of the desired height are added by plating and selective etching. Their height is adjusted to match the thickness of the semiconductor devices. Then a thin layer of fluorinated ethylene propylene (FEP) is bonded to the substrate such that its surface is coplanar with the top of the mesas. The FEP left on top of the mesas is removed by selective RF etching. Transistor and integrated circuit chips with gold terminations and thinned by lapping to a prescribed thickness to match the mesa height are bonded by pressing them into the FEP. The positioning of chips must be accurate. A cover of FEP is pressed and bonded over the entire substrate. RF plasma etching is then used to open window areas over the chip bonding pad areas. Copper conductors are then

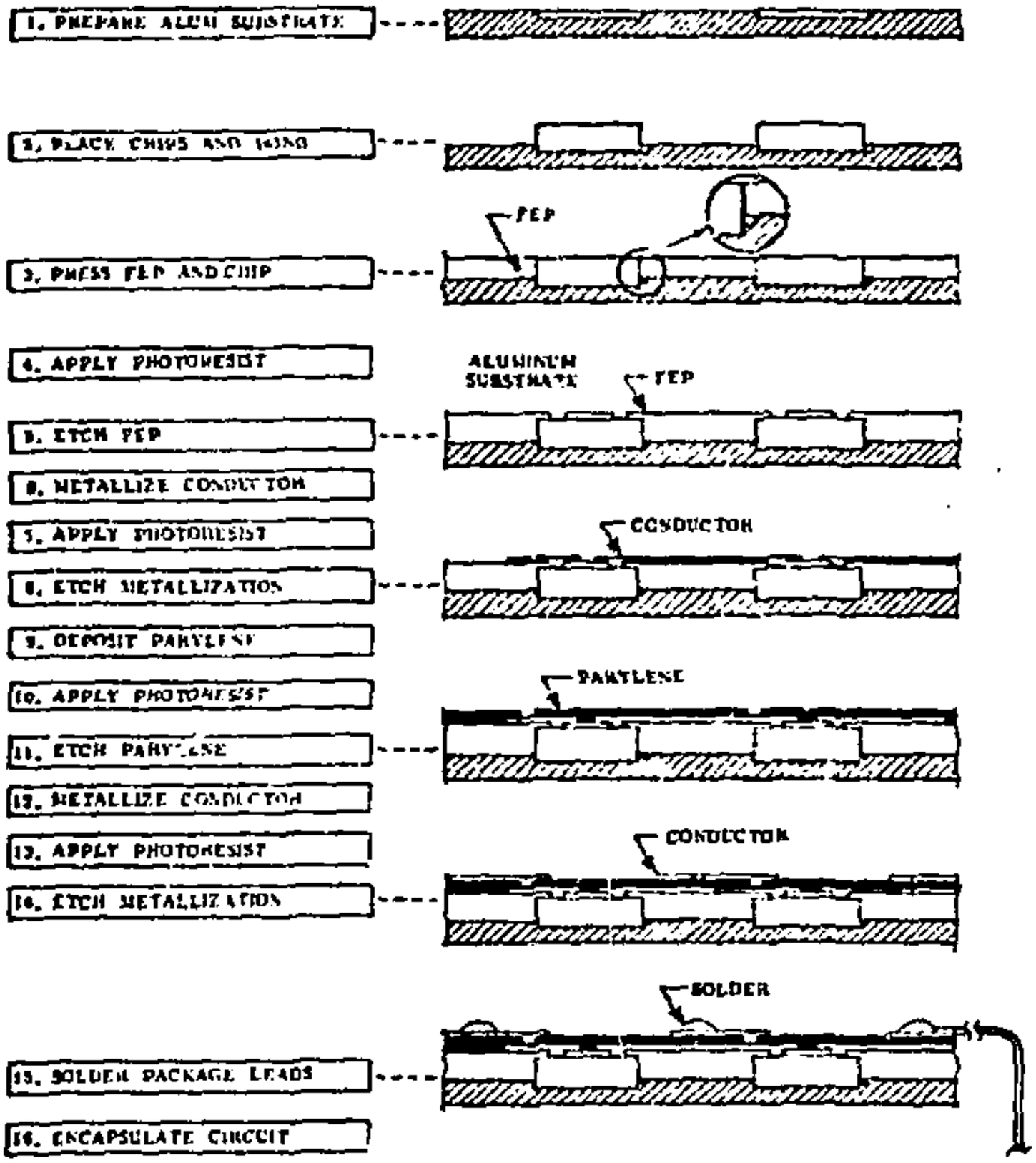


Fig. 2A. STD (G.E.) Multilayer Hybrid Technique.

deposited on top and photodefined to complete the interconnections to the chips and mesas. In later versions, the transistor and integrated circuits are eutectically or solder bonded directly to the gold surface of the first layer of metallization before the FEP layers are pressed on. Lead frames have also been incorporated.[49]

The second technique called BLIP (Beam Lead Interconnect Packaging) developed at Northrup Electronics is somewhat similar (see Fig. 3A). The substrate is metallized and photodefined using thin film techniques for a resistive layer (if desired) and lower level conductors. A dry film photopolymer spacer is then laminated to the substrate. After the lamination step, the photopolymer is exposed and developed to form device cavities. The devices are then placed in the cavities and resin bonded. Next an interconnecting laminate of alternating layers of thin epoxy-glass and metal conductors interconnected by plated through holes is made up in a pattern to provide all interconnections between devices and substrate metallization. Holes and protruding beam leads that match and cover the device bonding pads are provided. The laminate is then placed over the substrates and bonded in place. The beam lead terminations are ultrasonically bonded to the device bonding pads and the substrate terminations. External leads are bonded to the top metal layer and the circuit is then packaged.[50]

Both the STD and BLIP multilayer techniques require that device and component heights be uniform and carefully controlled and that the bonding pads be compatible with the metallization used as an interconnect. Neither technique is applicable here.

The third technique is based simply on thick and thin film combinations. Generally, the lower metal levels and the insulator layers are deposited using screened thick film techniques and the upper metal layer with thin film and photolithographic techniques. Thick and thin film resistor can be incorporated, thus theoretically incorporating the better features of each technology.[51] Little practical application has been noted.

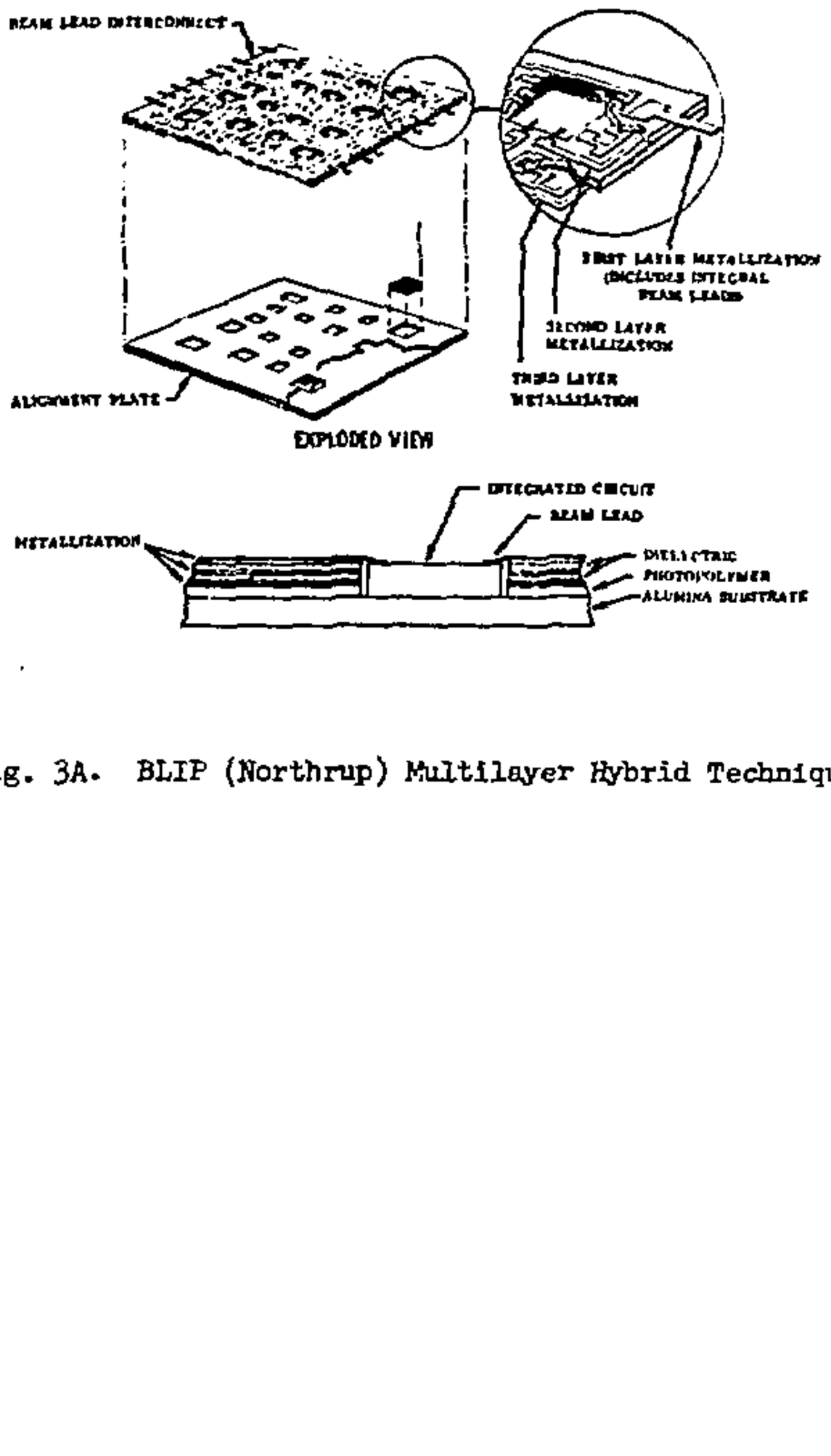


Fig. 3A. BLIP (Northrup) Multilayer Hybrid Technique.

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