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AUTOMATED ARRAY ASSEMBLY

Annual Report

B. F. Williams

May 1977

Work Performed Under Contract No. NAS-7-100-954352

RCA Laboratories
Princeton, New Jersey

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Division of Solar Energy

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RCA Laboratories
Princeton, New Jersey 08540

ANNUAL REPORT

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CALIFORNIA INSTITUTE OF TECHNOLOGY
Pasadena, California 91103

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PREFACE

This Annual Report, prepared by RCA Laboratories, Princeton, NJ 08540, describes the results of work performed from February 1976 to February 1977 in the Communications Research Laboratory, K. H. Powers, Director; Process and Applied Materials Research Laboratory, P. Rappaport, Director; Materials Research Laboratory, J. J. Tietjen, Director; Materials and Process Laboratory, Solid State Division, H. Veloric, Manager; and at the Advanced Technology Laboratory, Government and Commercial Systems, Camden, NJ, P. Wright, Director. The Program Manager is B. F. Williams. Others who participated in the research and writing of this report are:

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D. Richman - silicon material

H. Kressel, R. D'Aiello } junction formation

D. Redfield - device modeling

G. Schnable, W. Kern, K. Bube } metallization

B. Shelpuk, M. Crouthamel, P. Joy } panel design and fabrication

H. Veloric, F. Mayer } manufacturing

The JPL Task Manager is Don Bickler.

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SECTION I

SUMMARY

The goal of the ERDA/JPL LSSA program of $0.50/W selling price for array modules in 1986 turns out to have been remarkably appropriate. We have completed an extensive and detailed analysis of technologies which could be related to array module manufacturing and found a minimum manufacturing cost in a highly automated line of $0.30/W assuming the silicon is free. The panels are of a double glass construction and are based on round wafers. Screen-printed silver has been used as the metallization with a spray-coated AR layer. The least expensive junction formation technology appears to be ion implantation; however, several other technologies also may be used with very little cost penalty as described in this report.

Based on the required investment, a profit of $0.05/W appears reasonable. If silicon wafers are available at a price of $20-40/$M^2$, a selling price for these array modules of $0.50-0.66/W is projected.

An analysis of the impact of factory size has been made. For a production level of 500 MW/yr, the price above is derived. For comparison, a factory processing 50 MW/yr using the same technology would sell modules for $0.54/W to $0.70/W. An analysis of the impact of wafer size indicates that with traditional metallization and panel designs there is no advantage in increasing wafer size from 3 in. to 5 in., and, in fact, there is some penalty (10% in $/W) due to increased metallization costs and reduced system performance.

There is a premium placed on high efficiency due to its impact, not only on array module cost, but on system cost. For the near term goals of this program, wafers cut from single-crystal material seem the most likely sheet configuration.

SECTION II

INTRODUCTION

The purpose of this study was to assess manufacturing process sequences for silicon solar array modules which could be sold for $0.50/peak W in 1986 assuming a yearly sales volume of 500 MW. The study has identified such process sequences. All of the relevant technologies which exist in the semiconductor manufacturing art have been analyzed in detail. The basic philosophy of this study was to identify those manufacturing processes which had the smallest cost of consumed materials and expense items (defined later) based on this comprehensive analysis. It was assumed that the automation of these low material cost processes would result in the lowest cost array module. This philosophy has not changed.

There have been three levels of cost estimation applied to this task. Estimates of the present day costs for each of the potentially relevant processes were made as described above. For the class of processes which seemed the most attractive from a manufacturing cost point of view, the near term (approximately 5 years for full implementation) costs were developed. Finally, for the most cost-effective sequences, the manufacturing costs in a heavily automated facility were projected. A summary of this work is presented in Fig. 1.

In this report, the most cost-effective manufacturing sequence and panel design are described in detail. Variations on this sequence are also costed out.

In Section V we discuss the effect of wafer size on manufacturing cost. In most of the cost analysis in this report, 3-in. wafers were used as the sheet material. Factory level overhead costs are developed in Section VI.

COST ANALYSIS:PROCESS AND OTHER COST ESTIMATES

PROCESS COST ESTIMATE-$/WATT

ASSUMPTIONS: 0.500 WATTS PER SOLAR CELL AND $ 0.0 FOR 7.8 CM (3") DIAMETER WAFER.
100% YIELD FOR ALL PROCESSES FOLLOWING. ANNUAL PRODUCTION: 50.0 MEGAWATTS.

PAGE	YIELD	ITEM	TECH LEVEL	MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	TOTALS	INVEST
1	99.0%	SYSTEM "2" WAFER CLEANING	EXISTING	0.0	0.009	0.002	0.001	0.000	0.000	0.012	0.002
2	99.0%	SYSTEM "2" WAFER CLEANING	NEAR FUTURE	0.0	0.001	0.001	0.000	0.000	0.000	0.003	0.002
3	99.0%	SC-1 CLEANING	EXISTING	0.0	0.014	0.012	0.005	0.001	0.002	0.034	0.015
4	99.0%	WAFER SCRUBBER	EXISTING	0.0	0.025	0.004	0.005	0.001	0.002	0.037	0.014
5	99.0%	MEGASONIC CLEANING	EXISTING	0.0	0.016	0.007	0.006	0.001	0.002	0.032	0.012
6	95.0%	TEXTURIZING:HYDRAZINE	EXISTING	0.0	0.043	0.059	0.026	0.001	0.002	0.132	0.016
7	95.0%	TEXTURIZING:SODIUM HYDROXIDE	EXISTING	0.0	0.043	0.002	0.026	0.001	0.002	0.075	0.016
8	95.0%	SPIN-ON SOURCE	EXISTING	0.007	0.026	0.000	0.011	0.001	0.001	0.046	0.008
9	95.0%	SPIN-ON SOURCE:1 SIDE	NEAR FUTURE	0.007	0.010	0.000	0.005	0.002	0.002	0.025	0.017
10	95.0%	SPIN-ON SOURCE:2 SIDES	NEAR FUTURE	0.013	0.029	0.001	0.012	0.004	0.006	0.065	0.044
11	95.0%	SPIN-ON SOURCE:2 SIDES+EDGE STOP	NEAR FUTURE	0.013	0.048	0.002	0.020	0.007	0.010	0.100	0.072
12	99.0%	SPRAY-ON SOURCE & BAKE	EXISTING	0.0	0.022	0.005	0.032	0.001	0.001	0.062	0.010
13	98.0%	SCREEN PRINT SOURCE:2 SIDES	NEAR FUTURE	0.013	0.008	0.007	0.007	0.003	0.004	0.042	0.031
14	99.0%	SCREEN PRINT SOURCE:2 SIDES	FUTURE	0.013	0.005	0.007	0.005	0.004	0.006	0.040	0.045
15	99.0%	200 DEG. C. BAKE	EXISTING	0.0	0.019	0.000	0.005	0.000	0.000	0.024	0.000
16	99.0%	200 DEGREE C. OVEN BAKE-2	EXISTING	0.0	0.019	0.000	0.005	0.000	0.000	0.024	0.010
17	98.0%	DIFFUSION	NEAR FUTURE	0.0	0.009	0.002	0.002	0.001	0.003	0.016	0.012
18	99.0%	DIFFUSION:36" WIDE BELT	NEAR FUTURE	0.0	0.008	0.002	0.002	0.001	0.003	0.015	0.012
19	99.0%	DIFFUSION	FUTURE	0.0	0.003	0.002	0.001	0.001	0.003	0.009	0.010
20	99.0%	POCL3 DEPOSITION AND DIFFUSION	EXISTING	0.0	0.016	0.028	0.020	0.003	0.004	0.072	0.031
21	99.0%	POCL3 DEPOSITION AND DIFFUSION	FUTURE	0.0	0.003	0.028	0.001	0.001	0.001	0.033	0.006
22	99.0%	DOPED OXIDE DEPOSITION:P TYPE	EXISTING	0.0	0.028	0.040	0.019	0.005	0.008	0.100	0.057
23	99.0%	DOPED OXIDE DEPOSITION:N TYPE	EXISTING	0.0	0.028	0.040	0.019	0.005	0.008	0.100	0.057
24	98.0%	DOPED OXIDE DEPOSITION:2 SIDES	EXISTING	0.0	0.057	0.081	0.039	0.011	0.017	0.205	0.120
25	85.0%	CLOSE SPACE EPITAXY	NEAR FUTURE	0.0	0.068	0.258	0.020	0.026	0.042	0.415	0.294
26	99.0%	ION IMPLANTATION-FRONT	EXISTING	0.0	0.045	0.024	0.042	0.033	0.053	0.197	0.370
27	99.0%	ION IMPLANTATION-BACK	EXISTING	0.0	0.045	0.024	0.042	0.033	0.053	0.197	0.370
28	96.0%	ION IMPLANTATION:2 SIDES	NEAR FUTURE	0.0	0.010	0.011	0.009	0.013	0.021	0.066	0.150
29	99.0%	ION IMPLANTATION:2 SIDES	FUTURE	0.0	0.004	0.007	0.002	0.010	0.016	0.039	0.112
30	99.0%	POST DIFFUSION INSPECTION	EXISTING	0.0	0.015	0.000	0.005	0.003	0.005	0.028	0.033
31	99.0%	POST DIFFUSION INSPECTION	NEAR FUTURE	0.0	0.004	0.000	0.003	0.003	0.005	0.015	0.033
32	99.0%	POST DIFFUSION INSPECTION:10X	FUTURE	0.0	0.001	0.000	0.001	0.001	0.001	0.003	0.006
33	99.0%	FRONT SIDE RESIST APPLICATION	EXISTING	0.0	0.006	0.071	0.014	0.002	0.003	0.096	0.019
34	99.0%	RESIST REMOVAL	EXISTING	0.0	0.005	0.009	0.005	0.001	0.001	0.021	0.007
35	99.0%	GLASS REMOVAL	EXISTING	0.0	0.007	0.001	0.002	0.001	0.001	0.012	0.006
36	99.0%	GLASS REMOVAL	NEAR FUTURE	0.0	0.002	0.001	0.001	0.000	0.001	0.005	0.005
37	95.0%	RIM ETCH	EXISTING	0.0	0.012	0.034	0.013	0.002	0.003	0.064	0.020
38	95.0%	EDGE POLISH	NEAR FUTURE	0.0	0.002	0.004	0.001	0.000	0.001	0.008	0.005
39	100.0%	VACUUM EVAPORATION METALLIZATION	EXISTING	0.0	0.173	0.011	0.070	0.020	0.032	0.307	0.227
40	98.0%	TI/AG METALLIZATION-FRONT	EXISTING	0.019	0.177	0.011	0.072	0.024	0.039	0.342	0.271
41	98.0%	TI/AG METALLIZATION-BACK	EXISTING	0.022	0.177	0.011	0.072	0.024	0.039	0.345	0.271
42	99.0%	AL METALLIZATION-FRONT	EXISTING	0.004	0.177	0.011	0.072	0.021	0.033	0.318	0.232
43	98.0%	AL METALLIZATION-BACK	EXISTING	0.004	0.177	0.011	0.072	0.021	0.033	0.318	0.232
44	98.0%	MAGNETRON SPUTTERING TI/AG:FRONT	EXISTING	0.019	0.037	0.009	0.013	0.018	0.028	0.123	0.195
45	99.0%	MAGNETRON SPUTTERING TI/AG:BACK	EXISTING	0.022	0.037	0.009	0.013	0.018	0.028	0.126	0.195
46	98.0%	MAGNETRON SPUTTERING AL:FRONT	EXISTING	0.007	0.037	0.009	0.013	0.020	0.031	0.116	0.217
47	98.0%	MAGNETRON SPUTTERING AL:BACK	EXISTING	0.007	0.037	0.009	0.013	0.020	0.031	0.116	0.217
48	100.0%	SCREEN PRINT WAFER REWORK	NEAR FUTURE	0.0	0.001	0.000	0.001	0.000	0.000	0.002	0.001
49	100.0%	SCREEN PRINT WAFER REWORK	FUTURE	0.0	0.001	0.000	0.001	0.000	0.000	0.002	0.001
50	98.0%	THICK AG METAL-BACK:AUTO	NEAR FUTURE	0.026	0.004	0.005	0.006	0.003	0.005	0.049	0.035
51	99.0%	THICK AG METAL-BACK:AUTO	FUTURE	0.026	0.002	0.005	0.003	0.004	0.007	0.047	0.048
52	95.0%	THICK AG METAL-FRONT:AUTO	NEAR FUTURE	0.027	0.010	0.012	0.013	0.006	0.010	0.078	0.069
53	99.0%	THICK AG METAL-FRONT:AUTO	FUTURE	0.026	0.006	0.012	0.006	0.008	0.012	0.070	0.087
54	98.0%	THICK AL/AG METAL-BACK:AUTO	NEAR FUTURE	0.015	0.008	0.010	0.009	0.004	0.007	0.053	0.050
55	98.0%	THICK AL METAL-BACK:AUTO	NEAR FUTURE	0.011	0.004	0.005	0.006	0.003	0.005	0.034	0.035
56	98.0%	THICK AL METAL-FRONT:AUTO	NEAR FUTURE	0.012	0.010	0.012	0.013	0.006	0.010	0.063	0.069
57	95.0%	AR COATING:SPIN-ON	EXISTING	0.021	0.049	0.001	0.018	0.001	0.001	0.091	0.008
58	95.0%	AR COATING:SPIN-ON	NEAR FUTURE	0.021	0.019	0.001	0.007	0.002	0.004	0.053	0.025
59	99.0%	AR COATING:SPIN-ON	FUTURE	0.020	0.010	0.001	0.004	0.003	0.005	0.042	0.034
60	99.0%	AR COATING:SPRAY-ON	NEAR FUTURE	0.002	0.004	0.000	0.001	0.001	0.001	0.009	0.008
61	99.0%	AR COATING:EVAPORATE	EXISTING	0.010	0.070	0.006	0.035	0.011	0.018	0.150	0.128
62	80.0%	TEST	EXISTING	0.0	0.022	0.000	0.007	0.005	0.008	0.042	0.056
63	80.0%	TEST	NEAR FUTURE	0.0	0.005	0.000	0.005	0.005	0.008	0.023	0.056
64	90.0%	TEST	FUTURE	0.0	0.004	0.000	0.002	0.004	0.007	0.017	0.049
65	96.0%	ARRAY FAB.:RS:ACRYLIC PANEL,CB	EXISTING	0.359	0.159	0.066	0.048	0.010	0.016	0.657	0.109
66	96.0%	ARRAY FAB.:RS:GLASS SUPERSTRATE	EXISTING	0.152	0.159	0.066	0.048	0.010	0.016	0.450	0.109
67	96.0%	ARRAY FAB.:GW:ACRYLIC PANEL,CB	EXISTING	0.382	0.125	0.000	0.045	0.009	0.014	0.575	0.096
68	96.0%	ARRAY FAB.:GW:GLASS SUPERSTRATE	EXISTING	0.152	0.125	0.000	0.045	0.009	0.014	0.353	0.096
69	96.0%	ARRAY FAB.:ULS:ACRYLIC PANEL,CB	EXISTING	0.378	0.125	0.000	0.045	0.010	0.015	0.574	0.107
70	96.0%	ARRAY FAB.:ULS:GLASS SUPERSTRATE	EXISTING	0.156	0.125	0.000	0.045	0.010	0.015	0.352	0.107
71	99.0%	INTERCONNECT:REFLOW SOLDER	NEAR FUTURE	0.003	0.008	0.000	0.002	0.002	0.004	0.019	0.025
72	98.0%	INTERCONNECT:GAP WELDING	NEAR FUTURE	0.003	0.008	0.003	0.002	0.002	0.004	0.022	0.025
73	98.0%	INTERCONNECT:ULTRASONIC	NEAR FUTURE	0.003	0.013	0.000	0.003	0.002	0.004	0.025	0.025
74	100.0%	DOUBLE GLASS PANEL ASSEMBLY	NEAR FUTURE	0.103	0.003	0.003	0.001	0.002	0.003	0.114	0.018
75	100.0%	GLASS SUPERSTRATE PANEL ASSEMBLY	NEAR FUTURE	0.150	0.003	0.000	0.001	0.002	0.003	0.159	0.018
76	100.0%	RIBBON IN TUBES PANEL ASSEMBLY	NEAR FUTURE	0.140	0.003	0.000	0.001	0.002	0.003	0.148	0.018
77	100.0%	ARRAY MODULE PACKAGING	EXISTING	0.010	0.003	0.0	0.000	0.000	0.000	0.014	0.001

Figure 1. Cost analysis summary.

SECTION III

ARRAY MODULE MANUFACTURING COST

The lowest cost manufacturing process sequence which we have identified is shown in Fig. 2. As can be seen in the figure, the cost for this sequence is $0.264/peak W with 58% of the cost associated with material and expense items. This process sequence is identified as Ion Implantation (C) where the (C) denotes a heavily automated extrapolation of a near-future version, Ion Implantation (B), which will be evaluated later.

In the three class (C) cases which will be described, all of the machinery is fully automated and only the interfaces between each step involve people. The sheets, in this case 3-in. wafers, are transported between each step in 500-wafer cassettes. As will be shown below, additional people are involved in maintenance, support, and administrative functions.

ION IMPLANTATION (C)

ASSUMPTIONS: 0.717 WATTS PER SOLAR CELL AND $0.0 FOR 7.8 CM (3") DIAMETER WAFER

STEP	YIELD (%)	PROCESS		MAT'L.	EXP.	LABOR +O.H.	INT.+ DEPR.	TOTALS	INVEST
1	99.0	SYSTEM "Z" WAFER CLEANING	(B)	0.0	0.001	0.001	0.000	0.003	0.002
2	99.0	ION IMPLANTATION:2 SIDES	(C)	0.0	0.005	0.004	0.020	0.029	0.084
3	99.0	DIFFUSION	(C)	0.0	0.002	0.004	0.003	0.009	0.010
4	99.0	POST DIFFUSION INSPECTION 10%	(C)	0.0	0.000	0.000	0.000	0.001	0.003
5	99.0	THICK AG METAL-BACK:AUTO	(C)	0.021	0.004	0.004	0.008	0.041	0.037
6	99.0	THICK AG METAL-FRONT:AUTO	(C)	0.021	0.009	0.010	0.016	0.060	0.069
7	90.0	TEST	(C)	0.0	0.000	0.004	0.008	0.012	0.035
8	99.0	AR COATINGS:SPRAY-ON	(C)	0.002	0.002	0.005	0.002	0.011	0.008
9	98.0	INTERCONNECT:GAP WELDING	(B)	0.002	0.002	0.008	0.005	0.016	0.019
10	100.0	DOUBLE GLASS PANEL ASSEMBLY	(B)	0.072	0.002	0.003	0.003	0.080	0.014
11	100.0	ARRAY MODULE PACKAGING	(A)	0.007	0.0	0.001	0.000	0.009	0.000
	82.2	TOTALS		0.124	0.027	0.046	0.066	0.264	0.282
			%	47.22	10.35	17.12	25.31		

Figure 2. Ion implantation cost analysis.

As can be seen in Fig. 3, the factory on which these cost estimates are based produces 50 MW/year and operates 345 days/year. At this level of production, there is only a slight projectable advantage in increasing the factory size (Section VI). Ten such factories will produce 500 MW/year.

For understanding Fig. 2, Fig. 4 is a listing of all the material and expense items which have appeared during the entire analysis. As a rule, those materials which become part of the finished array module are considered "material" and those which are used up during the process sequence are considered "expense."

Figures 5 through 10 are the remaining cost summaries for the class B and class C process sequences which are considered the most cost-effective.

Figure 11 is a comparison of the three class (C) process sequences; Ion Impantation (C), Spin-On + $POCl_3$ Diffusion (C), and Screen Print 2 Sides (C). All of the processes in these three cases are the same except for the junction formation technique. In Spin-On + $POCl_3$ Diffusion (C), the back of the wafer is doped with a spin-on source during a $POCl_3$ diffusion of the front junction. In Screen Print 2 Sides (C), an appropriate source paste is screened onto each side of the wafer and the wafer doped in a subsequent diffusion step. The purpose of this figure is to emphasize that several cost-effective junction formation processes are available. Performance penalties which may be experienced with the nonstandard processes such as screened-on doping sources are not considered in this cost analysis.

It is the purpose of this analysis to provide guidance as to which technologies should be developed; it suggests ion implantation and screened-on doping sources are technologies worthy of further investigation.

Figure 12 is a cost comparison of these same technologies as we have evaluated them in a near-future context. Two factors result in lower cost in the automated line. First is a direct reduction in labor and process overhead. Second, the overall yield has increased from 65% to 80%. A detailed evaluation of the capital costs shows an actual reduction (slight) in the automated case due to substantially higher throughput for the fully automated equipment.

GENERAL INPUTS 01/20/77 16:15:43 PAGE 2

YEARS OF STUDY: 1 RUN TYPE:PRO-FORMA BASE YEAR OF RUN: 1

ANNUAL PRODUCTION IN WATTS: 5.000000E+07 PRODUCTION GROWTH PROFILE #: 0

2ND SHIFT PREMIUM:10.00% 3RD SHIFT PREMIUM:10.00%
WORKING DAYS/YR:345 # HOURS/SHIFT:12.00 # SHIFTS/DAY: 2

BOOK DEPRECIATION METHOD:SL TAX DEPRECIATION METHOD:SYD

FACTORY CONSTRUCTION COST,$/FT**2: 0.0 FACTORY DEPRECIATION LIFE-BOOK: 20 TAX: 20 INVESTMENT TAX CREDIT:YES
LAND COST,$/FT**2 OF FACTORY: 0.0 (NOT A DEPRECIABLE INVESTMENT) FACTORY EXCESS SPACE-1ST YR: 0.0%

INVESTMENT TAX CREDIT RATE: 10.00% INTEREST RATE ON DEBT: 9.00% INTEREST RATE GROWTH PROFILE #: 0
DEBT RATIO-INITIAL YEAR: 100.00%

PURCHASED SILICON COST: 0. $/SHEET. SILICON COST GROWTH PROFILE #: 0
SOLAR CELLS/SHEET: 1 # SOLAR CELLS/ARRAY MODULE: 224 AREA OF ARRAY MODULE:13564.0CM**2
WATTS PER SOLAR CELL (DEFAULT): 0.50 WATTS PER SOLAR CELL GROWTH PROFILE #: 0

WT. OF SHEET: 3.960 GRAMS. AREA OF SHEET: 47.800CM**2 FORM:3" WAFER.
DEFINITION OF SHEET: 7.8 CM (3") DIAMETER WAFER

GENERAL INPUTS:LABOR TYPE DEFINITIONS 01/20/77 16:15:43 PAGE 5

LABOR NAME	LABOR TYPE	WAGE RATE	GP#	FRINGE BENEFITS	GP#	EFFICIENCY
HOURLY OPERATOR	DIRECT	5.00$/HR	0	35.0%	0	85.0%
REWORK OPERATOR	DIRECT	5.00$/HR	0	35.0%	0	85.0%
HOURLY INSPECTOR	DIRECT	5.00$/HR	0	35.0%	0	85.0%
MACH. ATTENDANT	INDIRECT	5.60$/HR	0	35.0%	0	85.0%
FOREMAN	INDIRECT	7.65$/HR	0	35.0%	0	100.0%
ENGR. SUPPORT	INDIRECT	11.75$/HR	0	35.0%	0	100.0%
TECHNICIAN	INDIRECT	7.15$/HR	0	35.0%	0	100.0%
CLERICAL	INDIRECT	5.10$/HR	0	35.0%	0	100.0%
QUALITY CONTROL	INDIRECT	5.60$/HR	0	35.0%	0	100.0%
MAINTENANCE	INDIRECT	5.10$/HR	0	35.0%	0	100.0%
HANDLER	INDIRECT	5.10$/HR	0	35.0%	0	100.0%

Figure 3. Factory production analysis.

GENERAL INPUTS:EXPENSE TYPE DEFINITIONS 01/20/77 16:15:43 PAGE 6

EXPENSE NAME	RESTRICTION	TYPE	COST	GP#	SALVAGE	SALVAGE VALUE	GP#
AG-PLATED CU WIRE	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
AL CHANNEL	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
ALUMINUM	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
ALUMINUM RIBBON	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
AL FOIL SUBSTRATE	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
BOX FOR MODULE	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
CELL ADHESIVE	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
CONFORMAL COAT+3 MIL METAL	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
EDGE SEAL	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
END CAPS	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
EPOXY SPACER	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
EXTENDED HEAT SINK	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
FINAL ASSEMBLY MATERIAL	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
GLASS TUBING	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INDEX MATCHING MATERIAL	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
IN-HOUSE SPIN-ON AR COATING	NONE	MATERIAL	1.00000E-02$/CM**3	0	0.0%	0.0 $/CM**3	0
IN-HOUSE PASTE SOURCE	NONE	MATERIAL	4.00000E-03$/CM**3	0	0.0%	0.0 $/CM**3	0
IN-HOUSE SPIN-ON SOURCE	NONE	MATERIAL	4.00000E-03$/CM**3	0	0.0%	0.0 $/CM**3	0
INK AG-FRONT FINE GRID	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INK AG-FRONT FINE GRID LOST	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INK AG-FRONT BUS BAR	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INK AG-FRONT BUS BAR LOST	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INK AG-BACK GRID	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INK AG-BACK GRID LOST	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INK AG-BACK PAD	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INK AG-BACK PAD LOST	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INK AL-FRONT FINE GRID	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INK AL-FRONT FINE GRID LOST	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INK AL-FRONT BUS BAR	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INK AL-FRONT BUS BAR LOST	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INK AL-BACK GRID	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INK AL-BACK GRID LOST	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INTERCONNECT MATERIAL	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
INTERCONNECT METAL	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
PANEL ASSEMBLY MATERIAL	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
PANEL CONNECTOR	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
SILVER	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
SUBSTRATE	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
TANTALUM PENTOXIDE	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
TITANIUM	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
WINDOW	NONE	MATERIAL	SPECIFIED IN $	0	0.0%	$ 0.0	0
ACETIC ACID	NONE	DIRECT EXP.	1.72200E-03$/GM.	0			
AMMONIA GAS	NONE	DIRECT EXP.	5.50000E-06$/CM**3	0			
AMMONIUM HYDROXIDE	NONE	DIRECT EXP.	8.90000E-04$/CM**3	0			
BOATS,LINERS,ETC.	NONE	DIRECT EXP.	SPECIFIED IN $	0			
DEVELOPER	NONE	DIRECT EXP.	SPECIFIED IN $	0			
DETERGENT	NONE	DIRECT EXP.	0.0 $/GM.	0			
DE-IONIZED WATER	NONE	DIRECT EXP.	1.06000E-06$/CM**3	0			
DIAMOND BLADES,ETC.	NONE	DIRECT EXP.	SPECIFIED IN $	0			
DIBORANE 5% IN HYDROGEN	NONE	DIRECT EXP.	2.82700E-05$/CM**3	0			
ELECTRICITY	NONE	DIRECT EXP.	3.00000E-02$/KWH	0			
ELECTRODES	NONE	DIRECT EXP.	SPECIFIED IN $	0			
FILAMENTS/INSULATORS	NONE	DIRECT EXP.	SPECIFIED IN $	0			
FILTERS	NONE	DIRECT EXP.	SPECIFIED IN $	0			

Figure 4. Material and expense definition.

GENERAL INPUTS:EXPENSE TYPE DEFINITIONS 01/20/77 16:15:43 PAGE 6.1

EXPENSE NAME	RESTRICTION	TYPE	COST	GP#	SALVAGE	SALVAGE VALUE	GP#
HYDRAZINE	NONE	DIRECT EXP.	1.23000E-01$/GM.	0			
HYDROCHLORIC ACID	NONE	DIRECT EXP.	8.36000E-04$/GM.	0			
HYDROFLUORIC ACID	NONE	DIRECT EXP.	1.23000E-03$/CM**3	0			
HYDROGEN	NONE	DIRECT EXP.	2.65000E-07$/CM**3	0			
HYDROGEN CHLORIDE	NONE	DIRECT EXP.	6.60000E-03$/CM**3	0			
HYDROGEN PEROXIDE	NONE	DIRECT EXP.	1.14000E-03$/CM**3	0			
ION SOURCE GAS	NONE	DIRECT EXP.	SPECIFIED IN $	0			
LIME	NONE	DIRECT EXP.	4.65000E-05$/GM.	0			
LIQUID NITROGEN	NONE	DIRECT EXP.	7.50000E-05$/CM**3	0			
NITRIC ACID	NONE	DIRECT EXP.	1.03400E-03$/GM.	0			
NITROCELLULOSE LACQUER	NONE	DIRECT EXP.	1.50000E-03$/CM**3	0			
NITROGEN	NONE	DIRECT EXP.	4.77000E-08$/CM**3	0			
NITROGEN AMBIENT	NONE	DIRECT EXP.	4.77000E-08$/CM**3	0			
NITROGEN CURTAINS	NONE	DIRECT EXP.	4.77000E-08$/CM**3	0			
O-RINGS & FILTERS	NONE	DIRECT EXP.	SPECIFIED IN $	0			
OUTSIDE ENGR. SERVICES	NONE	DIRECT EXP.	SPECIFIED IN $	0			
OXYGEN	NONE	DIRECT EXP.	1.84000E-07$/CM**3	0			
PHOSPHINE 5% IN HYDROGEN	NONE	DIRECT EXP.	2.88000E-05$/CM**3	0			
PHOSPHORUS OXYCHLORIDE	NONE	DIRECT EXP.	2.04000E-02$/GM.	0			
PHOTORESIST	NONE	DIRECT EXP.	SPECIFIED IN $	0			
QUARTZ	NONE	DIRECT EXP.	SPECIFIED IN $	0			
SCREENS	NONE	DIRECT EXP.	SPECIFIED IN $	0			
SILANE 100%	NONE	DIRECT EXP.	4.04000E-01$/GM.	0			
SILICON TETRACHLORIDE	NONE	DIRECT EXP.	5.72000E-03$/GM.	0			
SODIUM HYDROXIDE	NONE	DIRECT EXP.	3.77000E-05$/GM.	0			
SOLVENT	NONE	DIRECT EXP.	SPECIFIED IN $	0			
SOLVENT-INK	NONE	DIRECT EXP.	5.27700E-04$/CM**3	0			
SOLVENT-PASTE	NONE	DIRECT EXP.	5.27700E-04$/CM**3	0			
SPRAY-ON SOURCE	NONE	DIRECT EXP.	SPECIFIED IN $	0			
SQUEEGEES	NONE	DIRECT EXP.	SPECIFIED IN $	0			
SULFURIC ACID	NONE	DIRECT EXP.	6.82000E-04$/GM.	0			
THERMOCOUPLE,ETC.	NONE	DIRECT EXP.	SPECIFIED IN $	0			
SUSCEPTORS	NONE	DIRECT EXP.	SPECIFIED IN $	0			
TRANSDUCERS & TUBES	NONE	DIRECT EXP.	SPECIFIED IN $	0			
TRICHLOROSILANE	NONE	DIRECT EXP.	1.98000E-03$/GM.	0			
WATER-COOLING	NONE	DIRECT EXP.	2.00000E-07$/CM**3	0			

Figure 4. Material and expense definition (Continued).

COST ANALYSIS:CASE II:SPIN-ON +POCL3 DIFFUSION(C) 02/03/77 13:09:18 PAGE 1

PROCESS COST OVERVIEW-$/WATT

ASSUMPTIONS: 0.717 WATTS PER SOLAR CELL AND $ 0.0 FOR 7.8 CM (3") DIAMETER WAFER

STEP	YIELD	PROCESS		MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	%	INVEST	%
1	99.0%	SYSTEM "Z" WAFER CLEANING	(B)	0.0	0.001	0.001	0.000	0.000	0.000	0.003	0.0	0.003	1.2	0.002	0.8
2	95.0%	SPIN-ON SOURCE:1 SIDE	(B)	0.006	0.009	0.000	0.004	0.001	0.002	0.022	0.0	0.022	7.8	0.015	7.0
3	99.0%	POCL3 DEPOSITION AND DIFFUSION	(C)	0.0	0.003	0.024	0.001	0.001	0.001	0.030	0.0	0.030	10.3	0.006	2.7
4	95.0%	EDGE POLISH	(B)	0.0	0.002	0.004	0.001	0.000	0.001	0.007	0.0	0.007	2.5	0.005	2.5
5	99.0%	GLASS REMOVAL	(B)	0.0	0.001	0.001	0.000	0.000	0.000	0.003	0.0	0.003	1.1	0.003	1.5
6	99.0%	POST DIFFUSION INSPECTION:10%	(C)	0.0	0.000	0.000	0.000	0.000	0.000	0.001	0.0	0.001	0.5	0.003	1.4
7	99.0%	THICK AG METAL-FRONT:AUTO	(C)	0.021	0.005	0.009	0.005	0.006	0.010	0.056	0.0	0.056	19.4	0.069	31.7
8	99.0%	THICK AG METAL-BACK:AUTO	(C)	0.021	0.002	0.004	0.002	0.003	0.005	0.037	0.0	0.037	12.9	0.037	17.1
9	99.0%	AR COATING:SPRAY-ON	(B)	0.002	0.004	0.002	0.001	0.001	0.001	0.011	0.0	0.011	3.6	0.008	3.9
10	90.0%	TEST	(C)	0.0	0.003	0.000	0.001	0.003	0.005	0.012	0.0	0.012	4.2	0.035	16.1
11	98.0%	INTERCONNECT:GAP WELDING	(B)	0.002	0.006	0.002	0.002	0.002	0.003	0.016	0.0	0.016	5.6	0.019	8.9
12	100.0%	DOUBLE GLASS PANEL ASSEMBLY	(B)	0.072	0.002	0.002	0.001	0.001	0.002	0.080	0.0	0.080	27.7	0.014	6.3
13	100.0%	ARRAY MODULE PACKAGING	(A)	0.007	0.001	0.0	0.000	0.000	0.000	0.009	0.0	0.009	3.1	0.000	0.2
	74.2%	TOTALS		0.130	0.039	0.049	0.019	0.020	0.031	0.289	0.0	0.289	100.0	0.218	100.0
			%	45.18	13.52	17.12	6.64	6.78	10.76	100.00					

NOTE: (A)=EXISTING TECHNOLOGY; (B)=NEAR FUTURE; (C)=FUTURE ANNUAL PRODUCTION: 50.0 MEGAWATTS.

Figure 5. Cost summary - spin-on + $POCl_3$ diffusion (C).

COST ANALYSIS:CASE IV:SCREEN PRINT 2 SIDES(C) 02/03/77 13:09:18 PAGE 1

PROCESS COST OVERVIEW-$/WATT

ASSUMPTIONS: 0.717 WATTS PER SOLAR CELL AND $ 0.0 FOR 7.8 CM (3") DIAMETER WAFER

STEP	YIELD	PROCESS		MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	%	INVEST	%
1	99.0%	SYSTEM "2" WAFER CLEANING	(B)	0.0	0.001	0.001	0.000	0.000	0.000	0.003	0.0	0.003	1.2	0.002	0.7
2	99.0%	SCREEN PRINT SOURCE:2 SIDES	(C)	0.011	0.004	0.006	0.004	0.004	0.006	0.035	0.0	0.035	12.8	0.040	16.6
3	99.0%	DIFFUSION	(C)	0.0	0.003	0.002	0.001	0.001	0.002	0.009	0.0	0.009	3.2	0.010	4.1
4	99.0%	GLASS REMOVAL	(B)	0.0	0.001	0.001	0.000	0.000	0.000	0.003	0.0	0.003	1.2	0.003	1.3
5	99.0%	POST DIFFUSION INSPECTION:10%	(C)	0.0	0.000	0.000	0.000	0.000	0.000	0.001	0.0	0.001	0.5	0.003	1.2
6	99.0%	THICK AG METAL-BACK:AUTO	(C)	0.021	0.002	0.004	0.002	0.003	0.005	0.038	0.0	0.038	13.8	0.037	15.4
7	99.0%	THICK AG METAL-FRONT:AUTO	(C)	0.021	0.005	0.009	0.005	0.006	0.010	0.056	0.0	0.056	20.5	0.069	28.6
8	99.0%	AR COATING:SPRAY-ON	(B)	0.002	0.004	0.002	0.001	0.001	0.001	0.011	0.0	0.011	3.9	0.008	3.5
9	90.0%	TEST	(C)	0.0	0.003	0.000	0.001	0.003	0.005	0.012	0.0	0.012	4.5	0.035	14.5
10	98.0%	INTERCONNECT:GAP WELDING	(B)	0.002	0.006	0.002	0.002	0.002	0.003	0.016	0.0	0.016	5.9	0.019	8.1
11	100.0%	DOUBLE GLASS PANEL ASSEMBLY	(B)	0.072	0.002	0.002	0.001	0.001	0.002	0.080	0.0	0.080	29.2	0.014	5.7
12	100.0%	ARRAY MODULE PACKAGING	(A)	0.007	0.001	0.0	0.000	0.000	0.000	0.009	0.0	0.009	3.3	0.000	0.2
	81.4%	TOTALS		0.135	0.033	0.029	0.018	0.022	0.035	0.273	0.0	0.273	100.0	0.241	100.0
			%	49.58	12.11	10.68	6.68	7.95	13.00	100.00					

NOTE: (A)=EXISTING TECHNOLOGY; (B)=NEAR FUTURE; (C)=FUTURE ANNUAL PRODUCTION: 50.0 MEGAWATTS.

Figure 6. Cost summary - screen print 2 sides (C).

COST ANALYSIS:CASE I:ION IMPLANTATION(8) 02/03/77 13:09:18 PAGE 1

PROCESS COST OVERVIEW-$/WATT

ASSUMPTIONS: 0.717 WATTS PER SOLAR CELL AND $ 0.0 FOR 7.8 CM (3") DIAMETER WAFER

STEP	YIELD	PROCESS		MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	%	INVEST	%
1	99.0%	SYSTEM "Z" WAFER CLEANING	(B)	0.0	0.001	0.001	0.000	0.000	0.000	0.003	0.0	0.003	1.0	0.002	0.5
2	98.0%	ION IMPLANTATION:2 SIDES	(B)	0.0	0.010	0.010	0.009	0.013	0.020	0.061	0.0	0.061	17.9	0.140	38.8
3	98.0%	DIFFUSION	(B)	0.0	0.009	0.002	0.002	0.001	0.003	0.016	0.0	0.016	4.8	0.012	3.3
4	99.0%	POST DIFFUSION INSPECTION	(B)	0.0	0.003	0.000	0.003	0.003	0.004	0.013	0.0	0.013	3.9	0.030	8.3
5	98.0%	THICK AG METAL-BACK:AUTO	(B)	0.024	0.004	0.005	0.005	0.003	0.004	0.045	0.0	0.045	13.0	0.031	8.6
6	98.0%	THICK AG METAL-FRONT:AUTO	(B)	0.024	0.009	0.011	0.012	0.006	0.009	0.070	0.0	0.070	20.5	0.062	17.2
7	99.0%	AR COATING:SPRAY-ON	(B)	0.002	0.004	0.002	0.001	0.001	0.001	0.011	0.0	0.011	3.1	0.008	2.3
8	80.0%	TEST	(B)	0.0	0.004	0.000	0.003	0.004	0.006	0.018	0.0	0.018	5.1	0.042	11.6
9	98.0%	INTERCONNECT:GAP WELDING	(B)	0.002	0.006	0.002	0.002	0.002	0.003	0.016	0.0	0.016	4.7	0.019	5.4
10	100.0%	DOUBLE GLASS PANEL ASSEMBLY	(B)	0.072	0.002	0.002	0.001	0.001	0.002	0.080	0.0	0.080	23.3	0.014	3.8
11	100.0%	ARRAY MODULE PACKAGING	(A)	0.007	0.001	0.0	0.000	0.000	0.000	0.009	0.0	0.009	2.6	0.000	0.1
	70.2%	TOTALS		0.131	0.053	0.035	0.038	0.032	0.053	0.343	0.0	0.343	100.0	0.361	100.0
			%	38.21	15.54	10.31	11.09	9.48	15.36	100.00					

NOTE: (A)=EXISTING TECHNOLOGY; (B)=NEAR FUTURE; (C)=FUTURE ANNUAL PRODUCTION: 50.0 MEGAWATTS.

Figure 7. Cost summary - ion implantation.

COST ANALYSIS:CASE II:SPIN-ON +POCL3 DIFFUSION(B) 02/03/77 13:09:18 PAGE 1

PROCESS COST OVERVIEW-$/WATT

ASSUMPTIONS: 0.717 WATTS PER SOLAR CELL AND $ 0.0 FOR 7.8 CM (3") DIAMETER WAFER

STEP	YIELD	PROCESS		MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	%	INVEST	%
1	99.0%	SYSTEM "I" WAFER CLEANING	(B)	0.0	0.002	0.002	0.000	0.000	0.000	0.005	0.0	0.005	1.3	0.003	1.0
2	95.0%	SPIN-ON SOURCE:1 SIDE	(B)	0.007	0.010	0.000	0.005	0.002	0.003	0.026	0.0	0.026	6.9	0.018	6.5
3	99.0%	POCL3 DEPOSITION AND DIFFUSION	(A)	0.0	0.017	0.028	0.021	0.003	0.004	0.073	0.0	0.073	19.3	0.031	11.6
4	95.0%	EDGE POLISH	(B)	0.0	0.002	0.004	0.001	0.000	0.001	0.008	0.0	0.008	2.0	0.005	2.0
5	99.0%	GLASS REMOVAL	(B)	0.0	0.002	0.001	0.001	0.000	0.001	0.005	0.0	0.005	1.3	0.005	1.8
6	99.0%	POST DIFFUSION INSPECTION	(B)	0.0	0.003	0.000	0.003	0.003	0.004	0.013	0.0	0.013	3.6	0.030	11.1
7	98.0%	THICK AG METAL-FRONT:AUTO	(B)	0.025	0.009	0.011	0.012	0.006	0.009	0.071	0.0	0.071	18.7	0.062	23.1
8	98.0%	THICK AG METAL-BACK:AUTO	(B)	0.024	0.004	0.005	0.005	0.003	0.004	0.044	0.0	0.044	11.6	0.031	11.5
9	99.0%	AR COATING:SPRAY-ON	(B)	0.002	0.004	0.002	0.001	0.001	0.001	0.011	0.0	0.011	2.8	0.008	3.1
10	80.0%	TEST	(B)	0.0	0.004	0.000	0.003	0.004	0.006	0.018	0.0	0.018	4.7	0.042	15.6
11	98.0%	INTERCONNECT:GAP WELDING	(B)	0.002	0.006	0.002	0.002	0.002	0.003	0.016	0.0	0.016	4.3	0.019	7.2
12	100.0%	DOUBLE GLASS PANEL ASSEMBLY	(B)	0.072	0.002	0.002	0.001	0.001	0.002	0.080	0.0	0.080	21.1	0.014	5.1
13	100.0%	ARRAY MODULE PACKAGING	(A)	0.007	0.001	0.0	0.000	0.000	0.000	0.009	0.0	0.009	2.4	0.000	0.2
	64.6%	TOTALS		0.138	0.066	0.057	0.054	0.024	0.038	0.378	0.0	0.378	100.0	0.269	100.0
			%	36.47	17.46	15.11	14.37	6.41	10.18	100.00					

NOTE: (A)=EXISTING TECHNOLOGY; (B)=NEAR FUTURE; (C)=FUTURE ANNUAL PRODUCTION: 50.0 MEGAWATTS.

Figure 8. Cost summary - spin-on + $POCl_3$ diffusion.

COST ANALYSIS:CASE III:SPIN-ON 2 SIDES(B) 02/03/77 13:09:18 PAGE 1

PROCESS COST OVERVIEW-$/WATT

ASSUMPTIONS: 0.717 WATTS PER SOLAR CELL AND $ 0.0 FOR 7.8 CM (3") DIAMETER WAFER

STEP	YIELD	PROCESS		MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	%	INVEST	%
1	99.0%	SYSTEM "Z" WAFER CLEANING	(B)	0.0	0.002	0.002	0.000	0.000	0.000	0.005	0.0	0.005	1.3	0.003	1.0
2	95.0%	SPIN-ON SOURCE:2 SIDES	(B)	0.014	0.030	0.001	0.012	0.004	0.007	0.068	0.0	0.068	18.6	0.046	16.4
3	98.0%	DIFFUSION	(B)	0.0	0.009	0.002	0.002	0.001	0.003	0.016	0.0	0.016	4.5	0.012	4.3
4	95.0%	EDGE POLISH	(B)	0.0	0.002	0.004	0.001	0.000	0.001	0.008	0.0	0.008	2.1	0.005	1.9
5	99.0%	GLASS REMOVAL	(B)	0.0	0.002	0.001	0.001	0.000	0.001	0.005	0.0	0.005	1.3	0.005	1.7
6	99.0%	POST DIFFUSION INSPECTION	(B)	0.0	0.003	0.000	0.003	0.003	0.004	0.013	0.0	0.013	3.7	0.030	10.8
7	98.0%	THICK AG METAL-BACK:AUTO	(B)	0.024	0.004	0.005	0.005	0.003	0.004	0.045	0.0	0.045	12.3	0.031	11.2
8	98.0%	THICK AG METAL-FRONT:AUTO	(B)	0.024	0.009	0.011	0.012	0.006	0.009	0.070	0.0	0.070	19.4	0.062	22.4
9	99.0%	AR COATING:SPRAY-CN	(B)	0.002	0.004	0.002	0.001	0.001	0.001	0.011	0.0	0.011	3.0	0.008	3.0
10	80.0%	TEST	(B)	0.0	0.004	0.000	0.003	0.004	0.006	0.018	0.0	0.018	4.8	0.042	15.1
11	98.0%	INTERCONNECT:GAP WELDING	(B)	0.002	0.006	0.002	0.002	0.002	0.003	0.016	0.0	0.016	4.5	0.019	7.0
12	100.0%	DOUBLE GLASS PANEL ASSEMBLY	(B)	0.072	0.002	0.002	0.001	0.001	0.002	0.080	0.0	0.080	22.0	0.014	4.9
13	100.0%	ARRAY MODULE PACKAGING	(A)	0.007	0.001	0.0	0.000	0.000	0.000	0.009	0.0	0.009	2.5	0.000	0.2
	64.0%	TOTALS		0.145	0.078	0.031	0.043	0.025	0.041	0.363	0.0	0.363	100.0	0.278	100.0
			%	39.87	21.52	8.63	11.87	6.89	11.22	100.00					

NOTE: (A)=EXISTING TECHNOLOGY; (B)=NEAR FUTURE; (C)=FUTURE ANNUAL PRODUCTION: 50.0 MEGAWATTS.

Figure 9. Cost summary - spin-on 2 sides.

COST ANALYSIS:CASE IV:SCREEN PRINT 2 SIDES(B) 02/03/77 13:09:18 PAGE 1

PROCESS COST OVERVIEW-$/WATT

ASSUMPTIONS: 0.717 WATTS PER SOLAR CELL AND $ 0.0 FOR 7.8 CM (3") DIAMETER WAFER

STEP	YIELD	PROCESS		MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	%	INVEST	%
1	99.0%	SYSTEM "Z" WAFER CLEANING	(B)	0.0	0.001	0.001	0.000	0.000	0.000	0.003	0.0	0.003	1.0	0.002	0.7
2	98.0%	SCREEN PRINT SOURCE:2 SIDES	(B)	0.013	0.008	0.007	0.007	0.003	0.004	0.042	0.0	0.042	12.7	0.031	12.0
3	98.0%	DIFFUSION	(B)	0.0	0.009	0.002	0.002	0.001	0.003	0.016	0.0	0.016	5.0	0.012	4.7
4	99.0%	GLASS REMOVAL	(B)	0.0	0.002	0.001	0.001	0.000	0.001	0.005	0.0	0.005	1.5	0.005	1.9
5	99.0%	POST DIFFUSION INSPECTION	(B)	0.0	0.003	0.000	0.003	0.003	0.004	0.013	0.0	0.013	4.1	0.030	11.7
6	98.0%	THICK AG METAL-BACK:AUTO	(B)	0.024	0.004	0.005	0.005	0.003	0.004	0.045	0.0	0.045	13.6	0.031	12.1
7	98.0%	THICK AG METAL-FRONT:AUTO	(B)	0.024	0.009	0.011	0.012	0.006	0.009	0.070	0.0	0.070	21.4	0.062	24.3
8	99.0%	AR COATING:SPRAY-ON	(B)	0.002	0.004	0.002	0.001	0.001	0.001	0.011	0.0	0.011	3.3	0.008	3.3
9	80.0%	TEST	(B)	0.0	0.004	0.000	0.003	0.004	0.006	0.018	0.0	0.018	5.4	0.042	16.4
10	98.0%	INTERCONNECT:GAP WELDING	(B)	0.002	0.006	0.002	0.002	0.002	0.003	0.016	0.0	0.016	4.9	0.019	7.6
11	100.0%	DOUBLE GLASS PANEL ASSEMBLY	(B)	0.072	0.002	0.002	0.001	0.001	0.002	0.080	0.0	0.080	24.3	0.014	5.3
12	100.0%	ARRAY MODULE PACKAGING	(A)	0.007	0.001	0.0	0.000	0.000	0.000	0.009	0.0	0.009	2.7	0.000	0.2
	69.5%	TOTALS		0.144	0.054	0.033	0.037	0.023	0.038	0.328	0.0	0.328	100.0	0.257	100.0
			%	43.78	16.44	10.09	11.16	7.04	11.49	100.00					

NOTE: (A)=EXISTING TECHNOLOGY; (B)=NEAR FUTURE; (C)=FUTURE ANNUAL PRODUCTION: 50.0 MEGAWATTS.

Figure 10. Cost summary - screen print 2 sides.

	Ion Implant(C) (¢/W)	Spin-on + $POCL_3$(C) (¢/W)	Screen Print 2 Sides(C) (¢/W)
Junction Formation	4.2	6.6	5.1
Metallization	9.4	9.4	9.4
AR Coating	1.1	1.1	1.1
Test and Sort	1.2	1.2	1.2
Interconnect, Encapsulation & Packaging	10.5	10.5	10.5
	26.4	29.0	27.4
Labor & Process Overhead Content	4.6	5.8	5.1

Figure 11. Comparison of three class (C) (advanced) process sequences.

	Ion Implant (¢/W)	Spin-on + $POCl_3$ (¢/W)	Screen Print 2 Sides (¢/W)	Spin-on 2 Sides (¢/W)
Junction Formation	9.3	13.0	7.9	11.5
Metallization	11.5	11.5	11.5	11.5
AR Coating	1.1	1.1	1.1	1.1
Test and Sort	1.8	1.8	1.8	1.8
Interconnect, Encapsulation & Packaging	10.5	10.5	10.5	10.5
	34.3	37.8	32.8	36.3
Labor & Process Overhead Content	9.1	12.0	9.1	12.1

Figure 12. Comparison of four class (B) (near future) process sequences.

SECTION IV

DETAILED COST ESTIMATE FOR ION IMPLANTATION (C)

Because it is the lowest cost sequence, a complete description of Ion Implantation (C) will be given. Recall that except for the junction formation technology, this sequence is identical to the other two recommended class (C) process sequences.

A. SOLAR PANEL DESIGN

The single largest cost component in the assembly of a solar cell panel is the material required to provide structural and environmental projection for the photovoltaic circuit. It is, therefore, necessary to clearly define the panel design considered in the automation study in order that the assembly processes are consistent with the materials selected.

Figure 13 shows the panel design which is the basis for the cost analysis described in this report. The design is characterized by several features which are worthy of comment.

- Glass is used as both substrate and window for the enclosure. We are not convinced that there is a credible alternative to glass in terms of cost and reliable protection for environmental threats. The concept shown calls for the window and substrate to be bonded together structurally so that 1/8-in. sheet can be used in both places and the total assembly is structurally equivalent to a 1/4-in. or greater panel.
- The circuit is configured in a series-parallel arrangement in which four cells are connected in parallel to preserve panel performance if point failures occur at the cell level. The series circuit makes an odd number of traverses across the panel so that the panel interconnection terminals can occur at opposite corners on the panel diagonal. This feature permits ease of packaging for shipment and ease of system interconnection as will be discussed in a later paragraph. The interconnector design utilizes threaded terminals which are ruggedly imbedded into the panel to assure easy system assembly and maintenance (Fig. 14).

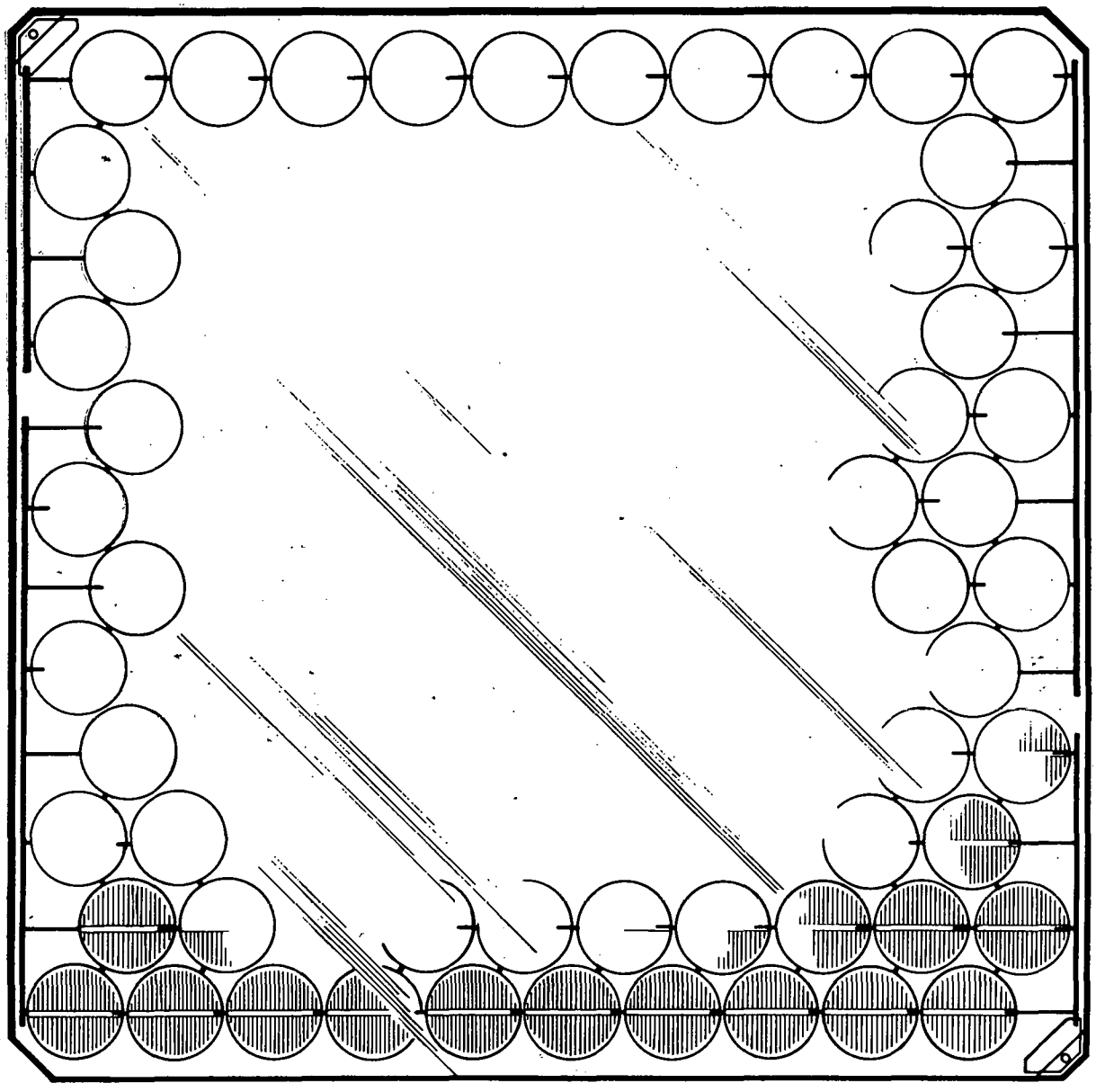

Figure 13. Solar panel design.

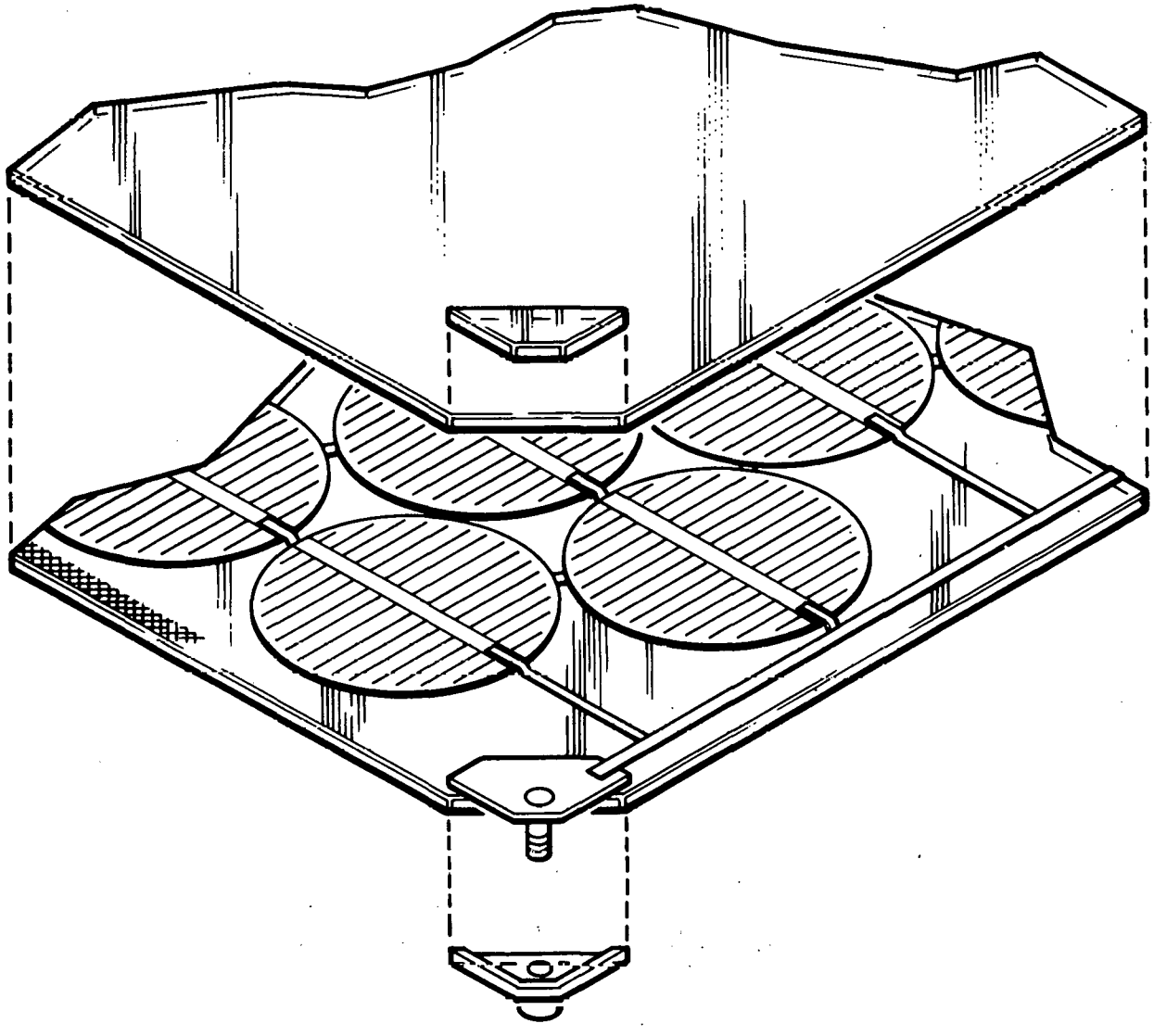

Figure 14. Interconnector design.

- Round cells are utilized since they are available in large quantity. As shown in Fig. 15, the cells are bonded to the substrate using a low-cost compliant bond. Compliant optical filler material is applied between the window and the cells to reduce optical losses in the photon path. By reducing the structural requirements on this material, lower cost compounds can be used. Table 1, originally shown in Quarterly Report No. 3 [1], compares the materials cost for various panel designs. The panel proposed here is column II. By comparing columns I and II, it is easily seen that the elimination of the use of transparent adhesive is a cost-effective step. Note the region between cells does not contain potting compound.

The panel shown in Fig. 13 uses a nonstandard cell size of 4.45-in. diameter in order to meet simultaneously the constraints of 4- x 4-ft panel size, four-parallel-cell circuit, and diagonally opposite circuit termination. The panel has a packing factor of approximately 83% and will deliver 15 V dc and a peak current of 13 A. We find no difficulty in specifying an odd cell size since this solar cell factory will have enough production volume to create as standard any size which meets the need of its products. A different cell size will change the panel dimensions to maintain high panel area efficiency. Detailed baseline cost estimates have been made on the basis of a 3-in. cell as the basic building block. Almost all of the costs of the panel itself are cell size independent, the one exception being interconnection and assembly capital equipment cost which decreases linearly as cell size goes up. Since the cost of this equipment is a small fraction of the total cost and the influence of cell size on its value is small, the analysis shows that the 3- to 5-in. cell size range, panel and assembly costs are almost independent of cell size (10.5¢/W compared with 9.9¢/W for 5-in. cell; see Fig. 36).

B. PANEL INSTALLATION

The proposed panel design is configured for simple and low cost installation. Figure 16 shows a system configuration of solar cell panels which is six panels wide and five panels high (24 x 20 ft). The configuration shows that the panels are installed using standard window glazing techniques. Each

1. B. F. Williams, *Automated Array Assembly*, Quarterly Report 3, ERDA/JPL-954352-76/3, prepared under Contract No. 954352 for Jet Propulsion Laboratory, September 1976.

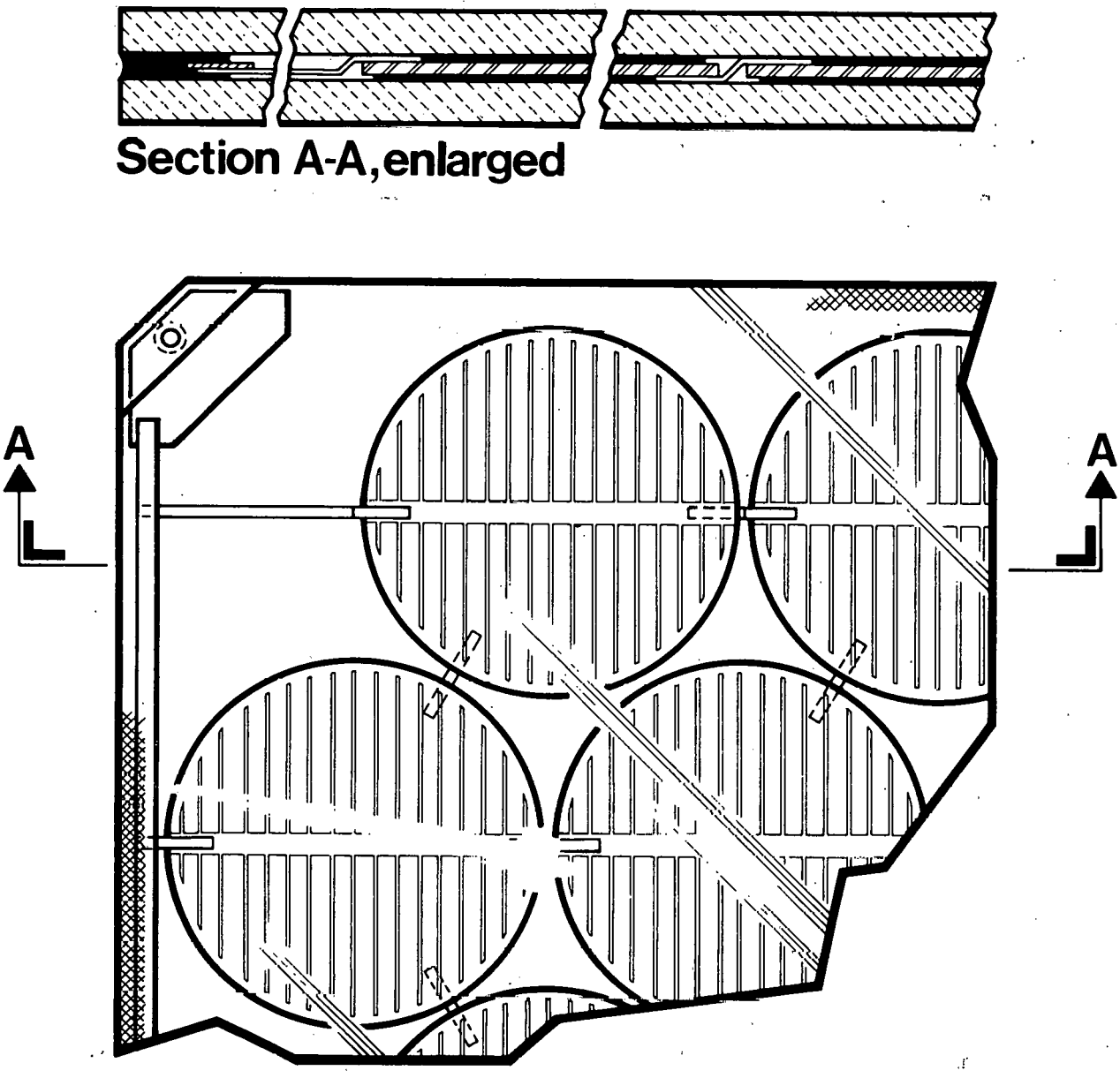

Figure 15. Round cell configuration.

TABLE 1. COST COMPARISON OF PACKAGING MATERIALS

Item	I	II	III	IV	V	VI	VII
Substrate							
1/16 glass sheet					0.19		
1/8 glass sheet		0.22					
0.005 alum. foil			0.05			0.05	0.05
Cell Adhesive							
RTV15/Primer	0.41			0.41			
RTV 102		0.10	0.10		0.10	0.10	0.10
Window							
1/16 glass sheet					0.19		
1/8 glass sheet		0.22		0.22			
1/4 glass sheet	0.44						
1-in.-diam R6 tubing			.45				
1-in.-diam N51 tubing						0.60	
2-in.-diam R6 tubing							1.07
Assembly Closure							
Conformal coating + 3-mil metal	0.11			0.11			
Edge seal		0.04			0.06		
End caps			0.06			0.06	0.03
Panel Connector	0.09	0.09	0.18	0.36	0.36	0.18	0.13
Aluminum Structural Channel	____	____	0.10	____	____	0.10	0.10
Total	1.05	0.67	0.94	1.10	0.90	1.09	1.48

Column Identification:

I - 1/4 glass with conformal coating 4 x 4 ft module
II - 1/8 glass window and substrate bonded together 4 x 4 ft module
III - 1-in.-diam R6 tubing with aluminum for substrate (48 tubes in module)
IV - 1/8 glass with conformal coating (four) 2 x 2 ft panels in a 4 x 4 ft module
V - 1/16 glass window and substrate bonded together into four 2 x 2 ft panels in a 4 x 4 ft module
VI - 1-in.-diam N51 tubing with aluminum foil substrate (48 tubes in module)
VII - 2-in.-diam R6 tubing with aluminum foil substrate (24 tubes in module)

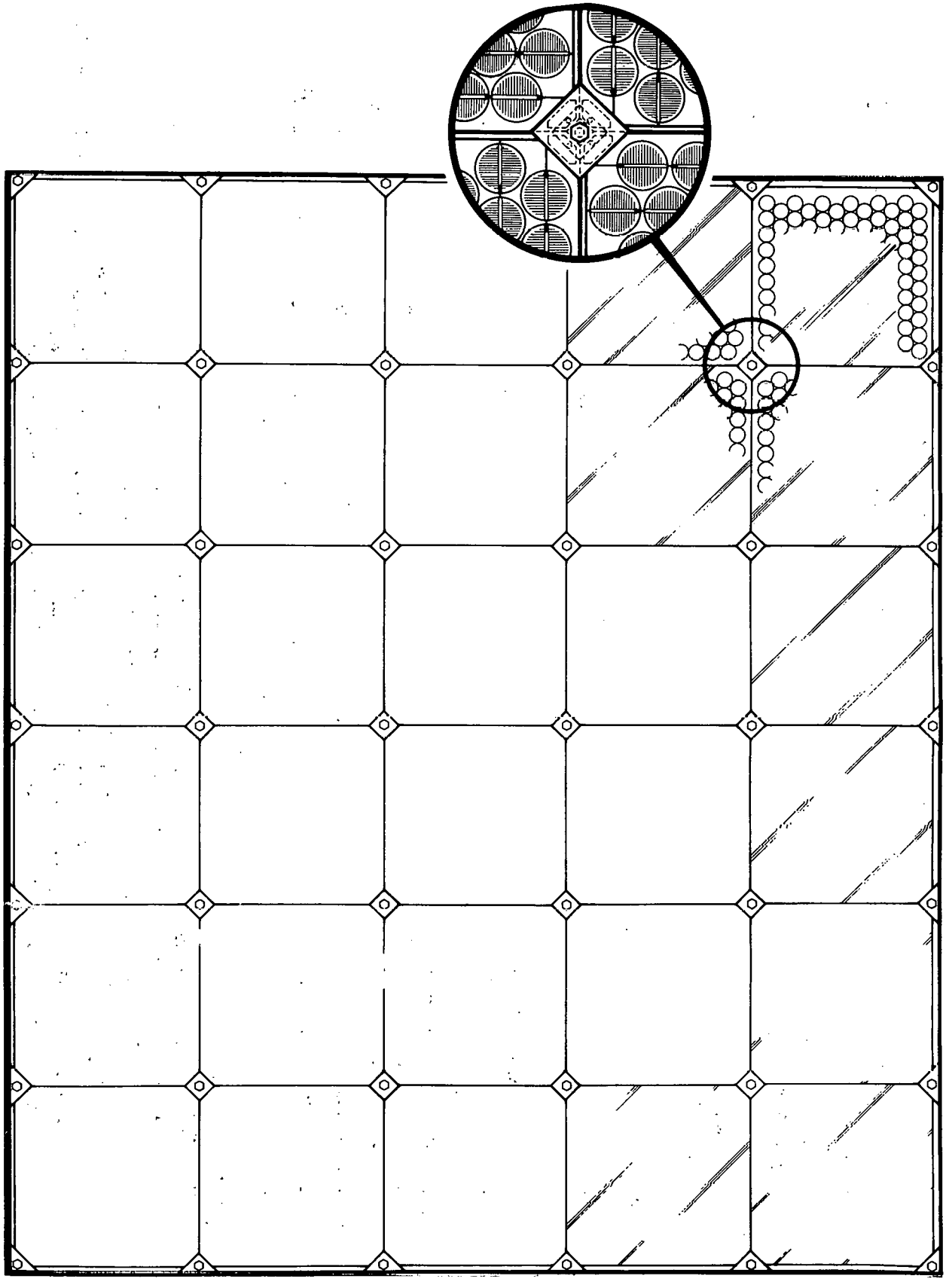

Figure 16. Solar cell panel system configuration.

panel is bedded in a compliant sealing compound and is structurally secured at the corners using a diamond-shaped retaining clip. The spaces between the panels are caulked with clear compliant sealant which give the final assembly the appearance of monolithic glass. The "I" sections of the supporting superstructure all project from the back of the system. All electrical interconnections are made at the point where the four corners of adjacent panels meet. These connections are made at every other intersection point in the panel array. Protection of the interconnection is accomplished using waterproof junction boxes on the back of the structure as shown in the detail view of Fig. 17. Termination of the entire assembly can occur wherever desired by appropriate system layout. In Fig. 16, they are shown at the top of the assembly, the assumption being that a power bus can be safely brought to this point. It should be obvious that a range of series-parallel possibilities can be achieved with the proposed construction because of the symmetry between positive and negative panel terminals. This same symmetry could, of course, cause assembly errors unless adequate coding is used.

C. SOLAR CELL PANEL ASSEMBLY

The floor plan for a production line to assemble solar cell panels is shown in Fig. 18. This diagram indicates the process flow, equipment complement, factory floor space, and operating personnel required to accomplish automated assembly of solar cells. The floor plan is laid out in lines so that multiples of its design throughput can be achieved by locating parallel lines side by side. The nominal throughput of the line shown in the figure is approximately 40,000 W per day or 15 MW per year (345 working days per year) As indicated on the figure the production floor space is 16 x 50 ft, and the associated storage and aisle space is 16 x 30 ft. The numbers on the drawing correspond to pieces of important capital equipment required as part of this line. A listing of this equipment and our estimate of its cost is shown in Table 2. The assembly procedure sequence is described below.

D. PANEL ASSEMBLY LINE FUNCTIONS

1. Sorting

The input into the panel assembly area is cartridges of sorted cells. The exact nature of this sort will not be determined until the distribution

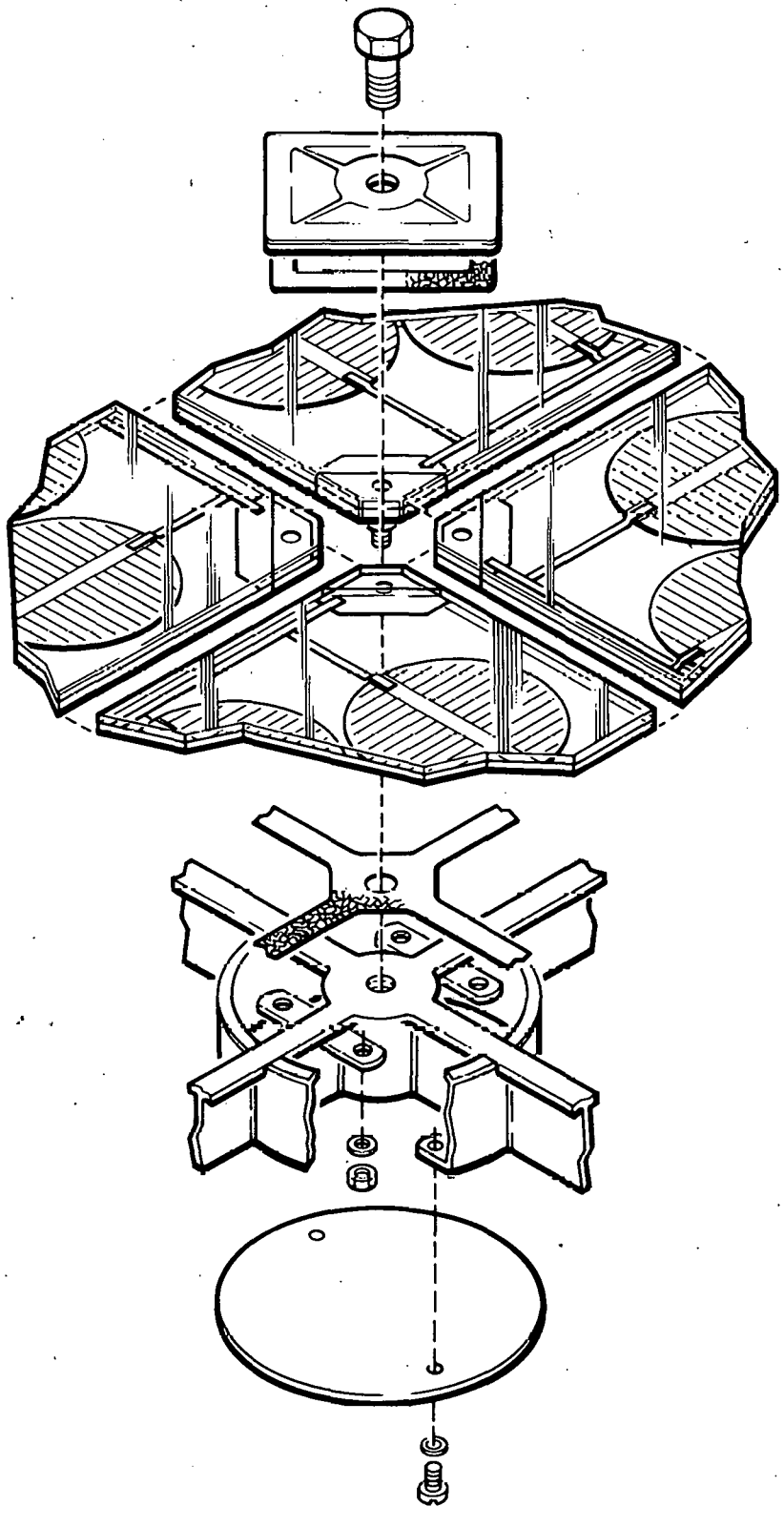

Figure 17. Detail rear view of interconnection.

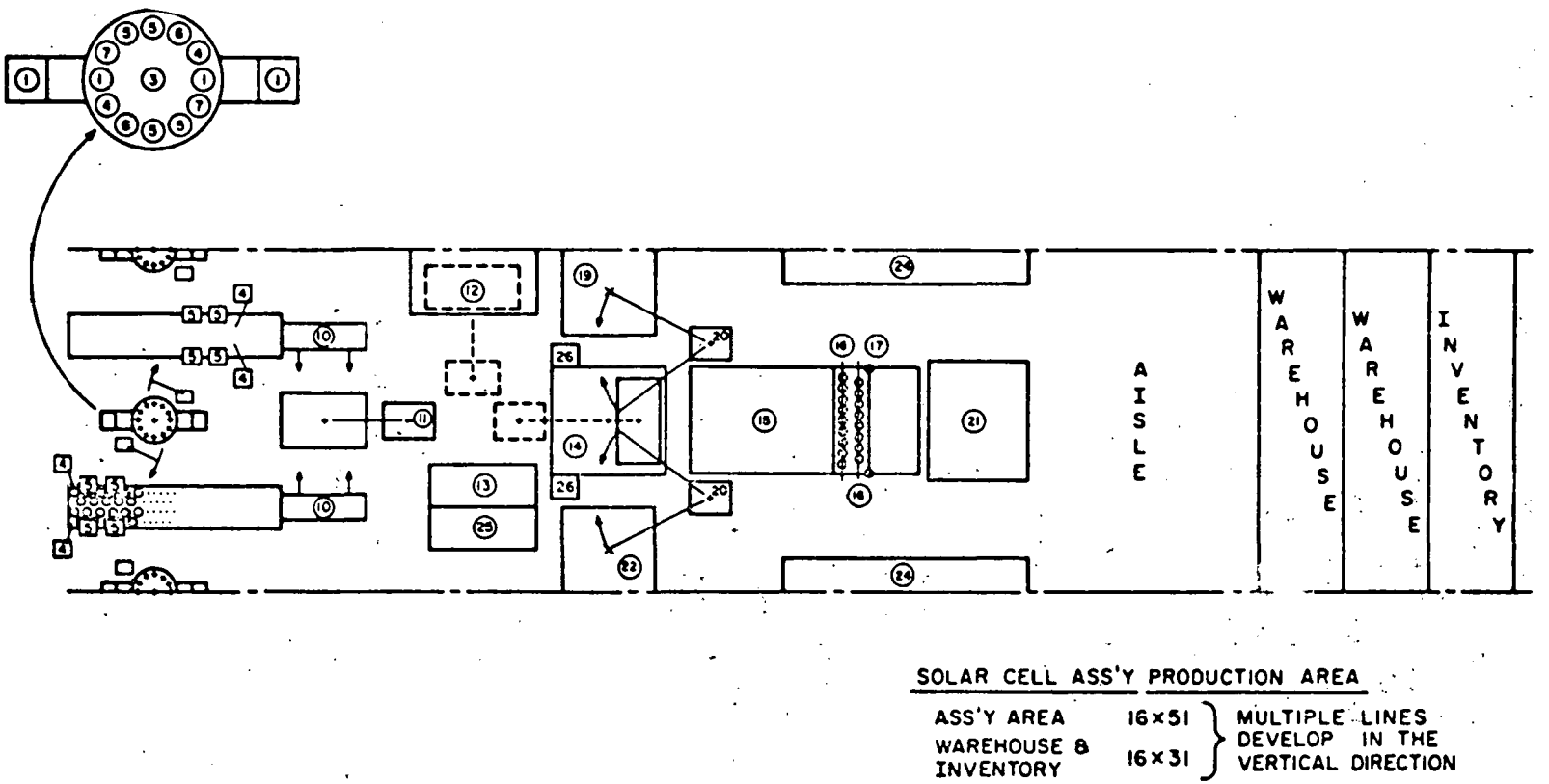

Figure 18. Production line floor plan.

TABLE 2. SOLAR CELL PANEL ASSEMBLY EQUIPMENT

Station No.	Equipment Description	Qty Req'd	Unit Cost $K
1	Wafer Unloader	4	4
2	Linear Index Table	2	10
3	Rotary Index Table	2	25
4	Pick & Place Assembly	10	5
5	Parallel Gap Bonder	18	5
6	Wafer Turner	2	4
7	Interconnect Formation Tool	4	15
8	Microprocessor Control	1	15
9	Sensors & Assembly Wiring	Lot	20
10	Linear Index Table	2	7.5
11	Robot Arm & Vacuum Hand	1	25
12	Pulse Xenon I-V Tester	1/2	80
13	String Reject Position	1	2
14	Assembly Fixture	1	15
15	Linear Index Table	1	10
16	Adhesive Dispenser	2	10
17	Sealant Bead Dispenser	1	10
18	Panel Assembly Sensors	Lot	15
19	Window Supply Fixture	1	5
20	Glass Handling Robot	2	17.5
21	Substrate Storage/Dispenser	1	5
22	Curing Rack	1	20
23	System Integration	Lot	50
24	Repair Bench	1	3
25	Repaired String Position	1	6
26	Electrical Connector Dispenser	2	6
27	Linear Index Table	1	10

of electrical properties versus yield of low-cost solar cells is determined. If one can presume that there will be a greater variation in the properties of a low-cost cell than now exists with space-quality products, then such sorting will be a crucial importance. Several sorting strategies are now being investigated to determine how to configure a panel to most closely approach the performance inherent in the individual cells.

2. Cell Handling

A key element of a solar module factory will be the cell-handling equipment. It is this equipment which will determine the speed and throughput of

the line and be responsible for most of the physical breakage which occurs during the various processes. Ideally, it would be desirable to have a continuous process with no operator intervention until the operation is complete. For reasons of process flexibility, the need for buffering between various stations, sorting after various steps, and just the practicality of building up a production line incrementally, cartridge cell handling has been built around each process. It appears that 500-cell cartridges are feasible so that at 1000 cells per hour reasonable amounts of operator attention are possible.

The cell-handling sequence during assembly takes the cell from the cartridge to a rotary table and then to linear assembly table. Circuit strings are created on this table and combined into parallel arrangements in subsequent steps. The handling of strings from this point to final assembly is controlled by a robot arm which interfaces the circuit with a vacuum pickup hand.

a. Airtrack Cell Transport - Figure 19 shows a cartridge of cells pneumatically unloaded onto a linear air-track cushion for transport to a vacuum chuck position on a rotary index welding table. Air transport of the cells helps to reduce physical damage to the cells during transport; it is being used increasingly in the semiconductor industry and would become more highly recommended as cell size increases. Handling rates of 1200 cells/hour are feasible with minor extrapolation from present equipment. A circular cell format is most compatible with this transport technique since edge chipping of any noncircular format has always been a problem during wafer handling.

b. Rotary Index Table - A rotary index table is used at the first interconnect station since it permits all of the preparatory steps for string assembly to be completed off-line. The table in Fig. 19 has six positions, but notice that the throughput of the line would not change regardless of how many positions were on the table. As presently conceived, the operations completed on the rotary table are:

- position the cell
- orient the cell with regard to angular position

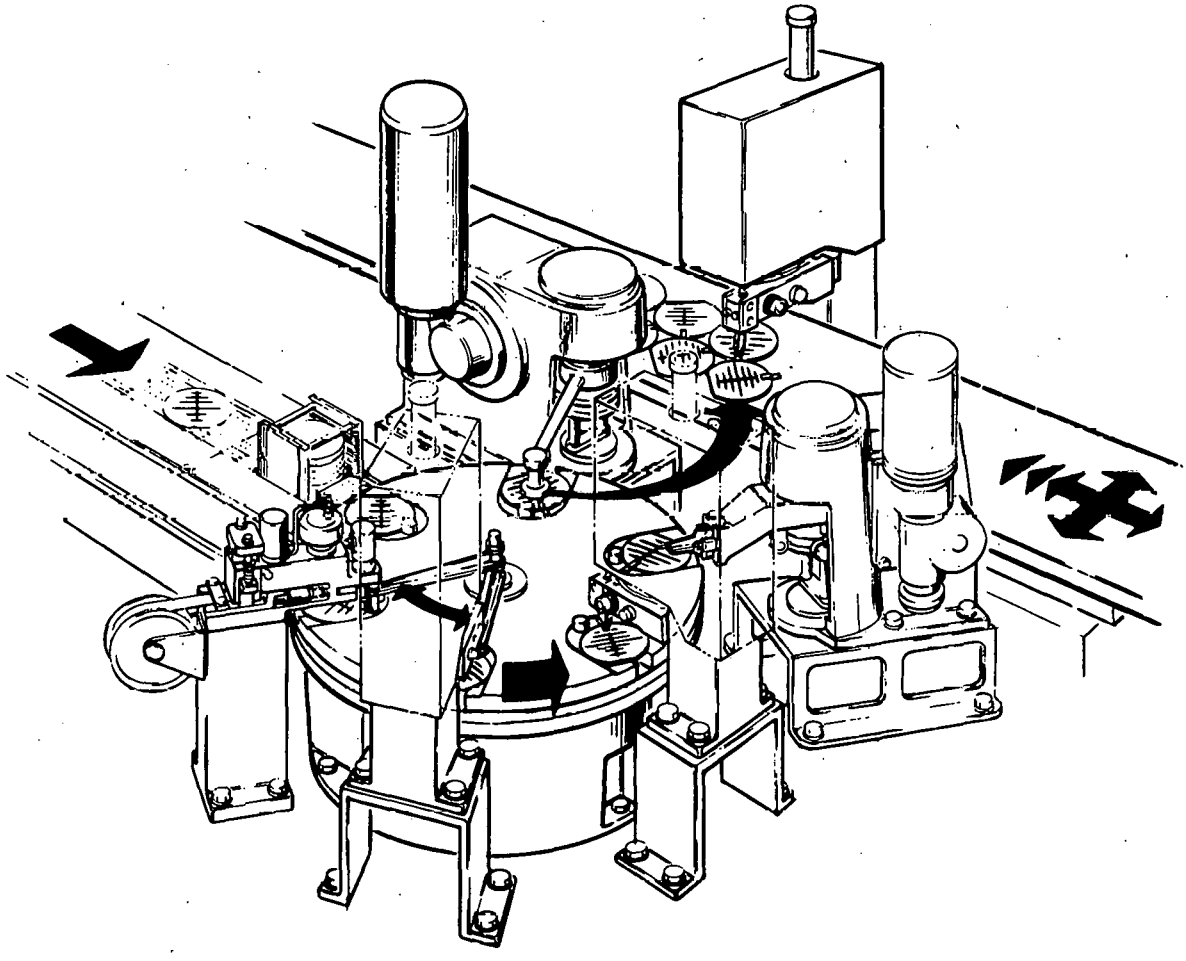

Figure 19. Air-track cell transport of cells onto rotary.

- form and place interconnects
- make two front side welds
- turn over cells
- prepare contact areas for interconnection (if necessary)
- pick up position for string assembly table

c. Series Connection Table - Series and parallel interconnections are made on a linear motion table. In Fig. 18, station 10 represents the interconnection assembly area. Four bonds are made at this station. Two of these are the series connections for each of the two strings being assembled at the station. The others are the bonds necessary to make parallel connection between each of the cells in the two series strings.

When the strings are completed, they are advancing to a combining position indicated by the arrows at station 10. Two groups of cells from adjacent tables are combined at a pickup point for the assembly robot at station 11.

d. Panel Assembly Robot - After the cells are bonded together electrically, they are handled by a multiported vacuum pickup hand which is 4 ft long and four circuit strings wide. This vacuum hand will be mounted on the end of a robot arm which has 5 degrees of freedom, namely, X translation, Y translation, Z translation, rotation about the arm axis at the carriage, and rotation about the arm axis at the vacuum head. The robot arm, under computer control, can address five string positions: string pickup, string test, panel placement, string reject, and repair pickup.

The function at each of these positions will be discussed in later paragraphs. The cell handling until the cells have been bonded to the panel substrate is by virtue of vacuum contact at the robot arm pickup hand. The total cycle time for the robot is 100 s per four-string placement. Since each robot has two arms each acting 180° out of phase with the other, the effective cycle rate is 50 s. The timing sequence for this position is shown in Table 3.

3. Panel Materials Handling

The other panel materials are glass (substrate and window), adhesives and sealants, and electrical components. Glass and final panel handling will be accomplished using a simplified robot arm with vacuum pickup hand. Adhesive and sealant will be dispensed in dots and beads from an automatic pneumatic dispensing machine. Electrical parts will be located and placed using pick and place equipment fed from a vibrating bowl.

4. Panel Assembly Processes

In addition to material handling, panel assembly involves five other significant processes, namely, electrical interconnect bonding, physical bonding of cells to substrate and window, electrical testing of circuit strings, final panel wiring, and protective envelope closure.

TABLE 3. PANEL ASSEMBLY TIMING SEQUENCE

Step	Time Sequence (s) Arm 1	Arm 2
Four-string pickup	0-2	50-52
Transfer to test	2-4	52-54
Test sequence	4-6	54-56
Transfer to rejects	6-10	56-60
Drop defective part (if any)	10-12	60-62
Pick up replacement string (if required)	12-14	62-64
Index to final bonding station	14-16	64-66
Dwell at bonding station	16-46	66-96
Index to panel placement	46-66	96-16
Dwell at panel placement	66-96	16-46
Return to pickup	96-100	46-50

a. Solar Cell Interconnection - Interconnection of solar cells can be done most quickly and reliably using parallel gap techniques in conjunction with appropriate automated material-handling equipment. This technique permits the metallurgical operation to proceed quickly, under close control, and with minimum consumables. The cost, thus, is low because consumed material is minimum and process yield is maximum.

There is no final conclusion on which metallurgical process is preferred since more technology input is required with regard to application of the candidate processes applied to thick-film conductors. Our analysis shows that the cost to create the interconnect bond will not be significantly different if the bonding technique is solder reflow, welding, or ultrasonic bonding.

b. Electrical test - Testing of assembled solar cell strings will be accomplished using a pulsed Xenon I-V tester. Existing equipment is available to generate a detailed I-V curve in less than 1 s. Since the illuminated aperture of this tester can be large and testing time is only a fraction of string dwell at the test site, it will be possible to share a tester for two assembly lines.

Testing criteria can be established on the strings based on the input cell characteristics. Cell changes induced by interconnect bonding or poor quality bonds can be identified using this technique and the involved circuit strings rejected.

c. Cell Bonding - The preferred technique for bonding solar cells to a structural substrate is through the use of a compliant silicone rubber adhesive on the backside of the cell. This allows the use of higher strength and lower cost compounds for this purpose. It will be necessary to use a transparent material between the cells and the panel window in order to reduce the optical losses caused by refractive index mismatch. By reducing the structural demand on this material, simpler and low-cost materials can be used.

The proposed design calls for a structural epoxy bond between substrate and window. This bond will allow the load incident on the panel to be shared by both panel and substrate. This epoxy will be dispensed at the same time as the cell bonding adhesive and will be located in the spaces adjacent to every fourth cell in the panel.

d. Final Panel Wiring - The panel design shown in Fig. 13 utilizes a corner connector bonded between the substrate and window to make electrical penetration from the protective envelope. The positive and negative connectors and associated power bus will be bonded to the appropriate string interconnectors after the cells are bonded to the substrate. Placement of these components is done automatically with pick and place equipment.

e. Protective Envelope Closure - The final assembly operation calls for placement of the panel window onto a completely assembled circuit substrate. In

this operation previously metered quantities of spacer and connector adhesives, optical matching material, and panel edge sealant are compressed to create intimate contacts with their related parts. The finished panel is positioned in a wiring rack which is kept at elevated temperature during a short cure cycle. The closure is visually examined at this point along with other physical properties of the assembly. Final packaging in a shock-isolated crate prepares the products for delivery from the plant.

5. Panel Assembly Summary

The assembly procedures and associated equipment can be divided into four groupings: string interconnection, testing, panel assembly, and final assembly. The following summary description lists the steps on the assembly procedure and by reference to Fig. 18 identifies the equipment required to perform each function.

	Assembly Step	Station No.
INTERCONNECTION	1. Unload cells from cartridge	1
	2. Form and place series interconnects	4
	3. Bond interconnect to cell (2 places)	5
	4. Turn over cell	6
	5. Lift and place on linear table	7
	6. Make cell series connection	5
	7. Form and place parallel interconnects	4
	8. Make cell parallel connection	5
	9. Advance double string to assembly pickup point	10
TEST	10. Lift two double strings and index to test position	11
	11. Generate illuminated I-V curve for each of two double strings	13
PANEL ASSEMBLY	12. Index string to reject position and leave any rejected string	13
	13. Index to repaired string pickup position and lift replacement strings	25
	14. Return to parallel bonding station and combine double strings	10
	15. Eject panel substrate to panel prep area	21
	16. Dispense closure bead onto substrate	16

	Assembly Step	Station No.
PANEL ASSEMBLY	17. Dispense structural epoxy onto substrate	16
	18. Dispense cell adhesive onto substrate	16
	19. Advance prepared substrate to assembly position	15
	20. Place quadruple string on a prepared panel substrate	14
	21. Place and bond panel connectors and bus	26,5
FINAL ASSEMBLY	22. Dispense optical matching material onto panel window	19
	23. Lift and place window onto completed circuit assembly	20
	24. Lift and place complete assembly in a curing rack	20
	25. Place curing rack in curing oven	22
	26. Remove finished assembly for final inspection and packaging	-

String repair take place at station 24. Repaired strings are placed at station 25 for automatic pickup.

The process parameters for the interconnect step, the double glass panel assembly, and the array module packing are given in Figs. 20, 21, and 22.

E. PROCESS: TEST

This step automatically tests the completed cells for photovoltaic performance, separates the acceptable cells from the rejects, and sorts the good cells according to efficiency in 1% increments. The machine is microprocessor-controlled and consists of a test station and sorter. At the test station the wafer is contacted by probes and exposed to a known light source. The shape of the I-V curve is determined in the region of the knee (maximum power point) to determine the fill factor. The open-circuit voltage and short-circuit current are determined by the preset test program, and from these results the efficiency is calculated. The sorter, which is activated by the result of the test station, automatically assigns the cell to a cassette of the right classification. Process parameters are shown in Fig. 23.

PROCESS PARAMETERS:INTERCONNECT:GAP WELDING 04/18/77 09:51:24 PAGE 72

ESTIMATE DATE:12/27/76 BY:BEN SHELPUK, PC4971, CAMDEN, BLDG. 10-8-12 CLASS:ARRAY FABRICATION
CATEGORY:PROCESS DEFINITION TECHNOLOGY LEVEL:NEAR FUTURE MATERIAL FORM:3" WAFER.
INPUT UNIT:SOLAR CELLS OUTPUT UNIT:SOLAR CELLS TRANSPORT IN:500 SHEET CASSETTE TRANSPORT OUT:PICKUP TABLE
PROCESS YIELD: 98.0% YIELD GROWTH PROFILE: C
INPUT UNIT SALVAGE FACTOR: 0.0 FACTOR GP#: 0 SALVAGE OPTION:VALUE INS
PERFORMANCE FACTORS-I(R)/I(SC): 1.0000000E+00 V(R)/V(OC): 1.0000000E+00 F(R)/F: 1.0000000E+00

INPUT UNITS:	0.	0.	0.
FLOOR SPACE,FT**2:	0.	0.	0.

DESCRIPTION:INTERCONNECTION:GAP WELDING(B)

ASSUMPTIONS:

1. 3" DIAMETER WAFER, 12-14 MILS THICK,(100) ORIENTATION,P-TYPE, 1-5 OHM-CM.
2. REWORK OPERATOR REWORKS STRING TEST REJECTS (=3% OF INPUT)

PROCEDURE

1. WAFER FROM CASSETTE TO AIR TRACK TO ROTARY TABLE FOR P-CONTACT BOND.
2. AUTOMATIC PICKUP AND PLACE FROM ROTARY TABLE TO LINEAR TABLE FOR SERIES BOND.
3. INDIVIDUAL STRINGS ARE PRESENTED TO THE TEST STATION USING PICK AND PLACE HANDLING.
4. STRINGS ARE ILLUMINATED WITH A PULSED XENON LAMP AND A COMPLETE I-V CURVE IS GENERATED.
5. ACCEPTANCE CRITERIA WILL BE PROGRAMMED INTO TEST LOGIC.

INVESTMENTS

INVESTMENT NAME	MAX. THRUPUT UNITS	% INPUT UNITS PROCESSED	FIRST COST	AVAIL.	AREA,FT**2
GW INTERCONNECT EQUIP.(B)	3800.00 CELLS/HR	100.0%	$ 271000.	85.0%	130.
STRING TEST EQUIPMENT(B)	7600.00 CELLS/HR	100.0%	$ 80000.	95.0%	110.

LABOR

(DL=DIRECT LABOR PERSONS;TL=TOTAL LABOR PERSONS)

NAME	LABOR REQUIREMENTS BASE	# PERSONS/SHIFT/BASE UNIT	THRUPUT/HR/PERSON	% INPUT UNITS PROCESSED
HOURLY OPERATOR	GW INTERCONNECT EQUIP.(B)	3.330E-01		
REWORK OPERATOR	GW INTERCONNECT EQUIP.(B)	1.000E+00		
HOURLY OPERATOR	STRING TEST EQUIPMENT(B)	2.000E-01		
MAINTENANCE	GW INTERCONNECT EQUIP.(B)	1.000E-01		
MAINTENANCE	STRING TEST EQUIPMENT(B)	1.000E-01		
FOREMAN	DL	1.000E-01		

SUPPLIES/EXPENSES

EXPENSE NAME	ANNUAL FIXED PART	VARIABLE PART	UNITS	BASE
ELECTRICITY	0.0	6.000E+00	KWH.	PER AVAILABLE INVESTMENT-HOUR OF GW INTERCONNECT EQUIP.(B)
ELECTRICITY	0.0	3.000E+00	KWH.	PER AVAILABLE INVESTMENT-HOUR OF STRING TEST EQUIPMENT(B)
AG-PLATED CU WIRE	0.0	1.430E-03	$	PER INPUT UNIT. % UNITS= 100.0%
ELECTRODES	0.0	1.430E-03	$	PER INPUT UNIT. % UNITS= 100.0%

Figure 20. Process parameters - interconnect step.

PROCESS PARAMETERS:DOUBLE GLASS PANEL ASSEMBLY 04/18/77 09:51:24 PAGE 74

ESTIMATE DATE:01/25/77 BY:BEN SHELPUK, PC4971, CAMDEN, BLDG. 10-8-12 CLASS:ARRAY FABRICATION
CATEGORY:PROCESS DEFINITION TECHNOLOGY LEVEL:NEAR FUTURE MATERIAL FORM:3" WAFER.
INPUT UNIT:SOLAR CELLS OUTPUT UNIT:ARRAY MODULES TRANSPORT IN:PICKUP TABLE TRANSPORT OUT:CURING RACK
PROCESS YIELD:100.0% YIELD GROWTH PROFILE: 0
INPUT UNIT SALVAGE FACTOR: 0.0 FACTOR GP#: 0 SALVAGE OPTION:VALUE IN$
PERFORMANCE FACTORS-I(R)/I(SC): 1.000000E+00 V(R)/V(OC): 1.000000E+00 F(R)/F: 1.000000E+00

INPUT UNITS:	0.	0.	0.
FLOOR SPACE,FT**2:	0.	0.	0.

DESCRIPTION:PANEL ASSEMBLY, FINAL ASSEMBLY, & TEST(B)

ASSUMPTIONS:

1. 3" DIAMETER WAFER, 12-14 MILS THICK,(100) ORIENTATION,P-TYPE, 1-5 OHM-CM.
2. NO BREAKAGE ASSUMED.
3. DOUBLE GLASS PANEL, 14.6FT**2, SEE QUARTERLY REPORT #3, PAGE 38, TABLE 5, COLUMN 2.
4. NOTE: TO DETERMINE MATERIAL $/FT**2, MULTIPLY MATERIAL COST SHOWN($/CELL) X 224 CELLS/14.6FT**2.
5. 5 CURING RACKS NEEDED FOR EACH PIECE OF PANEL ASSEMBLY EQUIPMENT.

PROCEDURE

1. AUTOMATIC PICK UP & PLACEMENT OF MULTIPLE STRINGS ONTO SUBSTRATE POSITIONED ON X-Y MOTION TABLE.
2. STRINGS COMPLIANTLY BONDED TO GLASS SUBSTRATE.
3. PARALLEL ELECTRICAL CONNECTION OF STRINGS.
4. SERIES CONNECTION TO POWER TERMINATIONS BY PARALLEL GAP WELDING.
5. FINAL ASSEMBLY:WINDOW IS APPLIED TO THE ASSEMBLY USING PICK AND PLACE.
6. WINDOW IS BONDED TO THE SUBSTRATE USING A MULTIPLICITY OF EPOXY BONDED SPACERS.
7. ENCLOSED SPACE IS SEALED FROM MOISTURE PENETRATION BY A PERIMETER BOND OF POLYISOBUTYLENE.
8. FINAL ASSEMBLY IS TRANSFERRED TO CURING RACKS USING PICK AND PLACE.

INVESTMENTS

INVESTMENT NAME	MAX. THRUPUT	UNITS	% INPUT UNITS PROCESSED	FIRST COST	AVAIL.	AREA,FT**2
PANEL ASSEMBLY EQUIPMENT(B)	3724.00	CELLS/HR	100.0%	$ 103000.	85.0%	300.
FINAL ASSEMBLY EQUIPMENT(B)	3724.00	CELLS/HR	100.0%	$ 125000.	85.0%	280.
CURING RACK	744.80	CELLS/HR	100.0%	$ 50.	100.0%	20.

LABOR

(DL=DIRECT LABOR PERSONS;TL=TOTAL LABOR PERSONS)

NAME	LABOR REQUIREMENTS BASE	# PERSONS/SHIFT/BASE UNIT	THRUPUT/HR/PERSON	% INPUT UNITS PROCESSED
HOURLY OPERATOR	PANEL ASSEMBLY EQUIPMENT(B)	2.500E-01		
HOURLY OPERATOR	FINAL ASSEMBLY EQUIPMENT(B)	2.500E-01		
MAINTENANCE	PANEL ASSEMBLY EQUIPMENT(B)	1.000E-01		
MAINTENANCE	FINAL ASSEMBLY EQUIPMENT(B)	1.000E-01		
FOREMAN	DL	1.000E-01		

SUPPLIES/EXPENSES

EXPENSE NAME	ANNUAL FIXED PART	VARIABLE PART	UNITS	BASE
ELECTRICITY	0.0	8.000E-01	KWH.	PER AVAILABLE INVESTMENT-HOUR OF PANEL ASSEMBLY EQUIPMENT(3)
ELECTRICITY	0.0	4.000E+00	KWH.	PER AVAILABLE INVESTMENT-HOUR OF FINAL ASSEMBLY EQUIPMENT(3)
SUBSTRATE	0.0	1.430E-02	$	PER INPUT UNIT. % UNITS= 100.0%
CELL ADHESIVE	0.0	6.520E-03	$	PER INPUT UNIT. % UNITS= 100.0%
WINDOW	0.0	1.430E-02	$	PER INPUT UNIT. % UNITS= 100.0%
PANEL CONNECTOR	0.0	5.870E-03	$	PER INPUT UNIT. % UNITS= 100.0%
EDGE SEAL	0.0	3.910E-03	$	PER INPUT UNIT. % UNITS= 100.0%
EPOXY SPACER	0.0	2.610E-03	$	PER INPUT UNIT. % UNITS= 100.0%
SOLVENT	0.0	1.300E-03	$	PER INPUT UNIT. % UNITS= 100.0%

Figure 21. Process parameters - double glass panel assembly.

PROCESS PARAMETERS:ARRAY MODULE PACKAGING 04/18/77 09:51:24 PAGE 77

ESTIMATE DATE:12/28/76 BY:BEN SHELPUK, PC4971, CAMDEN, BLDG. 10-8-12 CLASS:PACKAGING
CATEGORY:PROCESS DEFINITION TECHNOLOGY LEVEL:EXISTING MATERIAL FORM:3" WAFER.
INPUT UNIT:ARRAY MODULES OUTPUT UNIT:ARRAY MODULES TRANSPORT IN:CURING RACK TRANSPORT OUT:BOX
PROCESS YIELD:100.0% YIELD GROWTH PROFILE: 0
INPUT UNIT SALVAGE FACTOR: 0.0 FACTOR GP#: 0 SALVAGE OPTION:VALUE IN$
PERFORMANCE FACTORS-I(R)/I(SC): 1.000000E+00 V(R)/V(OC): 1.000000E+00 F(R)/F: 1.000000E+00

INPUT UNITS:	0.	0.	0.
FLOOR SPACE,FT**2:	0.	0.	0.

DESCRIPTION:ARRAY MODULES PLACED IN WOOD CRATE.

ASSUMPTIONS:

1. 14.6 FT**2 PANEL.
2. 14.6 FT**2 OF WOOD CRATE NEEDED AT $.08 PER FT**2 OF PANEL.
3. 1 OPERATOR CAN PACKAGE 50 MODULES/HR USING PACKAGING EQUIPMENT.
4. N, THE NUMBER OF PANELS PER WOOD CRATE, IS TO BE DETERMINED.

PROCEDURE

1. OPERATOR REMOVES N PANELS FROM CURING RACK & PLACES THEM IN BOX.
2. BOX STAPLED.
3. BOX PLACED ON STACK FOR REMOVAL TO WAREHOUSE.

INVESTMENTS

INVESTMENT NAME	MAX. THRUPUT UNITS	% INPUT UNITS PROCESSED	FIRST COST	AVAIL.	AREA,FT**2
PACKAGING EQUIPMENT	50.00 A.M./HR	100.0%	$ 25000.	100.0%	100.

LABOR

(DL=DIRECT LABOR PERSONS;TL=TOTAL LABOR PERSONS)

NAME	LABOR REQUIREMENTS BASE	# PERSONS/SHIFT/BASE UNIT	THRUPUT/HR/PERSON	% INPUT UNITS PROCESSED
HOURLY OPERATOR	PACKAGING EQUIPMENT	1.000E+00		
FOREMAN	DL	1.000E-01		

SUPPLIES/EXPENSES

EXPENSE NAME	ANNUAL FIXED PART	VARIABLE PART	UNITS	BASE
BOX FOR MODULE	0.0	1.170E+00	$	PER INPUT UNIT. % UNITS= 100.0%

Figure 22. Process parameters - array module packing.

PROCESS PARAMETERS:TEST 04/18/77 09:51:24 PAGE 63

ESTIMATE DATE:12/27/76 BY:DAVE RICHMAN, X3207, RCA LABS, E-321A CLASS:TEST
CATEGORY:PROCESS DEFINITION TECHNOLOGY LEVEL:NEAR FUTURE MATERIAL FORM:3" WAFER.
INPUT UNIT:SHEETS OUTPUT UNIT:SOLAR CELLS TRANSPORT IN:500 SHEET CASSETTE TRANSPORT OUT:500 SHEET CASSETTE
PROCESS YIELD: 80.0% YIELD GROWTH PROFILE: 0
INPUT UNIT SALVAGE FACTOR: 0.0 FACTOR GP#: 0 SALVAGE OPTION:FRACTION OF INPUT UNIT VALUE
PERFORMANCE FACTORS-I(R)/I(SC): 1.000000E+00 V(R)/V(OC): 1.000000E+00 F(R)/F: 1.000000E+00

INPUT UNITS:	0.	0.	0.
FLOOR SPACE,FT**2:	0.	0.	0.

DESCRIPTION:WAFER ELECTRICAL TEST AND SORT.

ASSUMPTIONS:

1. 3" DIAMETER WAFER, 12-14 MILS THICK,(100) ORIENTATION,P-TYPE, 1-5 OHM-CM.
2. TEST FOR: OPEN CIRCUIT VOLTAGE;SHORT CIRCUIT CURRENT;REVERSE BIAS LEAKAGE; FILL FACTOR.
3. MINICOMPUTER-CONTROLLED MEASUREMENT OF 12 POINTS ALONG KNEE OF I-V CURVE FOR KNOWN LIGHTING.
4. WAFERS BELOW 10% EFFICIENCY ARE REJECTED. 80% YIELD ESTIMATED.

PROCEDURE

1. OPERATOR LOADS CASSETTE INTO MACHINE.
2. WAFERS AUTOMATICALLY FED TO TEST EQUIPMENT AND MEASUREMENTS MADE.
3. WAFERS SORTED INTO MAGAZINES USING CRITERIA TO BE DEFINED.
4. OPERATOR REMOVES CASSETTES AS THEY ARE FILLED.

INVESTMENTS

INVESTMENT NAME	MAX. THRUPUT	UNITS	% INPUT UNITS PROCESSED	FIRST COST	AVAIL.	AREA,FT**2
SILTEC WAFER SORTER-W.E.T.	1200.00	SH/HR	100.0%	$ 175000.	80.0%	200.

LABOR

(DL=DIRECT LABOR PERSONS;TL=TOTAL LABOR PERSONS)

NAME	LABOR REQUIREMENTS BASE	# PERSONS/SHIFT/BASE UNIT	THRUPUT/HR/PERSON	% INPUT UNITS PROCESSED
HOURLY OPERATOR	SILTEC WAFER SORTER-W.E.T.	2.500E-01		
MAINTENANCE	SILTEC WAFER SORTER-W.E.T.	2.000E-01		
FOREMAN	DL	1.000E-01		

SUPPLIES/EXPENSES

EXPENSE NAME	ANNUAL FIXED PART	VARIABLE PART	UNITS	BASE
ELECTRICITY	0.0	5.000E+00	KWH.	PER AVAILABLE INVESTMENT-HOUR OF SILTEC WAFER SORTER-W.E.T.

Figure 23. Process parameters - test.

F. ANTIREFLECTION COATING, SPRAY-ON

Use of conventional spin-on application of solutions for depositing the AR coating on solar cells is expensive because of the low rate of throughput and will cause problems of film uniformity because of the metallization pattern interfering with the uniform spreading of the solution.

We have examined the technical and economic feasibility of spray coating techniques as an alternative, and we are entirely convinced that spray coating is indeed the technique of choice for this particular application.

Commercial equipment, designed primarily for the semiconductor industry, offers excellent control and performance of high-quality film deposits, and remarkable economy.

The heart of the machine is the vapor carrier system which uses a superheated chemically inert hydrocarbon vapor of high molecular weight as the transporting medium for the coating material. The low velocity and pressure at which the coating material is conveyed by the vapor to the target surface minimizes the problems encountered with systems based on pressurized gasses as the carrier. The solar cells are transported in a 6-wafer-wide stream by a conveyor belt from the load station into the spray station. The coating is applied by a fully automated and adjustable spray gun which traverses the six 3-in.-diam wafers at a set speed and distance. Work flow proceeds at a rate of typically 3/4-in./s. Under these conditions the Autocoater can process 5,400 cells per hour, or 4.4×10^7 cells per year.

The thickness of the $SiO_2 + TiO_2$ containing AR film after drying and baking is specified to be 700 Å. The control of coating thickness is within $\pm$5%. Figure 24 shows the performance of such an AR coating which was spun-on compared with thermally oxidized Ta_2O_5. Both layers make a very good AR coating.

An additional part of the system is an infrared-heated section capable of attaining 500°C. Since we require only 200° and 400°C for bake out (15 min each, at present), this limit is quite adequate. The rate of throughput may be a problem, however, and may require either a change in processing or the addition of heaters working in parallel.

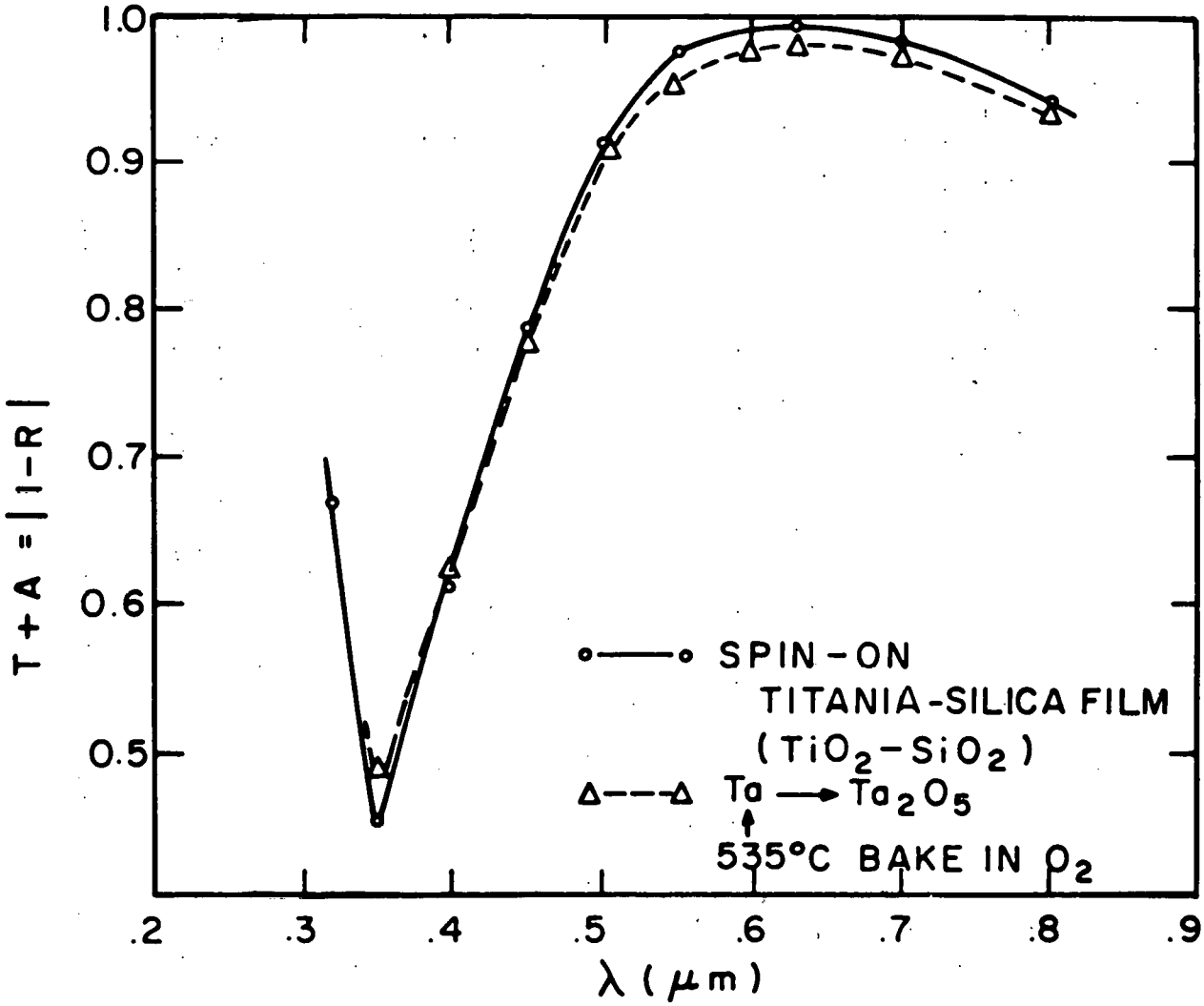

Figure 24. Reflection spectra: spin-on titania-silica film and Ta_2O_5 formed by thermal oxidation of evaporated Ta.

PROCESS PARAMETERS:AR COATING:SPRAY-ON 04/18/77 09:51:24 PAGE 60

ESTIMATE DATE:02/28/77 BY:RCA ESTIMATES CLASS:AR COATING
CATEGORY:PROCESS DEFINITION TECHNOLOGY LEVEL:NEAR FUTURE MATERIAL FORM:3" WAFER
INPUT UNIT:SHEETS OUTPUT UNIT:SHEETS TRANSPORT IN:500 SHEET CASSETTE TRANSPORT OUT:500 SHEET CASSETTE
PROCESS YIELD: 99.0% YIELD GROWTH PROFILE: C
INPUT UNIT SALVAGE FACTOR: 0.0 FACTOR GP#: 0 SALVAGE OPTION:FRACTION OF INPUT UNIT VALUE
PERFORMANCE FACTORS-I(R)/I(SC): 1.000000E+00 V(R)/V(OC): 1.000000E+00 F(R)/F: 1.000000E+00

INPUT UNITS:	0.	0.	C.
FLOOR SPACE,FT**2:	0.	0.	C.

DESCRIPTION:SPRAY-ON ANTIREFLECTION COATING(B)

ASSUMPTIONS:

1. 3" DIAMETER WAFER, 12-14 MILS THICK,(100) ORIENTATION,P-TYPE, 1-5 OHM-CM.
2. 500 WAFERS/CASSETTE
3. NOTE: IN-HOUSE AR COATING NEEDS TO BE DEVELOPED.
4. LIQUID SPRAY-ON SOURCE(TIO2,SIO2) AT $10/LITER. 0.1 CM**3 WILL COVER 1 SIDE WITH 0.07 MICRONS.
7. APPLIED AFTER FINAL METALLIZATION.
8. OVEN BAKE REQUIRED AT 400 C. FOR 1/2 HR. IN AIR.
9. ROOM REQUIREMENTS: DRY,CLEAN FILTERED AIR, 2830 LITERS/HR/SYSTEM.

PROCEDURE

1. WAFERS ARE LOADED FROM CASSETTE TO DEPOSITION ZONE.
2. INERT HYDROCARBON CARRIER GAS TRANSPORTS COATING MATERIAL.
3. AFTER DEPOSITION, WAFER TRANSPORTED VIA BELT TO INFRARED DRYING ZONE.
4. WAFERS ARE BAKED FOR 1/2 HR. AT 400 C. IN AIR.
5. WAFERS LOADED INTO CASSETTE.

INVESTMENTS

INVESTMENT NAME	MAX. THRUPUT	UNITS	% INPUT UNITS PROCESSED	FIRST COST	AVAIL.	AREA,FT**2
ZICON MODEL 11000 AUTOCOATER	5400.00	SH/HR	100.0%	$ 120000.	85.0%	100.
OPTICAL REFLECTOMETER	5400.00	SH/HR	100.0%	$ 20000.	85.0%	16.

LABOR

(DL=DIRECT LABOR PERSONS;TL=TOTAL LABOR PERSONS)

NAME	LABOR REQUIREMENTS BASE	# PERSONS/SHIFT/BASE UNIT	THRUPUT/HR/PERSON	% INPUT UNITS PROCESSED
HOURLY OPERATOR	ZICON MODEL 11000 AUTOCOATER	1.000E+00		
MAINTENANCE	ZICON MODEL 11000 AUTOCOATER	2.500E-01		
MAINTENANCE	OPTICAL REFLECTOMETER	5.000E-02		

SUPPLIES/EXPENSES

EXPENSE NAME	ANNUAL FIXED PART	VARIABLE PART	UNITS	BASE
ELECTRICITY	0.0	1.000E+01	KWH.	PER AVAILABLE INVESTMENT-HOUR OF ZICON MODEL 11000 AUTOCOATER
VAPOR CARRIER	0.0	3.000E-01	$	PER AVAILABLE INVESTMENT-HOUR OF ZICON MODEL 11000 AUTOCOATER
IN-HOUSE SPRAY-ON AR COATING	0.0	1.000E-01	CM**3	PER INPUT UNIT, % UNITS= 100.0%

Figure 25. Process parameters - antireflection coating, spin-on.

G. METALLIZATIONS

1. Thick-Film Screen Printing

We believe that a metallization technology based on screen-printed contacts is the most cost effective. The principal problem with this technology is to combine low contact resistance with low penetration and high adhesion.

In Quarterly Report No. 3 [1] we showed that the contact resistance must be below 0.1 Ω-cm^2 to not seriously affect device performance. In an experimental evaluation of commercial Al, Ni, and Ag inks we have not found it possible to produce this low a contact resistance without producing excessive penetration.

Therefore, we have investigated formulating a silver metallization with the proper n-type dopant, phosphorus, which would require a low firing temperature and thereby minimize penetration and contact resistance simultaneously. $AgPO_3$ was selected because of its low melting point, i.e., 485°C. Similar Ag-P compounds are under study. A small amount of the material was prepared by reacting $AgNO_3$ with $NaPO_3$-stabilized metaphosphoric acid (HPO_3). The precipitate was dried, crushed, and ground to pass through a 325-mesh sieve. An "off-the-shelf" silver powder was mechanically blended with the $AgPO_3$ powder to yield 95 wt pct Ag-5 wt pct $AgPO_3$. This mixture was suspended in a cellulosic-type organic vehicle and screen printed using a newly designed pattern containing two rows of 0.2-cm-diam dots. The dots were fired onto the same silicon material, i.e., n-type, (100), 5 x 10^{19}/cm^3, as that used for the evaluation of the commercial inks. The lowest test firing temperature was 500°C, since the $AgPO_3$ melting point is 485°C and a contact angle of 8° was found for $AgPO_3$ on silicon when fired for 2 min at this temperature. A summary of the results for 5-min firings at 500°, 600°, and 700°C is shown in Table 4.

Determination of the least square fit is based on at least four test points. The lowest specific contact resistance was found to be 0.11 Ω-cm^2 at 600°C. However, the poor correlation in each case suggested that the metal-to-silicon contacts are spotty in nature. Angle lapping and metallographic examination disclosed two contributing causes for the poor correlation: gaps in the physical contact between metallization and silicon and voids in the metal. The gap does, however, decrease with increasing temperature, and, most

TABLE 4. SPECIFIC CONTACT RESISTANCE OF Ag-$AgPO_3$ METALLIZATION*

Firing Temperature (°C)	Least Square Fit, $y = b + mx$	r^2	Specific Contact Resistance Ω-cm^2
500	$y = 39.88 + 122.56\ x$	0.49	0.65
600	$y = 6.55 + 32.54\ x$	0.29	0.11
650	$y = 17.44 + 6.94\ x$	0.17	0.28
700	$y = 24.15 - 2.12\ x$	0.34	0.39

*Dot-to-dot spacing ranged from 0.6 to 1.9 cm, center-to-center. Gold wire Kelvin connection was used for resistance measurements. Specific contact resistance, ρ_c, = 1/2 b times dot area.

important at the highest temperature, there is no evidence of metallization penetration into the silicon. The high density of voids present in the metallization also contributes to an apparently high specific contact resistance. Closing of the silicon-to-metal gap and reduction of voids in the fired film will result when changes are made in the silver and $AgPO_3$ particle size distribution and relative amounts of each.

We believe this is an area very worthy of continued attention.

In our cost estimates we have assumed this technology has been developed, and we use ink costs as they exist today. For this metallizing step, cassettes with silicon wafers arrive on carts from the preceding test station (i.e., that following n-p junction formation) and the cassettes are manually placed into the loader adjacent to the screen-printing machine. The loader automatically feeds silicon wafers into the screen printer which applies the particular metallization pattern. This sequence requires three printing and drying operations prior to firing: first the back, then the collecting grid and then the bus bar on the front.

Detailed evaluation of the technique using printing pastes based on silver, aluminum, and nickel have been carried out from technical and cost viewpoints. The minimum cost of typical Al and Ni pastes ($1.90/troy ounce) is lower than that of Ag paste ($5.42/troy ounce based on the December 1976 market price for Ag). All three pastes shrink close to 50% on drying and firing. The electrical conductivity of a fired coating depends on the paste

composition and the firing conditions, and has been assumed in all calculations to be one-half of the bulk conductivity for Ag and one-third for both Al and Ni. For comparing various metallizations, it is important to point out that simply changing metal thickness to provide equal conductivity is not the appropriate course. The metals all cost different amounts and have different conductivities, and the optimum thickness must be determined from minimizing the overall system $/W.

The cost optimization factor (F) with respect to Ag is

$$\left.\begin{array}{l}\text{Factor for}\\ \text{optimizing}\\ \text{pattern}\\ \text{thickness}\end{array}\right\} = F = \frac{\left(\frac{\rho_M}{\rho_{Ag}}\right)^{1/2}}{\left(\frac{\$cm^{-3}_M}{\$cm^{-3}_{Ag}}\right)^{1/2}}$$

where M refers to any fired metal paste and Ag refers to the fired Ag paste.

Compared with Ag, the optimum Al thickness is 4.22 times as thick and the optimum Ni is 6.63 times as thick. The actual thickness of the optimum Ag pattern is derived below.

As can be seen in the cost summary (Fig. 2), the total cost for the metallization step is on the order of 10¢/W. The process parameters for the front and back metallization are shown in Figs. 26 and 27.

2. Metallizing by Nickel/Solder Deposition

a. Basic Process - Because of its seeming cost effectiveness, a cost estimate has been completed for this alternate metallization process for the purpose of comparison with other methods. Several techniques and process combinations of metal depositions by plating are possible. The process sequence selected is based on well-established electroless plating and solder deposition technology. Essentially, a thin layer of electroless nickel is selectively deposited on both sides of the cell, followed by sintering to create a nickel silicide with good ohmic contact, electroless plating of one additional nickel layer, and, finally, deposition of molten tin-lead solder to provide an ample thickness of metal for good conductance. The entire process is an almost fully automated batch operation where unit lots of 1000 wafers are processed automatically on a continuous basis requiring a minimal amount of labor.

PROCESS PARAMETERS:THICK AG METAL-FRONT:AUTO 01/20/77 16:15:43 PAGE 53

ESTIMATE DATE:01/13/77 BY:WERNER KERN, X2094, RCA LABS, 03-076 CLASS:METALLIZATION
CATEGORY:PROCESS DEFINITION TECHNOLOGY LEVEL:FUTURE MATERIAL FORM:3" WAFER.
INPUT UNIT:SHEETS OUTPUT UNIT:SHEETS TRANSPORT IN:500 WAFER CASSETTE TRANSPORT OUT:500 WAFER CASSETTE
PROCESS YIELD: 99.0% YIELD GROWTH PROFILE: 0
SUBPROCESS USED:SCREEN PRINT WAFER REWORK
INPUT UNIT SALVAGE FACTOR: 0.0 FACTOR GP#: 0 SALVAGE OPTION:VALUE IN$
PERFORMANCE FACTORS-I(R)/I(SC): 1.000000E+00 V(R)/V(OC): 1.000000E+00 F(R)/F: 1.000000E+00

INPUT UNITS:	0.	0.	0.
FLOOR SPACE,FT**2:	0.	0.	0.

DESCRIPTION:SCREEN PRINTING AND SINTERING CONDUCTIVE NETWORK-FRONT

ASSUMPTIONS:

1. 3" DIAMETER WAFER, 12-14 MILS THICK,(100) ORIENTATION,P-TYPE, 1-5 OHM-CM.
2. BACK METALLIZATION PATTERN MUST BE SCREEN PRINTED FIRST.
3. AG PASTE: $5.42/TROY OZ. = $.1743/GM, 80% AG, WHEN AG COSTS $4.40/TROY OZ.
   DENSITY OF AG PASTE=3.75G/CM**3. (31.1G=1 TROY OZ.)
   2:1 RATIO FOR INK THICKNESS TO POST FIRING AG THICKNESS.
4. FRONT AG FINE GRID: 5% COVERAGE, 17 MICRONS THICK AFTER FIRING.
5. FRONT BUS BAR: 1% COVERAGE, 170 MICRONS THICK AFTER FIRING.
6. SCREEN PRINT & DRY SYSTEM:

ITEM	COST	POWER	COMMENTS
LOADER	10.7K	1KW	INSERTS WAFER INTO PRINTER
PRINTER	24.4K	1KW	PRINTER APPLIES PATTERN
COLLATOR	10.0K	1KW	FORMS PARALLEL ROWS FOR DRYER.
DRYER	20.0K	10KW	DRIES INK TO PREVENT SMEARING.
RELOADER	14.7K	1KW	RELOADS WAFERS INTO CASSETTE.
CASSETTES	4.0K	-	HOLDS WAFERS FOR PRINTER.
TOTALS	83.8K	14KW	

   ********NOTE: $125K ESTIMATED FOR ADVANCED SYSTEM.
7. SCREEN PRINT & FIRE SYSTEM:

ITEM	COST	POWER	COMMENTS
LOADER	10.7K	1KW	INSERTS WAFER INTO PRINTER
PRINTER	24.4K	1KW	PRINTER APPLIES PATTERN
COLLATOR	10.0K	1KW	FORMS PARALLEL ROWS FOR DRYER.
DRYER	20.0K	10KW	DRIES INK TO PREVENT SMEARING.
FURNACE	45.0K	15KW	SINTERS PATTERN AT 550 C.
RELOADER	14.7K	1KW	RELOADS WAFERS INTO CASSETTE.
CASSETTES	4.0K	-	HOLDS WAFERS FOR PRINTER.
TOTALS	128.6K	29KW	

   *********NOTE: $200K ESTIMATED FOR ADVANCED SYSTEM.
8. BELT->CASSETTE LOADER CAN DO 6000 WAFERS/HR.
9. SCREEN AT $25, REPLACED 3 TIMES PER DAY FOR FINE GRID.
   SCREEN IS REPLACED 2 TIMES PER DAY FOR BUS BAR SYSTEM.
   SQUEEGES AT $.40, REPLACED ONCE PER HOUR.

Figure 26. Process parameters - front metallization.

PROCEDURE

1. OPERATOR LOADS CASSETTE FROM BACK METALLIZATION STEP INTO LOADER.
2. SCREEN PRINT & DRY SYSTEM APPLIES FINE GRID.
   OPTICAL SCANNER VALIDATES PATTERN. 10% REJECT ESTIMATE.
3. OPERATOR LOADS CASSETTE FOR SCREEN PRINT & FIRE SYSTEM.
4. SYSTEM APPLIES FRONT BUS BAR & FIRES. (SEPARATE PRINT STEP NEEDED SINCE PATTERN IS THICKER THAN FINE GRID.)
   OPTICAL SCANNER VALIDATES PATTERN BEFORE FIRING. 1% BUS BAR REJECTS ESTIMATED.
   REJECTS ARE LOADED INTO A CASSETTE BY BELT->CASSETTE STACKER FOR REWORK.

INVESTMENTS

INVESTMENT NAME	MAX. THRUPUT	UNITS	% INPUT UNITS PROCESSED	FIRST COST	AVAIL.	AREA,FT**2
SCREEN PRINT & DRY SYSTEM-2	1800.00	SH/HR	111.0%	$ 125000.	80.0%	1600.
OPTICAL SCANNER	1800.00	SH/HR	111.0%	$ 50000.	80.0%	16.
BELT->CASSETTE STACKER	1800.00	SH/HR	111.0%	$ 15000.	80.0%	0.
SCREEN PRINT & FIRE SYSTEM-2	1800.00	SH/HR	101.0%	$ 200000.	80.0%	1600.
OPTICAL SCANNER	1800.00	SH/HR	101.0%	$ 50000.	80.0%	16.
BELT->CASSETTE STACKER	1800.00	SH/HR	101.0%	$ 15000.	80.0%	0.

LABOR

(DL=DIRECT LABOR PERSONS;TL=TOTAL LABOR PERSONS)

NAME	LABOR REQUIREMENTS BASE	# PERSONS/SHIFT/BASE UNIT	THRUPUT/HR/PERSON	% INPUT UNITS PROCESSED
HOURLY OPERATOR	SCREEN PRINT & DRY SYSTEM-2	2.000E-01		
HOURLY OPERATOR	SCREEN PRINT & FIRE SYSTEM-2	2.000E-01		
MAINTENANCE	SCREEN PRINT & DRY SYSTEM-2	2.000E-01		
MAINTENANCE	SCREEN PRINT & FIRE SYSTEM-2	2.000E-01		
MAINTENANCE	OPTICAL SCANNER	1.000E-02		
FOREMAN	DL	1.000E-01		

SUPPLIES/EXPENSES

EXPENSE NAME	ANNUAL FIXED PART	VARIABLE PART	UNITS	BASE
ELECTRICITY	0.0	1.400E+01	KWH.	PER AVAILABLE INVESTMENT-HOUR OF SCREEN PRINT & DRY SYSTEM-2
ELECTRICITY	0.0	2.900E+01	KWH.	PER AVAILABLE INVESTMENT-HOUR OF SCREEN PRINT & FIRE SYSTEM-2
ELECTRICITY	0.0	1.000E-01	KWH.	PER AVAILABLE INVESTMENT-HOUR OF OPTICAL SCANNER
SCREENS	0.0	2.880E+00	$	PER AVAILABLE INVESTMENT-HOUR OF SCREEN PRINT & DRY SYSTEM-2
SCREENS	0.0	1.920E+00	$	PER AVAILABLE INVESTMENT-HOUR OF SCREEN PRINT & FIRE SYSTEM-2
SQUEEGEES	0.0	4.000E-01	$	PER AVAILABLE INVESTMENT-HOUR OF SCREEN PRINT & DRY SYSTEM-2
SQUEEGEES	0.0	4.000E-01	$	PER AVAILABLE INVESTMENT-HOUR OF SCREEN PRINT & FIRE SYSTEM-2
SOLVENT-INK	0.0	1.440E-01	CM**3	PER INPUT UNIT. % UNITS= 111.0%
SOLVENT-INK	0.0	1.440E-01	CM**3	PER INPUT UNIT. % UNITS= 101.0%
THERMOCOUPLE,ETC.	0.0	6.060E-04	$	PER INPUT UNIT. % UNITS= 111.0%
THERMOCOUPLE,ETC.	0.0	6.060E-04	$	PER INPUT UNIT. % UNITS= 101.0%
INK AG-FRONT FINE GRID	0.0	3.820E-03	$	PER INPUT UNIT. % UNITS= 100.0%
INK AG-FRONT FINE GRID LOST	0.0	1.600E-03	$	PER INPUT UNIT. % UNITS= 11.0%
INK AG-FRONT BUS BAR	0.0	8.950E-03	$	PER INPUT UNIT. % UNITS= 100.0%
INK AG-FRONT BUS BAR LOST	0.0	3.760E-03	$	PER INPUT UNIT. % UNITS= 1.0%

Figure 26. (Continued).

PROCESS PARAMETERS:THICK AG METAL-BACK:AUTO 04/18/77 09:51:24 PAGE 51

ESTIMATE DATE:02/03/77 BY:WERNER KERN, X2094, RCA LABS, 03-076 CLASS:METALLIZATION
CATEGORY:PROCESS DEFINITION TECHNOLOGY LEVEL:FUTURE MATERIAL FORM:3" WAFER.
INPUT UNIT:SHEETS OUTPUT UNIT:SHEETS TRANSPORT IN:500 SHEET CASSETTE TRANSPORT OUT:500 SHEET CASSETTE
PROCESS YIELD: 99.0% YIELD GROWTH PROFILE: 0
INPUT UNIT SALVAGE FACTOR: 0.0 FACTOR GP#: 0 SALVAGE OPTION:VALUE IN$
PERFORMANCE FACTORS-I(R)/I(SC): 1.000000E+00 V(R)/V(OC): 1.000000E+00 F(R)/F: 1.000000E+00

INPUT UNITS:	0.	0.	0.
FLOOR SPACE,FT**2:	0.	0.	0.

DESCRIPTION:SCREEN PRINTING AND SINTERING CONDUCTIVE NETWORK-BACK

ASSUMPTIONS:

1. 3" DIAMETER WAFER, 12-14 MILS THICK,(100) ORIENTATION,P-TYPE, 1-5 OHM-CM.
2. BACK METALLIZATION PATTERN MUST BE SCREEN PRINTED FIRST.
3. AG PASTE: $5.42/TROY OZ. = $.1743/GM, 80% AG, WHEN AG COSTS $4.40/TROY OZ.
   DENSITY OF AG PASTE=3.756/CM**3. (31.1G=1 TROY OZ.)
   2:1 RATIO FOR INK THICKNESS TO POST FIRING AG THICKNESS.
   NOTE: 5 MILS THINNEST LINE POSSIBLE. WIDTH GREATER THAN OR EQUAL TO 4 TIMES THICKNESS.
4. BACK AG GRID: 25% COVERAGE, 8.5 MICRONS THICK AFTER FIRING.
5. SCREEN PRINT & FIRE SYSTEM:

ITEM	COST	POWER	COMMENTS
LOADER	10.7K	1KW	INSERTS WAFER INTO PRINTER
PRINTER	24.4K	1KW	PRINTER APPLIES PATTERN
COLLATOR	10.0K	1KW	FORMS PARALLEL ROWS FOR DRYER.
DRYER	20.0K	10KW	DRIES INK TO PREVENT SMEARING.
FURNACE	45.0K	15KW	SINTERS PATTERN AT 550 C.
RELOADER	14.7K	1KW	RELOADS WAFERS INTO CASSETTE.
CASSETTES	4.0K	-	HOLDS WAFERS FOR PRINTER.
TOTALS	128.8K	29KW	

   *******NOTE: $200K ESTIMATED FOR ADVANCED SYSTEM.
6. BELT->CASSETTE LOADER CAN DO 6000 WAFERS/HR.
7. SCREEN AT $23, REPLACED 2 TIMES PER DAY.
   SQUEEGES AT $.40, REPLACED ONCE PER HOUR.
8. COST OF 0.5% BACK REWORK IGNORED.
9. FIRING OF BACK NEEDED SO THAT PASTE IS NOT REMOVED IN CASE OF FRONT GRID REWORK.

PROCEDURE

1. OPERATOR LOADS CASSETTE FROM PREVIOUS STEP INTO LOADER.
2. SCREEN PRINT & FIRE SYSTEM APPLIES BACK GRID.
   OPTICAL SCANNER VALIDATES PATTERN. 0.5% REJECTS REWORKED.
   REJECTS ARE LOADED INTO A CASSETTE BY BELT->CASSETTE STACKER FOR REWORK.
3. CASSETTE TRANSFERRED TO FRONT METALLIZATION PROCESS.
4. REJECTS ARE REWORKED & RECYCLED.

INVESTMENTS

INVESTMENT NAME	MAX. THRUPUT	UNITS	% INPUT UNITS PROCESSED	FIRST COST	AVAIL.	AREA,FT**2
SCREEN PRINT & FIRE SYSTEM-2	1800.00	SH/HR	100.5%	$ 200000.	80.0%	1600.
OPTICAL SCANNER	1800.00	SH/HR	100.5%	$ 50000.	80.0%	16.
BELT->CASSETTE STACKER	1800.00	SH/HR	100.5%	$ 15000.	80.0%	0.

Figure 27. Process parameters - back metallization.

PROCESS PARAMETERS:THICK AG METAL-BACK:AUTO 04/18/77 09:51:24 PAGE 51.1

LABOR

(DL=DIRECT LABOR PERSONS:TL=TOTAL LABOR PERSONS)

NAME	LABOR REQUIREMENTS BASE	# PERSONS/SHIFT/BASE UNIT	THRUPUT/HR/PERSON	% INPUT UNITS PROCESSED
HOURLY OPERATOR	SCREEN PRINT & FIRE SYSTEM-2	2.000E-01		
MAINTENANCE	SCREEN PRINT & FIRE SYSTEM-2	2.000E-01		
MAINTENANCE	OPTICAL SCANNER	1.000E-02		
FOREMAN	DL	1.000E-01		

SUPPLIES/EXPENSES

EXPENSE NAME	ANNUAL FIXED PART	VARIABLE PART	UNITS	BASE	
ELECTRICITY	0.0	2.900E+01	KWH.	PER AVAILABLE INVESTMENT-HOUR OF SCREEN PRINT & FIRE SYSTEM-2	
ELECTRICITY	0.0	1.000E-01	KWH.	PER AVAILABLE INVESTMENT-HOUR OF OPTICAL SCANNER	
SCREENS	0.0	1.920E+00	$	PER AVAILABLE INVESTMENT-HOUR OF SCREEN PRINT & FIRE SYSTEM-2	
SQUEEGEES	0.0	4.000E-01	$	PER AVAILABLE INVESTMENT-HOUR OF SCREEN PRINT & FIRE SYSTEM-2	
SOLVENT-INK	0.0	1.440E-01	CM**3	PER INPUT UNIT. % UNITS=	101.0%
THERMOCOUPLE,ETC.	0.0	6.060E-04	$	PER INPUT UNIT. % UNITS=	101.0%
INK AG-BACK GRID	0.0	1.280E-02	$	PER INPUT UNIT. % UNITS=	100.0%
INK AG-BACK GRID LOST	0.0	5.380E-03	$	PER INPUT UNIT. % UNITS=	0.5%

Figure 27. Process parameters - back metallization. (Continued)

b. Outline of Processing Sequence

(1) Deposition of Mask Pattern

- Screen print a reverse metallization pattern of organic masking material on the cell front side to protect 95° of area. Leave the cell backside exposed.
- Pass the wafers through a drying oven to evaporate solvent material from the masking material.

(2) Surface Cleaning

- Immerse the wafers in mild oxidizing solution to remove organic impurities from the exposed surface without affecting the mask coating.
- Rinse in deionized water.
- Dry mechanically.

(3) Sensitization and Complexing

- Sensitize in bath of $PdCl_2$ (activator)-HF-CH_3CO_2H.
- Rinse in deionized water.
- Complex in bath of H_2O-C_3H_7OH (wetting agent)-NH_4OH (neutralizer)-NH_4Cl (complexant).

(4) First Plating and Mask Removal

- Immerse in bath containing $NiCl_2$, NaH_2PO_2, $Na_3C_6H_5O_7$, NH_4Cl, NH_4OH, and H_2O.
- Plate at 80°C for 45 s to deposit a P-containing Ni film of 500 to 750 Å thickness.
- Rinse in deionized water.
- Remove organic mask coating by solvent extraction.

(5) Sintering

- Transfer the wafers onto conveyor belt and into furnace.
- Expose to 550° to 600°C in an atmosphere of N_2-H_2 to create nickel silicide.

(6) Nickel Stripping

- Immerse in HNO_3.
- Rinse in deionized water.
- Apply light oxide etch in HF-NH_4F-H_2O solution.
- Rinse in deionized water.

(7) Second Plating

- Re-immerse in nickel plating bath to deposit 0.3 to 0.5 μm of Ni (P).
- Rinse in deionized water.

(8) Fluxing and Solder Deposition

- Immerse in flux solution.
- Drain, dry, and preheat the wafers.
- Introduce into 5% Sn-95% Pb solder bath at 350°C.
- Hold in bath for an optimal residence time.
- Withdraw at a controlled velocity.

(9) Final Cleaning

- Remove flux residue by immersion in ultrasonic cleaning bath.
- Rinse in deionized water.
- Dry mechanically.

c. Cost Estimation - Estimates of production cost were based on the assumption that 1×10^8 wafers of 3-in. diameter are to be processed in a three-shift, 24-hour operation of 345 days per year. Unit batches of 1000 wafers would be processed automatically through the process sequence outlined in the previous section. Calculation of the time requirements for each process step indicates that five separate production lines operating in parallel would be required, each line producing 2×10^7 wafers per year. Not considering the yield factor, cost per wafer has been computed as approximately $0.30, of which 64% accounts for materials, 19% for equipment, and 17% for labor. The product yield is estimated to be no better than 95% due to the large number of process steps. It is quite obvious from these figures that this method of metallization is considerably more expensive than the screen-printing process, as had been predicted from preliminary estimates.

3. Metal Thickness

A central goal of the analyses performed under this contract is the maximization of the cost effectiveness of every step in module fabrication. The attainment of that goal requires the simultaneous minimization of cost and maximization of power delivered within the constraints that may be imposed by the technologies used. The analytic procedure described here provides a general, quantitative framework for such optimizations. This procedure begins by the careful characterizations of the two contributing factors to the $/W cost (a) the cost per unit area for every "step" and (b) the power loss associated with each step. It turns out that the different characters of these

two factors have a profound impact on the optimization. The notion of a succession of independent "steps" forming a complete module is vital; experience shows that many fabrication process steps are independent to the first order and that those processes which interact strongly can be grouped into a single "step" that can analyzed as a whole. For example, the fine grid metallization pattern can be optimized without reference to the junction characteristics and the bus bar can be analyzed independently of the fine grid pattern under most conditions.

This procedure is derived and applied to the important problems of fine grid and bus bar metallizations where the effect is dramatic. It is extremely important to maximize the performance of the system, and additional costs such as adding considerable Ag to recover a few percent of system performance can be cost effective. Below we will derive the criterion.

These applications provide instructive design specifications and indicate the generality of the basic approach. Among the other "steps" that may be amenable to this type of analysis are the quantity and quality of the Si itself.

a. General Derivation - The quantity to be minimized in all cases is the total cost per watt

$$\frac{\$}{W} = \frac{K}{G_o} \tag{1}$$

where K ≡ total cost per unit of module area and G_o ≡ output power per unit of module area. We first treat the cost factor and show the nontrivial result that it may be expressed as

$$K = \sum_{j=1}^{n} C_j \tag{2}$$

where there are n of the independent "steps" in the entire fabrication process *including* the silicon cost, and the C_j are a set of effective step costs per unit area that are, in general, not simply the individual step costs.

Equation (2) is proved by the following argument. Let D ≡ total cost of fabricating A_p cm^2 of complete modules that have cell coverage fraction ϕ so

that ϕA_p = total cell area. Then we separate the steps into two groups, those involving the full module area and those involving only the cell area

$$D = A_p \left[\frac{k_n}{Y_n} + \frac{k_{n-1}}{Y_n Y_{n-1}} + \cdots + \frac{k_i}{Y_n \cdots Y_i} \right] \text{ for module steps}$$

$$+ \phi A_p \left[\frac{k_{i-1}}{Y_n \cdots Y_{i-1}} + \cdots + \frac{k_1}{Y_n \cdots Y_1} \right] \text{ for cell steps}$$

where $k_i \equiv$ actual cost/unit area of performing step i and $Y_i \equiv$ yield of step i. This shows the well-known impact that each yield factor has on all *preceding* steps. Now we define

$$C_j \equiv \begin{cases} \dfrac{k_j}{Y_n \cdots Y_j} & \text{for all } \textit{module} \text{ steps} \\ \phi \dfrac{k_j}{Y_n \cdots Y_j} & \text{for all } \textit{cell} \text{ steps} \end{cases} \tag{3}$$

Since $K = D/A_p$, these definitions lead to Eq. (2) and show quantitatively what the C_j are. To deal with any individual step m, we simply subtract out its cost contribution per unit module area

$$K' \equiv K - C_m \tag{4}$$

Next we treat the output power density of the module G_o by relating it to G, the power density potentially available.

$$G_o \equiv FG \tag{5}$$

where F is a fraction that may exceed one, depending on the choice that is made for G; that choice is quite arbitrary and might correspond to a 10% module efficiency or any other convenient value. The feature of major importance here is that F is generally the cumulative *product* (not sum) of the individual step factors

$$F = \prod_{j=1}^{n} f_j \tag{6}$$

where each f_j must be self-consistently defined as the fraction of potentially available power that is actually obtained after step j. (These f_j are the same as "performance indexes" in our first report.) To deal with an individual step m we now must separate it by dividing by its performance contribution

$$F' \equiv \frac{F}{f_m} \tag{7}$$

Now using these relations in Eq. (1)

$$\frac{\$}{W} = \frac{K}{G_o} = \frac{K}{FG} = \frac{1}{F'G}\left(\frac{K' + C_m}{f_m}\right) = \frac{K'}{F'G}\left(\frac{1 + C_m/K'}{f_m}\right)$$

$$= \frac{K'}{F'G}\left(\frac{1 + \kappa_m}{f_m}\right) \tag{8}$$

where $\kappa_m \equiv C_m/K'$ is the cost fraction of step m.

Equation (8) shows a result of first importance: *every step-efficiency factor f_m has its fractional impact on the TOTAL cost per watt.* This is a direct consequence of the multiplicative roles of the f_j in contrast to the additive contributions of the cost terms. In physical terms it says that any loss in power must in effect be paid for by making more complete modules. It follows then that no step can be optimized properly by considering only its own cost and performance; rather an equation of the form of Eq. (8) must be minimized.

Next we develop the appropriate optimization conditions for Eq. (8). To aid in this we introduce the fractional power *loss* associated with any step $\lambda_j \equiv 1 - f_j$. Using this in Eq. (8) gives

$$\frac{\$}{W} = \frac{K'}{F'G}\left[\frac{1 + \kappa_m}{1 - \lambda_m}\right] \tag{9}$$

This is the form in which we minimize the \$/W contribution of step m by differentiating with respect to any relevant variable of step m. It is clear that when such a derivative is set equal to zero, the prefactors K'/F'G always

drop out since by definition they cannot contain the variable of step m. Thus only the term in brackets in Eq. (9) need be minimized. It is trivial to show that the condition for minimization is

$$\frac{1}{1 + \kappa_m} \frac{d\kappa_m}{dx} = - \frac{1}{1 - \lambda_m} \frac{d\lambda_m}{dx} \tag{10}$$

where x represents any appropriate variable for step m. In nearly all cases that will be acceptable we will find that $\kappa_m << 1$ (i.e., $C_m << K'$) and $\lambda_m << 1$. Then we obtain the simplified approximate relation

$$\frac{d\kappa_m}{dx} = - \frac{d\lambda_m}{dx} \tag{11}$$

We note also that in this approximation

$$\frac{\$}{W} \simeq \frac{K'}{F'G} [1 + \kappa_m + \lambda_m] \tag{12}$$

and we can set $K' \simeq K$ and $F' \simeq F$.

This is the general procedure. It can be applied to every fabrication step for which there is information enough to evaluate both κ and λ.

b. Application to Front Metallizations - The optimization procedure described above is now applied first to the bus bar and then to the fine grid on the front of solar cells by finding the optimum geometry for each that minimizes the cost/W. We make use of a fortuitous result for these metallization steps: ϕ, the cell coverage fraction of the module, $\simeq 0.83$ and the product of the estimated yields for all steps following metallization is $\simeq 0.87$ so that in Eq. (3) we find that $C_m \simeq k_m$. Furthermore, the metallization process to be evaluated, screen-printed Ag, has a cost that can be expressed as $C_m \simeq h + \beta v_m$ where the contribution h is independent of the amount of metal (it is basically machinery and handling costs) and v_m is the volume of metal used, with β an appropriate coefficient. So differentiating as in Eq. (11) with amount of metal as the variable, causes the term h to drop out and only the metal cost need be evaluated in C_m, hence κ_m.

The metal cost/cm^2 = pv_m/A where p ≡ price/cm^3 of metal in its final condition (i.e., after firing) and A ≡ cell area. But $v_m = ta_m = tSA$ where a_m ≡ area of metal, t ≡ metal thickness, and S ≡ shadow fraction of metal on cell. So

$$C_m = pSt \tag{13}$$

$$\kappa_m = pSt/K' \tag{14}$$

Before proceeding to specific power loss evaluations we note that our calculations have been revised to optimize the $/W for performance averaged over a day rather than just at solar noon. This reduces all resistive losses by a factor of $\pi/4$.

First this optimization procedure is applied to the bus bar; we limit consideration to a single, central bar for simplicity. It has already been shown in Quarterly Report No. 3 [1] that when the fine grid line length ℓ is determined (by cell size, for example), the treatment of the bus bar becomes independent of the fine grid design. For the bus bar the only sources of loss are the shadowing and resistive drop of the metal; it can be shown that there is no way of simultaneously optimizing both the metal thickness and the shadow fraction of the bus bar. This can be seen physically by the recognition that minimum loss for any metal volume would lead to zero shadow fraction (i.e., bar width) and infinite thickness. Therefore, one additional constraint must be imposed on the problem. We choose this constraint as a condition that will give the *thickest* line that seems printable. (The bus bar will have to be printed separately from the fine grid although they can be fired together.) One way of achieving this thick-bar condition is to require that its thickness t_2 always be 1/4 of the line width W. (Since the thickness shrinks roughly in half during firing, this represents a thickness/width ratio of ~1/2 at the printing, a reasonable upper limit on t_2.)

The shadow fraction of the bus bar is $S_2 = W/\ell_{eff} = A/L$ with L ≡ bus bar length. Thus, since $W = 4t_2$

$$S_2 = 4t_2/\ell_{eff} \tag{15}$$

and from Eqs. (13) and (14)

$$C_m = pS_2t_2 = 4pt_2^2/\ell_{eff} \tag{16}$$

$$\kappa_m = 4pt_2^2/K'\ell_{eff} \tag{17}$$

so that

$$\frac{d\kappa_m}{dt} = \frac{8pt_2}{K'\ell_{eff}} \tag{18}$$

The fractional loss is the sum of shadow and line drop

$$\lambda_m = S_2 + \frac{J}{V}\frac{\rho_m}{S_2t_2}\frac{L^2}{3} = \frac{4t_2}{\ell_{eff}} + \frac{J}{V}\frac{\rho_m}{4t_2^2}\frac{L^2}{3}\ell_{eff} \tag{19}$$

where $\rho_m \equiv$ metal resistivity. Then

$$\frac{d\lambda_m}{dt} = \frac{4}{\ell_{eff}} - \frac{1}{t^3}\left(\frac{J}{V}\frac{\rho_m}{6}L^2\ell_{eff}\right) \tag{20}$$

Now invoking the optimization condition (11) we obtain an equation for the optimum bar thickness t_{2opt}

$$\frac{8p}{K'\ell_{eff}}t_{2opt} + \frac{4}{\ell_{eff}} - \frac{1}{t_{2opt}^3}\left(\frac{J}{V}\frac{\rho_m}{6}L^2\ell_{eff}\right) = 0 \tag{21}$$

which must be solved numerically. For a 7.6-cm (3-in.) wafer, L = 7.6, ℓ_{eff} = 6 cm. We take also J/V = 0.05 $(\Omega\text{-cm}^2)^{-1}$, p = \$1.30/cm^3 and $\rho_m = 3.2 \times 10^{-6}$ Ω-cm for screen-printed Ag and K' = \$0.0125/cm^2 ($\sim$\$1/W). This leads to t_{2opt} = 150 μm so that W $\underset{\sim}{}$ 0.60 mm and S_2 = 0.010. The total fractional loss due to the bar is evaluated now by Eq. (19) giving λ_m = 0.03 while Eq. (17) gives κ_m = 0.015.

Next we treat the fine grid pattern using the same basic approach but we find the problem significantly more complicated because there are four power-loss terms aside from the cost term. First we note that C_m and κ_m are given

by the same relations as for the metal of the bus bar, Eqs. (13) and (14). As shown in Quarterly Report No. 3 [1], the fractional power losses are given by

$$\lambda_m = S_1 + \frac{J}{V}\left[\frac{\rho_s}{S_1^2}\frac{w^2}{12} + \frac{\rho_c}{S_1} + \frac{\rho_m \ell^2}{3 S_1 t_1}\right] \tag{22}$$

where w ≡ the fine line width, ρ_s ≡ Si sheet resistivity (Ω/□), ρ_c ≡ metal-Si specific contact resistance (Ω-cm^2). (We have transformed the formulas of Quarterly Report No. 3 to express all the losses in terms of S rather than the line spacing d.) We fix w = 125 μm as the minimum printable width.

Now the minimization of \$/W requires that we optimize both t_1 and S_1 simultaneously. (In contrast to the bus bar case, this is possible here.) To do this we use the form of \$/W given by Eq. (12) and minimize $(\kappa_m + \lambda_m)$ with respect to both variables t_1 and S_1. Partial differentiation of $(\kappa_m + \lambda_m)$ with respect to t_1 gives, when set equal to zero, the first condition

$$t_{1opt} = \frac{\ell}{S_1}\sqrt{\frac{K' J \rho_m}{3\ pV}} \tag{23}$$

This has the important consequence, when substituted into $(\kappa_m + \lambda_m)$, that

$$\kappa_m(\text{cost fraction}) = \text{line loss fraction} = \ell\sqrt{\frac{pJ\rho_m}{3\ KV}}$$

They are thus *independent* of S_1 an t_1 so now differentiation of $(\kappa_m + \lambda_m)$ with respect to S_1 gives the surprisingly simple equation for S_{1opt}

$$S_{1opt}^3 - \left(\frac{J}{V}\rho_c\right) S_{1opt} - \left(\frac{J}{V}\frac{\rho_s w^2}{6}\right) = 0 \tag{24}$$

This is a remarkable result in that the optimum shadow fraction is independent of the metal resistivity, length, price, and the module cost. In fact, when ρ_c is small ($\lesssim 10^{-3}$ Ω-cm^2)

$$S_{1opt} = \left(\frac{J\rho_s w^2}{6V}\right)^{1/3} \tag{25}$$

so S_1 varies as the cube root of ρ_s.

The metal thickness, given by Eq. (23) once S_1 is found, is the only place where the costs and other parameters of the metal are found. Other useful consequences of these results are that varying the cell size has no effect on S_{lopt} and a simple linear effect on t_{lopt} through ℓ.

Taking again the example of the 7.6-cm wafer, with ℓ = 3 cm, J/V = 0.05 $(\Omega\text{-cm}^2)^{-1}$ and ρ_s = 50 $\Omega/\square$ for the Si, $\rho_c = 10^{-3}$ $\Omega\text{-cm}^2$ and using w = 125 μm, we find S_1 = 0.040. Then using the other parameter values given after Eq. (21), κ_m = 0.007 and t_{lopt} = 16 μm. With these optimized values of t_1 and S_1 we can readily calculate λ_m = 0.068. (This entire optimization and evaluation is performed numerically with a straightforward computer program.)

Combining now the optimized contributions of the fine grid and the bus bar

$$\lambda_{Tot} = \lambda_1 + \lambda_2 = 0.068 + 0.030 = 0.098$$
$$\kappa_{Tot} = \kappa_1 + \kappa_2 = 0.007 + 0.015 = 0.022 \qquad (26)$$

so the performance penalties far outweight the cost contributions. These terms are to be used in Eq. (12) to evaluate the cost/W contributions of the two metallizations under optimum conditions.

An illustration of the use of these results appears in Fig. 28 for 7.6-cm wafers with total module cost per W as the independent variable. The lowest curve shows the cost of the optimum amount of Ag to be used as the module or system cost changes. It can be seen that for more expensive systems, it is worthwhile to increase greatly the amount of Ag to obtain a gain in performance.

Another use of these calculations is in connection with the question of how large should the individual cells be; this will become an important question as large-area sheets become available. Apart from any other considerations, it is clear qualitatively that as cell size increases, resistance losses will increase and the amount of Ag needed *per cm*^{2} will increase. It is necessary therefore to determine quantitatively what impact those increases will have on the \$/W because they will have to be offset by potential benefits in handling fewer cells (e.g., fewer interconnections in the module). We have calculated the variation in optimum \$/W as a function of cell size, using as reference a \$1/W module with 7.6-cm (3-in.) cells. The results shown in Fig. 29 indicate,

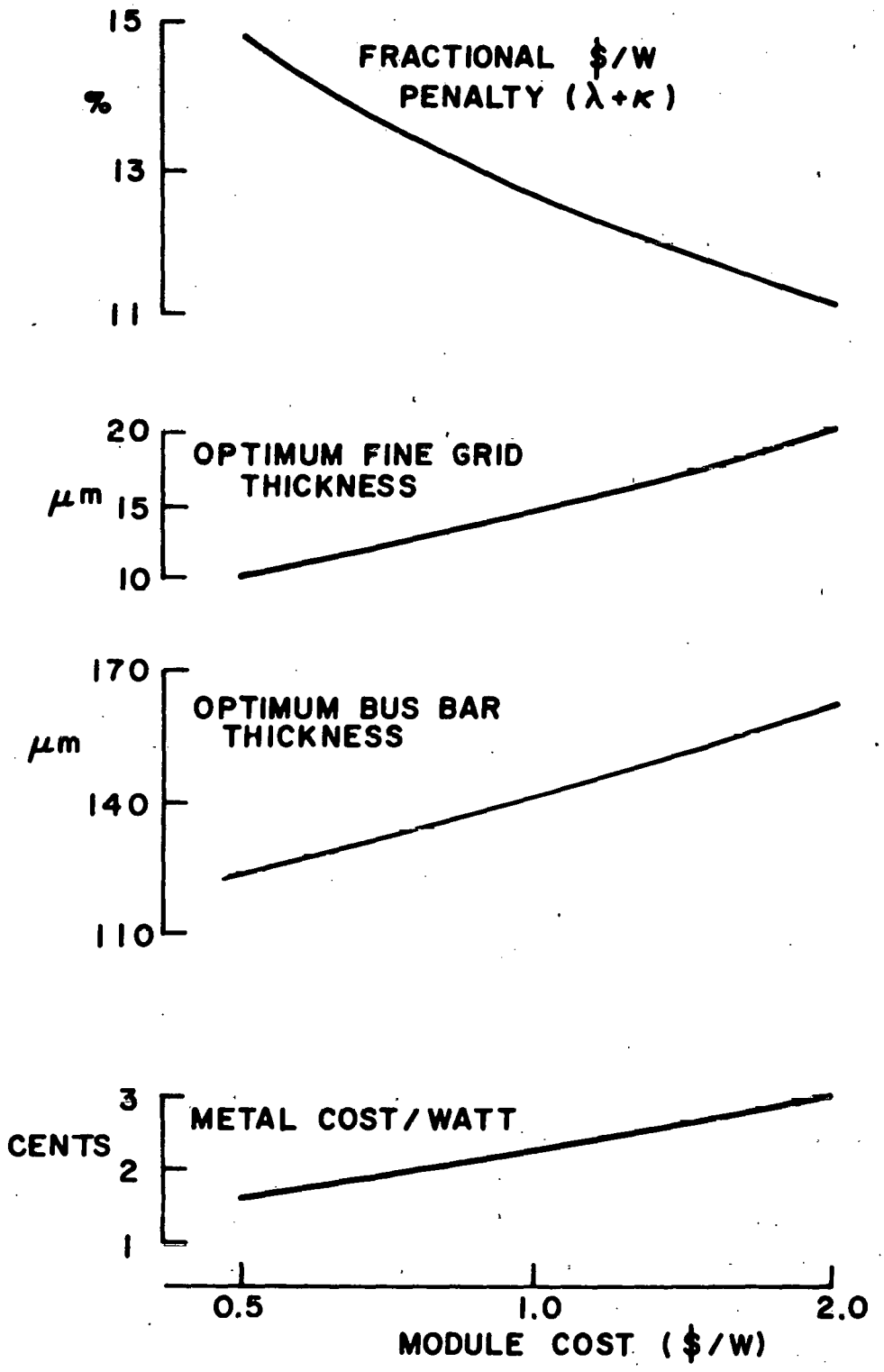

Figure 28. Effect of total module cost in $/W (plotted logarithmically) on several front metallization parameters of 7.6-cm-diam cells with screen-printed Ag lines having straight, parallel sides. The curve ($\lambda + \kappa$) is obtained from totals like those in Eq. (26).

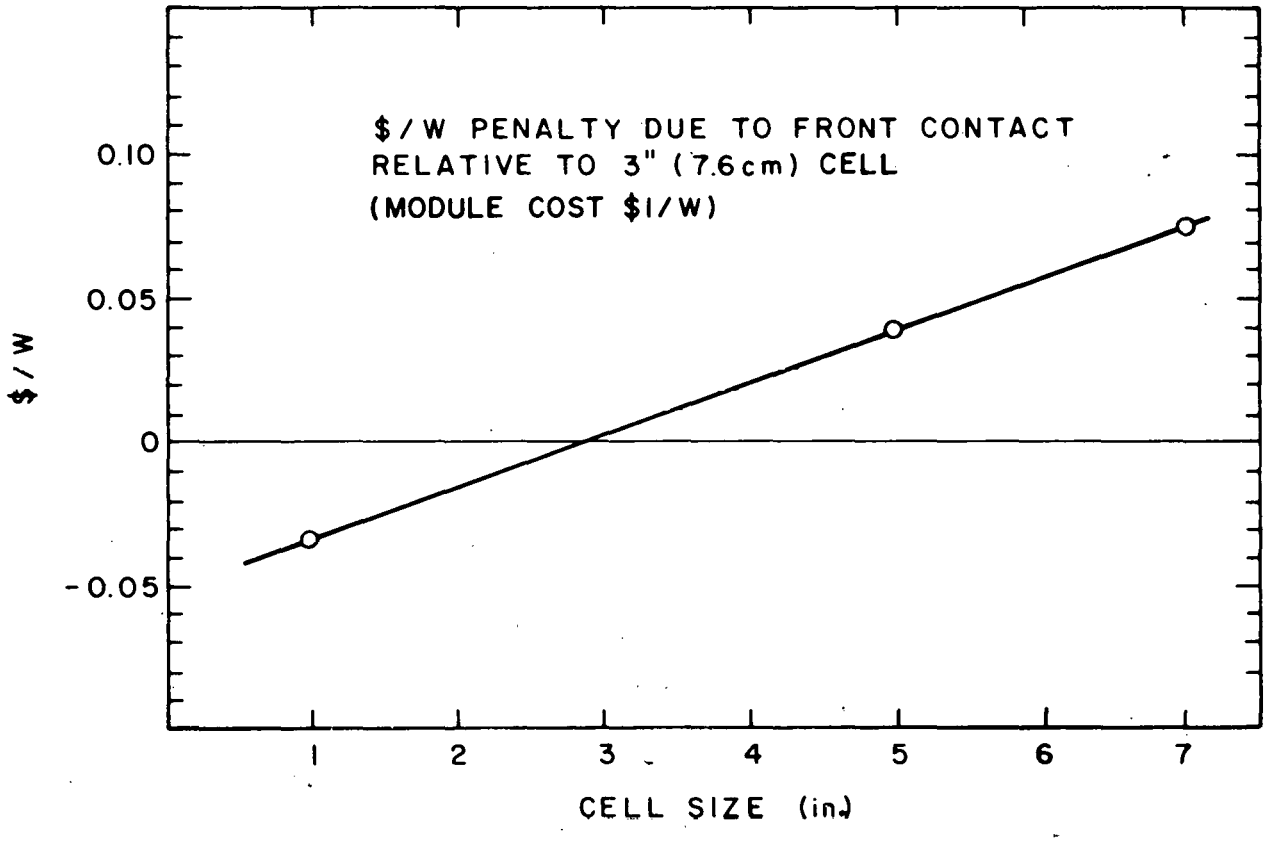

Figure 29. Calculated penalty in $/W due to optimized cost and performance contributions of combined fine grid and bus bar on cell front as a function of cell size. The penalty is shown as a change from a reference module cost of $1/W for all cell sizes with the zero arbitrarily set at the 3-in. (7.6-cm) wafer.

for example, that an increase from 3- to 5-in. (12.7-cm) wafers requires that 4% of the $/W must be gained elsewhere in the fabrication just to compensate for the penalty arising from the front metals alone; the back contact metals will undoubtedly add a few percent more penalty, but there is not sufficient information available now for the quantitative evaluation. In our cost summary we have used the same amount of metal on the back as on the front. See Section V for a discussion of cell size implications.

H. JUNCTION FORMATION

Ion implantation is now a well-established process in the semiconductor industry. Its application to the fabrication of solar cells has been successfully demonstrated with reported AM1 efficiencies in the 10 to 13% range with higher efficiency expected in the near future. The major advantages of ion implantation applied to high-volume production of solar cells are control, reproducibility, and the elimination or reduction of wet chemicals and gases required by other junction-formation processes.

In this section, a broad outline is given of a proposed ion-implantation process capable of the high throughput required for large-scale, low-cost solar cell production.

First, it is assumed that advances in the development of ion implanters will result in implant machines capable of producing 10-mA beams of both n and p-type dopants in a sequential operation. This is not an unreasonable assumption since production machines are now available which can deliver more than 2 mA of phosphorus. A 10-mA machine could process approximately 100 cm^2 of silicon area in 1 s, which approximately equals the area of both sides of a 3-in.-diam wafer, so that 3600 wafers could theoretically be implanted in 1 h. This calculation assumes dose requirements of $\sim 1 \times 10^{15} cm^{-2}$ of phosphorus on the top side and $5 \times 10^{14} cm^{-2}$ boron on the back.

Since material consumption is low using an ion-implantation process, major cost reductions can be achieved by maximum use of automation. The system described here processes 2000 3-in. wafers/h, a reduction from the 3600/h, allowing time for beam scanning and beam loss at edges. A schematic block diagram of one possible embodiment of such a system is shown in Fig. 30.

In this system wafers are manually moved to the implant station in two 500-wafer cartridges, and one is automatically transferred to 50-wafer cassettes. The two input chambers are air-locked and operate in "push-pull" fashion so that no time is lost during transfer loading from cassettes to the platens. The platens are designed to hold several wafers during implant and to provide for a masked implant (planar junction) on the active side of the cell and a full-area implant on the reverse side. It is assumed that the input chamber pump-down time is 1 min. The platens then move, belt driven, from either chamber to the beam slit and are implanted from opposite sides.

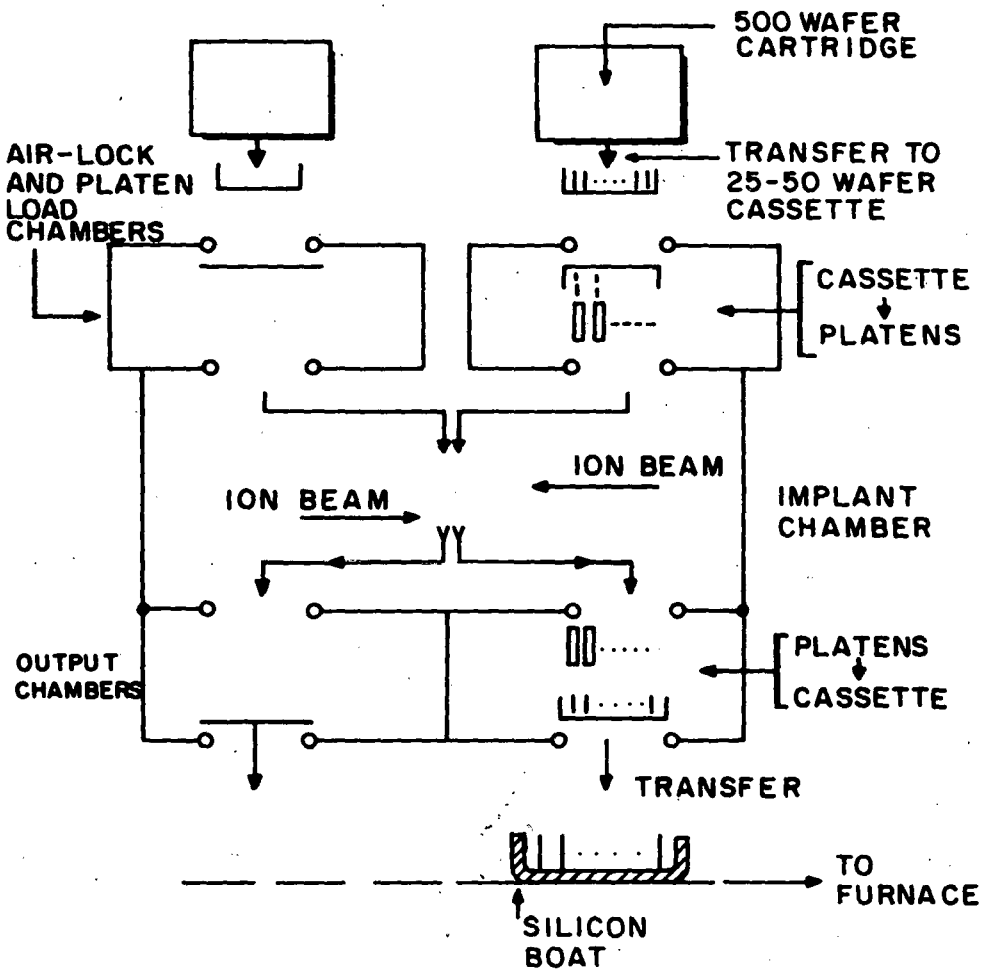

Figure 30. Schematic block diagram - ion implantation and junction formation. (Transfer to silicon boat must include flipping wafers so that like sides face.)

PROCESS PARAMETERS:ION IMPLANTATION:2 SIDES 04/18/77 09:51:24 PAGE 29

ESTIMATE DATE:01/12/77 BY:RCA ESTIMATES CLASS:ION IMPLANTATION
CATEGORY:PROCESS DEFINITION TECHNOLOGY LEVEL:FUTURE MATERIAL FORM:3" WAFER.
INPUT UNIT:SHEETS OUTPUT UNIT:SHEETS TRANSPORT IN:500 SHEET CASSETTE TRANSPORT OUT:SILICON BOAT
PROCESS YIELD: 99.0% YIELD GROWTH PROFILE: 0
INPUT UNIT SALVAGE FACTOR: 0.0 FACTOR GP#: 0 SALVAGE OPTION:FRACTION OF INPUT UNIT VALUE
PERFORMANCE FACTORS-I(R)/I(SC): 1.000000E+00 V(R)/V(OC): 1.000000E+00 F(R)/F: 1.000000E+00

INPUT UNITS:	0.	0.	0.
FLOOR SPACE,FT**2:	0.	0.	0.

DESCRIPTION:ION IMPLANTATION-BOTH SIDES

ASSUMPTIONS:

1. PROCESS FOLLOWED BY DIFFUSION STEP
2. DOUBLE IMPLANTER. ONE IMPLANTER FOR EACH SIDE OF WAFER.
3. FRONT SIDE OF ONE WAFER IMPLANTED SIMULTANEOUSLY WITH BACK SIDE OF A SECOND WAFER.
3. 10 GAL/MIN OF COOLING WATER AT 20 DEG. C. NEEDED PER IMPLANTER.

PROCEDURE

1. CARTRIDGE FEED SYSTEM FEEDING IMPLANTER.
2. FIRST IMPLANTER FEEDS SECOND IMPLANTER FOR BACK SIDE IMPLANTATION
3. SECOND IMPLANTER UNLOADS DIRECTLY INTO SILICON DIFFUSION BOAT.
ALTERNATE WAFERS ARE FLIPPED DURING LOAD SO THAT LIKE SIDES FACE.

INVESTMENTS

INVESTMENT NAME	MAX. THRUPUT UNITS	% INPUT UNITS PROCESSED	FIRST COST	AVAIL.	AREA,FT**2
ION IMPLANTER(C)	2000.00 SH/HR	100.0%	$ 700000.	85.0%	850.

LABOR

(DL=DIRECT LABOR PERSONS;TL=TOTAL LABOR PERSONS)

NAME	LABOR REQUIREMENTS BASE	# PERSONS/SHIFT/BASE UNIT	THRUPUT/HR/PERSON	% INPUT UNITS PROCESSED
HOURLY OPERATOR	ION IMPLANTER(C)	4.000E-01		
MAINTENANCE	ION IMPLANTER(C)	1.000E-01		
FOREMAN	DL	1.000E-01		

SUPPLIES/EXPENSES

EXPENSE NAME	ANNUAL FIXED PART	VARIABLE PART	UNITS	BASE
ELECTRICITY	0.0	4.000E+01	KWH	PER AVAILABLE INVESTMENT-HOUR OF ION IMPLANTER(C)
LIQUID NITROGEN	0.0	1.000E+04	CM**3	PER AVAILABLE INVESTMENT-HOUR OF ION IMPLANTER(C)
FILAMENTS/INSULATORS	8.000E+03	0.0	$	PER AVAILABLE INVESTMENT-HOUR OF ION IMPLANTER(C)
WATER-COOLING	0.0	2.400E+06	CM**3	PER AVAILABLE INVESTMENT-HOUR OF ION IMPLANTER(C)
ION SOURCE GAS	0.0	2.280E+00	$	PER AVAILABLE INVESTMENT-HOUR OF ION IMPLANTER(C)

FOR INVESTMENT OR LABOR BASES, "FIXED PART" IS MULTIPLIED BY NO. OF BASE UNITS PRESENT.

Figure 31. Process parameters - ion implantation.

PROCESS PARAMETERS:DIFFUSION 04/18/77 09:51:24 PAGE 19

ESTIMATE DATE:01/12/77 BY:FRED MAYER, X6334, SOMERVILLE, ZONE 6 CLASS:DIFFUSION
CATEGORY:PROCESS DEFINITION TECHNOLOGY LEVEL:FUTURE MATERIAL FORM:3" WAFER.
INPUT UNIT:SHEETS OUTPUT UNIT:SHEETS TRANSPORT IN:SILICON BOAT TRANSPORT OUT:500 SHEET CASSETTE
PROCESS YIELD: 99.0% YIELD GROWTH PROFILE: 0
INPUT UNIT SALVAGE FACTOR: 0.0 FACTOR GP#: 0 SALVAGE OPTION:FRACTION OF INPUT UNIT VALUE
PERFORMANCE FACTORS-I(R)/I(SC): 1.000000E+00 V(R)/V(OC): 1.000000E+00 F(R)/F: 1.000000E+00

INPUT UNITS:	0.	0.	0.
FLOOR SPACE,FT**2:	0.	0.	0.

DESCRIPTION:DOPANTS ARE DRIVEN INTO SILICON BY HEAT TREATMENT IN FURNACE

ASSUMPTIONS:

1. 3" DIAMETER WAFER, 12-14 MILS THICK,(100) ORIENTATION,P-TYPE, 1-5 OHM-CM.
2. DIFFUSION VIA ION IMPLANTATION OR DOPED OXIDE.
3. COIN STACK APPROACH (NOT CONSIDERED) NEEDED FOR MORE VOLATILE SOURCES.
4. 40 MINUTE DIFFUSION TIME AT 1000 C. AND 90 MINUTE PREPROGRAMMED COOLING TO 750 C. + 10 MIN. HOLD AT 600C. + AIR QUENCH.
5. 250 SILICON BOATS, EACH 12" LONG AND 4" WIDE AT $550 EACH NEEDED. 100 WAFERS/BOAT. 3 YR. LIFE.
6. FURNACE HAS 12" BELT, 15' HEAT ZONE, 55' COOLING SECTION, 20' LOAD/UNLOAD SECTION. 30 FT./HR BELT RATE.
7. ALTERNATE WAFERS MUST BE FLIPPED SO THAT LIKE SIDES FACE.
8. P-SIDE AND N-SIDE OF WAFER MUST BE EASILY DIFFERENTIABLE.
9. 100 WAFERS IN EACH INCOMING SILICON BOAT.

PROCEDURE

1. INCOMING WAFERS WITH DIFFUSION SOURCE APPLIED TO BOTH SURFACES. WAFERS HAVE BEEN LOADED INTO A SILICON BOAT BY PRECEDING STEP.
2. BOATS PLACED ONTO MOVING BELT FURNACE.
3. DIFFUSION FOR 40 MIN. AT 1000 C.
4. FORCE AIR COOL OF WAFERS TO ROOM TEMPERATURE.
5. LOADER-FLIPPER TRANSFER OF WAFERS INTO 500 WAFER CASSETTE.

INVESTMENTS

INVESTMENT NAME	MAX. THRUPUT	UNITS	% INPUT UNITS PROCESSED	FIRST COST	AVAIL.	AREA,FT**2
LINDBERG FURNACE-12" BELT	9000.00	SH/HR	100.0%	$ 72000.	95.0%	800.
250 12"-SILICON BOATS	9000.00	SH/HR	100.0%	$ 137500.	95.0%	0.
CASSETTE LOADER-FLIPPER	3000.00	SH/HR	100.0%	$ 20000.	95.0%	0.

LABOR

(DL=DIRECT LABOR PERSONS;TL=TOTAL LABOR PERSONS)

NAME	LABOR REQUIREMENTS BASE	# PERSONS/SHIFT/BASE UNIT	THRUPUT/HR/PERSON	% INPUT UNITS PROCESSED
HOURLY OPERATOR	LINDBERG FURNACE-12" BELT	1.000E+00		
MAINTENANCE	LINDBERG FURNACE-12" BELT	1.000E-01		
MAINTENANCE	CASSETTE LOADER-FLIPPER	1.000E-01		
FOREMAN	DL	5.000E-02		

SUPPLIES/EXPENSES

EXPENSE NAME	ANNUAL FIXED PART	VARIABLE PART	UNITS	BASE
ELECTRICITY	0.0	1.000E+02	KWH.	PER AVAILABLE INVESTMENT-HOUR OF LINDBERG FURNACE-12" BELT
WATER-COOLING	0.0	8.000E+05	CM**3	PER AVAILABLE INVESTMENT-HOUR OF LINDBERG FURNACE-12" BELT
NITROGEN	0.0	4.500E+07	CM**3	PER AVAILABLE INVESTMENT-HOUR OF LINDBERG FURNACE-12" BELT

Figure 32. Process parameters - diffusion.

PROCESS PARAMETERS:POST DIFFUSION INSPECTION:10% 04/18/77 09:51:24 PAGE 32

ESTIMATE DATE:12/22/76 BY:DAVE RICHMAN, X3207, RCA LABS, E-3214 CLASS:TEST
CATEGORY:PROCESS DEFINITION TECHNOLOGY LEVEL:FUTURE MATERIAL FORM:3" WAFER.
INPUT UNIT:SHEETS OUTPUT UNIT:SHEETS TRANSPORT IN:500 SHEET CASSETTE TRANSPORT OUT:500 SHEET CASSETTE
PROCESS YIELD: 99.0% YIELD GROWTH PROFILE: 0
INPUT UNIT SALVAGE FACTOR: 0.0 FACTOR GP#: 0 SALVAGE OPTION:VALUE IN$
PERFORMANCE FACTORS-I(R)/I(OC): 1.000000E+00 V(R)/V(OC): 1.000000E+00 F(R)/F: 1.000000E+00

INPUT UNITS:	0.	0.	0.
FLOOR SPACE,FT**2:	0.	0.	0.

DESCRIPTION:POST DIFFUSION 4-POINT PROBE RESISTIVITY MEASUREMENT:10% SAMPLE.

ASSUMPTIONS:

1. 3" DIAMETER WAFER, 12-14 MILS THICK,(100) ORIENTATION,P-TYPE, 1-5 OHM-CM.
2. 100% WAFER SHEET RESISTIVITY TEST.

PROCEDURE

1. OPERATOR LOADS CASSETTE INTO MACHINE.
2. WAFERS AUTOMATICALLY FED TO TEST EQUIPMENT.
3. WAFERS SORTED INTO MAGAZINES.

INVESTMENTS

INVESTMENT NAME	MAX. THRUPUT UNITS	% INPUT UNITS PROCESSED	FIRST COST	AVAIL.	AREA,FT**2
SILTEC WAFER SORTER-PROBE	1450.00 SH/HR	10.0%	$ 150000.	80.0%	200.

LABOR

(DL=DIRECT LABOR PERSONS,TL=TOTAL LABOR PERSONS)

NAME	LABOR REQUIREMENTS BASE	# PERSONS/SHIFT/BASE UNIT	THRUPUT/HR/PERSON	% INPUT UNITS PROCESSED
HOURLY OPERATOR	SILTEC WAFER SORTER-PROBE	2.500E-01		
MAINTENANCE	SILTEC WAFER SORTER-PROBE	2.000E-01		
FOREMAN	DL	1.000E-01		

SUPPLIES/EXPENSES

EXPENSE NAME	ANNUAL FIXED PART	VARIABLE PART	UNITS	BASE
ELECTRICITY	0.0	5.000E+00	KWH.	PER AVAILABLE INVESTMENT-HOUR OF SILTEC WAFER SORTER-PROBE

Figure 33. Process parameters - inspection.

PROCESS PARAMETERS:SYSTEM "Z" WAFER CLEANING 04/18/77 09:51:24 PAGE 2

ESTIMATE DATE:01/12/77 BY:FRED MAYER, X6334, SOMERVILLE, ZONE 8 CLASS:CLEANING
CATEGORY:PROCESS DEFINITION TECHNOLOGY LEVEL:NEAR FUTURE MATERIAL FORM:3" WAFER.
INPUT UNIT:SHEETS OUTPUT UNIT:SHEETS TRANSPORT IN:500 SHEET CASSETTE TRANSPORT OUT:500 SHEET CASSETTE
PROCESS YIELD: 99.0% YIELD GROWTH PROFILE: 0
INPUT UNIT SALVAGE FACTOR: 0.0 FACTOR GP#: 0 SALVAGE OPTION:FRACTION OF INPUT UNIT VALUE
PERFORMANCE FACTORS-I(R)/I(SC): 1.000000E+00 V(R)/V(OC): 1.000000E+00 F(R)/F: 1.000000E+00

INPUT UNITS:	0.	0.	0.
FLOOR SPACE,FT**2:	0.	0.	0.

DESCRIPTION:WAFERS ARE CLEANED IN SULFURIC/HYDROGEN PEROXIDE MIXTURE

ASSUMPTIONS:

1. 3" DIAMETER WAFER, 12-14 MILS THICK,(100) ORIENTATION,P-TYPE, 1-5 OHM-CM.
2. NOTE: DOES NOT REMOVE PARTICLES (DUST,SILICON CHIPS,ETC.)
3. 500 WAFERS/TEFLON CASSETTE
4. 1 TEFLON BOAT PER TANK; 2 TANKS PER HOOD.
5. 7.5 CYCLES/HR X 2 BOATS/CYCLE X 500 WAFERS/BOAT=7500 WAFERS/HR.
   (8 MIN. DRYING CYCLE IS LIMITING FACTOR.)
6. 1 OPERATOR REQUIRED FOR 2 HOODS.
7. NOTE: SYSTEM COST ESTIMATED TO BE $30,000. $15,000 FOR BACKUP.
   TOTAL SYSTEM COST=$45,000 WITH BACKUP.

PROCEDURE

1. TEFLON CASSETTE MANUALLY INSERTED IN TANK (1 MIN.)
2. 7 MINUTES IN HOT CAROS ACID.
3. AUTOMATIC TRANSFER TO 1ST CASCADE RINSE, 8 MINUTE RINSE.
4. AUTOMATIC TRANSFER TO 2ND & 3RD RINSES, EACH ABOUT 3 MINUTES.
5. AUTOMATIC TRANSFER TO HOT AIR TUNNEL. DRY FOR 8 MINUTES.

INVESTMENTS

INVESTMENT NAME	MAX. THRUPUT UNITS	% INPUT UNITS PROCESSED	FIRST COST	AVAIL.	AREA,FT**2
SYSTEM "Z" STATION(B)	7500.00 SH/HR	100.0%	$ 45000.	85.0%	200.

LABOR

(DL=DIRECT LABOR PERSONS;TL=TOTAL LABOR PERSONS)

NAME	LABOR REQUIREMENTS BASE	# PERSONS/SHIFT/BASE UNIT	THRUPUT/HR/PERSON	% INPUT UNITS PROCESSED
HOURLY OPERATOR	SYSTEM "Z" STATION(B)	5.000E-01		
MAINTENANCE	SYSTEM "Z" STATION(B)	5.000E-02		
FOREMAN	DL	5.000E-02		

SUPPLIES/EXPENSES

EXPENSE NAME	ANNUAL FIXED PART	VARIABLE PART	UNITS	BASE
ELECTRICITY	0.0	3.500E+01	KWH.	PER AVAILABLE INVESTMENT-HOUR OF SYSTEM "Z" STATION(B)
SULFURIC ACID	0.0	2.310E-01	GM.	PER INPUT UNIT. % UNITS= 100.0%
HYDROGEN PEROXIDE	0.0	2.100E-01	CM**3	PER INPUT UNIT. % UNITS= 100.0%
DE-IONIZED WATER	0.0	1.000E+06	CM**3	PER AVAILABLE INVESTMENT-HOUR OF SYSTEM "Z" STATION(B)

Figure 34. Process parameters - Z wafer cleaning.

Wafer feed can proceed in either direction, so that when the first 50 wafers are done, the second air-lock chamber begins to discharge wafers. Implanted wafers then move, again belt driven, to the output chambers, where the wafers are transferred to cassettes and then to silicon boats.

After implantation, junction annealing and drive-in are required. The silicon boats ride on a continuous belt through a multizone diffusion furnace. The time and temperature requirements for annealing and drive-in will vary with the type of dopant used in the junction formation. A typical sequence for an n/p/p+ solar cell with phosphorus and boron dopants is 15 min at 1000°C with temperature gradients before and after the 1000°C hot-zone to allow for slow warm-up, cooling, and annealing of the junction.

The process parameters for the ion-implantation step, diffusion step, and inspection step are shown in Figs. 31, 32, and 33.

I. PROCESS: Z WAFER CLEANING

This process is designed to assure a clean surface on the silicon sheet before it is started through the automated array process. It consists of a hot Caro's acid immersion followed by three cascade rinses in deionized water and spin drying.

Caro's acid is especially effective for eliminating any organic or metallic contamination but does not remove particles such as silicon chips. This step may not be necessary depending on the condition of the incoming wafers. It is included to show what the costs of such a cleaning or etching procedure can be if the system is automated. Process parameters are shown in Fig. 34.

SECTION V

EFFECT OF SHEET SIZE ON MANUFACTURING COST

All of the analyses have considered 3-in. wafers since the most realistic projections could be made with equipment which exists to handle this material. In this section we will estimate the effect of increasing the wafer size to 5 in.

In the most optimistic (and unrealistic) case, we will assume that there will be no increase in labor or capital cost per unit handled so that each of the processes produces 25/9 W where it produced 1 W before. The material and expense items in terms of $/W in general will remain the same. However, the metallization cost will increase due to the increased current-handling requirements. We have calculated the optimum metallization pattern based on an overall system of $1/W. The cost of the metal increases by $0.046/W. Figure 35 is a summary of this comparison. It is important to emphasize that the performance of these larger cells is poorer, even in the optimized case, than the 3-in. cells, and, therefore, there is a penalty to pay at the system level. The performance is 2.3% poorer. Since the system is assumed to cost $1/W, we will add this penalty, $0.023/W, to the cost of the array module. In this "best case" analysis, the costs for array modules based on 3-in. and 5-in. wafers are almost identical.

A somewhat more detailed estimate is given in Fig. 36. In this case, we assume that the cassettes handling the larger wafers have larger spacing between cells and the wafers must be handled more slowly. It is clear that in processes such as ion implantation, the rate of which is beam limited, there is no change in the capital expenses. In each case we have estimated the reduction in labor capital, materials, and expense. Again we must add $0.023/W for the reduction in panel performance. There is an increase of about 10% in the manufacturing cost of array modules based on 5-in. wafers compared with modules based on 3-in. wafers.

This result is due to the interconnect technology. In these panels, the cells are interconnected with one contact at the rim of the cell. In the event that numerous contact points are made within the cell area, the optimum metallization design will change and this result can be reversed. We have

not analyzed the effect on panel design, panel life, and panel performance of these contacts to crossing the face of the cell. However, because of the enormous cost of the metallization step in the present configuration, such an analysis is surely appropriate.

	3-in. Cell ($/W)	5-in. Cell ($/W)
Materials & Expense	0.152	0.198
Labor Overhead Interest Depreciation	0.112	0.040
System Performance Degradation Cost		0.023
Final Comparison	0.264	0.261

Figure 35. "Best case" array module manufacturing cost summary, 3- and 5-in. cells.

	3-in. Cell ($/W)	5-in. Cell ($/W)	Notes
Cleaning	0.003	0.002	Down linearly with radius
Ion Implantation	0.029	0.026	Labor down linearly, rest same
Diffusion	0.009	0.005	All linear decreases
Metallization	0.094	0.132	Labor down linearly, metal up by 4.6¢/W, machines same
AR Coating	0.011	0.007	Material same, rest linear decrease
Test	0.012	0.004	Squared reduction in all costs
Interconnect	0.016	0.010	Linear reduction in all costs
Panel Assembly & Packaging	0.089	0.089	Unchanged
	0.264	0.275	
Penalty due to System Performance Degradation		0.023	
TOTAL	0.264	0.298	

Figure 36. Detailed array module manufacturing cost estimate, 3- and 5-in. cells.

SECTION VI

FACTORY LEVEL OVERHEAD COSTS

In none of the manufacturing cost analyses presented above are factory overhead, distribution, advertising, or profit considered. For the process sequence, Ion Implantation (C) factory level overhead costs will now be estimated.

We have evaluated the factory level costs for two factories, one producing 50 MW/year and the other, 500 MW/year. A summary of these evaluations, which appear as Fig. 37, is given below.

	$/W	
	50 MW	500 MW
Support Personnel	0.035	0.010
Cassette Depreciation	0.002	0.002
Heating, Lighting, and Air-Conditioning	0.004	0.003
Insurance (building & all capital)	0.002	0.002
Local Taxes	0.005	0.004
Factory Depreciation	0.008	0.006
Factory Interest	0.014	0.012
Support Equipment Depreciation	0.002	0.000
Support Equipment Interest	0.001	0.000
	0.072	0.039

The manufacturing cost as a function of factory size is shown in Fig. 38.

	50 MW	500 MW
These costs are	0.264	0.253
Total	0.336	0.292

It will be noticed that this entire factory and the capital equipment are financed by debt. In order to remove considerations of debt ratio (% of assets financed by debt) from an estimate of profit, we will assume the following relationship:

$$\frac{\text{Net profit after taxes + after tax interest}}{\text{Assets less accumulated depreciation}} = 15\%$$

For this manufacturing facility, the before-tax profit in the first year of operations is then $0.05/W.

Assumptions:
(1) 3-in. wafers
(2) 15% cell efficiency, 0.717 W/wafer.
(3) Overall process yield: 82.2%
(4) Cafeteria run by outside firm using company facilities, but food company personnel. No cost to factory other than cost of facilities (depreciation, allocated interest, and taxes).
(5) 345 working days per year.
(6) Two 12-h shifts per day. 10% shift premium for night shift.

Work Schedule

Four groups of personnel; two for night shift and two for day shift. Schedule is 4 working days, 3 days off, 3 working days, 4 days off.
Other schedules could also be inplemented. Salaried people work a 5-day, 40-h week.

	50 MW-YR			500 MW/YR			
INVESTMENT	#	$	$/W	#	$/W	$	NOTES
PLANT:							
Process	54K ft^2	5400K	0.108	464K ft^2	46400K	0.093	@ $100/$ft^2$
Offices	10K ft^2	600K	0.012	15K ft^2	900K	0.002	
Cafeteria	5K ft^2	300K	0.006	25K ft^2	1500K	0.003	
Array Storage	0.5K ft^2	30K	0.001	4K ft^2	240K	0.000	@ $60/$ft^2$
Wafer Storage	10K ft^2	600K	0.012	100K ft^2	6000K	0.012	
Chemical Storage	10K ft^2	600K	0.012	100K ft^2	6000K	0.012	
Maint. Shops	5K ft^2	30K	0.001	50K ft^2	3000K	0.126	
TOTAL	95K ft^2	7560K	0.151	758K ft^2	64,040K	0.128	
LAND	160K ft^2	40K	0.001	1200K ft^2	300K	0.001	
Parking & Receiving	60K ft^2	60K	0.001	400K ft^2	400K	0.001	
Office Equipment		20K	0.000		50K	0.000	
Purchased Material Inspection & Q/C Equipment		500K	0.010		1000K	0.002	
Minicomputers for Payroll & MIS	2	250K	0.005	3	375K	0.001	
Cassettes	3500	350K	0.007	35000	3500K	0.007	1 week production
GRAND TOTAL	-	72,877K	0.458	-	133,705K	0.388	
PERSONNEL							
PLANT ADMINISTRATION							
Factory Mgr	1	50K	0.001	1	80K	0.000	
Ass't. Mgr	1	40K	0.001	3	180K	0.000	
Secretaries	1	10K	0.000	3	30K	0.000	
Receptionist	1	10K	0.000	1	10K	0.000	
Industrial Relations	1	18K	0.000	5	75K	0.000	
Secretaries	1	10K	0.000	3	30K	0.000	
Financial Services	2	60K	0.001	3	80K	0.000	
Secretaries	1	10K	0.000	2	20K	0.000	
Accounting Services	2	45K	0.001	3	65K	0.000	
Secretaries/Clerks	4	40K	0.001	8	80K	0.000	
Computer Service	2	40K	0.001	3	60K	0.000	
Computer Operators	1/shift	48K	0.001	2/shift	96K	0.000	
Purchasing	2	45K	0.001	3	65K	0.000	
Secretaries	1	10K	0.000	3	30K	0.000	
FACILITIES							
Guards	3/shift	144K	0.003	15/shift	720K	0.001	
Maintenance	3/shift	200K	0.004	15/shift	1000K	0.002	
Janitors	3/shift	100K	0.002	10/shift	80K	0.000	
Warehouse	1	25K	0.001	1	K	0.000	
Material Handlers	3/shift	144K	0.003	15/shift	720K	0.001	
Dispensary	1/shift	60K	0.001	2/shift	120K	0.000	
Industrial Engineering	10	250K	0.005	20	500K	0.001	
Quality Control & Purchased Material Inspection	5/shift	360K	0.007	15/shift	1080K	0.002	
Support People	107	1719K	0.034	314	5146K	0.010	
Direct Labor Process	106	1531K	0.031	912	13183K	0.027	
Indirect Labor Process	46	726K	0.014	408	6529K	0.013	
TOTAL PEOPLE	259	3976K	0.080	1634	24,858K	0.050	
EXPENSES							
Cassettes, Depr.		87.5K	0.002		875K	0.002	4-yr life
Heating & A/C		113K	0.002		1065K	0.002	
Lighting		75K	0.002		600K	0.001	$3W/ft^2$
Insurance		115K	0.002		1018K	0.002	0.5% of asset value
Local Taxes		230K	0.005		1942K	0.004	3% of plant and land
Factory Depr.		381K	0.008		3222K	0.006	20-yr life
Factory Interest		686K	0.014		5800K	0.012	9%
Support Equipment Depreciation		110K	0.002		204K	0.000	7-yr life
Support Equipment Interest		69K	0.001		128K	0.000	9%

Figure 37. Factory cost evaluations.

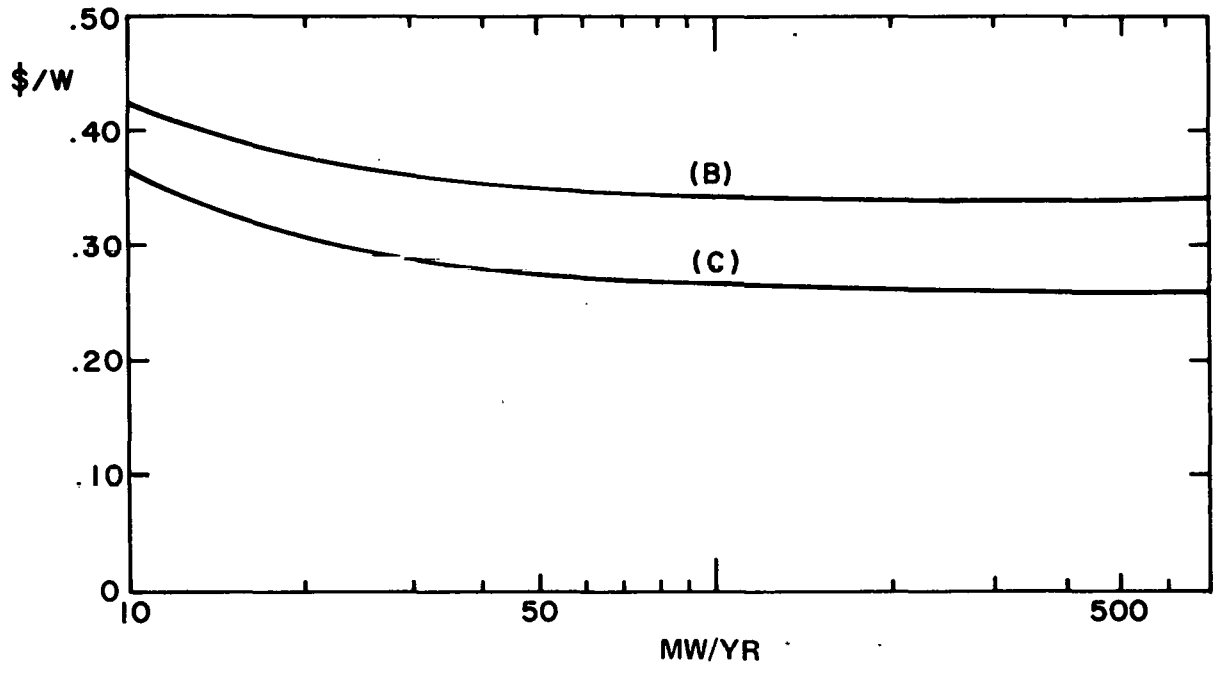

Figure 38. Manufacturing cost as a function of factory size.

These estimates of the array module manufacturing cost, including factory level overhead have been done in considerable detail. In every case the financial assumptions have been made using data from a wide variety of sources and reasonable values reflecting the general industry have been assumed. This is RCA's estimate of the cost, not RCA's cost.

For purposes of illustration it is interesting to assume a price for the silicon material which has not been included in any of this analysis. We assume silicon wafers are available for \$20 to \$40/M^2.

	500 MW/yr	
Silicon cost	\$20/M^2	\$40/M^2
Manufacturing cost + Factory level overhead	\$0.292/W	\$0.292/W
Yielded silicon cost	0.162/W	0.324/W
Profit	0.504/W	0.05/W
	0.504/W	0.666/W

We would like to assure the reader that the similarity between the goals of the LSSA program and these results is completely coincidental. It perhaps bespeaks the wisdom of the planners who established the goals in the first place. A selling price of $0.50/W turns out to have been a very meaningful goal. As further studies are conducted, this may turn out to be a transitory coincidence as even lower costs are achieved!

SECTION VII

SHEET ALTERNATIVES

Assessing the state of the technology for preparing single-crystal silicon sheet at this time leads to the same conclusions as we have found previously. Only wafers cut from Czochralski-pulled ingots will be available in the quantity and with the quality required by the near-term needs of the Automated Array Processing Task of the Low Cost Silicon Solar Array Project. There is, however, the ever-present question of cost. In the analysis above, the wafers are assumed to cost \$0.16 to \$0.32/W and the resulting solar cells are 15% efficient. The effect of lower efficiency impacts the total system cost. If we assume that the total system cost is \$1/W, a 30% reduction in cell efficiency increases the system cost by \$0.40/W. Even if the material which provided this performance were free, there is still a net increase in the system cost. At a system cost of \$0.50/W, such free material will result in a cost saving compared with the higher assumed price of wafers. It seems that 15% efficiency is a useful goal. Only Czochralski-pulled material and epitaxially grown layers of single-crystal silicon have been able to demonstrate cells of this efficiency.

Ribbon techniques have made steady progress during the year. Cells in the 10 to 12% efficiency range have been fabricated in ribbon material. However, before such material will be suitable for the Automated Array Assembly Task, several further advances will be required. The included particle count must be reduced or the location at which the particles appear must be controlled so that they can be removed from the active cell area. The residual strain must be reduced to the point where the mechanical stability of the ribbon will be sufficient to prevent a high yield loss due to cracking. Also, the strain should be low enough so that the ribbon does not shatter on being cut or scribed to be divided into sections of a given length.

It is the higher efficiency requirement which will be the most restrictive for any silicon sheet forming technique. Such a high efficiency will require that the silicon be prepared from a very high purity SiO_2 container or one with which it has little interaction. Any appreciable solubility of impurities

is going to limit the cell efficiency either through degradation of lifetime or degradation of junction properties. Even the recently reported high efficiency cells prepared in polycrystalline silicon used a high purity grade of poly to achieve their outstanding result. Therefore, any technique in which the surface-to-volume ratio of the silicon in contact with a container is high, must be evaluated very carefully to assure that good cystallinity is not being acheived at a sacrifice to bulk electronic properties.

At this time, methods which are "containerless," i.e., ribbon-to-ribbon zone refining, regular float zone refining, or CVD, are either not fully developed or too expensive in their present form.

Thus, only wafers sliced from ingots are presently available as starting sheet for array processing. Further, it would appear that with new wafering methods and cheaper poly, a significant reduction in cost of this material can be acheived.

SECTION VIII

CONCLUSIONS

As a result of an extensive and detailed examination of the present day art in semiconductor manufacturing we conclude that:

(1) The goal of a selling price of $0.50/W for a volume of 500 MW/year in 1986 is attainable assuming $20/M^2 for silicon sheet.

(2) The most cost-effective panel design is a double glass panel.

(3) The highest performance (for aging) panel design is a double glass panel.

(4) Automated interconnection using gap welding, ultrasonic bonding, or spot reflow soldering are all cost effective.

(5) Application of antireflection coating using automated spray-on equipment is cost effective.

(6) Screen-printed Ag metallization is cost effective although a serious cost component.

(7) Several junction formation technologies are cost effective. Ion implantation has a slight advantage.

Principal problem areas are;

(1) Maintenance of high cell efficiency at high yield. 15% with 82% yield was assumed in our analysis.

(2) Achievement of high mechanical yield with automated handling equipment.

(3) Development of low-cost screening inks which reliably provide low contact resistance, stable metallization.

(4) Demonstration of reliable automated interconnect technology.

(5) Demonstration of glass encapsulation techniques suitable for 20-year life.

(6) Minimizing factory level overhead. Marketing, sales, distribution, service, and warranty costs have not been considered.

APPENDIX A

A. COST ANALYSIS PROCEDURE

For purposes of cost analysis, the manufacture of solar array modules has been represented by a series of technological process. (See Appendix B for definition of terms). Each technological process must be described in terms of the following:

(1) Incoming material requirements.

(2) Value added - material, labor, overhead.

(3) Equipment requirements as a function of production levels.

(4) Process yield - ratio of output units to input units. (Note that this is a measure of *physical flow*, not product quality.)

After these parameters have been provided, alternative manufacturing processes can be defined in terms of a subset of these technological processes. For a specified level of output (measured in megawatts), cost data will be provided for each technological process and the total manufacturing process.

The following problems arise even in this simple cost model:

(1) The electrical characteristics of the output of two alternative technological processes may differ.

(2) The quality of two alternative processes may differ.

(3) Synergistic effects of combining various processes may need consideration.

In the initial model implementation, the material input to any technological process i will be M_i units. If y_i is the process yield and r_i is the number of input units constituting one output unit (e.g., 7.35 g per wafer), then the output M_i of this process will be $(M_i/r_i)y_i$. The number of input units scrapped in the process will be $M_i - M_i' r_i = M_i(1-y_i)$.

Figure A-1 depicts a technological process used in the manufacture of solar array modules. M_i incoming units valued at $\$X_i$ per unit are processed. Direct material, direct labor, and overhead increase the value of each unit to $\$X_i'$. M_i' units leave the process and enter the next step; the remaining input units are scrapped, with the salvage value being used to reduce process overhead. The average output unit cost X_i' is determined from process cost information, as shown in Appendix C.

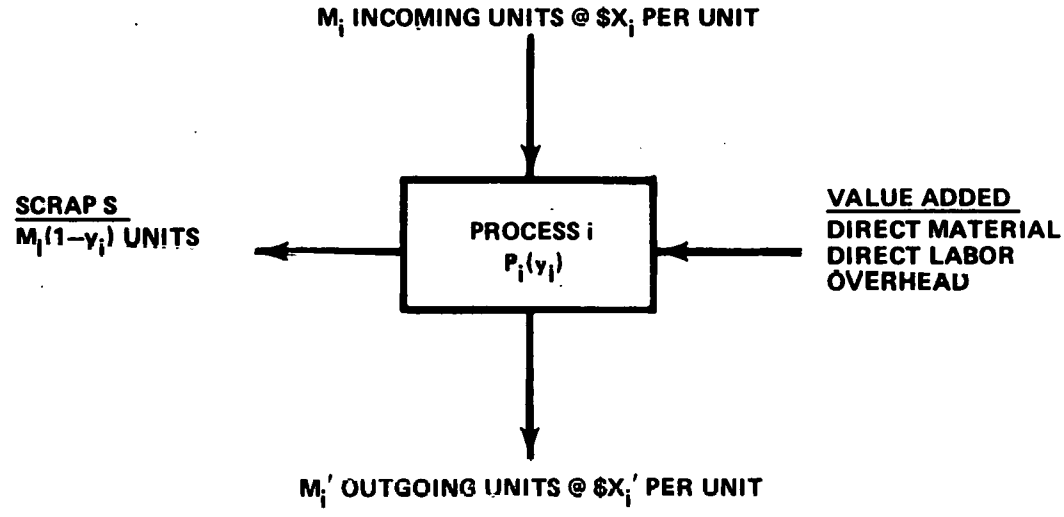

Figure A-1. Technological process representation.

It is important to note that the number of units entering a process normally will be greater than the number leaving the process. Hence, the capacity requirements of various processes may differ. This simple model assumes that flow is from one process to the next; no feedback of units to an earlier stage is currently permitted. Therefore, for a given megawatt requirement, the processing requirements of each technological process can be determined and then the cost of processing a unit computed.

Once a description of each technological process has been made, the user of the model must specify the output requirements (megawatts), the technological processes to be used, and the electrical characteristics of the final solar cells (electrical characteristics will be dependent upon the processes used). The model will then compute the cost of output requirements and provide detailed cost estimates on a process basis. Alternative strategies can be explored. Also sensitivity of cost to various parameters can be studied by varying the individual parameters.

Once a small number of feasible alternatives have been selected, a detailed financial analysis could be made of each alternative. This analysis could use a simulation approach in order to incorporate uncertainty rather than the deterministic approach utilized in the initial screening process in order to estimate the risk involved in each alternative scheme.

This model facilitates the analysis of alternative manufacturing approach It is only a first approximation, however, whose primary purpose is to systemat---

the financial analysis and permit comparisons with current state-of-the-art cost estimates. This initial model will need enhancements to incorporate some os all of the following items:

(1) Multi-year analysis capability utilizing discounted cash flow techniques.

(2) Distribution of electrical characteristics to represent the "quality" of individual processes. This would be based upon the performance approach described in Quarterly Report No. 1 [A-1].

(3) Synergistic effects of combining certain processes.

The selection of those features to be implemented will depend upon the number of different process combinations to be analyzed and the accuracy to which process parameters can be estimated.

The cost estimates provided by the model include:

(1) Processing cost, expressed in $/W

(2) Floor area requirements for manufacturing area

(3) Direct and indirect labor personnel required

(4) Material and direct expense summary

In order to estimate selling price, wafer cost, factory investment, interest and depreciation on this investment, and salaries of support personnel must be determined. (Support personnel includes administration, warehouse personnel, finance, quality control, etc.)

That is,

Wafer cost, $/W
+ Processing cost, $/W
+ Heating, cooling, lighting, $/W
+ Insurance, $/W
+ Factory interest & depreciation, $/W
+ Administrative & support salaries, $/W
+ Profit, $/W

= Selling price, $/W

A-1. B. F. Williams, *Automated Array Assembly*, Quarterly Report No. 1, ERDA/JPL-954352/1, prepared under Contract No. 954352 for Jet Propulsions Laboratory, March 1976.

APPENDIX B - GLOSSARY OF TERMS

A. GENERAL INPUT PARAMETERS

1. Growth profile - not used currently
2. Shift premium - 2nd or 3rd shift bonus rate
3. Depreciation method: SL = straightline; SYD = sum-of-the-year-digits
4. Interest rate on debt - interest rate on borrowed funds
5. Debt ratio - % of fixed assets financed by debt
6. Sheet - 7.8-cm (3.07)-diameter wafer
7. Solar cell - a "sheet" after electrical test
8. Array module - a 14.6 ft^2 panel containing 224 solar cells
9. Purchased silicon cost, $/W - not used currently

B. GENERAL INPUTS: INVESTMENT TYPE DEFINITIONS

1. Name - investment name
2. Type - process or factory
3. Availability - % of time investment is available for use. Remainder of time consists of preventive maintenance, unscheduled maintenance, or idle time due to lack of availability of related investments
4. Cost - first cost + delivery charges + taxes + installation costs
5. Book life - estimated life for depreciation purposes
6. Area - area, in ft^2, occupied by investment and associated operators

C. GENERAL INPUTS: LABOR TYPE DEFINITIONS

1. Labor name - labor category
2. Labor type - direct: labor which varies directly with the level of production; indirect: labor which is constant over a range of production
3. Wage rate = $/hr base pay
4. GP# - not used
5. Fringe benefits - cost of employee fringe benefits expressed as a % of wage rate
6. Efficiency - ratio of labor required to actual labor (allows for rest periods, lunch periods, absences, etc.)

D. GENERAL INPUTS: EXPENSE TYPE DEFINITIONS

1. Expense name - material or direct expense name
2. Type - material: items which become an integral part of solar cell or array module; direct expense: items consumed in cell or array manufacture which do not become an integral part of assembly
3. Cost - (a) cost of item, in $/cm^3, $/gram, $/kwh (process expenses will be expressed in units specified); (b) "specified in $" if process expense will be expressed in $
4. Salvage value - not used currently

E. PROCESS PARAMETERS

1. Process - group of operations associated with a specific technology step
2. Subprocess - a group of operations shared by one or more processes
3. Input unit, output unit - "sheet," "solar cell," or "array module"
4. Transport In, Transport Out - method of transferring units into and out of the process area
5. Process yield ("YIELD") - ratio of output units to input units. This is a measure of physical flow, not process quality
6. Input unit salvage value ("SALVAGE VALUE") - estimated recovery value of a scrapped input unit. At this moment, all values are zero
7. Production area floor space requirements - estimate of floor area needed, excluding area occupied by investments. "Floor space" is calculated using the "AREA (SQ.FT.)" value associated with the largest "INPUT UNITS" volume less than or equal to current production volume. The area associated with investments is added to this base area amount to determine the "estimated floor area" of the process
8. Description - brief process description
9. Assumptions - list of assumptions made in preparing cost estimate
10. Procedure - description of process major steps
11. Investments - (a) name: investment name, defined in B above; (b) maximum throughput units: throughput of investment (sheets/h, solar cell/h, or array module/h. Effective rate = maximum throughput x availability. (If both sides of an input wafer are to be processed separately, either adjust the throughput rate *or* adjust the "fraction of input units processed" parameter.) (c) % input units processed: used to adjust input volume for rework and for processing both sides of a wafer separately. It may also be used for "rework only" investments to specify fraction of input units requiring rework. NOTE: If two or more different investments are part of a set, the *effective* throughput rates must be the same.

12. Labor - (a) name: defined in C above; (b) labor requirements base: (1) investment name or (2) "fixed" - # persons/shift fixed (3) "DL" - base is # of direct labor persons; (4) "TL" - base is # fo labor persons associated with process (c) # of persons/shift/base unit - ratio of persons of specified labor type to # units of specified base *or* (d) throughput/h/person - # of input units per hour handled by specified labor type

    % input units processed - % of input units for which this type of labor is required. If an input unit is processed more than once (both sides and/or rework), this factor may be less than 100%. If only reworked units or units passing some internal test are processed, this factor may be less than 100%.

$$\#\ \text{operators/shift} = \frac{\#\ \text{input units/yr} \times \%\ \text{input units processed}/100}{\text{throughput/h} \times \#\ \text{hours/year} \times \text{efficiency}}$$

13. Supplies/expenses - (a) name - see D above; (b) annual fixed part - fixed part of expense (multiplied by # labor persons or investment units for labor or investment bases). Must be specified in same units as espense name. (c) variable part - units - variable part of expense; (d) base - (1) per input unit, % input units processed (2) per available investment/hr of specified investment

$$\$\ \text{Cost} = (\text{Annual fixed part} + \text{variable part} \times \text{base units}) \times (\$/\text{unit})$$

F. COST ANALYSIS: PROCESS AND OTHER COST ESTIMATES

1. Material - material cost, $/W
2. D.L. - direct labor cost, including fringe benefits, $/W
3. EXP. - direct expense cost, $/W
4. P.OH. - process overhead cost, $/W (indirect labor cost)
5. INT. - interest cost, $/W
6. DEPR. - depreciation cost, $/W
7. TOTALS - total of items 1-6, above
8. INVEST - investment required, $/W

G. COST ANALYSIS: MANUFACTURING SEQUENCE NAME

1. Material, etc. - as in F above
2. SALVG. - estimated recovery value of scrap, $/W