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Processing and Modeling Issues for Thin-Film Solar Cell Devices

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Summary

During the second phase of the subcontract, IEC researchers have continued to provide the thin film PV community with greater depth of understanding and insight into a wide variety of issues including: the deposition and characterization of $CuIn_{1-x}Ga_xSe_2$, CdTe, CdS, a-Si, and TCO thin films; the relationships between film and device properties; and the processing and analysis of thin film PV devices. This has been achieved through the analysis and quantification of the reaction chemistries involved in thin film deposition and through the thorough and systematic investigation of all aspects of film and device production. This methodology has led to improved process control of the fabrication of a-Si solar cells, in-depth and device-specific modeling, reliable and generally applicable procedures for contacting CdTe films, and controlled fabrication of a 15% efficient $CuIn_{1-x}Ga_xSe_2$ solar cell. Specific accomplishments are listed below.

$CuIn_{1-x}Ga_xSe_2$ Solar Cells

1. Presented a simplified set of four chemical reactions and estimated the values of reaction rate constants and activation energies which are sufficient to explain the observed growth kinetics of $CuInSe_2$ films obtained by the selenization of Cu/In bi-layers. This set of reactions has been successfully applied to selenizations carried out in a CVD tubular reactor with H_2Se and in a PVD reactor using an elemental Se source.
2. Characterized the reaction pathways to produce $CuIn_{1-x}Ga_xSe_2$ films through the selenization with H_2Se or Se of Cu, In, and Ga films. The initial layer stacking sequence Mo/Cu/Ga/In is preferred over the alternative Mo/Cu/In/Ga. $CuIn_{1-x}Ga_xSe_2$ is formed from the intermediate ternary phases $CuInSe_2$ and $CuGaSe_2$ which then react to form $CuIn_{1-x}Ga_xSe_2$. An excess of Se vacancies is believed to enable the complete reaction of precursors to form $CuIn_{1-x}Ga_xSe_2$.
3. Demonstrated, by a systematic investigation of a variety of temperature - time sequences of the individual sources and the substrate, that four source evaporation of $CuIn_{1-x}Ga_xSe_2$ films is a procedure with wide process latitude.
4. Developed a two step deposition process to control the adhesion and internal stress of the Mo contact for $CuInGaSe_2$ and demonstrated that the relative crystal orientation of the Mo directly affects the orientation of the $CuInGaSe_2$ film.
5. Demonstrated the dependence of device properties on the characteristics and deposition procedures employed to deposit CdS and ZnO films.
6. Demonstrated the relevance and validity of these studies by the fabrication of a 15% efficient $CuIn_{1-x}Ga_xSe_2$ solar cell with V_{oc}=0.62 V.

CdTe solar cells

7. Developed the Cu diffused back contact - an effective and reproducible method for fabrication of low resistance contacts to CdTe/CdS solar cells.
8. Demonstrated that the Cu diffused contact is not "process specific" by application to CdTe films produced by a variety of procedures at several laboratories.
9. Demonstrated that the Cu diffused contact is suitable for use with a wide variety of metallic conductors independent of their work functions.
10. Demonstrated progress toward producing devices with both high V_{oc} and thin CdS by using CBD CdS to produce devices with V_{oc} ~ 800 mV and CdS layer thickness ~ 1000 Å.
11. Began experiments to investigate the influence of CdS-CdTe interdiffusion through experiments in which $CdTe_xS_{1-x}$ films are intentionally and controllably incorporated into CdTe/CdS devices.
12. Began experiments to evaluate the utility of substitution of HCl gas for $CdCl_2$ in the CdTe post deposition heat treatment step.

a-Si Solar Cells

13. Completed a thorough analysis of the influence of deposition conditions on the properties of the p, buffer, i, and n layers of a-Si solar cells.
14. Completed modifications to the PECVD reactor which minimize carry over of process by-products and impurities from one process step to the next.
15. Demonstrated reproducibility and process control by the performance of a series of 10 processing runs which produced devices in the range of 7.8 - 8.1% efficiency.
16. Demonstrated the ability to deposit high quality i-layers and low resistance contacts by producing devices with FF > 74% and $R_{oc} < 5\ \Omega\text{-cm}^2$ by reducing the delay between the a-Si and TCO deposition to ~ 1 day.
17. Developed an effective and simplified optical model for evaluating triple stacked a-Si solar cells.
18. Developed and verified a model for a-Si device operation which emphasized the role of the ratio of carrier collection length to i-layer thickness.

Device Analysis

19. Developed simplified procedures for accurately representing the J-V characteristics of polycrystalline and a-Si solar cells.
20. Established a set of baseline values for CdTe, $CuIn_{1-x}Ga_xSe_2$, and a-Si solar cells produced at IEC.

In addition to these in-house activities, IEC has maintained an active role in the collaboration with over ten different PV and thin film research and development organizations. More specifically, IEC personnel have leadership roles in both the a-Si and CdTe teamed research activities. It is through these activities that IEC personnel assure that the results of their scientific accomplishments are disseminated throughout the PV community.

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1.0 INTRODUCTION

1.1 Overview

The overall mission of the IEC is the development of thin film photovoltaic cells, modules and related manufacturing technology and the education of students and professionals in photovoltaic technology. The objectives of this four year NREL subcontract are to advance the state-of-the-art and acceptance of thin film PV modules in the areas of improved technology for thin film deposition, device fabrication and material and device characterization and modeling relating to solar cells based on CdTe, on $CuInSe_2$ and its alloys, and on a-Si and its alloys.

In the area of $CuInSe_2$ and its alloys, IEC researchers have produced $CuIn_{1-x}Ga_xSe_2$ films by selenization of elemental and alloyed films with H_2Se and Se vapor and by a wide variety of process variations employing co-evaporation of the elements. Careful design, execution and analysis of these experiments has led to an improved understanding of the reaction chemistry involved including estimations of the reaction rate constants. Investigation of device fabrication has also included studies of the processing of the Mo, CdS and ZnO deposition parameters and their influence on device properties. An indication of the success of these procedures was the fabrication of a 15% efficiency $CuIn_{1-x}Ga_xSe_2$ solar cell.

Activities related to CdTe-based solar cells include investigations of the low resistance back contact to the CdTe, the CdS window/heterojunction partner to the CdTe, and the post-deposition processing of the CdTe/CdS layers. These activities have led to the development of an effective and reproducible method for producing the back contact using a diffused Cu junction, the investigation of CBD CdS window layers, and the substitution of HCl for $CdCl_2$ in the post-deposition heat treatment.

In the a-Si area, reproducibility and process control have been achieved through the redesign and rebuilding of the PECVD reaction canister combined with an optimization of processing parameters related to each of the a-Si layers -p, buffer, i, and n, as well as the TCO window and back contact. Success has been demonstrated by the performance of a series of 10 processing runs producing devices with best efficiencies in the range 7.8 - 8.1%. In addition, a simplified model has been produced for characterizing device operation of single junction devices in which the ratio of collection length to i-layer thickness is identified as the key indicator of device performance and a straight-forward optical model has been successfully applied to analysis of the current generation in each layer of triple stacked a-Si cells.

The measurement, characterization and modeling of thin film device operation has been specialized independently for devices produced with each class of materials. Also, data has been accumulated and analyzed to develop baseline device parameters for each type of cell. These baseline values will be used as the basis for evaluation of the effects of future process modifications.

IEC personnel are active in teamed research in all three thin film material areas, both through NREL's Thin Film PV Partnership program and on a less formal, one-on-one basis. It is partly through these interactions that IEC serves to disseminate PV expertise throughout the PV community and thereby achieve its larger goals.

1.2 Solar Cell Baseline Process

In order to provide a basis for evaluating the effects of various process modifications on device performance, we have identified "baseline" values for each type of cell produced.

Selection Criteria

A set of devices has been selected from each of the basic types of solar cells that IEC makes (i.e. $Cu(In,Ga)Se_2$,CdTe, selenized $CuInSe_2$ and a-Si). This set was chosen to represent the level of performance (in power output) that can be achieved by the better devices during the use of standard processing conditions. The cells were chosen by selecting the highest power output device on each substrate or sample. Then the best six samples were chosen, their output parameters were normalized to the same test conditions and then averaged to give the baseline output numbers.

Device Measurements

Table 1. Shows the measured parameters and test conditions of the devices selected.

V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	T (°C)	Area (cm^2)	Date tested	Sample #	Cell #
$Cu(In,Ga)Se_2$							
0.604	31.5	72.9	36	0.43	07-Dec	32535-33	2
0.597	32.0	72.2	33	0.43	07-Dec	32535-23	3
0.548	32.6*	69.4	32	0.133	01-Dec	32527-33	8
0.547	31.3*	70.9	32	0.133	29-Sep	32467-33	2
0.570	30.1*	69.4	32	0.133	25-Oct	32530-23	7
0.566	28.6*	72.5	32	0.133	08-Dec	32548-23	7
CdTe							
0.802	22.0*	67.5	32	0.31	15-Aug	40826-13	5
0.767	22.3*	64.2	32	0.20	15-Jul	40823-12	2
0.748	21.6*	62.1	32	0.20	15-Aug	40826-12	6
0.764	22.0*	59.3	32	0.20	14-Jul	40823-11	1
0.712	20.5	59.8	37	0.21	14-Oct	40832-13	15
0.737	21.9*	53.6	32	0.20	16-Aug	40826-21-2	2
Selenized $CuInSe_2$							
0.431	35.8*	65.9	32	0.133	08-Dec	89292-2	11
0.410	34.7*	63.2	32	0.133	27-Nov	89286-1	11
0.417	33.9*	63.0	32	0.081	02-Dec	89291-2	10
0.413	36.4*	56.7	32	0.133	31-Oct	89279-1	10
0.383	37.1*	58.9	32	0.133	28-Oct	89279-2	7
0.393	33.1*	61.8	32	0.133	02-Dec	89287-1	11
a-Si							
0.805	14.0	71.3	32	0.071	09-Sep	GD4344-22	3
0.800	13.7	72.7	30	0.071	12-Aug	GD4336-22	2
0.821	13.7	70.9	30	0.071	04-Aug	GD4320-11	2
0.795	13.9	71.5	29	0.071	21-Dec	GD4373-11	1
0.786	14.0	72.1	33	0.071	19-Dec	GD4373-22	2
0.809	13.7	71.3	33	0.071	19-Dec	GD4374-22	2

* device was measured under a tungsten-halide (ELH) illumination source (see text)

Table 1. Measured parameters of the devices selected for the baseline process.

These devices were measured at different temperatures and under two separate illumination conditions. Those measured under the tungsten-halide source (ELH) were not quite at an equivalent illumination level of 100 mW/cm^2. To compare the output of these devices, all of them were adjusted to about the same ambient test conditions. This was done by scaling the short circuit current, in the case of the tungsten-halide illumination to a 100 mW/cm^2 equivalent and adjusting the open circuit voltage to both the new adjusted short circuit current and a standardized 25°C test temperature using the equations:

$$\mathrm{Ln}(J_{00}) = \mathrm{Ln}(J_{SC}) + \left(\frac{q}{2kT}\right)\left(\frac{E_G}{q} - \frac{2V_{OC}}{A}\right) \qquad \text{(B.1)}$$

and:

$$V_{OC} = A\left[\frac{E_G}{q} + \left(\frac{2kT}{q}\right)\mathrm{Ln}\left(\frac{J_{SC}}{J_{00}}\right)\right] \qquad \text{(B.2)}$$

The values used for the corrections are shown in Table 2.

Device Type	W-I (ELH) (mW/cm^2)	E_G (eV)	A-factor
$Cu(In,Ga)Se_2$	93	1.15	1.5
CdTe	103	1.40	2.0
selenized $CuInSe_2$	95	1.00	1.8
a-Si		1.60	1.7

Table 2. Adjustment parameters used.

Because the corrections to the open circuit voltage and short circuit current are fairly small, no adjustment was made to the fill factor. The output parameters adjusted to standard test conditions are then shown in Table 3. The final baseline of the averaged output is shown in Table 4.

Eff (%)	FF (%)	V_{OC} (V) @25°C	J_{SC} (mA/cm^2) @AM1.5
Cu(In,Ga)Se_2			
14.1	72.9	0.614	31.5
13.9	72.2	0.604	32.0
13.6	69.4	0.558	35.1
13.3	70.9	0.557	33.6
13.0	69.4	0.579	32.3
12.8	72.5	0.575	30.7
CdTe			
11.7	67.5	0.814	21.4
10.9	64.2	0.780	21.7
9.9	62.1	0.761	20.9
9.8	59.3	0.777	21.4
9.0	59.8	0.738	20.5
8.6	53.6	0.751	21.3
selenized CuInSe$_2$			
11.0	65.9	0.444	37.7
9.8	63.2	0.424	36.5
9.7	63.0	0.431	35.7
9.3	56.7	0.427	38.3
9.1	58.9	0.397	39.1
8.8	61.8	0.407	34.9
a-Si			
8.2	71.3	0.817	14.0
8.1	72.7	0.809	13.7
8.0	70.9	0.830	13.7
8.0	71.5	0.802	13.9
8.1	72.1	0.801	14.0
8.0	71.3	0.823	13.7

Table 3. Output parameters under standard test conditions

Device Type	Eff (%)	FF (%)	V_{OC} (V)	J_{SC} (mA/cm^2)
Cu(In,Ga)Se_2	13.4	71.2	0.581	32.5
CdTe	10.0	61.1	0.770	21.2
Selenized CuInSe$_2$	9.6	61.6	0.422	37.0
a-Si	8.1	71.6	0.814	13.8

Table 4. Output parameters of the baseline process

2.0 MATERIAL AND DEVICE FABRICATION

2.1 REACTION CHEMISTRY OF THE $CuInSe_2$ AND $CuIn_{1-x}Ga_xSe_2$ SYSTEMS

2.1.1 $CuInSe_2$ Reaction Chemistry

For the effective design and real time control of processing equipment to produce $CuInSe_2$ modules, it is essential to understand the mechanism of the growth of $CuInSe_2$ and to obtain the pertinent kinetic data. A chemical engineering reaction analysis of the film growth supplies the quantitative information needed to make $CuInSe_2$ in any reactor scheme. Thus, such an analysis could be used to interpret reactions which take place during formation of $CuInSe_2$ in a three source physical vapor deposition reactor as well as selenization of metal precursors in a physical or a chemical vapor deposition reactor. As was reported in the previous annual report (1), at IEC, $CuInSe_2$ has been formed by selenization of Cu/In layers in either H_2Se or elemental selenium. Our aim was to combine the results obtained in these two methods of production to get a better analysis of the reaction pathways and obtain the activation energies for the rate constants of the pertinent chemical equations.

2.1.1.1 Summary of the Previous Work:

In the first method $CuInSe_2$ was formed in a tubular chemical vapor deposition reactor. The experimental apparatus and set-up has been described in the previous annual report and several publications(1,2). Molybdenum coated soda lime glass was first sputter coated with copper and indium layers . The thickness of the layers were adjusted to get a ratio of Cu/In=0.9. These bilayers were then reacted in the tubular reactor using 1.7% H_2Se in argon. The reaction was carried out at 410°C under isothermal conditions. The reaction time was varied between 1 and 45 minutes. The samples were analyzed using X-ray diffraction, XRD to identify the chemical species and the peak intensities were used to determine the composition of each species. The time progressive concentration profiles of the chemical species during the selenization reaction were thus obtained. Based on the identified chemical species, a reaction pathway was proposed as follows:

Reaction	Rate Constant	
$2\ In + Se \Rightarrow In_2Se$	k_2	
$In_2Se + Se \Rightarrow 2\ InSe$	k_3	
$2Cu_{11}In_9 + 20\ Se \Rightarrow 11\ Cu_2Se + 9\ In_2Se$	k_5	(Set 1)
$Cu_2Se + In_2Se + 2\ Se \Rightarrow 2\ CuInSe_2$	k_6	
$Cu_2Se + 2\ InSe + Se \Rightarrow 2\ CuInSe_2$	k_7	

Using these chemical equations differential mass balances are written and the resulting simultaneous set of differential equations are solved to obtain the reaction rate constants. This procedure and the results are summarized in the previous annual report (1).

In the second method $CuInSe_2$ was formed with elemental selenization of Cu/In bilayers in a physical vapor deposition system. The copper and indium were sequentially deposited at room temperature on 1 mm thick Mo-coated soda lime glass substrates by electron gun evaporation to form the starting Cu/In layers. The copper thickness was fixed at 2500 Å while the indium thickness was varied to control the initial Cu/In ratio from 0.8 to 0.9. Approximately 1.5 μm of selenium, enough to completely react the Cu-In layer, was evaporated onto the Cu-In substrates at room temperature. Following the selenium

deposition, the substrate temperature was ramped to the reaction temperature at a rate of ~35°C/minute, then held for 30 minutes for reaction while Se vapor was maintained at 10 Å/s. The selenized Cu-In layers were evaluated with XRD to identify the species as a function of temperature and initial Cu/In ratio. Based on this information the following reaction pathway was proposed:

Reaction	Rate Constant	
$2\ In + Se \Rightarrow In_2Se$	k_2	
$In_2Se + Se \Rightarrow 2\ InSe$	k_3	
$2Cu_{11}In_9 + 29\ Se \Rightarrow 11\ Cu_2Se + 18\ InSe$	k_{5n}	(Set 2)
$Cu_2Se + 2\ InSe + Se \Rightarrow 2\ CuInSe_2$	k_7	

The selenization of Cu/In bilayers in a PVD system is presented in detail in the previous annual report (1).

2.1.1.2 Present work:

In the present study we analyzed the results obtained from the two reactor systems to understand the formation chemistry better and to obtain the kinetic data as rate constants and activation energies.

The XRD scans for the selenized films in the PVD reactor is analyzed by the technique proposed by Verma (2) and the concentration profile for each species is obtained. This analysis complements the information gathered from the CVD reactor since it gives species concentrations at other temperatures and Cu/In ratios. However, in contrast to the results obtained from the CVD reactor, the species concentration information from the PVD reactor is obtained only at the end of an experimental run -which was 30 minutes- since the present design of the reactor does not render possible time progressive experiments. The data obtained is presented in Table 5.

Table 5. Moles (gmol) of chemical species obtained at the end of 30 minutes from the PVD reactor.

T (°C)	$Cu_{11}In_9$	In_2Se	InSe	$CuInSe_2$
		CuIn = 0.8		
250	0.57×10^{-6}	5.8×10^{-6}	0.7×10^{-6}	3×10^{-6}
300	0.2×10^{-6}	0	5.6×10^{-6}	9×10^{-6}
		CuIn = 0.9		
250	0.63×10^{-6}	2.6×10^{-6}	2.5×10^{-6}	3×10^{-6}
300	0.11×10^{-6}	0	4.5×10^{-6}	9.5×10^{-6}

The information from the PVD and CVD reactors is brought together to get a better understanding of the reaction mechanism. Examination of the experimental data from both reactors suggest that the following set of chemical equations for $CuInSe_2$ film growth of Cu-In layers will allow film growth to be satisfactorily modeled.

Reaction	Rate Constant	
$2\ In + Se \Rightarrow In_2Se$	k_2	
$In_2Se + Se \Rightarrow 2\ InSe$	k_3	
$2Cu_{11}In_9 + 20\ Se \Rightarrow 11\ Cu_2Se + 9\ In_2Se$	k_5	(Set 3)
$Cu_2Se + 2\ InSe + Se \Rightarrow 2\ CuInSe_2$	k_7	

This set of chemical equations does not include a reaction originally proposed in Set 1 between Cu_2Se and In_2Se to produce $CuInSe_2$.

Table 6. Reaction Analysis Model Equations

$$\frac{d([In]V_f)}{dt} = -2k_2[Se][In]V_f = -2k_2'[In]V_f$$

$$\frac{d([In_2Se]V_f)}{dt} = (k_2[Se][In] - k_3[Se][In_2Se] + 9k_5[Se][Cu_{11}In_9])V_f = (k_2'[In] - k_3'[In_2Se] + 9k_5'[$$

$$\frac{d([InSe]V_f)}{dt} = (2k_3[Se][In_2Se] - 2k_7[Se][InSe][Cu_2Se])V_f = (2k_3'[In_2Se] - 2k_7'[InSe][Cu_2Se])$$

$$\frac{d([Cu_{11}In_9]V_f)}{dt} = -2k_5[Se][Cu_{11}In_9]V_f = -2k_5'[Cu_{11}In_9]V_f$$

For any proposed set of chemical reactions species mass balance equations can be written and solved simultaneously to obtain the rate constants. The set of rate constants that best predict the concentration profiles can then be selected. The mass balance equations for the simplified chemical reaction set (Set 3) is given in Table 6. These equations can further be simplified assuming that the Se concentration in the film is a constant. This assumption has been justified experimentally (1,2). Thus, each k_i' is related to k_i as follows:

$$k_i' = k_i [Se]$$

The simultaneous set of differential equations given in Table 6 is solved numerically. An optimization program involving the simplex algorithm is used. The simplex algorithm is a multidimensional minimization, finding the minimum of an objective function of more than one independent variable. The objective function in our case is the sum of squares of the difference between the experimental and predicted species concentration for all the data points. The optimized set of rate constants are given in Table 7. The concentration profiles obtained with this rate constant set is plotted as solid lines in Figure 1; good agreement with the experimental data is obtained.

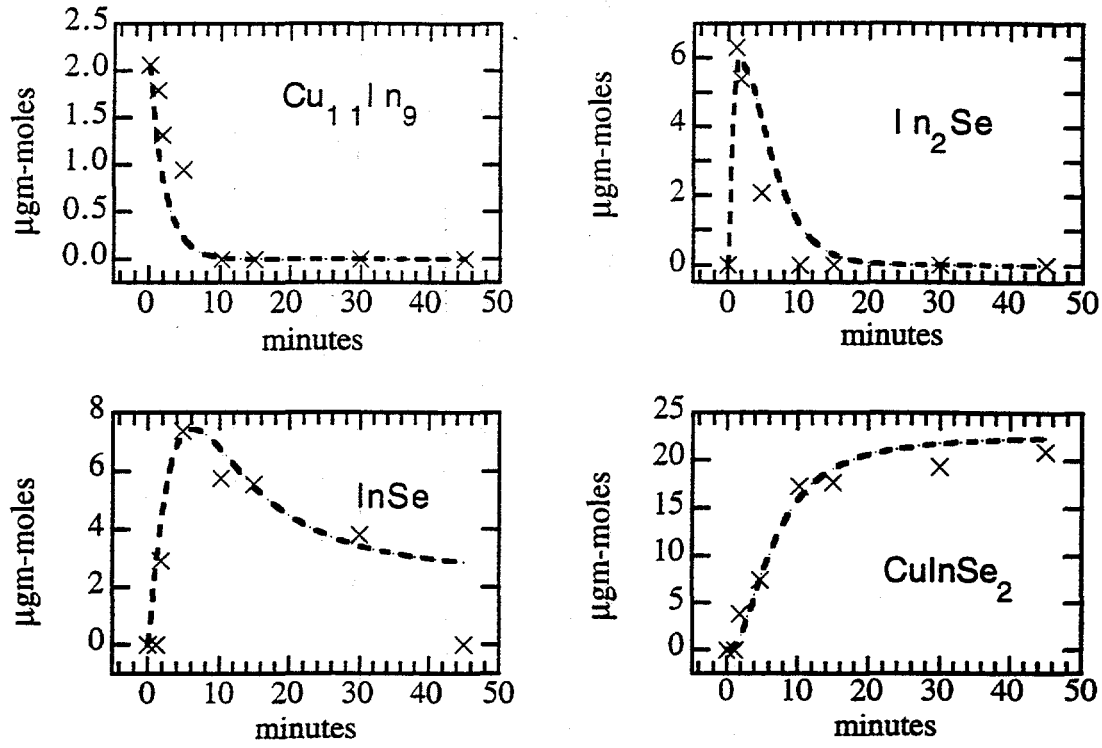


Figure 1. Comparison of measured (x) vs. calculated (--) data for the time progressive selenization of Cu-In layers in the tubular CVD reactor

Table 7. Optimized Set of Rate Constants

Reaction Rate Constants	CVD Reactor 400°C	PVD Reactor 300°C	PVD Reactor 250°C	Energy of Activation. kJ/mole (factor of 2 estimate)	Frequency Factor
k_2' min^{-1}	1.5	N/A	N/A		
$k_3'min^{-1}$	0.3	0.04	0.02	E_{a3}=53	$k'_{03}=4.1x10^3$ (min^{-1})
$k_5'min^{-1}$	0.2	0.05	0.02	E_{a5}=48	$k'_{05}=1.3x10^3$ (min^{-1})
$k_7'cm^3/gmol\text{-}min$	26	8.0	5	E_{a7}=32	$k'_{07}= 9.4x10^3$ $cm^3/gmol\text{-}min$

Species mass balance equations can be written for the chemical reactions described as Set 1 and Set 2. Solution of the differential equations of Set 1 gives a reasonable prediction of the experimental species concentration data whereas the In_2Se concentration could not be predicted with good accuracy with Set 2. Since good predictions are obtained with a simpler chemistry with Set 3, this set is taken to represent the mechanism in the rest of the calculations.

Using this chemical reaction set (Set 3) we next tried to estimate the values of rate constants at other temperatures. For this purpose we used the data obtained from the PVD reactor at 250°C and 300°C (Table 5). As indicated previously chemical species concentrations cannot be obtained as a function of time in our PVD reactor so the rate constants are estimated using only the species concentrations measured initially and at the end of the experimental run (30 minutes). Good agreement is obtained for two different Cu/In ratios

(0.8 and 0.9). Experiments are planned in the CVD reactor to obtain time progressive concentrations so more accurate estimates of the rate constants can be made at 250°C and 300°C.

Rate constants are dependent upon temperature through the Arrhenius relation:

$$k_i = k_{oi} \exp(-E_i / RT)$$

where k_{oi} is the frequency factor and E_i is the activation energy. A double logarithmic plot of k_i as a function of the reciprocal of temperature gives a straight line. (Fig. 2) the activation energy and the frequency factor can thus be obtained from the slope and intercept respectively. Once this information is obtained the value of the rate constant at any temperature can be estimated using the Arrhenius relation. Such information is invaluable in the design of any type of reactor for the production of $CuInSe_2$.

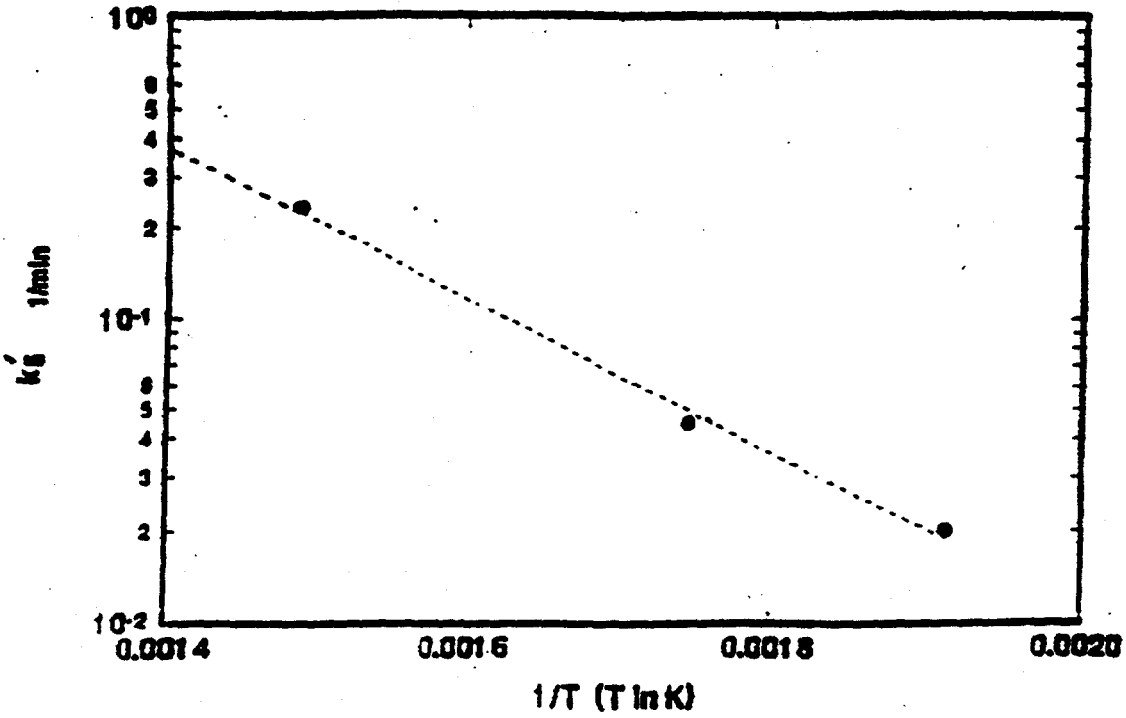


Figure 2. The arrhenius plot to get the activation energy E_{a5} and frequency factor K_{05}.

The set of rate constants k'_2, k'_3, k'_5, k'_7 are obtained at 250°C, 300°C and 400°C and the activation energies and the frequency factors are estimated. These results are tabulated in Table 3. Since we don't have concentration-time profiles for the data obtained from the PVD reactor, in our opinion the activation energies are accurate within a factor of two.

2.1.2 $CuIn_{1-x}Ga_xSe_2$ Reaction Chemistry

The $CuIn_{1-x}Ga_xSe_2$ films used for all high efficiency, >15%, solar cells where the Ga/(Ga+In) ratio is >0.2 have been deposited by physical vapor deposition (3,4). Most approaches to fabricate modules based on $CuInSe_2$ and its alloys, however, react metal precursor layers in a Se atmosphere. In this section the processing and characterization of the stacked Cu-In-Ga layers and the resulting films obtained by reacting the precursors with H_2Se or elemental Se at 400°C and 500°C are discussed.

Cu/In/Ga and Cu/Ga/In stacked precursors with Ga/(Ga+In) ratios from 0.2 to 1.0 were deposited on molybdenum-coated soda lime glass substrates. Cu and In were sputtered from elemental targets in a DC magnetron sputtering system and the Ga was deposited by physical vapor deposition to obtain Cu/(In+Ga) ≈1.0 The substrates were maintained at room temperature during the deposition of Cu, In and Ga. The Cu film thickness was chosen to yield 2 μm $CuIn_{1-x}Ga_xSe_2$ film. The Cu/Ga/In films were heat treated in an Ar atmosphere at 250°C for 1 hour to alloy the films. Each film was characterized by XRD and the morphology was characterized by SEM before and after heat treatment. The composition of the heat treated films was evaluated by energy dispersive spectroscopy (EDS).

The as-deposited stacked precursors were reacted in a selenium atmosphere, by H_2Se(5) or elemental Se, at 400°C and 500°C. The reacted precursors were characterized by XRD, SEM and EDS. The films obtained by reacting Cu/In/Ga films in H_2Se were heat treated in an Ar atmosphere at 500°C to 600°C for 1 hour and in an H_2Se atmosphere at 500°C for 1 hour in separate experiments. The heat treated films were characterized by XRD and SIMS.

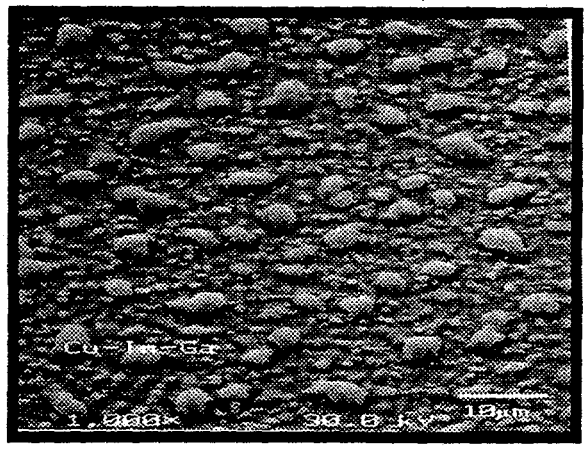
2.1.2.1 Stacked Precursor Layers

Results of X-ray diffraction analysis of stacked elemental layers for deposition sequences Mo/Cu/In/Ga and Mo/Cu/Ga/In are summarized in Table.8. The phases formed in the as-deposited condition for both sequences are identical. The films contained only elemental phases of Cu and In and binary phases Cu-In and $CuGa_2$. The morphology of the Mo/Cu/Ga/In films were more uniform than that of Mo/Cu/In/Ga (see Fig. 3) and were most likely controlled by the $CuGa_2$ phase. Since the morphology was uniform only for the sequence Mo/Cu/Ga/In, only these films were heat treated and their composition was evaluated after heat treatment. The morphology of the films did not change upon heat treatment. The heat treated films contained elemental phases Cu and In and binary phases $Cu_{11}In_9$, Cu_9Ga_4 and $CuGa_2$; no ternary phases were detected. The Cu_9Ga_4 phase was observed only in films with Cu/Ga > 2.0

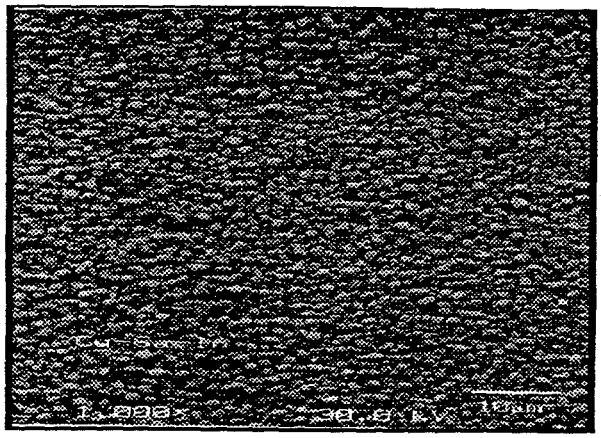
2.1.2.2 Reacted Precursors

The phases formed and the composition of the films reacted with H_2Se at 400°C and 500°C are shown in Table 9 for as-deposited precursors. The phases formed were found to be independent of the Ga and In deposition sequence and the morphology of the reacted films retained that of the precursors. Similar results were obtained for films reacted with elemental Se at the same temperatures. As shown in the table the films contained mixtures of $CuInSe_2$, $CuGaSe_2$ and secondary phases consisting of $Cu_{2-x}Se$, GaSe, Ga_2Se_3 and Cu-Ga depending on the starting Ga/(Ga+In) ratios. The secondary phases were observed only in films with Ga/(Ga+In) > 0.4. No binary phases containing In were observed. These two observations suggest that the reaction rates for the formation of the ternary $CuGaSe_2$ is lower than that of the $CuInSe_2$. The binary phases of Cu-In and Cu-Ga present in the precursors react with H_2Se or elemental Se to form the ternaries $CuInSe_2$ and $CuGaSe_2$. Further alloying between these ternaries was not favored for the reaction conditions investigated. The secondary phases were detected only for films with Ga/(Ga+In) > 0.4. Ga/(Ga+In) ratios measured by EDS, a technique that probes only

0.5 μm - 1.0 μm from the top surface. were less than expected in films containing In suggesting that in these films the Ga content was lower near the surface than at the Mo interface. This observation was supported by SIMS measurements.



a) Cu/In/Ga



b) Cu/Ga/In

Fig. 3 Difference in morphology between a) Cu/In/Ga and b) Cu/Ga/In films with Ga/(Ga+In)=0.8. Spot EDS/X-ray mapping revealed that the protruding regions on the surface of Cu/In/Ga films were In rich.

Table 8. Composition and phases formed for different Ga/ (Ga+In) ratios.

Composition (at. %) (Determined for sequence Mo/Cu/Ga/In)	**Phases in Mo/Cu/In/Ga**	**Phases in Mo/Cu/Ga/In**	**Phases in Mo/Cu/Ga/In Annealed in Ar at 250° C for 1 hr.**
Cu= 0.52 Ga= 0.48	Cu, $CuGa_2$	Cu, $CuGa_2$	Cu, $CuGa_2$
Cu=0.45 In=0.12 Ga=0.43	Cu, In, $CuGa_2$	Cu, In, $CuGa_2$	Cu, In, $CuGa_2$
Cu=0.3 In=0.1 Ga=0.6	In , $CuGa_2$	In , $CuGa_2$	In , $CuGa_2$
Cu=0.43 In=0.38 Ga=0.19	Cu, In , CuIn , $CuGa_2$	Cu, In , CuIn , $CuGa_2$	In, Cu_9Ga_4
Cu=0.54 In=0.33 Ga=0.13	Cu, In , CuIn, Amorphous Ga	Cu, In , CuIn, $CuGa_2$	In , $Cu_{11}In_9$, Cu_9Ga_4

Table 9. Precursors reacted in H_2Se at 400°C.

Phases and Composition of Cu/In/Ga films reacted at 400°C for 90 mins.		**Phases and Composition of Cu/In/Ga films reacted at 500°C for 90 mins.**	
Compn. (at. %)	**Phases**	**Compn. (at. %)**	**Phases**
Cu=0.29 Ga=0.29 Se=0.42	$CuGaSe_2$, $Cu_{2-x}Se$, Cu-Ga	*	$CuGaSe_2$, $MoSe_2$
Cu=0.24 Ga=0.19 In=0.07 Se=0.5	Multiphase $CuIn_{1-x}Ga_xSe_2$, Cu-Ga	Cu=0.22 Ga=0.19 In=0.08 Se=0.51	$CuInSe_2$, $CuGaSe_2$ GaSe, Ga_2Se_3
Cu=0.20 Ga=0.18 In=0.10 Se=0.52	$CuInSe_2$, $CuGaSe_2$, GaSe, Cu-Ga	Cu=0.19 Ga=0.14 In=0.16 Se=0.51	$CuInSe_2$, $CuGaSe_2$, Ga_2Se_3,GaSe
Cu=0.23 Ga=0.04 In=0.19 Se=0.54	$CuInSe_2$, $CuGaSe_2$	*	$CuInSe_2$, $CuGaSe_2$, $MoSe_2$
Cu=0.24 Ga=0.01 In=0.18 Se=0.57	$CuInSe_2$, $CuGaSe_2$	*	$CuInSe_2$, $CuGaSe_2$, $MoSe_2$

Secondary phases $Cu_{2-x}Se$,Ga_2Se_3,GaSe and Cu-Ga were present in minor amounts.
* Film peeled

The films reacted at 400°C were heat treated at temperatures from 500°C to 600°C in Ar and H_2Se atmospheres. Fig. 4 shows a detailed XRD scan of (220) and (204) peaks of the film with overall $Ga/(Ga+In) \approx 0.8$ heat treated in an H_2Se atmosphere and of a film with the same composition heat treated in an Ar atmosphere. Heat treatment in a H_2Se atmosphere improved only the crystallinity of the $CuInSe_2$ and $CuGaSe_2$ phases. The Se content increased from 51.8 at. % to 54.2 at.% and the Ga/(Ga+In) ratio was effectively constant at 0.62. Single phase $CuIn_{0.22}Ga_{0.78}Se_2$ was obtained for the film heat treated in an Ar atmosphere. The Se content decreased from 51.8 at. % to 50.2 at. % and the Ga/(Ga+In) ratio increased to 0.78. The excess anion vacancies formed as a result of Se loss during the heat treatment in an Ar atmosphere could have promoted interdiffusion of In and Ga between the $CuInSe_2$ and $CuGaSe_2$ phases. Single phase $CuIn_{1-x}Ga_xSe_2$ films were also obtained for all Ga/(Ga+In) ratios by heat treating in an Ar atmosphere while no homogenization was obtained in H_2Se heat treatment. Some of the secondary phases were still present after heat treatment in films with $Ga/(Ga+In) > 0.4$ independent of the heat treatment.

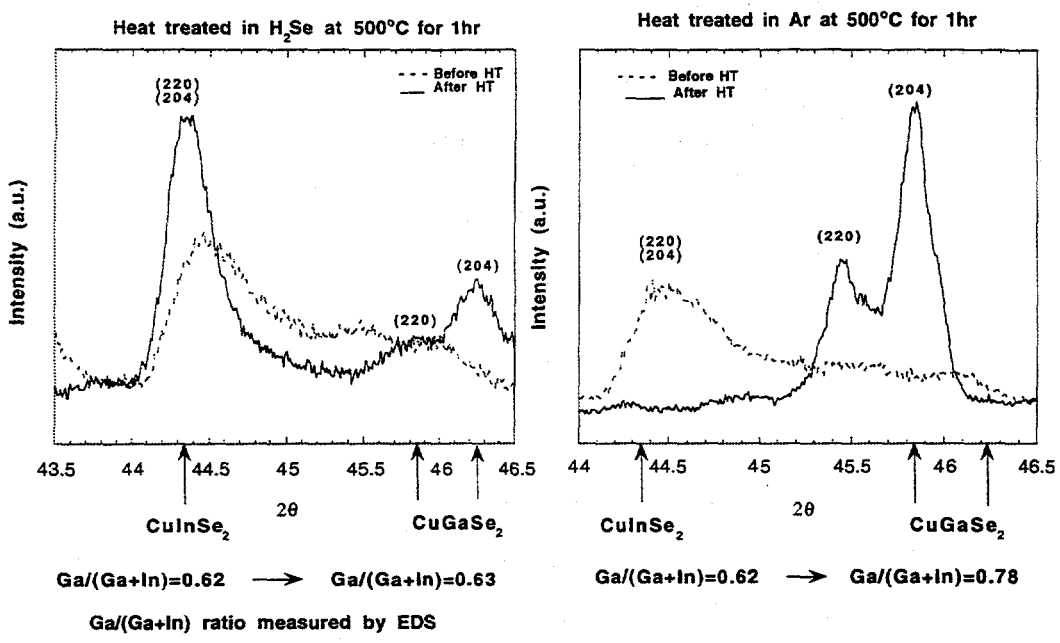


Fig.4. Detailed XRD scans of (220) and (204) peaks of the reacted films with Ga/(Ga+In)≈0.8 heat treated in an Ar atmosphere and in an H_2Se atmosphere.

Higher temperature heat treatments were required for producing single phase films with lower Ga content, i.e., Ga/(Ga+In) <0.4 . This can be explained by one or both of the following: 1) the grain sizes in films with Ga/(Ga+In) < 0.4 are large, therefore lattice diffusion is dominant, or 2) the diffusivities of In and Ga are low in $CuIn_{1-x}Ga_xSe_2$ films with lower Ga content. In either case higher temperatures would be required for interdiffusion. Similar heat treatment results, in Ar and H_2Se, were obtained for films reacted with elemental Se at 500°C.

2.1.2.3 Summary

The stacked Cu-In-Ga precursor layers contained only elemental and binary phases before and after heat treatment. The morphology of the precursors with Mo/Cu/Ga/In sequence was found to be more uniform than that of Mo/Cu/In/Ga sequence. The reacted films contained mixtures of $CuInSe_2$, $CuGaSe_2$ and secondary phases. The presence of secondary phases in films with Ga/(Ga+In) > 0.4 suggests that reaction with Se was not complete in those films. Heat treatment in an Ar atmosphere produces single phase films whereas heat treatment in an H_2Se atmosphere does not yield single phase films. Excess Se vacancies which may have formed due to Se loss during heat treatment in Ar, but are unlikely to form during H_2Se heat treatment, probably aided the interdiffusion of In and Ga leading to single phase films.

2.2. $CuIn_{1-x}Ga_xSe_2$ BY MULTISOURCE EVAPORATION

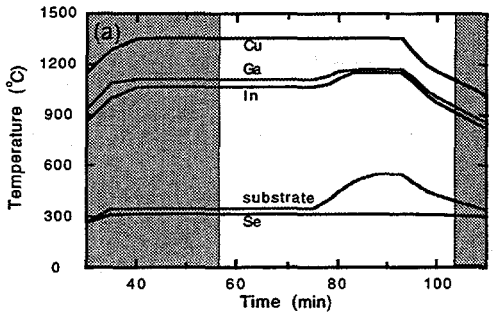
The performance of $CuInSe_2$ based solar cells has been improved significantly with the addition of gallium and/or sulfur to increase the bandgap. Previous results (6) with $CuIn_{1-x}Ga_xSe_2$ deposited by multisource evaporation have shown that the best cell efficiency is achieved with $E_g \sim 1.10\text{-}1.15$ eV. This corresponds to $x \sim 0.2 - 0.3$ where $x = Ga/(In+Ga)$. There are several issues that need to be addressed so that the bandgap can be increased further without significant losses in efficiency. This should enable the fabrication of cells with higher V_{oc} and lower J_{sc} which are more compatible with module fabrication. These issues include: 1) characterizing the effect of compositional non-uniformity both lateral and through the film; 2) determining the reaction mechanisms for the formation of $CuIn_{1-x}Ga_xSe_2$ by multisource evaporation; 3) developing improved substrates and metal contacts to provide good adhesion and electrical behavior; and 4) improving the window/heterojunction layers.

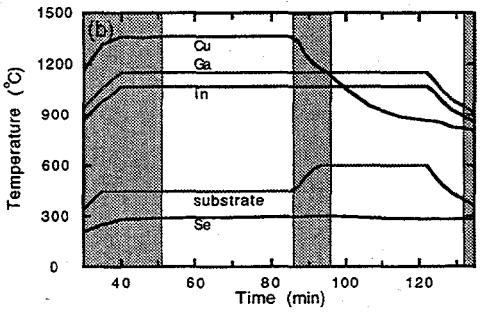
In this report results are presented with $CuIn_{1-x}Ga_xSe_2$ films deposited by four source elemental evaporation to have $x \sim 0.25$. The results are presented in two sections. The first section covers the $CuIn_{1-x}Ga_xSe_2$ deposition and film characterization. The second covers non-absorber layers including their fabrication and affect on $CuIn_{1-x}Ga_xSe_2$ films and devices. Device fabrication includes a large number of steps both before and after the $CuIn_{1-x}Ga_xSe_2$ deposition and several of these are evaluated in detail. In particular, the glass preparation and Mo deposition are found to be critical to providing good adhesion of the $CuIn_{1-x}Ga_xSe_2$ and affect the $CuIn_{1-x}Ga_xSe_2$ structure. The CdS is deposited by chemical bath deposition (CBD), and ZnO deposited by RF sputtering.

The best cell achieved during this period had $V_{oc} = 0.62$ V, $J_{sc} = 33.9$ mA/cm^2, FF = 72 %, and efficiency = 15.0 %. This is based on an active area measurement with area = 0.13 cm^2. The cell had a MgF_2 anti-reflection coating. In addition, cells have been fabricated with efficiencies ~ 13% with a wide variety of modifications to the $CuIn_{1-x}Ga_xSe_2$ deposition as well as the Mo, CdS, and ZnO layers.

2.2.1 $CuIn_{1-x}Ga_xSe_2$ Deposition and Film Characterization

$CuIn_{1-x}Ga_xSe_2$ was deposited using three different sequences in which the temperatures for the four sources and the substrates were varied as well as the times for separate layers.





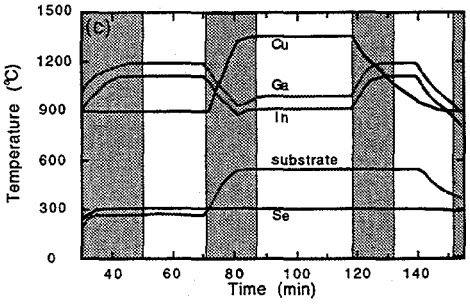


Figure 5. Temperature-time profiles for different deposition sequences of $CuIn_{1-x}Ga_xSe_2$ evaporation. Shaded areas show times when a shutter between the four sources and the substrates was closed.

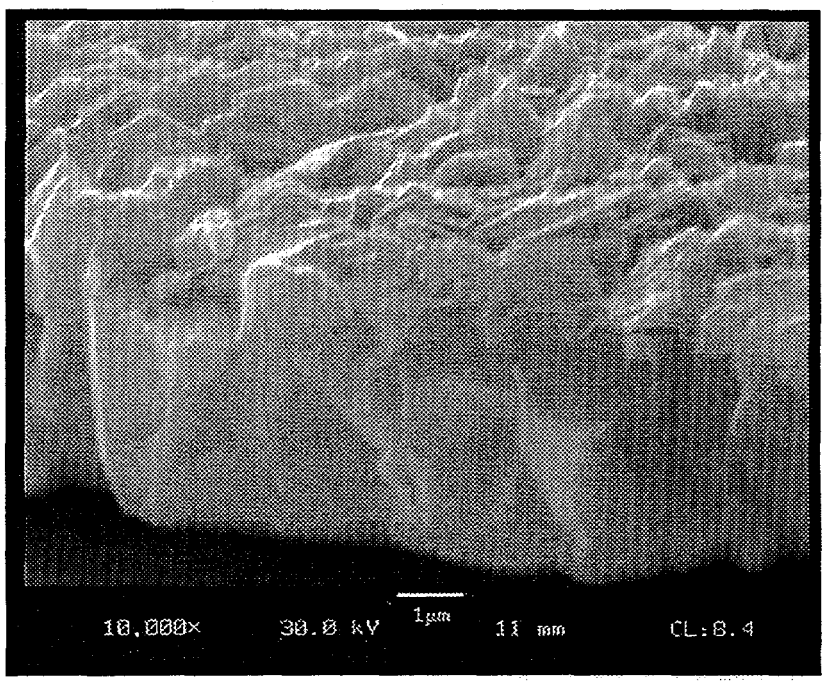
All processes included a final step with substrate temperature Tss ≥ 550°C and a substrate cool-down to Tss ≤ 400°C in the presence of a Se vapor. A shutter under one sample in each deposition is deployed to enable the composition to be measured after only the first 1 or 2 layers of a multi-layer deposition. Films are generally 2.5-3.0 μm thick.

The first sequence, shown schematically in Figure 5 (a), is a modified version of the Boeing bi-layer process developed for $CuInSe_2$ (7). This begins with a Cu-rich $CuIn_{1-x}Ga_xSe_2$ layer, with [Cu] >[In] + [Ga], deposited at Tss = 450°C, followed by a Cu-deficient layer achieved by increasing the In and Ga source temperatures while Tss is increased to 550-°C. A model for the growth of the $CuIn_{1-x}Ga_xSe_2$ starting from a Cu-rich layer has been proposed by Klenk et. al. (8). According to this model, the Cu-rich film consists of stoichiometric $CuIn_{1-x}Ga_xSe_2$ and Cu_xSe_y which, at T > 520°C, is primarily in the liquid CuSe phase. The CuSe phase is converted to $CuIn_{1-x}Ga_xSe_2$ with the arrival at the surface of In, Ga, and Se. The second layer then is used to reduce the total composition of the films to slightly Cu-deficient. The properties of the film may be improved by the high mobility of species in the liquid phase.

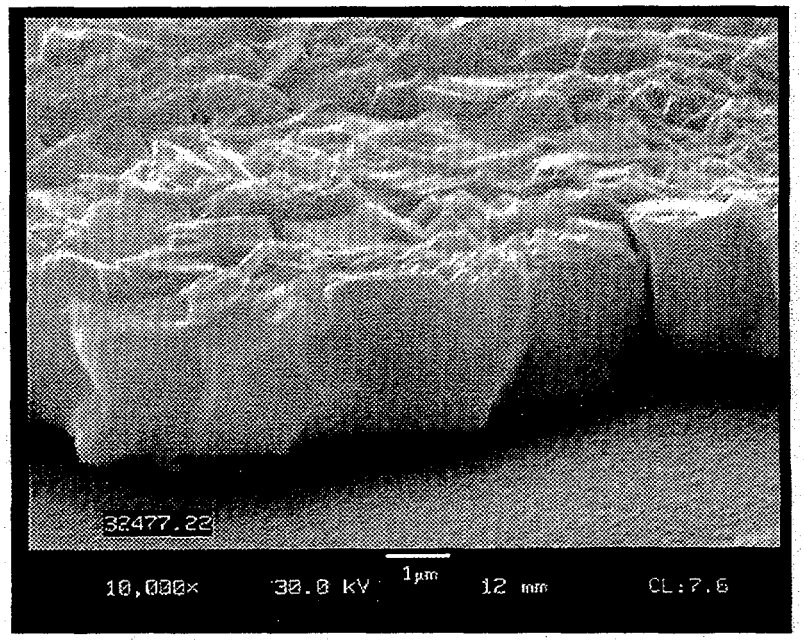
The second sequence, shown in Figure 5 (b), is a simplified version of the first with the same first layer followed by an In/Ga/Se layer deposited at 550-600°C to just convert the Cu_xSe_y to $CuIn_{1-x}Ga_xSe_2$. In this case, the In, Ga, and Se source temperatures are kept constant through both layers and the Cu source is just turned off. The Cu/(In+Ga) ratio can be varied by simply changing the relative times of the two layers. A possible advantage is that the absence of any Cu flux in the final layer of the run may encourage formation of a Cu deficient surface phase.

The third sequence is similar to the three-layer process described by Gabor et. al. (9). In this process, the first layer contains In/Ga/Se deposited at Tss ≈ 280°C. This is followed by a Cu/Se layer which is deposited at Tss = 550°C until the total film is Cu-rich, again containing a mixture of $CuIn_{1-x}Ga_xSe_2$ and Cu_xSe_y. The final layer is an In/Ga/Se layer deposited at 550°C to convert the Cu_xSe_y back to $CuIn_{1-x}Ga_xSe_2$.

The elemental composition of films from all depositions was determined by EDS measurements. These were performed with a 20 kV acceleration voltage and measure the composition of the top 0.5-1.0 μm of the film. The grain size of the films and their surface morphology were characterized by SEM and the morphology was further characterized with a Dektak surface profilometer. X-ray diffraction (XRD) was used to determine the relative orientation of the crystallites within the film and to evaluate the compositional uniformity. Scanning 2q XRD measurements were performed using standard Cu Kα radiation. The orientation of the films was determined from the relative intensities of the different diffraction peaks. Optical transmission and reflection and sheet resistance measurements were performed on samples deposited on bare glass substrates.



a)



b)

Figure 6. SEM micrographs comparing the grain size and surface of films deposited by (a) a bi-layer process with a Cu-rich first layer and (b) a tri-layer process with an In/Ga/Se first layer.

The primary means of characterization is done by fabricating devices on standard glass/Mo/ $CuIn_{1-x}Ga_xSe_2$ substrates. These are completed with CdS deposited by chemical bath deposition (CBD), sputtered ZnO:Al, and Ni contacts. The standard configuration has 6-9 cells on a substrate, each with 0.13 cm^2 active area. Results on the non-absorber layers are discussed in Section 2.2.2.

The morphology of $CuIn_{1-x}Ga_xSe_2$ films deposited by the three sequences shown in Figure 5 was compared by SEM and surface profilometry. SEM micrographs show that the first two sequences, which are bi-layer depositions with the same Cu-rich $CuIn_{1-x}Ga_xSe_2$ first layer, have similar grain size and structure. A typical film, shown in Figure 6 (a), has average grains ~1 μm across. In contrast a film grown with the three layer method from an In/Ga/Se first layer has slightly larger grains and a smoother surface as shown in Figure 6 (b). A relative measure of the surface morphology was obtained by scanning across the samples with a Dektak profilometer. These profiles are shown in Figure 7. Clearly, the films grown with the In/Ga/Se first layer have a much smoother surface.

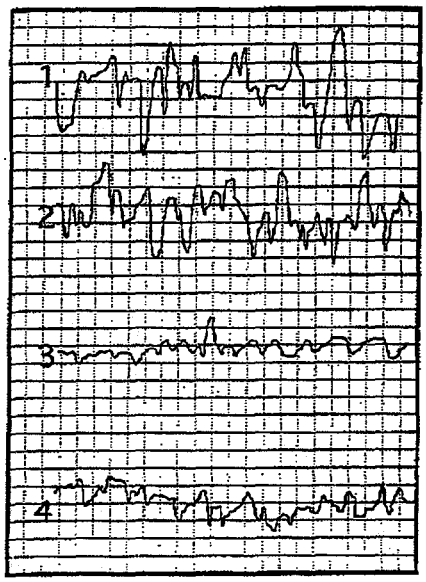


Figure 7. Surface profile scans of $CuIn_{1-x}Ga_xSe_2$ films showing a relatively smoother surface when the first layer is In/Ga/Se (3 and 4) than when the first layer is Cu-rich $CuIn_{1-x}Ga_xSe_2$ (1 and 2). Films were deposited by: 1) bi-layer sequence (a), 2) sequence (b) with no Cu in the second layer, 3) an In/Ga/Se layer followed by a Cu/Se layer, i.e. the first 2 layers of sequence (c), and 4) the complete 3 layer process of sequence (c).

Cell results with the three different deposition sequences are listed in Table 10. These cell results are all with no post-deposition heat treatment and no AR coating. Cell #32535.33 reached V_{oc}=0.62 V with 15.0 % efficiency with a 1 minute heat treatment at 200°C in air and an MgF_2 AR coating. The first two processes gave comparable results while the best cell with the three layer deposition has a lower V_{oc}. In general, it can be concluded that there is a wide latitude in the deposition method for fabricating $CuIn_{1-x}Ga_xSe_2$ cells.

Table 10. Cell results with three different $CuIn_{1-x}Ga_xSe_2$ deposition sequences as shown in Figure 5. Cells had no post-fabrication heat treatment and no AR coating.

Cell #	$CuIn_{1-x}Ga_xSe_2$ deposition	V_{oc} (Volts)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
32444.33	(a) 2-layer	0.60	31.9	71.1	13.5
32535.33	(b) 2-layer	0.59	32.5	72.4	13.8
32476.32	(c) 3-layer	0.53	30.6	72.4	11.7

Several variations in the $CuIn_{1-x}Ga_xSe_2$ bi-layer deposition with Cu-rich $CuIn_{1-x}Ga_xSe_2$ followed by an In/Ga/Se layer have been evaluated. These results can be compared to the model for the $CuIn_{1-x}Ga_xSe_2$ film growth discussed above. A set of $CuIn_{1-x}Ga_xSe_2$ films was deposited with the Se source temperature varied from 350 to 322°C to change the average Se effusion rate from the source, r (Se), from 57 to 11 mg/min. The Cu, In, and Ga rates were kept constant and Tss was 550°C for the second layer. This resulted in a change in the ratio of r (Se) /r (Cu) from 11 to 1.4. A ratio of 2 would be the minimum needed to provide sufficient Se for stoichiometric $CuIn_{1-x}Ga_xSe_2$ formation. The composition of these films, as determined by EDS, is plotted versus this ratio in Figure 8.

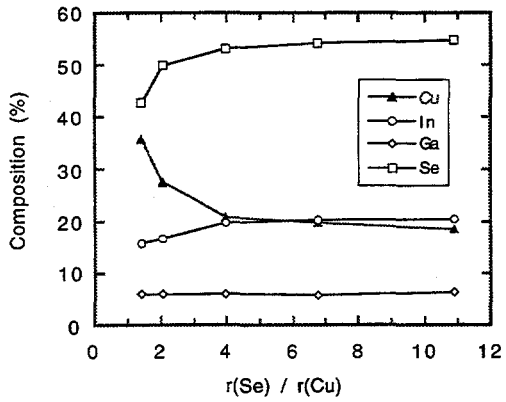


Figure 8. Variation of the Cu, In, Ga, and Se compositions, determined by EDS, in $CuIn_{1-x}Ga_xSe_2$ films deposited with varying Se effusion rate, r(Se), and constant Cu effusion rate, r(Cu).

The composition was fairly constant when there was excess Se, as r (Se) /r (Cu) increased from 4 to 11. At the lowest Se rates, when there was no excess Se available, the Cu content in the films increased sharply to 36% and the film surface had large defects. The increased Cu content in these films may be due to metal inclusions in the film. In addition, there may be formation of Cu_2Se rather than CuSe even at 550°C as a result of the Se deficiency. The reaction of In, Ga, and Se with the Cu_2Se to form $CuIn_{1-x}Ga_xSe_2$ may not proceed as rapidly as the equivalent reaction with CuSe. If the In and Ga form intermediate binary selenides, they may be more volatile with less Se available (10) resulting in the observed loss of In. The composition of the Cu-rich layer, measured independently on a shuttered piece, was not affected by the change in Se effusion rate, with ~28% Cu for r (Se) /r (Cu) = 2.0 or 7.8. Overall, there is a wide range of Se effusion rate which can be used to grow $CuIn_{1-x}Ga_xSe_2$ as long as there is sufficient excess. Standard deposition conditions used r (Se) /r (Cu) = 6-8, or a Se excess of 3-4 times what is needed for stoichiometric film deposition.

The effect of substrate temperature was evaluated by comparing films with the second deposition sequence in Figure 5 with Tss = 550 and 600°C for the second layer. The increase in Tss did not result in any apparent change in the composition, thickness, morphology, or film orientation although the optical transmission increased slightly at the higher Tss. The resistivity determined from 4-point probe measurements on a glass/$CuIn_{1-x}Ga_xSe_2$ monitor piece decreased from an average of 50 Ω-cm at Tss = 550°C to 20 Ω-cm at Tss = 600°C. This increase may be related to increased diffusion of Na impurities from the soda lime glass. Preliminary results of SIMS depth profiles completed at the University of Illinois show a higher Na level with the higher Tss, both in the Mo and in the $CuIn_{1-x}Ga_xSe_2$. Finally, while there was no conclusive improvement in cell performance, the highest efficiency was achieved with Tss = 600°C.

Several other modifications to the bi-layer deposition were evaluated. The standard process includes a cool down in the presence of Se vapor to Tss = 400°C. Runs were completed without this cool-down and with the cool down extended to Tss = 300°C. In each case, no difference in film properties were observed and there was no significant difference in device performance as shown in Table 11. A second modification was to close the substrate shutter between the A and B layers during process (a) in Figure 5. This allows Tss to reach 550°C, enabling complete formation of liquid CuSe, before the Cu-poor flux is introduced to the surface. Again, no difference in film or device results was observed.

Table 11. $CuIn_{1-x}Ga_xSe_2$ cell results with modifications to the $CuIn_{1-x}Ga_xSe_2$ deposition as listed.

Cell #	Process	V_{oc} (Volts)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
32459.33	standard bi-layer (a)	0.56	33	70	13.1
32460.23	Shutter closed - no Se vapor during cooldown	0.55	34	70	13.1
32466.23	Shutter open during cooldown to 300°C	0.54	34	70	12.9
32467.23	shutter closed btw. A & B	0.55	34	71	13.5

2.2.2 Non-absorber Layers

There are a large number of processing steps involved in the complete fabrication of a $CuIn_{1-x}Ga_xSe_2$ solar cell, even without the extra scribe steps needed for module interconnection. The basic steps are listed below:

1. determine non-float side of glass
2. break into 1"x1" substrates and mark them
3. polish glass
4. ultrasonic clean and rinse and hot air dry glass
5. examine glass, discard scratched or improperly cleaned substrates
6. deposit Mo by DC sputtering, store in desiccater
7. check adhesion, appearance of Mo
8. label substrates for absorber layer deposition, rinse and dry
9. deposit absorber
10. check composition of absorber by EDS, generally accept if $21 \leq Cu \leq 25\%$

11. deposit CdS by chemical bath deposition
12. dry substrate with 5 min, 120°C, heat treatment
13. deposit ZnO: Al by RF sputtering
14 deposit Ni contacts or Ni/Al grids by electron-beam evaporation
15. mechanical scribe to define cell areas
16. deposit MgF_2 anti-reflection layer by electron-beam evaporation

Significant questions remain about many of these steps. In particular, the substrate preparation and Mo deposition, the CdS deposition, and the ZnO deposition have been evaluated in detail.

2.2.2.1 Substrate Preparation and Mo Deposition

The critical issues addressed for the preparation of the glass/Mo substrate have been to provide good adhesion of the Mo to the glass and a surface relatively free of physical defects.

The glass used in this work is 1.0 or 1.5 mm thick float soda lime glass manufactured by Gloverbel in Belgium. The thicker glass is more resistant to warping at the high substrate temperature used for $CuIn_{1-x}Ga_xSe_2$ deposition. The thinnest float glass manufactured in the United States is 2.0 mm. Float glass has a residual thin tin-rich layer on one side from the manufacturing process which can be determined by its luminescence under the 254 nm UV radiation from a mercury lamp. We have found that the Mo adherence is better and more reproducible if deposited on the glass side without the tin layer. The most critical issues for adhesion of the Mo to the glass are the cleanliness of the glass surface and the deposition of the Mo in a manner which minimizes stress in the film.

Problems have occurred intermittently with the Mo deposition resulting in a hazy appearance caused by growth defects, which are typically ~1 μm, in the film. We have found that the defect growth is related to the glass preparation which must remove surface contamination from the manufacturing, shipping, and cutting processes. The standard glass cleaning has been an ultrasonic cleaning in a soap solution followed by an ultrasonic rinse in de-ionized water and a forced hot air drying. In conditions of low relative humidity, less than ~ 60%, this ultrasonic cleaning was sufficient to remove surface contamination and the hazy appearance of the films did not occur. However, in summer months when the relative humidity in the laboratory is typically >70% the hazy appearance occurred routinely. It has been reported that the adherence of surface contaminants to glass surfaces increase significantly as the humidity increases (11). There are many different methods of glass cleaning whose effectiveness depend on the size and nature of the surface contamination. In general, mechanical cleaning methods are considered superior to other methods including ultrasonic and chemical cleaning (12). When the glass is lightly polished with a 0.05 μm grit Al_2O_3 polish prior to the soap cleaning, the Mo growth defects were avoided and strongly adherent films were reproducibly obtained.

Adhesion of the Mo to the glass is also an intermittent problem and generally occurs after the deposition of $CuIn_{1-x}Ga_xSe_2$. When this occurs, the Mo films have wrinkles which indicate that it is under compressive stress. The Mo can also have fine cracks, indicating tensile stress, but this is not correlated with adhesion problems. Stress in the Mo can be controlled by varying the sputter pressure during the deposition (13). The objectives for the Mo film were to achieve good adhesion with sufficiently low resistivity, ρ. The maximum sheet resistance of the Mo depends on the cell configuration and specifically the lateral distance over which current must pass through the Mo. If this length is 1 cm, then a Mo sheet resistance of 0.2 Ω/□ will give a relative power loss of 0.1% for a typical $CuIn_{1-x}Ga_xSe_2$ cell. The objectives for the Mo were achieved with a bi-layer deposition in which a thin layer is sputtered with either the sputter pressure increased (14) or with

higher voltage between the glass and the bulk Mo film. As shown in Figure 9, ρ increases with sputter pressure.

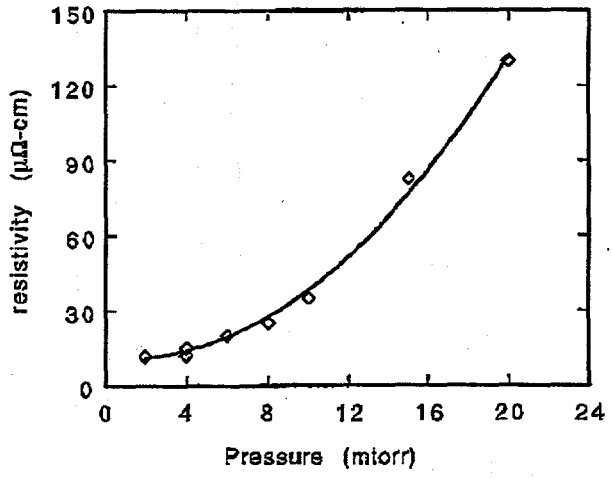


Figure 9. Resistivity of sputtered Mo films versus the sputter pressure.

The bulk ρ for Mo is 5.2 μΩ-cm so ρ for the films is higher by only ~3 times at the lowest pressures. In addition, the film stress goes from compressive to tensile as the pressure increases. The specific pressure values depend on the particular geometry of the system and other sputter parameters such as power. The standard bi-layer deposition has a first layer ~0.1 μm thick deposited at 16 mT to provide good adhesion to the glass. This is followed by a layer ~1 μm thick deposited at 3 mT to achieve a sheet resistance of the bi-layer ~0.2 Ω/□. This layer has good as-deposited adhesion, verified by tape-pull tests with mylar tapes of varying adhesive strength, and does not develop adhesion problems or stress cracks after the deposition of $CuIn_{1-x}Ga_xSe_2$ at Tss = 600°C. These properties could not be obtained with a single-layer film.

X-ray diffraction has shown that the orientation of the Mo has a direct effect of the orientation of the $CuIn_{1-x}Ga_xSe_2$ deposited on it, but there is no evidence of any correlation between the $CuIn_{1-x}Ga_xSe_2$ orientation and device performance. Two different sputtering systems have been used for the Mo deposition, one manufactured by CVC and one by Kurt Lesker. There are a number of differences between the systems in the both the geometry and deposition conditions. Films from the two systems have similar resistivity and adherence to the glass and no difference has been found in the performance of $CuIn_{1-x}Ga_xSe_2$ devices. However, X ray diffraction of the Mo films shows a clear difference in the degree of (110) orientation of the films deposited from the two systems. This is illustrated in Table 12 by two samples deposited with nearly identical $CuIn_{1-x}Ga_xSe_2$ deposition conditions on Mo films deposited in the two systems. The $CuInGaSe_2$ films both had $x \approx 0.30$ and devices fabricated on both pieces had $V_{oc} \approx 0.56$ V and efficiency ≈13 %. The Mo orientation is characterized by the ratios of the peak intensities of the two most prominent peaks, I(110)/I(211). The Joint Committee for Powder Diffraction Standards (JCPDS) value of this ratio for a randomly oriented Mo film is 2.6. So, while both films are preferentially (110) oriented, the film deposited in the CVC system is much more strongly oriented. Similarly, the $CuIn_{1-x}Ga_xSe_2$ orientation is characterized by the ratio I(112)/I(220). In this case the JCPDS value is 2.5 for x=0.3 The $CuIn_{1-x}Ga_xSe_2$ film deposited on the CVC Mo has a (220) preferred orientation while the film on the Lesker Mo has a strong (112) preferred orientation. This suggests that the more random orientation of the Mo provides a surface which more readily allows the $CuIn_{1-x}Ga_xSe_2$ to nucleate in its preferred (112) orientation.

Table 12. XRD peak intensities and ratios of the two most prominent Mo and $CuIn_{1-x}Ga_xSe_2$ peaks measured on $CuIn_{1-x}Ga_xSe_2$ films deposited on Mo films deposited in the different sputter systems. The JCPDS values for the normalized peak heights of a randomly oriented sample are listed for comparison.

Sample #	32394.33	32436.32	JCPDS
Mo system	CVC	Lesker	
		Mo peak intensities	
I(110)	4560	2410	100
I(211)	10	251	39
I(110)/I(211)	456	9.6	2.6
		$CuIn_{1-x}Ga_xSe_2$ peak intensities	
I(112)	881	36700	100
I(220)	846	397	40
I(112)/I(220)	1.0	92	2.5

Another aspect of the glass/Mo substrate is its ability to allow diffusion of Na and possibly other impurities from the glass into the $CuIn_{1-x}Ga_xSe_2$ film. SIMS results show similar levels of Na in $CuIn_{1-x}Ga_xSe_2$ films deposited at Tss = 600°C on Mo films deposited in the two different sputter systems.

In conclusion adherent Mo films with low resistivity have been deposited by a bi-layer process in two different sputtering systems which give a large difference in the relative (110) crystal orientation of the films. $CuIn_{1-x}Ga_xSe_2$ films deposited on these different Mo films in turn have a large difference in their relative (112) crystal orientation. Nevertheless, there is no apparent difference in device performance or in the diffusion of impurities from the glass through the Mo.

2.2.2.2 CdS Deposition

Two different CBD bath chemistries have been compared for the CdS deposition and have shown that the specific deposition chemistry can directly affect the electrical behavior of completed devices. $CuIn_{1-x}Ga_xSe_2$ cells were fabricated to compare CBD, CdS and ZnO deposition processes at IEC with those done at NREL. Cells were sent to NREL in pairs from the same $CuIn_{1-x}Ga_xSe_2$ deposition on which one piece had the CdS deposited at IEC. The other piece then had CdS deposited at NREL and all pieces had the bi-layer ZnO and Ni/Al grids deposited at NREL. Cell results for one set of samples are listed in Table 13 along with another sample from the same $CuIn_{1-x}Ga_xSe_2$ run which was fabricated entirely at IEC. The currents are low on the cells processed at NREL due to excessive absorption in the ZnO layer which apparently was not fully optimized at the time. The piece with the CdS deposited at NREL had the highest V_{oc} and fill factor. The cells with IEC CdS showed no significant differences with the ZnO deposited at either NREL or IEC. Differences in the ZnO deposition will be discussed below.

Table 13. $CuIn_{1-x}Ga_xSe_2$ cell results comparing different CdS baths and ZnO deposited at IEC and NREL. Cells contacted at NREL have area = 0.43 cm^2 with Ni/Al grids. Cells contacted at IEC have area = 0.13 cm^2 with Ni buss bars.

sample #	CdS bath	CdS deposition	ZnO and contacts	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
32442.33	1	IEC	NREL	0.578	26.6	70.7	10.9
32442.32	2	NREL	NREL	0.604	25.8	73.1	11.4
32442.23	1	IEC	IEC	0.572	31.1	70.0	12.5

The CdS deposited at IEC used a $CdCl_2$ based bath (Bath 1) (15). The NREL CdS is deposited from a $CdSO_4$ based bath (Bath 2) which is essentially the same as that developed by Kessler et. al. (16) .

The reactant concentrations and temperatures of the two baths are:

Bath 1: $[CdCl_2] = 0.001$ M
$[NH_4Cl] = 0.0025$ M
$[NH_4OH] = \sim 1.4$ M
$[(NH_2)2CS] = 0.01$ M
temperature = 85°C (constant)

Bath 2: $[CdSO_4] = 0.0015$ M
$[NH_4OH] = \sim 2$ M
$[(NH_2)2CS] = 0.15$ M
temperature = 40-70°C (ramped during deposition)

In addition to the different Cd salts, the baths differ in 3 distinct ways: 1) bath 1 is run at a higher temperature, while the temperature in bath 2 is ramped up during the deposition, 2) bath 1 uses a Cd/S ratio of ~10 while bath 2 has a ratio of ~100, and 3) bath 1 uses an ammonium chloride buffer. Both baths have a pH~10.5.

These two CdS baths are further compared in Table 14 for $CuIn_{1-x}Ga_xSe_2$ layers deposited in the same run with all layers deposited at IEC. Cell results are listed for an initial test after device fabrication is completed and after being heat treated for 1 minute in air at 200°C. The cells with the CdS deposited from bath 1 generally do not improve with heat treatment. However, cells from bath 2 improve significantly and consistently achieve higher V_{oc} after the heat treatment although J_{sc} decreases by ~0.5 mA/cm^2. The normalized quantum efficiencies of the two cells from run 32522 are plotted in Figure 10.

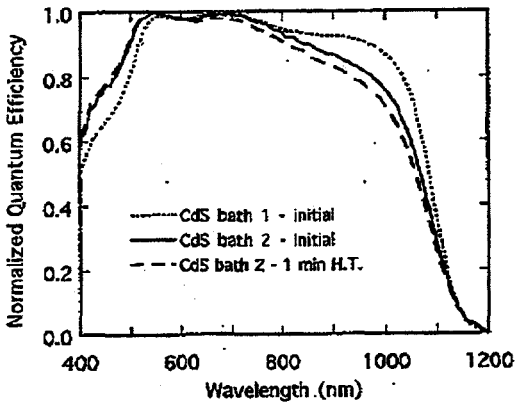


Figure 10. Quantum efficiencies of cells processed with different CdS baths. 32522.22 had CdS from bath 1 and 32522.23 CdS from bath 2.

The cell with the CdS from bath 2 has a lower response at long wavelength, which decreases even further with the heat treatment, and therefore the lower J_{sc}. The total collection length, L_{eff}, has been determined from the QE data using the method described below in Section 3.4.3. With CdS bath 1, L_{eff}=1.5 μm at 0 V while with bath 2, L_{eff}=0.9 μm before heat treatment and 0.7 μm after. This poorer long wavelength 0, collection maybe due to a greater effective carrier concentration, N_A, of the $CuIn_{1-x}Ga_xSe_2$ which causes a narrower region for field assisted collection and the lower value of L_{eff}. This can also explain the higher V_{oc} in this case since V_{oc}œAKT $\ell n\sqrt{N_A}$ capacitance measurements on the same cells show a lower doping density with bath 1 (see Figure 54).

In conclusion, a comparison of devices fabricated with two different CdS baths has shown several differences in the electrical behavior of the devides dependent on the CdS deposition. The differences in V_{oc}, long wavelength current collection, and capacitance suggest that the carrier concentration in the $CuIn_{1-x}GaxSe_2$ absorber is directly affected by the CdS deposition. Preliminary experiments to determine which aspect of the differences in these baths is responsible for the differences in doping have not been successful.

Table 14. $CuIn_{1-x}Ga_xSe_2$ cell results comparing different CdS baths and the response to post-fabrication heat treatment.

sample #	CdS bath	H. T. (min)	V_{oc} (V)	J_{sc} (mA/cm^2)	Roc (Ω-cm^2)	FF (%)	eff (%)
32522.22	1	0	0.513	33.7	1.8	67.0	11.6
32522.23	2	0	0.559	33.5	2.4	64.7	12.1
		1	0.572	32.7	2.0	67.3	12.6
32530.33	1	0	0.544	32.2	1.6	68.4	12.0
		1	0.542	32.1	1.7	67.5	11.8
32530.23	2	0	0.519	32.0	2.5	63.9	10.6
		1	0.587	31.5	1.8	69.7	12.9

2.2.2.3 ZnO Deposition

The ZnO is deposited in two layers with a high resistivity A-layer followed by a low resistivity B-layer. This is achieved by RF magnetron sputtering from a $ZnO/Al_2O_3(2\%)$ target with different compositions of the O_2/Ar sputtering atmosphere. The A-layer is deposited with 2.0% O_2 to give a sheet resistance of $R_{\square}$= $10^{-5}10^{-6}$ Ω/□ with thickness ~50 nm Then the B-layer is deposited with 0.2% O_2 to give a sheet resistance of $R_{\square}$ = 15Ω /□with thickness ~500 nm. An alternative method, is to deposit the high resistivity ZnO A-layer from an intrinsic ZnO target with no O_2 in the sputter atmosphere for this layer. The ZnO layers deposited at NREL in Table 13 were deposited this way and in combination with the CdS deposited at NREL produced the cells with the highest FF.

Cells with different thicknesses of the ZnO A-layer deposited from the doped target showed the cell performance to be insensitive this layer, even when it was eliminated entirely. The improvement reported by other groups (3) with the high resistivity ZnO layer was not observed and may depend on the CdS deposition, which in this case was from bath 1. Another set of samples to further evaluate the differences in ZnO depositions was fabricated using $CuIn_{1-x}Ga_xSe_2$ deposited at NREL with the CdS and ZnO deposited at either IEC or NREL and the CdS deposited by bath 2 in both cases. The cell with the ZnO A-layer deposited at NREL from an intrinsic target with no oxygen in the sputter gas had FF= 76% while the cell with ZnO deposited at IEC had FF=70%. There was no difference in Roc, the slope dV/dJ at V_{oc}, indicating no difference in series resistance. These results suggest that the ZnO deposition may also play a direct role in controlling the electronic behavior of the $CuIn_{1-x}Ga_xSe_2$ devices in conjunction with the CdS deposition and should be evaluated further.

2.3 CdTe FILMS AND DEVICES

The CdTe research effort was concentrated on issues relating to the fabrication of the CdS window layer, of the characterization of the CdTe deposition and post deposition processing and development of a CdTe back contacting process.

Investigations of the microstructure and composition of CdTe/CdS thin films deposited by physical vapor deposition (PVD) were continued so that parameters that limit efficiency in the PVD devices could be further identified and overcome. In particular, the loss in open circuit voltage obtained when thin (< 120 nm) evaporated CdS is employed can be explained by a combination of the effects of pinholes in the CdS layer and of CdS consumption during the $CdCl_2$ treatment. Chemical bath deposited (CBD) CdS films are shown to have a significantly lower pinhole density than evaporated CdS films but are harder to control chemically. CdTe and CdS film deposition conditions were varied to increase as-deposited grain size of both layers but the larger grains did not enhance device performance.

CdTe/CdS structures made by other research groups were analyzed in view of the processing perspective developed at IEC previously (17,18) in which CdTe microstructure and sulfur diffusion into CdTe during the $CdCl_2$ treatment were cited as a key component of CdTe/CdS device performance. A recent photoluminescence study of the junction region in CdTe/CdS devices made by different methods lends support to this view (19). The relationship between the extent of the interdiffused layer produced during the $CdCl_2$ heat treatment and device performance, however, remains to be determined. Investigations were thus initiated to study these effects by producing devices with $CdTe_{1-x}S_x$ layers deposited with S concentrations near the equilibrium miscibility gap concentration or deposited with a $CdTe_{1-x}S_x$ interlayer between the CdTe and CdS films.

Investigations of alternative halide treatments to replace the $CdCl_2$ treatment were continued and focused on post deposition heat treatments in HCl vapor. Promising structural modifications and device results were obtained with HCl treatments. It is believed that the experience and results obtained investigating vapor phase treatments such as $CdCl_2$ and HClwill lead to a CdTe deposition technology in which the halide treatment can be conducted *in situ* (during the CdTe deposition) thereby reducing the number of processing steps required.

A new contacting process for the CdTe back contact was developed and has been shown to produce fill factors on devices with high V_{oc} that are equivalent or superior to those obtained with other contacting methods. The process has been demonstrated on $CdTe_{1-x}S_x$ devices fabricated by different research groups and is compatible with module fabrication technologies.

2.3.1 Fabrication Process and Analytical Techniques

The process used to fabricate CdTe/CdS thin film solar cells is as follows:

1. Superstrate preparation
2. CdS deposition
3. CdS treatment with $CdCl_2$
4. CdTe deposition
5. CdTe treatment with $CdCl_2$
6. Contact formation

The details and variations on these steps are discussed in the sections below.

Analytical quantities used to characterize films and device structures and the techniques used to measure them are listed below:

1. Thickness: gravimetry, optical transmission, SEM cross-section.
2. Morphology: optical microscopy, SEM.
3. Grain size and structure: SEM, TEM (performed at NREL), XRD peak analysis.
4. Phase and compositional distribution: EDS, XRD precision parameter determinations, XRD peak modeling and analysis, SIMS (performed at NREL), XPS (performed at NREL).
5. Optical properties: optical transmission and reflection, spectral response of completed devices.
6. Device characterization Current-voltage-temperature (J-V-T) measurements, spectral response (SR), and capacitance.
7. Spatial device performance: light beam induced current (LBIC).

2.3.1.1 Superstrate Preparation

Indium-tin oxide (ITO) films on Corning type 7059 borosilicate glass were used as the superstrates for the work reported here. The films were deposited by RF sputtering in a stationary mode at a deposition rate of 17 Å/s to a thickness of 170-200 nm. Films of 17-23 Ω/□ were obtained by control of oxygen partial pressure during the deposition. As-deposited films are amorphous or weakly crystalline as determined by their x-ray diffraction patterns and have less than 4% absorption from 450 nm to 850 nm. Carrying the ITO films through the various stages of device processing, in particular the heating during CdS and CdTe depositions and post-deposition treatments, causes the ITO film to crystallize with negligible effects on the sheet resistance and the optical properties.

Optically the ITO films are planar and possess significant interference fringes in transmission and reflection. The reflection maxima of the combined ITO/CdS structure are not ideally located for optimal current generation in the devices (Figure 11). Use of textured superstrates or index-matching interlayers such as Al_2O_3 between the ITO and the glass could be employed to reduce the overall coherency or the specific reflection maximum located near 600 nm. Additionally, the extremely smooth surface of ITO may not be the ideal choice for best adhesion, but the smooth planar ITO surface is generally free of particulate defects and texture which might otherwise interfere with device operation.

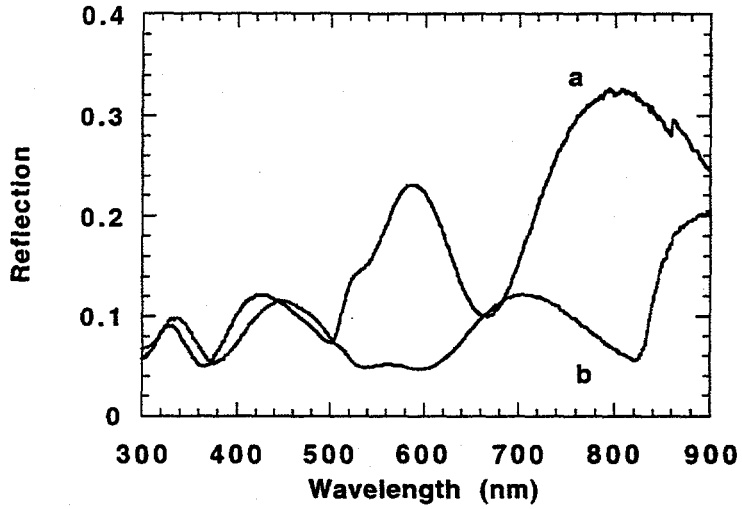


Figure 11. Optical reflection of a) 120 nm CdS/200 nm ITO/7059 and b) with an additional 5 μm of CdTe.

2.3.1.2 CdS Film Deposition - Evaporated Films

Undoped cadmium sulfide films were deposited by physical vapor deposition using high purity General Electric CdS powder which was evaporated from a boron nitride effusion cell at ~800°C. To evaluate the effect of CdS growth conditions on the properties of the layers and devices, films were deposited at substrate temperatures from 130°C (the temperature used in previous years) to 280°C. The growth rate was held in the range of 1 to 3 Å/s, resulting in deposition times of ~10 minutes for 120 nm thick films. Films from 50 nm to 350 nm were deposited, although the majority of films deposited for devices and contact development were 120 to 180 nm thick. The loss in Jsc attributed to parasitic absorption in CdS of this thickness is ~5 mA/cm^2, resulting in devices having J_{sc} values up to 21.5 mA/cm^2.

For device fabrication, the CdS films were heat treated with $CdCl_2$ to increase their grain size and improve their optical properties. The films were coated with ~0.15 μm of $CdCl_2$ by application of 10 drops per square inch of 0.1 wt % $CdCl_2$ in methanol and were subsequently dried. Heat treatment was carried out at 410°C in Ar/O_2 for 30 minutes. The $CdCl_2$ was rinsed from the surface with deionized water.

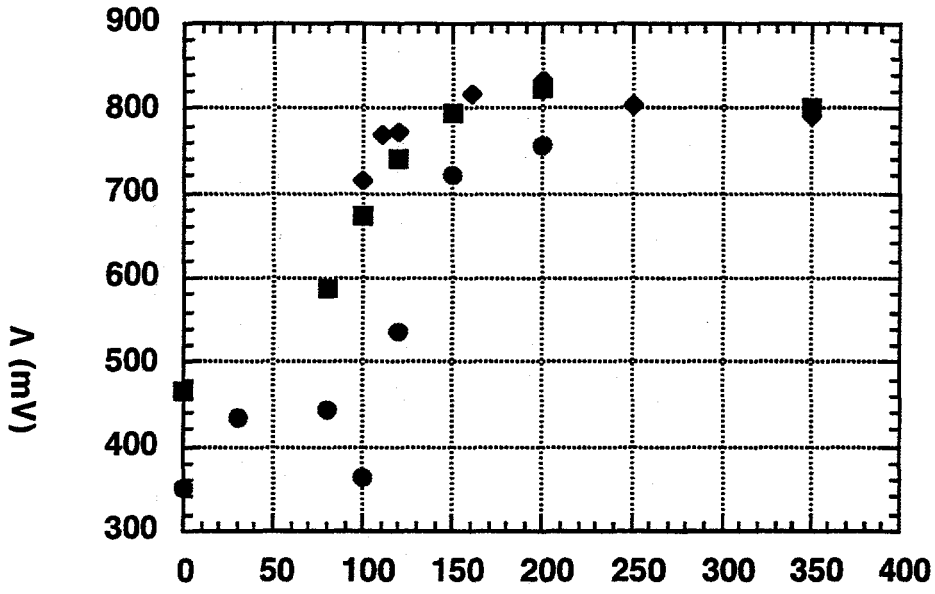


Figure 12. Maximum V_{oc} obtained on PVD CdTe/CdS devices as a function of CdS film thickness for the years ●-1992 ■-1993 and ◆-1994.

An ongoing difficulty encountered using evaporated CdS films is a falloff in the open circuit voltage of devices with CdS thinner than about 150 nm. Figure 12 shows the maximum V_{oc} achieved versus CdS thickness for devices fabricated in previous years (1992-1994). In the 1992 data set, the falloff occurred for devices with CdS thinner than 200 nm. Processing refinements such as shorter heat treatment times, which reduce the loss of CdS due to interdiffusion, allowed high V_{oc} to be maintained with thinner CdS, but the falloff thickness was still unacceptable. Explanations for the falloff include spatial non-uniformity in the CdS due to the $CdCl_2$ processing and the existence of discontinuities such as pinholes in the thinner CdS layers. To address this issue the microscopic condition of the films was assessed quantitatively by optical microscopic surveys for pinholes and surfacial debris. Pinhole surveys were conducted by back illumination of the films with blue light obtained by passing the microscope illuminator light through a 400 nm bandpass filter. This increased pinhole contrast, especially on very thin (<120 nm) CdS films, since the CdS film absorbs most of the blue light and appears dark; pinholes thus appeared white against a grey-black background. For the surveys three strips 0.1 cm x 2.4 cm were examined, encompassing a survey area of 0.72 cm^2 representing 14% of the total film area. Projection of the survey regions onto a television screen with a transparent scale allowed pinholes to be counted by size, thereby permitting semi-quantitative area reductions to be performed. Pinholes were grouped by diameter: 10-20 μm, 20-50 μm, 50-100 μm. The average area in each group was estimated and these were added to give a total area lost to pinholes for each survey.

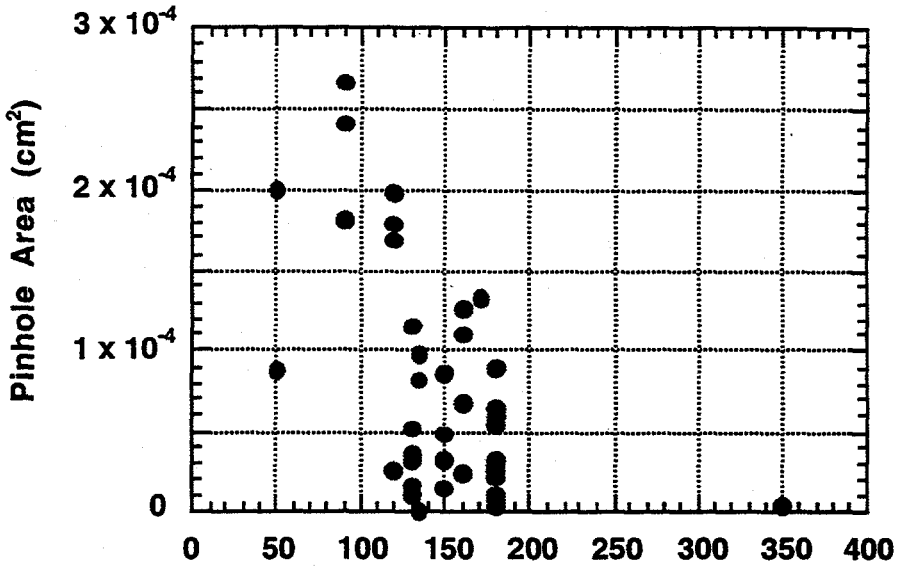


Figure 13. Total pinhole area versus CdS film thickness based on 0.72 cm^2 survey area.

The results of the pinhole survey are shown in Figure 13 for all of the evaporated CdS films examined, spanning thickness from 50 to 350 nm. Within each thickness group there are examples with high and low pinhole area density, but the overall trend of maxima and minima suggests a strong thickness dependence for films thinner than 200 nm. The implication is that the V_{oc} of a device can be reduced by the parallel junctions of CdTe/CdS and CdTe/ITO. The latter structure is known to produce devices with V_{oc} ~ 400 mV. For 100 nm thick films in Figure 13, there were roughly 30 pinholes per cm^2 greater than 10 μm, and the total pinhole area was ~2 x 10^{-4} cm^2 which amounts to 0.03% of the total film area. This may be sufficient area to account for the V_{oc} falloff observed as CdS thickness is reduced below 150 nm. Note that this pinhole area, which may be sufficient to reduce V_{oc} in devices, is significantly less than can be observed by standard parallel-beam optical transmission measurements. The $CdCl_2$ treatment did not reduce or increase the pinhole density on any films measured. Utilization of evaporated CdS less than ~120 nm will depend on successful reduction of the pinhole density.

To attain the highest crystalline quality in as-deposited CdS films, the substrate temperature at which the films were deposited was increased from the baseline of 130°C to 280°C. To keep the growth rate constant, within the range 1 to 3 Å/s, the source effusion rate was also increased to compensate for re-evaporation of Cd and S. Above 280°C it was not possible to obtain uniform CdS deposits in the 100-200 nm range at reasonable effusion rates. X-ray diffraction measurements of the full width at half maximum (FWHM) of the (002) diffraction peak of CdS films ~150 nm thick show a decrease in FWHM with increasing substrate temperature, indicating larger average particulate size (Figure 14). The instrumental broadening is ~0.1 deg and constitutes the ordinate in the figure.

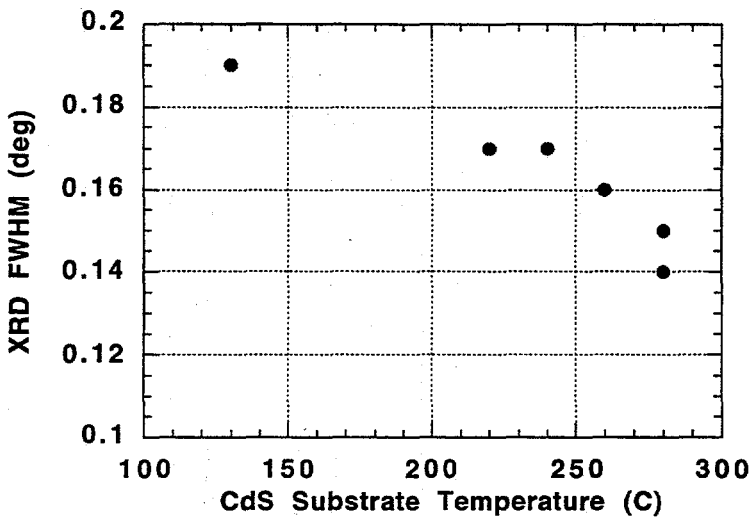


Figure 14. XRD FWHM versus CdS film thickness for evaporated CdS films. The instrumental FWHM is ~0.1 deg.

The improvement in average grain size as inferred from the diffraction measurements is consistent with reduced optical scattering in the films as is suggested by the normalized optical transmission curves for three of the films, grown at 180°C, 240°C, and 280°C, shown in Figure 15. No systematic effect on pinhole density with growth conditions was found other than the thickness relation described above. Following $CdCl_2$ processing, both the XRD FWHM and optical spectra of all films were identical. Devices with Cu/Au contacts achieved V_{oc} exceeding 800 mV using evaporated CdS deposited at 180°C (40807.31: V_{oc} = 817 mV, FF = 69.2%) and 240°C (40808.32: V_{oc} = 812 mV, FF = 71.5%). Thus it may be concluded that use of the $CdCl_2$ treatment of the CdS layer somewhat mitigates the need to deposit high quality as-deposited CdS films.

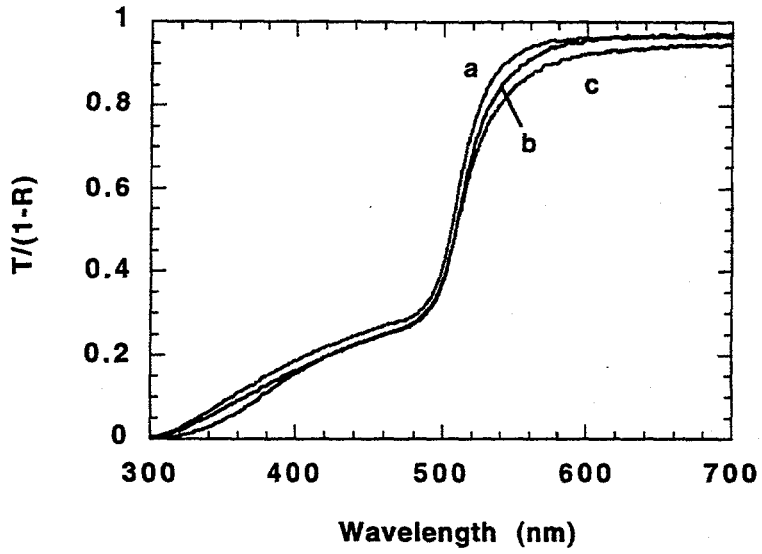


Figure 15. Normalized optical transmission, T/(1-R), of 120 nm thick evaporated CdS films deposited at substrate temperatures of: a) 280°C, b) 240°C and c) 180°C.

2.3.1.3 CdS Film Deposition - Chemical Bath Deposited Films

CdS films were grown in an aqueous solution consisting of a Cd ions, a salt, and thiourea as a source of sulfur. NH_4OH was added to bring the solution to a pH near 9.5. Typical reactants and concentrations were 0.001M $CdCl_2$, 0.0025M NH_4Cl, 1.3M NH_4OH and 0.01M $(NH_2)_2CS$. All reactants except for the last, thiourea, were mixed in a partially covered beaker and heated by a temperature-controlled hot plate. During the heatup period, glass or ITO/glass substrates were suspended in the solution by plastic clips. Thiourea was added only after the solution reached the desired reaction temperature (75-90°C). The solution was constantly stirred. Under the typical conditions listed above and at 85°C, the solution begins to obtain a yellow color after one minute, and CdS grows on the substrates at a rate of roughly 10 nm per minute for the first 12 minutes. After this time, the growth rate decreases dramatically due to increasing homogeneous CdS formation in the bath. Depending on the reaction rate and desired film thickness, films were removed from the bath after 3 to 20 minutes and rinsed by flushing with cool DI water. To grow films with thicknesses greater than 140 nm it was necessary to use a second bath.

The surfaces of the CBD CdS films were specular; individual grains were too small to be revealed by SEM. SEM and optical microscopy show that the surface is speckled with particles of up to 1 μm in diameter which are believed to be CdS particles that homogeneously nucleated in the bath and subsequently became attached to the film surface. Rinses in flowing water and ultrasonic dips in hot water failed to remove the particles, although wiping the surface with a vinyl glove removed the majority of the particles. After $CdCl_2$ treatment (discussed below), the average density of pinholes with diameters > 10 μm was found to be roughly 6 holes/cm^2 as compared to 30 for evaporated CdS films. For CBD films, roughly 0.005% of the area was occupied by pinholes, which is a factor of ten less than the pinhole area obtained on evaporated films of the same nominal thickness.

Similar to evaporated CdS films, the optical transmission spectra of as-deposited CBD CdS films feature a "soft" band edge. This may be due to scattering effects associated with the small grain size and structure, to the presence of contaminants in the film, or to the presence of some cubic

phase CdS. EDS performed on the films failed to detect contaminants (the dectability limit is ~1% for most elements). The films were generally too thin for XRD to detect the presence of cubic CdS as has been observed by others using similar bath chemistry (23).

Various heat treatments were performed on CBD CdS films in an effort to improve the optical and structural properties. Treatments in air, hydrogen, argon, 20% O_2 in Ar, and 4% H_2 in Ar at temperatures between 415 and 550°C all caused the optical band edge of the films to soften and to make the films appear darker than the as-deposited film. It was found, however, that treatments in 20% O_2 in Ar in the presence of $CdCl_2$ (IEC's "standard $CdCl_2$ pre-treatment" used on evaporated CdS films) sharpened the band edge making the optical quality of the films comparable to $CdCl_2$-treated evaporated CdS. The same qualitative results were found regardless of whether the solution used to grow the film was based on a chloride, sulfide, or acetate salt. Figure 16 shows transmission (corrected for reflection) of an as-deposited film, a film that received heat treatment in the presence of $CdCl_2$, and a film that received the same heat treatment but without $CdCl_2$. For the AM1.5 global standard solar spectrum, it is calculated that the increase in photon current that will pass through the $CdCl_2$ treated film compared to the as-deposited film is 0.5 mA/cm^2. As will be discussed later, there is also a correlation between the sharp band edge and higher V_{oc}.

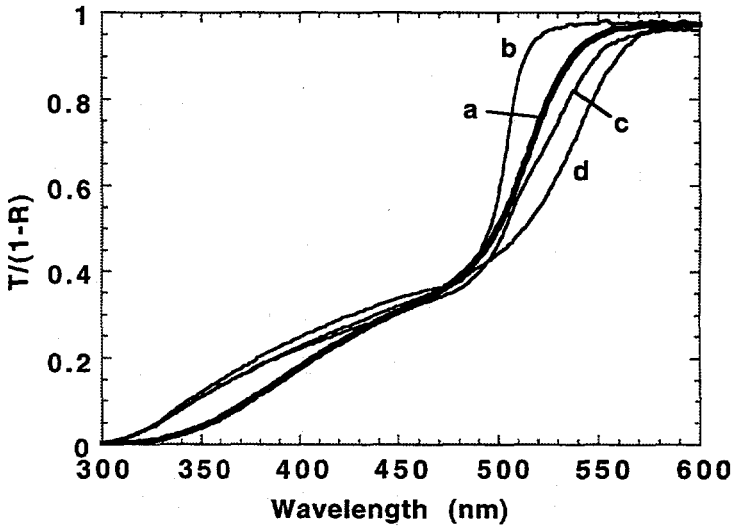


Figure 16. Normalized optical transmission, T/(1-R), of 120 nm thick CBD CdS films: a) as-deposited, b), c) treated at 400°C in air with $CdCl_2$ and d) heat treated at 400°C in air without $CdCl_2$.

Results of the $CdCl_2$ pre-treatment on CBD CdS have not been consistent. For example, the two films of Figure 16 were grown in the same bath, were both about 100 nm thick, and had nearly identical as-deposited transmission spectra. After $CdCl_2$ treatment, however, one film was uniformly yellow and featured a sharp band edge, while the other film contained some yellow areas and a large darker region which resulted in a soft band edge. Such inconsistent results were observed with films that were 220 nm thick, and occurred when the $CdCl_2$ concentration was increased tenfold. Sometimes a second $CdCl_2$ treatment would succeed in removing the darker regions and create a sharp band edge, and sometimes a second treatment would not. These results show that the concentration of $CdCl_2$ and heat treatment time are not critical parameters. Because

of this, and because the $CdCl_2$ treatment has never failed when applied to CdS films grown by evaporation, we believe the inconsistent results are due to inconsistencies in the CBD process rather than in the $CdCl_2$ treatment.

Of devices made from CBD CdS films, nearly all had V_{oc}'s of 600-750 mV and fill factors of 45-65%. The control devices made from evaporated CdS films also had performances in this range which was lower than typical. In some cases, cells made from CBD CdS performed better than the corresponding control cells. J_{sc}'s were consistent with the estimated thickness of the CdS. Unfortunately, variations in the performance of different cells scribed on the same sample (discussed below) made establishing correlation between CdS preparation technique and device performance very difficult. No devices made with CdS thicknesses of 70 nm or less had $V_{oc} > 600$ mV. Devices with voltages as high as 750 mV were made with CdS films the were estimated to be only 90 nm thick.

Laser beam induced current (LBIC) studies revealed that regional differences in material quality rather than the presence or absence of point defects such as shunts were responsible for the observed variation in performance between devices scribed on the same substrate. The higher quality regions were invariably near the edge of the samples. Cells scribed in the higher quality region had V_{oc}'s up to 150 mV higher, and, often, higher J_{sc} and fill factor. In order to determine if the low quality regions could be correlated to the darker areas of the CdS that sometimes appeared after the $CdCl_2$ pre-treatment, the dark regions of several films were accurately sketched, then these films were processed into cells. On each sample, one large cell (2cm x 2cm) was scribed to allow LBIC scans of the entire sample. LBIC showed that regions of poor collection closely match the dark regions of the CdS. Figure 17 shows the LBIC surface of one of these cells biased near V_{oc}. In this case, the region of poor collection is revealed in forward bias, but not under short circuit conditions. It should be noted that higher quality regions near the edges were noted even on some cells made from CBD CdS films that did not have a darker region. Since control cells made from evaporated CdS showed no such dramatic regional variations, it is believed that the variations arise from inconsistencies in the CBD process such as mixing in the CBD bath.

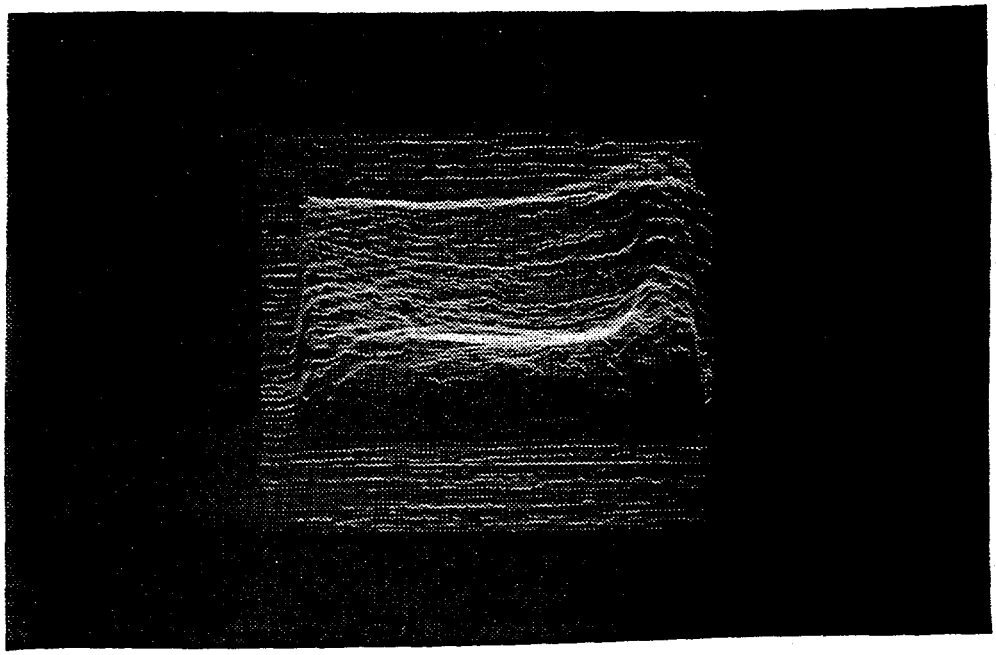


Figure 17. LBIC photograph of CdTe/CdS device #40835.12 with CBD CdS with a voltage bias of + 0.75 V.

2.3.1.4 CdTe Film Deposition

Undoped CdTe films were deposited by PVD from a boron nitride effusion source using 100 mesh (120 μm particle size) CdTe powder prepared by grinding and sieving 99.999% pure CdTe ingots from Alfa/Johnson Matthey. As with the CdS evaporated films, depositions were carried out at higher temperatures and different thicknesses to evaluate the effects, if any, of nucleating the films at higher temperatures within the limits of the capability of the deposition system. Growth rates were kept in the range from 5 to 8 Å/s, and substrate temperature was increased in selected runs from the baseline temperature of 250°C to 350°C. 350°C is near the maximum substrate temperature that can be used in the evaporator to produce CdTe films. The typical CdTe effusion rate needed was 25 mg/min, but higher effusion rates were needed for higher substrate temperatures to maintain the growth rate. At effusion rates > 50 mg/min however, the effusion source is depleted before a significant deposit is obtained.

As-deposited CdTe films exhibit visible grain facets which were characterized using the intercept method from SEM micrographs. Transmission electron micrographs of PVD film cross section performed at NREL in 1993 had confirmed that surface facet dimension is a good indicator of grain size within the CdTe films. The only correlation found for the facet dimension was that both the average and maximum facets observed on the CdTe surface increased roughly with film thickness, independent of growth rate or substrate temperature (Figure 18). No correlations were observed between facet dimension and device parameters. For devices, the nominal film thickness employed was 4-6 μm.

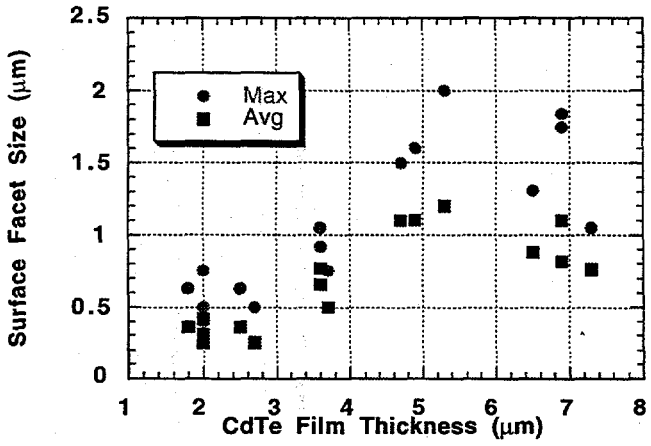
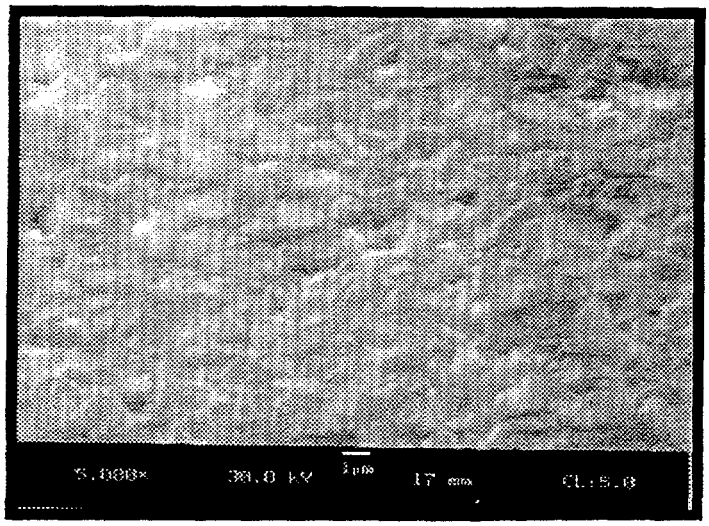


Figure 18. Plot of CdTe facet size versus film thickness.

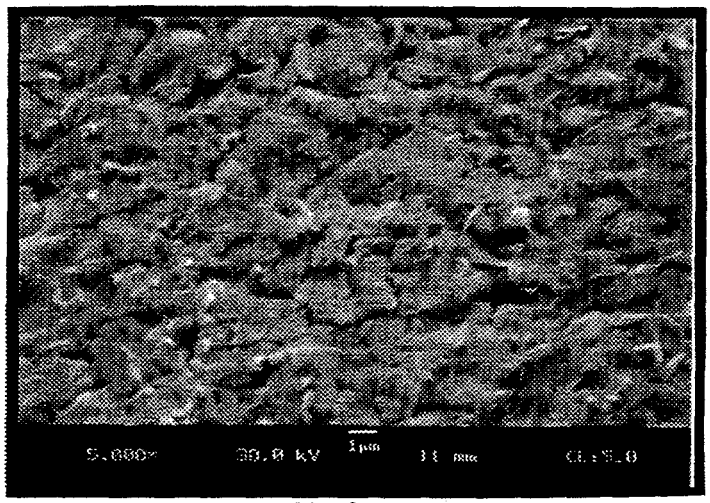
2.3.1.5 Post Deposition Processing

Device fabrication of CdTe/CdS films is completed by heat treating the structure with $CdCl_2$, rinsing and forming a contact. The $CdCl_2$ heat treatment is the same as was described in the report for the previous year (17).

Figure 19 is a scanning electron micrograph of the surface of a 5 μm thick CdTe film before and after the $CdCl_2$ treatment showing the grain enhancement obtained by the treatment.



a) before



b) after

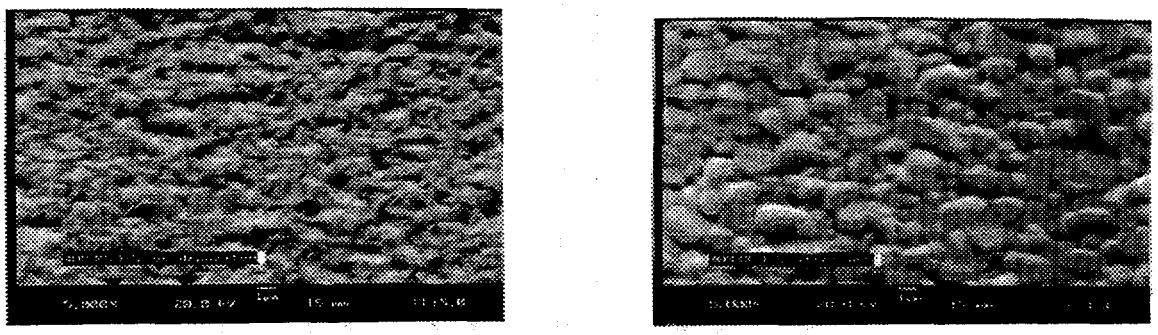
Figure 19. SEM micrograph of surface of 5 μm thick CdTe film a) before and b) after standard $CdCl_2$ treatment at 410°C in Ar/O_2 for 12 minutes.

2.3.1.6 HCl Vapor Treatment

In earlier work (17) physical results were presented for CdTe/CdS films treated with other halide systems showing that grain enhancement and lattice parameter shifts could be produced by treatment with various surface compounds such as $CdBr_2$ or in various vapor ambients such as $CdCl_2$, HCl, and $HgCl_2$. Subsequent work focused on treatment in $CdCl_2$ vapor (18) and in chlorine vapor. The $CdCl_2$ vapor was found to be very effective at promoting grain growth, left no detectable surface residue on the CdTe, and produced devices with uniform performance at the 10% efficiency level. Treatment in chlorine vapor was found to convert the surface of CdTe to $CdCl_2$ plus elemental Te which, in the concentration range examined, was destructive to the CdTe film integrity. In this period, experiments were begun to examine the feasibility of using HCl vapor to controllably treat the CdTe/CdS films for device fabrication. Such a process is envisioned to be simpler (fewer processing steps) than the surface $CdCl_2$ treatment and may be implemented within the deposition environment.

The preliminary treatments of CdTe/CdS structures in HCl gas were conducted in a quartz tube reactor and tube furnace at atmospheric pressure by transporting HCl across the heated CdTe/CdS

samples with an argon or argon/oxygen carrier gas bubbled through a column of concentrated $HCl:H_20$ solution. A lower bound on the average HCl concentration in the carrier gas was estimated by titration of the contents of a scrubber located downstream from the reaction chamber. Reactions were carried out by: 1) purging the samples for 30 minutes with HCl/Ar or $HCl/Ar/0_2$ with the samples located at the edge of the tube furnace (T ~ 100°C); 2) transferring the samples to the hot zone (T ~ 400°C); and 30 removing samples to the edge of furnace after the prescribed reaction time. No attempt was made to desiccate the vapor stream.



a) before b) after

Figure 20. SEM micrograph of surface of 5 μm thick CdTe film: a) before and b) after HCl treatment at 410°C in Ar for 30 minutes.

For films, reacted in 4% HCl/96% Ar at 400°C for 30 minutes, grain growth was observed, resulting in grain sizes up to 2 μm for 5 μm thick CdTe films as shown in SEM photographs (Figure 20). The grain size was larger at higher reaction temperatures, reaching a maximum size of 8-10 μm for films reacted at 450°C. EDS measurements did not indicate the presence of any chloride residues on the films reacted in HCl/Ar, nor was there a change in the ratio of Cd to Te EDS peak intensities.

For films reacted with oxygen added to the carrier gas, grain growth was not apparent from SEM images due to the formation of a surface layer that EDS showed to contain a significant chloride component. Rinsing the samples in deionized water removed this chloride layer, leaving a surface which was slightly Te-rich. This is summarized in Table 15 which shows the change in EDS count rate for Cd, Te, and Cl obtained for a sample treated in 4% HCl/48% Ar/48% 0_2.

Table 15. EDS count rates for Cd, Te and Cl on CdTe/CdS (40840.32) before heat treatment, after heat treatment at 400°C for 30 minutes in $HCl/Ar/0_2$ and, and after rinsing in deionized water.

Sample Conditions	Raw Count Rate cps			Raw Te/Cd Ratio
	Cd	Te	Cl	
As-deposited	226	149	0	0.66
Heat Treated	264	217	51	0.82
Rinsed	198	182	2	0.91

The reaction between the CdTe layer and the vapor is significantly altered by the addition of oxygen. Previous experience with $CdCl_2$ surface and vapor treatments have shown that the addition of oxygen during the treatment is essential to obtain high performance. A comparison of devices made with CdTe/CdS treated in HCl with and without additional oxygen suggests similar sensitivity as shown in Table 16. Also shown is a device processed with the standard $CdCl_2$

surface treatment which takes place in an oxygen containing ambient. The sample treated with no additional oxygen has a lower open circuit voltage and fill factor; its fill factor is dominated by series resistance in the light and dark J-V curves, which together with the lower V_{oc} may indicate lower conductivity in the CdTe layer.

Table 16. Device performance obtained for CdTe/CdS films reacted in 4% HC1/96% Ar and 4% HC1/48% Ar/48% 0_2.

Sample	Ambient	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF %
40837.32	HC1/Ar	675	~20	53
40845.32	HC1/Ar/O_2	710	20.5	65
40840.32	HC1/Ar/O_2	725	~20	62
40845.21	$CdC1_2$ Surf	810	19.8	63

2.3.1.7 CdTe Post-deposition Processing Perspective

The characterization of PVD CdTe/CdS structures under different processing conditions has led to a phenomenological model consistent with the observed effects of processing on the physical properties of the individual layers. Including data obtained from materials made by different methods allows us to establish a unified perspective applicable to all moderate to high efficiency device structures. The goal is to develop a common framework and then to identify performance limiting quantities.

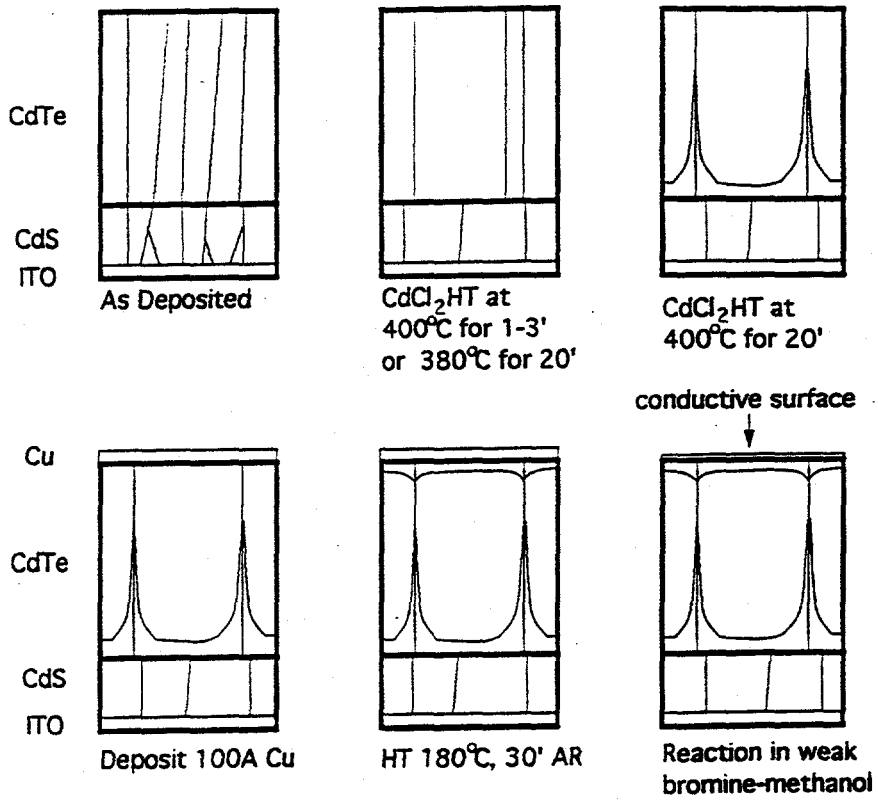


Figure 21. Cross section schematic of CdTe/CdS structures at different stages of post deposition heat treating and surface preparation for contact formation.

The phenomenological model is represented in Figure 21 for PVD devices. It depicts schematically the key physical and chemical features of the composite film at various stages of processing. This interpretation is consistent with the microstructural and compositional measurements mentioned above on device structures after CdTe deposition, $CdCl_2$ processing, and contact formation (20). As-deposited structures exhibit sharp interfaces and heteroepitaxial formation of CdTe on CdS. The CdTe-CdS lattice mismatch induces tensile strain in the CdTe layers. A short (1 to 3 minute) treatment at 400°C or above with $CdCl_2$ promotes independent grain recrystallization in the CdTe and CdS layers accompanied by relaxation of strain in the CdTe layer and interdiffusion between the CdTe and CdS. Treatment at temperatures below 400°C but for longer times produces similar effects. Increasing the treatment time to 15-30 minutes above 400°C promotes further enhancement of the CdTe grain size but also results in interdiffusion between the CdTe and CdS layers (lattice parameter progressively less than 6.481 Å).

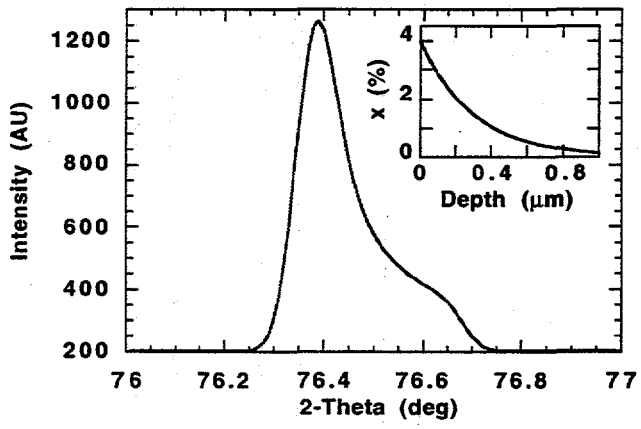


Figure 22. Computer generated XRD spectrum of the $CdTe_{1-x}S_x$ (511) peak for 1 μm thick $CdTe_{1-x}S_x$ film with an exponential S concentration, x, (mole %) specified by the profile shown.

For PVD devices the highest efficiency devices are obtained on material in which there is measurable interdiffusion, i.e., material treated for > 5 minutes at T > 400°C. Little or no interdiffusion is detected on samples treated below 400°C. Time-progressive lattice parameter measurements are consistent with S diffusion from the junction and along grain boundaries into the CdTe grains according to an exponential or similar concentration gradient as indicated by the computer generated composition profile and CdTe (511) XRD spectrum in Figure 22. The existence of elevated S concentrations near grain boundaries and at the CdTe/CdS interface was confirmed previously by TEM and micro-EDS measurements (18) and more recently by near-junction photoluminescence (19). In addition, oxygen from the heat treatment atmosphere was shown by SIMS studies to penetrate into the CdTe (43), and is believed to cause the CdTe layer to become weakly p-type by a mechanism that is not yet understood (23). Residual chlorine has also been detected in heat treated samples, with the maximum concentration located near the CdTe surface.

Devices are completed by one of several processes that provide a p-type dopant for the near-surface region of the CdTe and form a non-rectifying contact. The exact mechanism of the enhanced p-type doping attributed to dopants such as Cu or oxygen is not yet understood, but one idea is that the grain boundary walls and top surfaces become p+ which, for columnar grain structures, will repel minority carriers and reduce minority carrier recombination (24). One contacting process,

developed this year and described in detail below, features a Cu diffusion step followed by a Cu metal removal step prior to application of a current carrying material.

The above phenomenological model appears to be consistent with measurements made on films produced using diverse CdTe/CdS structures from other laboratories used to make devices with efficiency greater than 11%. In the past two years we have measured the physical properties of CdTe/CdS structures used to make high efficiency devices made by the different processes to provide comparative information about film thickness, grain size, orientation and composition as shown in Table 17. The mean grain size was determined from surface SEM micrographs; the average S content in the CdTe layer was estimated by reduction of the precision lattice parameter; and the orientation is the XRD intensity ratio of the (111) and (220) reflections. A notable feature of the table is that the CSS films which have the highest V_{oc} are very strongly oriented along the (111) crystallographic axis. This significant difference may be evidence that control of the interfacial chemistry and nucleation may be critical to device operation, and that the condition of the CdS surface at the start of the CdTe film formation in the CSS process could be a key to producing excellent junction characteristics on ultra thin CdS.

2.3.1.8 $CdTe_{1-x}S_x$

IEC has initiated experiments to intentionally modify the CdTe-CdS surface *in situ* prior to CdTe deposition. It is our intention to produce $CdTe_{1-x}S_x$ interlayers and layers spanning compositions above and below the CdTe-CdS equilibrium miscibility gap. The compositional profiles of the films before and after the $CdCl_2$ treatment will be measured and devices will be made and analyzed.

Table 17. Physical parameters measured at IEC on $CdCl_2$ treated CdTe/CdS structures made by different methods and the maximum V_{oc} obtained with small-area cells (< 1 cm^2). The % S is the value of x in $CdTe_{1-x}S_x$ expressed in percent. Deposition processes are represented: sp= spray pyrolysis (Golden Photon); PVD = physical vapor deposition (IEC); CSS = close spaced sublimation; (University of South Florida); EVD = elemental vapor deposition (Solar Cells, Inc.); ALE = atomic layer epitaxy (Micro chemistry). The samples are listed in order of decreasing CdTe film thickness.

Sample No.	Deposition Method	CdTe Thk (μm)	Mean Grain Size (μm)	%S	Orientation I(111)/I(220)	MaxV_{oc} (mV)
9107.1	SP	6	5-10	8	1.4	783 (9)
40839.11	PVD	5	2-4	2	0.6	830 (11)
1075	CSS	5	2-4	<1	55.5	854 (12)
N1941CD	EVD	5	2	<1	0.9	825 (13)
Y174A4	ALE	2	1	1	1.0	804 (14)

Employing alloy interlayers is expected to reduce the S diffusion rate from the CdS layer which may allow thinner layers to survive the post-deposition processing. In addition, such an interlayer may relax the strain in as-deposited PVD films induced by the CdTe-CdS lattice mismatch. The effects of growth rate for a fixed substrate temperature will be evaluated with respect to the as-deposited strain issue; higher growth rate may reduce the heteroepitaxial growth mode observed in PVD films.

The present status of this project is that a CdS effusion source has been added to the CdTe deposition system and calibrated for effusion rate and spatially variant deposition rate. One run with simultaneous CdTe and CdS deposition has been performed at 150°C substrate temperature. XRD lattice parameter analysis of the 3-4 μm thick films obtained indicated films with single alloy composition, varying in composition across the substrate array from 2.4 to 11.7% S content in $CdTe_{1-x}S_x$. The spatial dependence of S content corresponded generally to the independently measured distribution of the CdS flux in the deposition chamber and is shown in Figure 23. The computer model used to generate Figure 12, which is similar to another model developed for thin film XRD analysis (10), will be used to non-destructively assess the mole fraction of different $CdTe_{1-x}S_x$ alloy compositions within a film. XRD results will be combined with optical and EDS techniques to determine the spatial distribution. The device performance can then be evaluated against the micro composition of the structures fabricated.

7059 11.7%	ITO/ 7059 6.1%	7059 4.3%
ITO/ 7059 5.1%	7059 4.5%	ITO/ 7059 2.9%
7059 2.5%	SnO_2/ 7059 2.4%	TC

Figure 23. Spatial dependence of $CdTe_{1-x}S_x$ composition of films deposited by co-evaporation of CdTe and CdS at 150°C substrate temperature. Each block represents a 1" x 1" substrate.

2.3.2 CdTe DEVICES

2.3.2.1 Back Contact Development

A new method was developed for forming low resistance contacts to the CdTe surface of CdTe/CdS thin-film solar cells. After $CdCl_2$ processing, the CdTe surface is coated with a thin layer of copper which is heated and then reacted. The heat treatment diffuses Cu into CdTe, doping it p-type while the reaction removes elemental Cu and produces a conductive surface which is easily contacted using different materials. This process allows great flexibility in selection of a back contact material. High efficiency devices having fill factors up to 77% were fabricated. The process is applicable to CdTe/CdS devices having CdTe deposited by different techniques and should be compatible with module fabrication technologies.

2.3.2.2 Motivation

In many of the reported CdTe/CdS devices the fill factors are less than expected due in part to the device series resistance. Achieving low device series resistance requires controlling the conductivity of the CdTe layer and forming a non-rectifying low resistance contact. Formation of low resistance contacts to CdTe has been facilitated either by direct formation of a p^+ layer such as CdTe:Te (21), Cu_2Te (31), ZnTe:Cu (32), or HgTe (33) or by processes in which the contact materials such as Cu/Au layers (20, 22, 30, 34) or carbon paste containing Hg or Cu salts (35, 36, 37) are applied to a suitably prepared surface and then heated. The basis for these approaches has been extensively reviewed (38, 39, 40). Devices with contacts containing elemental Cu, such as Cu/Au, have achieved fill factors over 70% but are not always stable, and the mechanism for instability may be linked to chemical diffusion processes that are quite active at room temperature (41, 42). Furthermore, fabrication processes using Cu/Au contacts couple the CdTe doping with contact formation (43) which restricts the latitude for independent control over CdTe and contact properties. Devices with paste contacts containing Hg compounds have achieved fill factors up to 75% but may suffer from issues related to large scale commercialization such as toxicity and monolithic integration for module fabrication. We have developed a process, hereafter referred to as the diffused Cu process, that is compatible with module fabrication, separates the doping and contacting steps, leaves no elemental Cu in the finished device, is not sensitive to CdTe deposition method, and has demonstrated devices with high V_{oc} and fill factors exceeding 75%.

2.3.2.3 Contact Process Description

All of the devices were fabricated in a superstrate configuration as described above. Contact development was carried out on CdTe/CdS films deposited by physical vapor deposition (PVD) and were compared to devices made by our baseline process with Cu/Au contacts. The general applicability of the contacting process to devices made by other methods was tested using CdTe/CdS structures fabricated at other laboratories by: elemental vapor deposition (EVD) at Solar Cells, Incorporated; close-spaced sublimation (CSS) at the University of South Florida; and metal organic chemical vapor deposition (MOCVD) at Georgia Institute of Technology. The CdTe and CdS film thicknesses ranged from 2-6 μm and 0.15-0.25 μm, respectively.

The diffused Cu contact process consists of deposition of a Cu layer on the CdTe surface, heat treatment of the entire structure, etching, to remove elemental Cu and produce a Te rich surface; and application of the desired current-carrying contact material. Cu was deposited by electron beam evaporation to a thickness of 5 nm to 20 nm at a rate of 0.2 nm/s at a base pressure of 1×10^{-6} torr. Heat treatment was carried out in a tube furnace at 150°C to 200°C for 15 to 60 minutes with flowing argon to prevent oxidation of the Cu layer. Next the structure was immersed in 0.004 mol % bromine-methanol solution (Br_2:CH_3OH) for 5-10 s to remove metallic Cu and a thin layer of CdTe. The action of the Br_2:CH_3OH on metallic Cu layers was verified by reaction of

10 μm thick Cu on Corning 7059 glass in 0.004 mol % Br_2:CH_3OH. The Cu films completely dissolved in 1-3 sec. The etch rate of CdTe in this strength solution is 0.3 μm/min, as determined by removal time of 2-4 μm thick CdTe films on CdS/ITO/glass, and is estimated to remove 20-40 nm of CdTe during the etch step.

After rinsing in methanol the samples were contacted with the different current carrying conductors such as Ni, Cr, Pt, Mo, carbon paste, and ITO. No subsequent treatments were necessary to optimize devices. Cell areas up to 1 cm^2 were prepared by scribing through the entire structure down to the TCO. Indium solder was applied to the TCO to provide a low resistance contact point to the emitter side of the device.

Devices were evaluated by current-voltage, spectral response, and capacitance-voltage analysis techniques and were compared to devices fabricated with Cu/Au contacts. XPS and SIMS analysis was used to determine both surface composition and Cu concentration in CdTe.

2.3.2.4 Devices

The current-voltage (J-V) parameters obtained using the diffused Cu process and different conductors and CdTe deposition techniques are shown in Table 18. For the devices made with PVD CdTe, the performance of Cu/Au contact is shown for comparison. The diffused Cu contact yields similar performance to that obtained with the baseline Cu/Au contact for PVD devices and similar to that obtained by the contacts used by the respective groups on the material they provided. The result obtained with ITO contact offers the possibility that transparent cells can be fabricated for back wall analysis or tandem cell applications.

Table 18. J-V parameters of CdTe/CdS devices made with the diffused Cu contact process using the conductors and CdTe deposition techniques shown.

CdTe Method (Group)	Sample	Conductor	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
PVD (IEC)	40723.11	Cu/Au	790	20.1	69	11.0
PVD (IEC)	40821.11	Cr	811	20.7	66	11.1
	40821.21	Mo	821	22.4	63	11.6
	40827.13	Ni	775	21.3	71	11.7
	40826.32	Pt	795	19.6	75	11.7
	40816.23	C	825	21.0	68	11.8
	40826.32	C	830	19.4	73	11.8
	40832.13	ITO	712	20.5	60	8.8
EVD (SCI)	10304D2.2	Ni	804	18.0	77	11.0
	10304D2.3	C	828	18.1	74	11.1
CSS (USF)	1075	Ni	792	22.4	73	12.9
	1075	C	864	22.4	73	14.1
CVD (GIT)	GT1	C	757	20.6	61	9.5

Figure 24 is a light J-V plot of a 1 cm^2 device with EVD CdTe deposited at Solar Cells, Inc. and processed at IEC with the diffused Cu contact and carbon. The performance of this device is the

same as the best devices made by Solar Cells, Inc. Other devices, with Ni conductors, have been measured with fill factors as high as 77%, $V_{oc} > 800$ mV and resistance at V_{oc} of only 2 Ω cm^2. These fill factors are as high as can be expected from CdTe devices with A-factors of about 2.

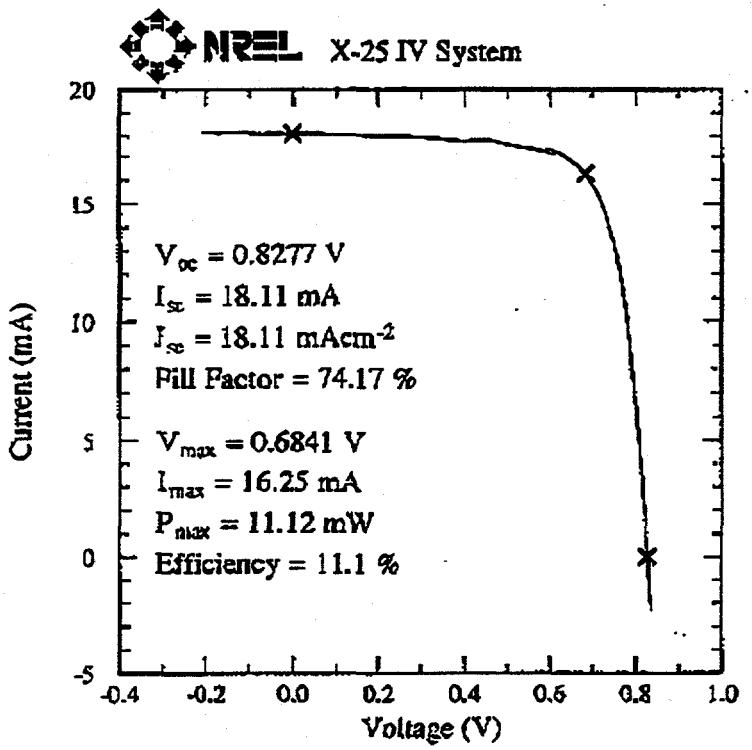


Figure 24. I-V curve of a CdTe/CdS device with EVD CdTe (Solar Cells, Inc.) using the IEC diffused Cu contact process.

Other than the observation that, on a given CdTe/CdS sample, the carbon contact often produces higher V_{oc} than other materials, no systematic dependence of device parameters or efficiency with contact material was found, indicating no influence of contact material work function. This together with the low resistances measured is consistent with our interpretation that the diffusion/etch produces a conductive surface on the CdTe which acts as the primary contact to CdTe; its presence allows for great flexibility in choice of contact material.

Capacitance-voltage measurements of ~11% efficient devices made with the diffused Cu process were compared to those devices made with Cu/Au contacts. Measurements were made at 100 kHz from -2 to 0 volts. $1/C^2$ versus voltage plots for a device with Cu/Au contact and with the diffused Cu process and a chrome conductor are shown in Figure 25. The device with Cu/Au contact exhibits non-linear behavior of $1/C^2$ versus voltage, indicating either a changing carrier concentration or the presence of a second capacitor in series. The linear portion of the curve represents an acceptor concentration of 2.4×10^{15} cm^{-3}. The device made with the diffused Cu process exhibits linear behavior over the same voltage range, indicating uniform carrier concentration of 2.4×10^{15} cm^{-3} near the junction. The difference between these two capacitance characteristics implies that there are significant differences between the electronic configuration of devices with Cu/Au contacts and those with the diffused Cu plus conductor.

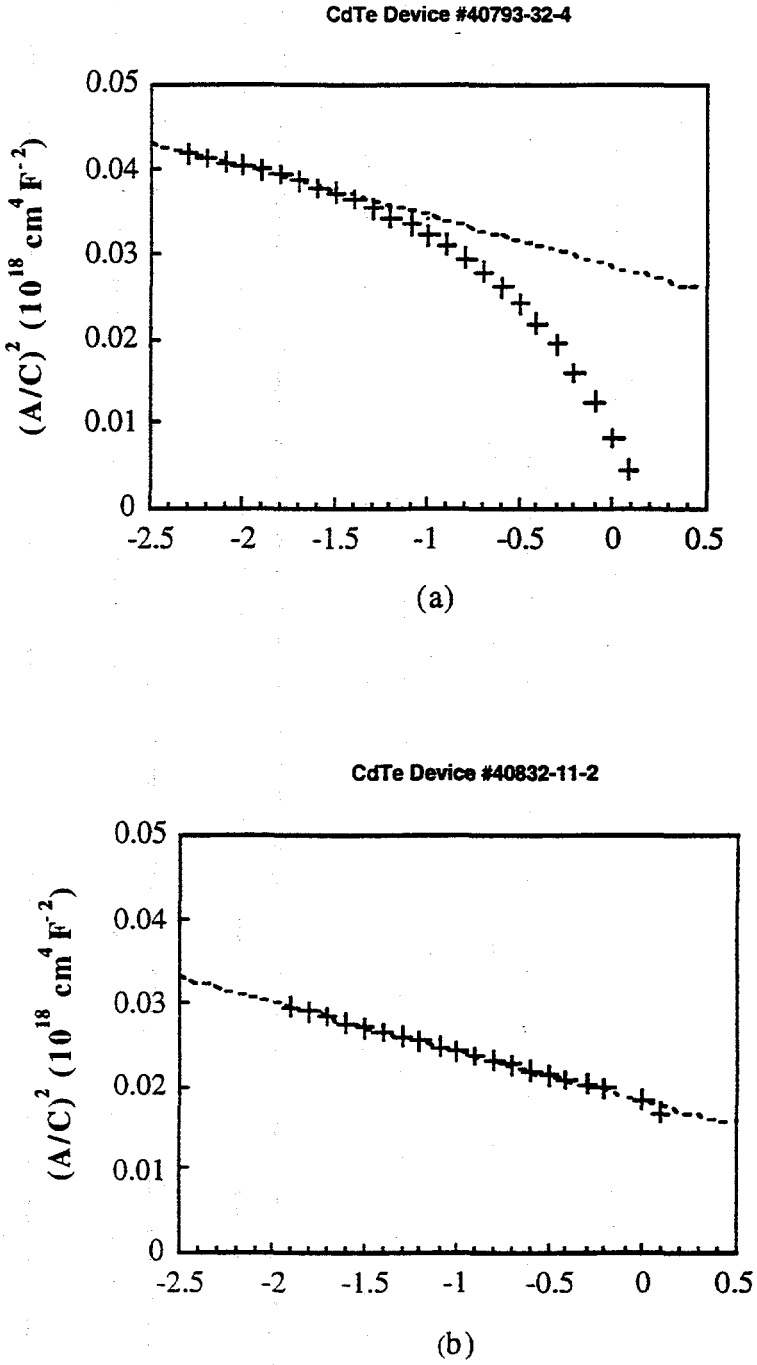


Figure 25. $1/C^2$ versus voltage curves for 11% efficient CdTe/CdS devices made with a) Cu/Au contact and b) diffused Cu process with chrome.

The sensitivity of this process to its individual steps was tested with respect to Cu layer thickness, heat treatment temperature and time, and etch time. No difference in device performance was obtained using 5 nm, 10 nm, and 20 nm of Cu, leading to the target thickness of 10 nm used for all

other evaluations. Cu in excess of 50 nm, however, leads to shunting behavior. Devices were fabricated with no Cu using Ni, Au, and carbon paste contacts on PVD and EVD films that were Br_2:CH_3OH etched after $CdCl_2$ treatment. In all cases, the J-V characteristic exhibited V_{oc} < 700 mV and severe double diode behavior in the forward bias portion of the light J-V curves. The low V_{oc} is attributed to low doping concentration in the CdTe while the non-ohmic forward bias characteristic arises from rectification between CdTe and the back contact materials.

It was necessary to optimize the treatment temperature and time for the CdTe thickness employed. In particular, insufficient treatment temperature and time yields low V_{oc} and suggests that the Cu may play a role in controlling the V_{oc} by modifying the CdTe conductivity. For 2 μm thick CdTe, 150°C for 60 minutes was found to be sufficient, while 5-7 μm thick films required 180°C for 30 minutes. This result is qualitatively similar to that found for devices with Cu/Au (17) and ZnTe:Cu (44) contacts, i.e., optimum V_{oc} is obtained when sufficient Cu is diffused into CdTe.

The diffused Cu process was not found to be very sensitive to etch time in the range of 5 sec to 1 minute, yielding linear J-V behavior in forward bias for etch times up to 1 minute, which removed ~0.3 μm of CdTe. Thus, the etch time of 5 sec was selected on the basis of removal of the Cu metal layer.

2.3.2.5 Surface Analysis and Chemical Interpretation

Within the respective detection limits, EDS measurements of device structures after etching do not reveal the presence of Cu or excess surface Te, this implies that any residual surface layer that might be produced during etching is less than 20 nm thickness. XPS reveals a quantity of Cu near the detection limit (45). SIMS detected a small quantity of Cu at the CdTe surface with decreasing concentration within the CdTe layer (46). In addition, it was found that Ni penetrated into the CdTe which may occur during the Ni deposition in the electron beam evaporator.

We speculate that the reaction with Br_2:CH_3OH forms a conductive layer on the CdTe consisting of either elemental tellurium or copper telluride of composition Cu_xTe, where x lies between 1 and 2. The reaction to form elemental Te is:

$$CdTe + Br_2 \rightarrow Te + CdBr_2$$

This could be followed by:

$$2Cu + Te \rightarrow Cu_2Te$$

The reaction to form Cu_xTe may occur in a single step as:

$$CdTe + xCu + Br_2 \rightarrow Cu_xTe + CdBr_2$$

or via three step reaction as:

$$2Cu + Br_2 \rightarrow 2CuBr$$
$$CdTe + Br_2 \rightarrow CdBr_2 + Te$$
$$xCuBr + Te \rightarrow Cu_xTe + (x/2)Br_2$$

In either case, the reaction product $CdBr_2$ is soluble in methanol and is expected to remain dissolved given the very low quantity of Cu and Cd reacted. The presence of a beneficial surface layer was tested by reacting the surface further prior to contact deposition. Samples were reacted in 0.2 M KCN at 50°C for 10 sec after the Br_2:CH_3OH etch and were contacted with carbon paste dots. KCN solution dissolves copper compounds of the type Cu_2S, Cu_2Se, and Cu_2Te as well as elemental tellurium, but does not react strongly with CdTe nor with Cu. The devices with KCN-etched surfaces exhibited similar V_{oc} to unetched samples but had a strong double diode characteristic in forward bias, indicative of a blocking contact between the carbon paste and the Cu-doped CdTe. This suggests that the beneficial layer formed by Br_2:CH_3OH was removed by the KCN treatment.

2.4 a-Si DEPOSITION AND PROCESS RESEARCH

Our goals are to investigate the effect of processing on device performance and to support the NREL Multijunction Device Design and Interface Team. Regarding device deposition, our main challenge this year was to establish reproducibility and repeatability. This has been largely accomplished as evidenced by producing devices from 10 a-Si runs and achieving efficiencies between 7.8 and 8.1% (Ti/Ag contacts). IEC's role on the NREL a-Si Research Team effort is to assist industry and other research groups by depositing a-Si layers and devices on substrates provided by others, providing detailed characterization of optical and electrical properties to others for further analysis, and to develop or assist development of optical and electrical models of multijunction cell performance to guide research priorities and optimization. This year our main efforts were to investigate devices with different front and back TCO contacts. As Team Leader, Dr. Hegedus makes periodic presentations to the NREL/DOE Guidance Team about the Team's progress, including a Multijunction Device Design Review.

2.4.1 Plasma Reactor Operation and Modifications

Reproducibility in our current single chamber reactor had been a major problem as reported in the previous Annual Report (1). Problems of dopant cross-contamination were caused by having an unnecessarily large volume and large internal surface area relative to the substrates, poorly defined gas flow patterns, and unconfined plasma. We sought to open up the internal deposition canister to improve pumping, operate at higher flows and higher substrate temperatures, and to eliminate the plasma below the electrode.

The plasma canister was modified to change the gas flow and improve the pumping conductance. The cylindrical wall previously had six 3/8" diameter holes for gas flow out of the deposition can. This was replaced with a can having 4 rectangular slots 1/4" deep and 3" long at the top of the can. The total opening area increased by more than a factor of 4 and the openings are now coplanar with the substrates, which should reduce turbulence and holding time. The source gas line was reconnected to the reactor can. All runs after 4252 were deposited with this configuration. Prior to installing the new slotted can, V_{oc} was 0.86-0.88 V but FF reproducibility was very poor. After installing the new can V_{oc} decreased to 0.77-0.80 V. After extensive p and buffer layer optimization, we were able to increase V_{oc} to 0.85 V (Section 2.4.3).

An insulating plate has been designed to confine the plasma between the electrodes and prevent plasma below the electrode. The insulator is now larger than the electrode, nearly as large as the can diameter, and has holes to force gas flow through the electrode. These two features increased the flow of gas directly impinging on the substrates. The insulator plate was machined out of Macor. Two different Macor discs were used, having different diameters. The first one was 7.25 inches in diameter and thus leaving a small space between the insulator and the can wall for gas flow. This was used from runs 4266 to 4343. The second Macor piece had a diameter of 7.50 which is the same as the can, thus forcing all gas through the electrode onto the substrates. This was used in all runs after 4343. A new Mo electrode was installed at that time as well. Figure 26 shows the improved FF and reproducibility with the first Macor piece.

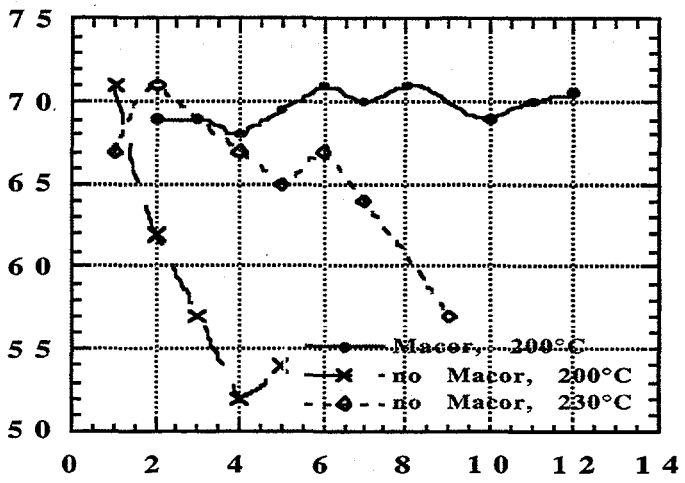


Figure 26. FF vs. the number runs after system cleaning before and after installing Macor insulator for 2 i-layer deposition temperatures.

Previously, FF decreased steadily with each run after cleaning. Based on bias dependence of QE measurements at long wavelengths, the successive decrease in FF was attributed to a successive build-up of P contamination (1). Installing the Macor insulator significantly improved the FF reproducibility. This was accompanied by a reduction in the bias dependence of the QE at long wavelengths, which we attribute to a reduction in P cross-contamination. However, significant deposition still occurred below the electrode with either of the Macor discs. There was especially heavy powder formation around the RF feed through even though it had a Macor insulating shield. A grounded stainless steel tube was placed around this Macor insulator to completely eliminate any RF potential leaking from the feed through into the lower part of the can but heavy powder formation still occurred. The powder problem in the lower part of the can was solved by re-installing the stainless steel shower head which we believe acts as a ground plane to short out the plasma around the feed through.

The recommendation to operate at higher temperatures (230°C) was counter-productive. Although resulting in less of a fall-off in FF after cleaning (see Fig. 26), an increase in bias dependence of QE at short wavelengths suggested an increase in B contamination at the p/i interface. Instead, lowering the temperature for all three layers to below 200°C was found to improve V_{oc} and FF, as described in more detail in the following sections.

Further evidence of the improved reproducibility and repeatability with the Macor insulator is shown in Figure 27. The FF and V_{oc} is shown for 30 device runs, including three system cleanings. The p and buffer layer conditions were varied to increase J_{sc} and V_{oc}. The FF ranges from 69 to 72%. The V_{oc} steadily increases from 0.78 to 0.83 V. The J_{sc} increases from 12 to 14 mA/cm^2. The plasma CVD system and downstream processing had achieved a stable baseline from which further optimization could occur. The main problem was low J_{sc} and V_{oc}.

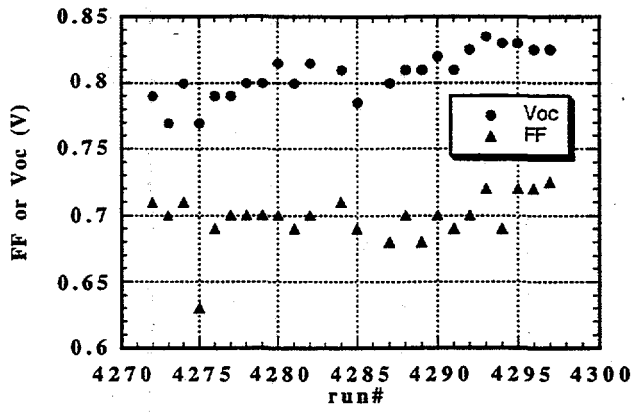


Figure 27. V_{oc} and FF for 26 device runs after installing Macor insulator with i-layer deposition at 200°C ρ and buffer layer conditions were varied to improve V_{oc} and J_{sc}. Note steady improvement in V_{oc} and reproducible FF. System was cleaned before runs 4268, 4280, and 4287. J_{sc} ranged from 12 to 14 mA/cm^2 with Ti/Ag contacts for these runs.

2.4.2 a-Si Film Deposition and Material Properties

A much greater range of conditions was explored directly in devices, as will be discussed in Sections 2.4.3, 2.4.4, and 2.4.5, than were explored as the single layer films discussed here. Film characterization included thickness, reflection and transmission to obtain bandgap; dark conductivity vs temperature to obtain activation energy, and photo conductivity. Bandgap was determined from a Tauc plot. The absorption was calculated assuming front surface reflection only.

We experienced difficulty depositing H_2 diluted layers after installation of the Macor insulator . Therefore, p, i and n layers were deposited to explore the effect of H_2 dilution. The p-layers were also intended to evaluate sensitivity of the window layer bandgap to gas composition.

The p-layers were all deposited at temperatures and pressures determined to give best device performance, T=150°C and P=0.2 torr. The low temperature is to minimize CVD of B_2H_6. The RF power, CH_4 and H_2 flow were varied. Results are in Table 19. Increasing the CH_4 flow from 15 to 25 sccm increased bandgap from 1.93 to 1.98 eV while the photo conductivity decreased from $1x10^{-6}$ to $2x10^{-7}$ S/cm. The dark conductivity and activation energy were relatively unaffected by the CH_4 flow. Increasing RF power to 15 W (#4353) had no effect on growth rate, bandgap or electrical properties. Dilution of 1:1 with H_2 (SiH_4+CH_4=30 sccm, H_2=30 sccm) reduced growth rate by a factor of 2 and increased photo conductivity by a factor of 2. Devices were deposited with p-layer conditions in the same range of CH_4 and power as in Table 19, as discussed in Section 2.4.3.

Table 19. a-SiC p-layer film properties with flow of 2% B_2H_6 in H_2=1.5 sccm, T=150°C and P=0.2 torr.

Run	RF Power	Flow Rate SiH_4	Flow Rate CH_4	Flow Rate H_2	Eg,	Growth Rate	Conductivity photo	Conductivity dark	Ea,
	W	sccm	sccm	sccm	eV	Å/s	S/cm	S/cm	eV
	10	10	15	0	1.93	3.2	$1x10^{-6}$	$3x10^{-7}$	0.48
4350									
4351	10	10	20	0	1.97	4.0	$4x10^{-7}$	$3x10^{-7}$	0.46
4352	10	10	25	0	1.98	4.1	$2x10^{-7}$	$1x10^{-7}$	0.48
4353	15	10	20	0	1.97	4.3	$3x10^{-7}$	$1x10^{-7}$	0.48
4354	15	10	20	30	1.97	2.0	$7x10^{-7}$	$2x10^{-7}$	0.50

The purpose of i-layer depositions was to establish parameters of stable plasma at moderate H_2 dilution. The H_2 dilution was necessary to improve the stability especially for devices deposited below 200°C (47). The i-layers were deposited at 175°C with varying RF power, pressure, and H_2 dilution as shown in Table 20. Typical values for an undiluted i-layer, representing our standard device i-layer, are shown for comparison. Compared to the undiluted i-layer, a 1:1 H_2 dilution at 7 or 15 W has no effect on bandgap or growth rate. It was difficult to establish or maintain a plasma at 0.2 torr at higher dilutions, in agreement with observations from other groups. It was suggested by several other researchers that systems should be operated at higher pressure when using higher H_2 dilution ratios. At 4:1 dilution and 15 W, pressure has a strong affect on growth rate. Significant powder was generated in run 4368 indicating gas phase polymerization despite the H_2 dilution.

Table 20. Hydrogen diluted i-layer properties (typical undiluted for comparison) T=175°C.

Run	Power		Flow Rate SiH_4	Flow Rate H_2	E_g,	Growth Rate	Conductivity photo	Conductivity dark	Ea,
	W	Press. torr	sccm	sccm	eV	Å/s	S/cm	S/cm	eV
undil.	7	0.2	20	0	1.74	2.2	$5x10^{-5}$	$1x10^{-10}$	0.75
4357	7	0.2	20	20	1.72	2.0	$5x10^{-6}$	$2x10^{-11}$	0.81
4358	15	0.2	20	20	1.74	2.1	$2x10^{-5}$	$7x10^{-12}$	0.72
4361	15	0.5	10	40	1.73	1.3	$1x10^{-4}$	$4x10^{-10}$	0.73
4368	15	1	10	40	1.73	6.7	$2x10^{-5}$	$1x10^{-10}$	0.82

Prior to installing the Macor insulator, we deposited n-layers for devices under conditions of very high H_2 dilution (40:1) and high RF power (55 W) which had led to microcrystallinity in 0.5 μm thick n-layers. Such conditions were not stable or achievable with the Macor insulator, forcing us to deposit most devices during this period with a "standard" a-Si n-layer deposited at low power (15 W) without H_2 dilution. However, V_{oc} remained under 0.84 V despite considerable variations in p and buffer layer conditions. Properties of n-layer films deposited at moderate RF power with H_2 dilution from 10:1 to 40:1 are listed in Table 21. None of the films had conductivities expected of microcrystalline materials (>1 S/cm). The plasma appeared spatially non-uniform (flickering cone-shaped bright spots originating at holes in the powered electrode or brighter around edges of electrode) for the first few minutes of some runs. Devices were deposited with n-layers similar to these conditions as discussed in Section 2.4.5.

Table 21. Properties of H_2 diluted n-layer films with H_2 flow= 80 sccm, T=175°C. PH_3 flow is 2% PH_3 in H_2. Films peeled from sample no.'s 4346 and 4348 before some measurements were completed.

Run	Power		Flow Rate,		Eg,	Growth Rate	Conductivity		
		Press,	SiH_4	PH_3			photo	dark	Ea,
	W	torr	sccm	sccm	eV	Å/s	S/cm	S/cm	eV
4346	30	0.5	8	4	1.77	3.0	-	-	-
4347	30	1	8	4	1.73	5.4	$3x10^{-3}$	$2x10^{-3}$	0.20
4348	45	1	8	4	-	7.2	$2x10^{-3}$	$2x10^{-3}$	0.21
4349	45	1	2	1	1.75	3.0	$6x10^{-4}$	$2x10^{-4}$	0.23

Section 2.4.3 Device Results - Effects of Varying p and Buffer Layer Conditions

As described in Section 2.4.1, increasing the conductance of the deposition canister by replacing the canister ring having 8 small holes with one having 4 large slots and increasing all gas flows improved reproducibility but reduced V_{oc} from >0.86 to <0.80 V. After reducing the P cross - contamination from run-to-run with the Macor insulator as described in Section 2.4.1, we sought to reduce the B cross- contamination. Reducing the temperature during the p and buffer layer depositions from 200 to 150°C greatly reduced the bias dependence of the QE at short wave lengths, which we attribute to reduction in B cross - contamination from the thermal CVD growth from B_2H_6. Together, the new Macor piece and lower p layer deposition temperatures allowed us to routinely achieve values of FF>70%. The main limitation on efficiency was then the low blue response and low V_{oc}. Since the FF was now under good control, we focused on varying the p and buffer layer. All devices discussed in this report had p and buffer layers deposited at 150°C to minimize the B cross-contamination. Analysis of the short wavelength QE taken at reverse bias was used to obtain the window layer Tauc gap and thickness, as described in last years annual report (1). Varying the p-layer and buffer layer properties individually allowed separate determination of their influence on the QE.

It is well established from both plasma CVD and our previous photo CVD work that the buffer layer thickness and bandgap can have a major influence on V_{oc}. Runs 4288-4292 and 4309-4312 varied the buffer bandgap grading (uniform or linear decrease in CH_4), the CH_4 flow from 10 to 20 sccm, the RF power from 10 to 20 W, and the buffer deposition time from 10 to 30 s. Despite these considerable variations, V_{oc} remained between 0.81-0.83 V with no clear trends. We concluded that V_{oc} was not limited by the buffer layer in our present devices as long as there was any buffer at all. Eliminating the buffer altogether significantly reduced blue response due to B cross- contamination.

Thus, the p-layer became a major focus. The following range of p layer conditions were explored: CH_4/SiH_4 = 0.5-2; $B_2H_6/(CH_4+SiH_4)$ = 0.1-0.2%, CH_4+ SiH_4 = 12-50 sccm, RF power = 10-37 W, and times from 20 to 40 s. The pressure was always 0.2 torr to keep the growth rate low and the temperature was always 150°C. The pump and flush purge step was performed after the p-layer or after the buffer. Minor variations in purge length and SiH_4 flow had no effect.

Results of one series are shown in Table 22. Increasing the p-layer B_2H_6 flow by 50%, increasing the CH_4 flow by 20%, the RF power by 25% or the thickness by 25% had little effect on V_{oc}. However, increasing the RF power to 37 W in 4292 was the first time V_{oc} exceeded 0.82 V in this entire series.

Table 22. Effect of p-layer deposition conditions on device performance. The SiH_4 flow in the p-layer was 20 sccm. All buffer layers were deposited in 20 s (except 4276 which was deposited in 30 s) with 20 sccm of CH_4 at the same power as the p-layer.

Piece No.	Flow Rate, sccm		deposition	Power,	V_{oc},	J_{sc}	FF	Eff
	CH_4	B_2H_6	time, s	W	V	mA/cm^2	%	%
4272-22	20	2.5	30	14	.79	13.9	71	7.7
4274-22	20	3.7	30	14	.80	13.5	71	7.6
4276-22	20	2.5	30	14	.79	13.7	69	7.6
4278-22	25	2.5	30	14	.80	14.0	70	7.7
4279-21	25	2.5	40	14	.80	13.5	70	7.5
4284-22	25	2.5	30	18	.81	13.0	71	7.4
4292-22	25	2.5	30	37	.83	12.7	68	7.1

The effect of p-layer deposition conditions was investigated in the devices using the Tauc analysis of the optically-limited QE taken at reverse bias as described in our previous annual report (1). Front reflection and absorption in the SnO_2 are accounted for at each wavelength. Figure 28 shows the modified Tauc plot derived from the QE for devices with p-layers deposited at 10, 18 and 37 W. The bandgap increases from 1.68 to 1.87 eV while the growth rate is unchanged at 6 Å/sec.

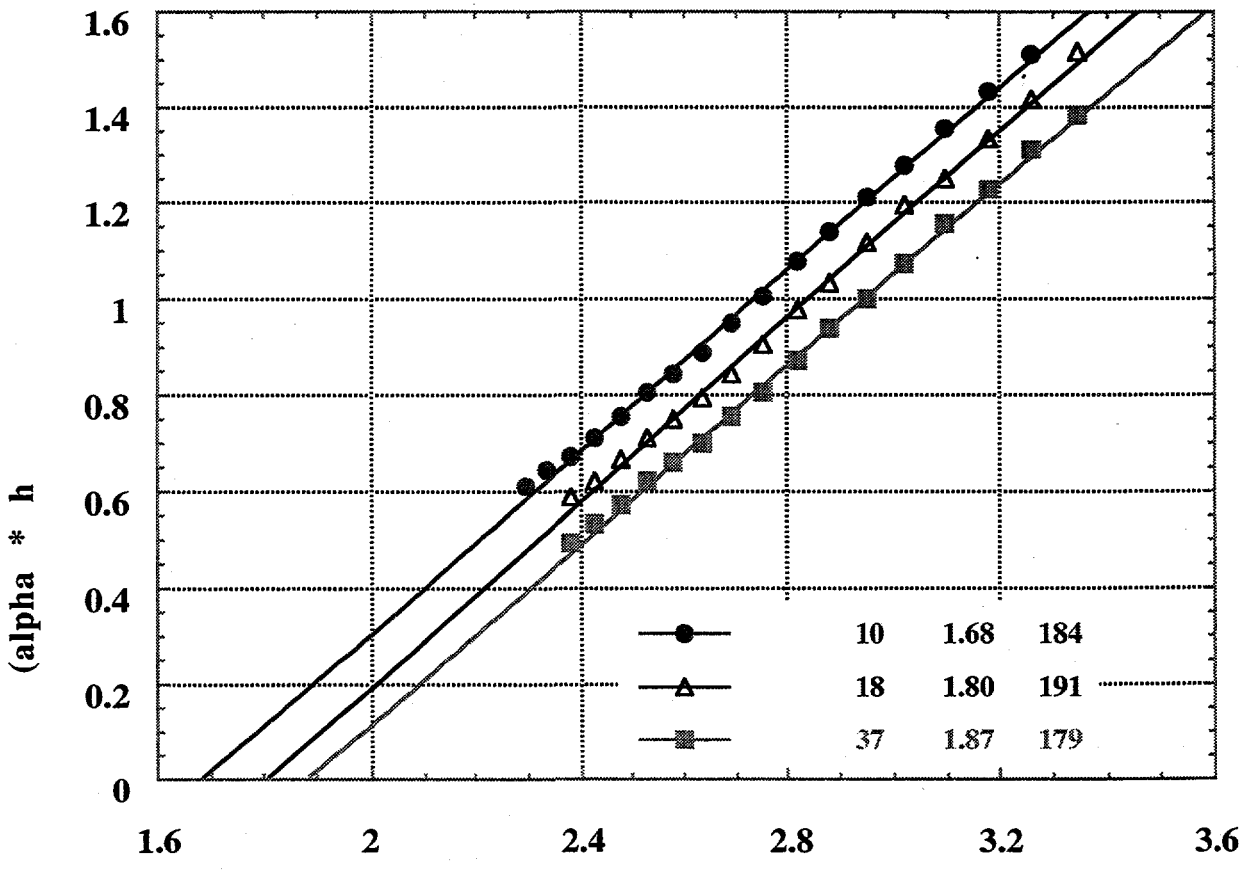


Figure 28. Modified Tauc plot from short wavelength reverse bias QE of three devices whose p-layers were deposited at different RF powers. The slope is proportional to the square root of the thickness and the intercept is the bandgap of the absorber layer.

This increase in bandgap with RF power is larger than expected from results on films as in Table 19. The growth rate is also 50% higher than expected, and may indicate contribution of the buffer layer absorption to limiting the blue response. In another series, increasing the CH_4/SiH_4 flows from 25/20 to 40/20 sccm/sccm had little effect on V_{oc} or blue response. The Tauc analysis of QE indicated that the bandgap only increased from 1.82 to 1.86 eV. Note that these bandgaps are lower and growth rates are higher than expected based on deposition of thick p-layer films. This suggests that we need significant changes in our p and buffer layer to improve V_{oc}.

Our p-layers are deposited under very similar conditions to those reported in the literature except that our RF power density may be higher. At 14 W, the power density is around 100 mW/cm^2 whereas most groups report using under 50 mW/cm^2 for their p-layer. This suggests that we are operating in the high power regime where film properties, notably C content and bandgap, are controlled by the RF power (48). In the low power regime, C content and bandgap are determined by the ratio of CH_4/SiH_4. Most groups deposit their p-layers in the low power regime. Plans include deposition at lower powers, using H_2 diluted gas mixtures, and replacing the CH_4 with CO_2.

2.4.4 Device Results- Effects of Varying i-Layer Conditions

There were very few changes in i-layer deposition conditions during this reporting period since most device runs routinely achieved FF values of 70-72%. The standard conditions were 7 W, 0.2 torr, and 20 sccm of SiH_4. The growth rate was typically 2.0-2.5 Å/s. Nearly all devices had i-layers deposited for 30 minutes leading to thicknesses of 0.40-0.45 μm. Until run 4293, the substrate temperature was 200°C. Reducing the temperature in run 4293 to 175°C gave V_{oc} of 0.83V and cells with efficiencies over 8% for the first time. FF values of 72-74% were common after lowering the temperature.

The influence of i-layer deposition temperature on stability was demonstrated by light soaking devices deposited at 150, 175, and 200°C. Their i-layers were all 0.4 μm deposited without H_2 dilution at nominally 2 Å/s as per above. Initial efficiencies were 7.5% with FF of 71-73%. They were exposed on the Oriel simulator and had JV curves taken every 5-10 minutes for an hour. Figure 29 shows the normalized FF over the 1 hr exposure. The cells with the highest i-layer temperature (200°C) had the least degradation as expected. Clearly there is significant degradation for our typical cells deposited at 175°C occurring in the 15-20 minutes required to test a piece. To improve stability of devices deposited below 200°C will probably require H_2 dilution as shown by others (47).

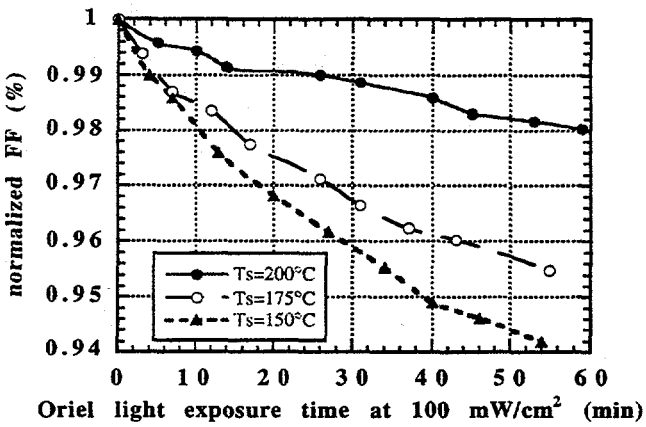


Figure 29. Change in normalized FF with light exposure on Oriel Simulator for three devices whose i-layers were deposited at different temperatures.

Properties of hydrogen diluted i-layers were given in Table 20. Two identical devices with 4:1 H_2 diluted i-layers have been deposited. Results are in Table 23. Both had 40 sccm of H_2 and 10 sccm of SiH_4 in the i-layer deposition. The n-layers were deposited at 10 W without H_2 dilution. Run 4371 was deposited following 2 device runs. Run 4377 was deposited after only a thin (1 min) H_2 diluted a-SiC p-layer.

Table 23. Performance of cells with H_2 diluted i-layers deposited with identical deposition parameters.

Run #	V_{oc}, V	J_{sc}, mA/cm^2	FF %	Eff. %	previous run
4371-22	0.75	14.2	59.5	6.3	p-i-n device
4377-22	0.84	13.9	65.8	7.7	p-layer in clean system

The large increase in V_{oc} following deposition of a a-SiC layer is reminiscent of the photo CVD system where we discovered that to obtain high V_{oc}, we had to seal in the P from the previous device's n-layer until deposition of the p-layer. The bias dependence of the red response of 4371-22 was much larger than for 4377-22. This suggests that the H_2 radicals are scouring P from the internal surfaces and incorporating it into the i-layer. Note that 4377 was the highest V_{oc} we had achieved in over 10 runs while 4371 had the lowest. Much of the work in the next year will focus on understanding how to deposit H_2 diluted i-layers at low temperature.

2.4.5 Device Results - Effects of Varying n-Layer Conditions

Since installing the Macor insulator, we had used an older n-layer recipe with low power (10 W) without H_2 dilution. This may have been responsible for some loss in V_{oc} (30-60 mV). Runs 4319-4324 looked at two RF power levels (30 and 45 W) and two H_2 dilutions (20 and 80 sccm). The SiH_4 flow was 2 sccm, the 2% PH_3 flow was 2 sccm, and temperature was 175°C (to be consistent with the i-layer). Results are in Table 24. Clearly, H_2 dilution ratios of 10:1 or 40:1 give 30-40 mV improvement in V_{oc} over the undiluted low power n-layer.

Table 24. Effect of n-layer conditions on device performance.

Run #	Power W	H_2, flow, sccm	Press, torr	V_{oc}, V	J_{sc}, mA/cm^2	FF %	Eff. %	Comment
4318	10	0	0.5	.80	13.1	70	7.4	a
4319	30	20	0.5	.83	12.6	70	7.4	
4320	30	80	0.5	.84	12.4	72	7.5	
4322	45	80	0.5	.84	13.2	71	7.9	b,c
4324	45	20	0.5	.83	12.4	72	7.5	
4338	30	80	0.2	.72	11.8	62	5.3	d,e
4339	30	80	0.5	.85	12.7	73	7.9	b
4342	30	80	0.5	.85	12.5	74	7.9	b,f

comments:

a- undiluted low power n-layer as control.

b- p-layer deposition time was 20 s (other pieces in this series had 30 s deposition time). c- plasma was very non-uniform spatially during n-layer deposit run.

d- n-layer deposited in 8 minutes (all other n-layers deposition in 4 minutes).

e- pale greyish-purple plasma, but uniform.

f- repeat 4339 after reactor cleaning to verify high V_{oc}.

Runs 4339 and 4342 verify that acceptable V_{oc} can be achieved reproducibly along with very good FF. For reasons which are not clear, the H_2 diluted n-layer also has slightly lower J_{sc} due to lower blue QE. The lower pressure H_2 diluted n-layer 4338 was clearly inferior. This may be related to insufficient etching by H radicals which is strongly related to pressure.

2.4.6 Effect of Front Textured TCO on Device Performance

A major emphasis of our team-related work involved studying ZnO materials as an alternative to standard textured SnO_2 from Solarex or LOF. It is well recognized that ZnO has higher transmission than SnO_2 over the solar spectrum relevant to a-Si cells but lower V_{oc} and FF have been reported which offset the gain in J_{sc} (49). This is attributed to a contact resistance or a barrier at the ZnO/p interface (50). Possible solutions include H_2 plasma treatments, modified p-layer growth, and other interfacial layers. We have investigated this problem by depositing cells on TCO bilayers, typically 1 μm of one textured TCO material overcoated with a thin (0.01-0.1 μm) layer of the other TCO. This allows for separation of bulk and interface effects. Front TCO studies carried out this year using ZnO included:

1. Cells deposited on smooth (sputtered) and textured (APCVD) ZnO to separate the effect of texture and ZnO/p interface effects.

2. Cells deposited on bilayers of ZnO/SnO_2 and SnO_2/ZnO where the first layer is textured and the second layer is a thin overcoating.

3. Optical studies of H_2 diluted p-layers deposited on textured ZnO from various sources.

In every study, a piece of our standard Solarex textured SnO_2 was included as a control. We collaborated on evaluation of ZnO materials provided by Prof. Gordon at Harvard (APCVD), Dr. Nagi Maley at Solarex Thin Film (LPCVD), and Mr. Kevin Mackamul at UPG (LPCVD). Transmission and reflection were measured on textured ZnO from the

above groups with an index matching liquid (n=1.7) sandwiched between the sample and a 7059 glass cover slide. The index matching liquid eliminates the effect of scattering and gives a measure of the true optical properties of the TCO material. Transmission and reflection were measured through the glass/ZnO substrate as light would enter in a superstrate device structure. Figure 30 shows the transmission of the samples corrected for front reflection and absorption in the index match liquid, compared to our standard textured SnO_2 substrate (from Solarex). The ZnO material from all groups has less absorption than the SnO_2. The sharp edge around 370 μm is due to the ZnO bandgap. Next, we deposited H_2 diluted p-layers on the ZnO materials, and measured the absorption and reflection again with the index matching liquid. The p-layer was deposited under the same conditions as 4354 in Table 19 for 60 s, which should have given a thickness of about 120 Å

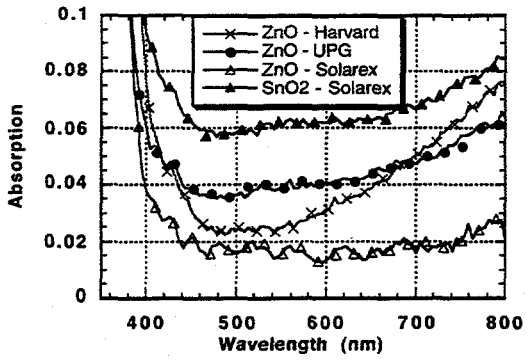


Figure 30. Absorption for textured ZnO from Solarex, Harvard, and UPG, and SnO_2 from Solarex. Measurements were made with an index matching liquid (n=1.70) to eliminate scattering.

in the liquid is shown in Figure 31. Again, all of the samples are very comparable and much better than the SnO_2. This shows that the ZnO made by each group is of similar optical quality, and none shows major degradation due to exposure to H_2 plasma during deposition. Future work will involve depositing devices on these textured ZnO substrates.

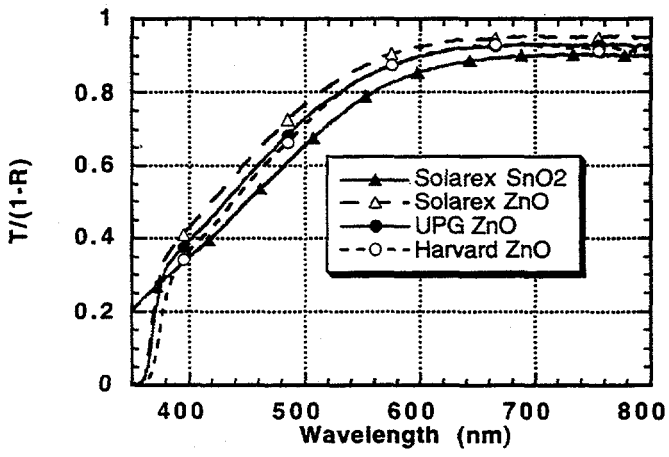


Figure 31. Transmission normalized by (1-R) for same four textured TCO substrates as Figure 30 after deposition of a thin H_2 diluted a-SiC p-layer.

Previously, we have deposited devices on textured ZnO made by APCVD at Harvard by Dr. Gordon's group (1). Compared to the standard Solarex SnO_2 control piece, comparable V_{oc} (0.84 V) was found for SnO_2 and ZnO. However, the J_{sc} and FF were poorer for the ZnO substrate. The lower J_{sc} for ZnO was due to insufficient texture (haze less than 8%). The reduction in FF is correlated with an increase in R_{oc} which may be due to a change in the ZnO surface properties during heat-up and bake-out of the a-Si chamber under vacuum, described below.

ZnO films having more texture (higher haze) were prepared by APCVD at Harvard then coated with a thin (0.1 μm) layer of SnO_2 which would present the same surface for p/TCO contact formation as the standard thick textured SnO_2. Table 25 compares devices deposited on standard textured SnO_2, and the ZnO/SnO_2 bilayers. The devices on SnO_2 and ZnO/SnO_2 have very comparable performance, e.g. high FF (72%) indicating good i-layer quality and low resistance. The similar values of J_{sc} achieved with the various structures indicates equivalent absorption losses and scattering due to texture between textured ZnO and textured SnO_2. This is confirmed by comparing the QE on these devices (Figure 32).

We observed that cells deposited on ZnO had a greater sensitivity to the pre-deposition bake-out cycle than cells on SnO_2 or ZnO/SnO_2 bilayers. Table 26 shows the results for cells deposited in run 4299 after a weekend bakeout under vacuum at 250°C.

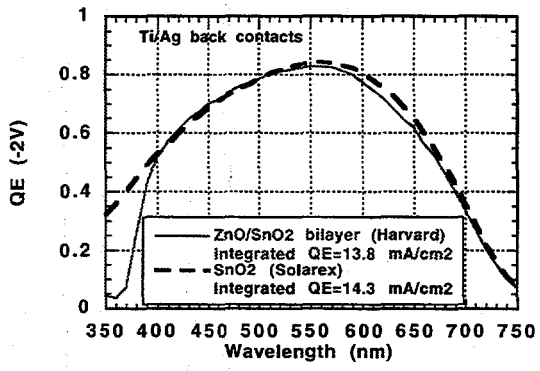


Figure 32. QE at -2 V comparing textured TCO films. Devices from run 4300 were deposited on standard Solarex SnO_2 and on ZnO (1 μm)/SnO_2 (0.1 μm) bilayers from Harvard. AM1.5 integrated currents are shown. Cell performance is shown in Table 25.

The SnO_2 and ZnO/SnO_2 are the same substrate types as shown in Table 25. In fact, they were deposited on the same day (Monday) following a weekend bakeout under vacuum but at different bakeout temperatures. The cells on textured ZnO suffer significant loss in V_{oc}, J_{sc} and FF. The cells on ZnO/SnO_2 suffer mostly in J_{sc}. As shown in Table 26, the loss in J_{sc} is due mostly to a loss in the blue response. This suggests a degradation in the optical properties of the ZnO occurs for both substrates but the electrical properties of the SnO_2 are not degraded by the bakeout as much as the ZnO surface. Furthermore, the significant loss in blue QE for the SnO_2 piece in Table 26 compared to the SnO_2 piece in Table 25 suggests that something is thermally evolved from the ZnO and re-deposited onto all the substrates. Typically we find that SnO_2 substrates show no sensitivity to a 48 hr bakeout under vacuum at 250°C. (The 4295 pieces in Table 27 had a weekend bakeout at

250°C yet they had nearly 8% efficiency.) This strongly suggests a different optimization of bake-out and p-layer deposition may be required for ZnO substrates compared to SnO_2.

Table 25. Cell results comparing ZnO (1 μm)/SnO_2 (0.1 μm) bilayers and SnO_2 as a front TCO. Cells had 2 hr bake-out at 250°C under vacuum, after 48 hr under vacuum at 120°C.

Run #	TCO Window	V_{oc}, V	J_{sc}, mA/cm^2	FF %	Eff. %	R_{oc}, Ωcm^2	QE(400)
4300-22	SnO_2	0.83	13.0	72	7.9	5	0 53
4300-11	ZnO/SnO_2	0.84	12.6	72	7.6	6	0.51

Table 26. Cell results comparing SnO_2, ZnO and ZnO/SnO_2 bilayer (from same ZnO/SnO_2) substrate as in Table 25, except cells had a 48 hr bakeout at 250°C under vacuum.

Run #	TCO Window	V_{oc}, V	J_{sc}, mA/cm^2	FF %	Eff. %	R_{oc}, Ωcm^2	QE(400)
4299-22	SnO_2	0.83	11.0	72	6.6	6	.40
4299-21	ZnO/SnO_2	0.83	9.3	67	5.0	8	.30
4299-12	ZnO	0.78	8.0	60	3.7	9	.18

TCO bilayers were also made at IEC by sputtering 200 or 1000 Å of Al-doped ZnO onto standard textured SnO_2 from Solarex. This type of substrate is favored by several groups (50, 51) because the thin ZnO layers protects the SnO_2 from reduction by H_2. Cells were deposited on these SnO_2/ZnO bilayers to determine their ability to resist reactive H_2 plasma in H_2 diluted p-layers. As a control, they were used in initial runs with H_2 diluted i-layers. All these devices were poor independent of substrate. The cells on ZnO/SnO_2 bilayers were no different than those on standard SnO_2 substrates. Further studies using these substrates have been postponed until after establishing a higher efficiency process with H_2 diluted layers.

2.4.7 TCO/Ag Back Contact Studies

Improving the optical performance of the back contact could have a major impact on multijunction cell performance. Reducing parasitic absorption losses and improving reflection would allow the bottom cell to be made thinner and/or to have a higher bandgap while maintaining the same J_{sc}. This would improve the stabilized FF and the V_{oc} of the bottom cell, respectively. Detailed calculations estimate that 3-4 mA/cm^2 are lost at the back contact due to absorption and poor reflectivity even with a TCO/Ag contact (52, 53). We evaluated TCO/Ag contacts using our sputtered ZnO or ITO and evaporated Ag. Previously we have reported (1) that ITO/Ag gave a 1-2 mA/cm^2 increase in J_{sc} compared to Ti/Ag. However, this was always accompanied by a decrease in FF and an increase R_{oc}. Therefore, we investigated the effect of the TCO deposition and post-processing to determine the source of the decrease in FF.

ZnO films of three thicknesses (200, 800 and 1600 Å) each at two resistivities (10^{-3} and 10^{-2} Ω-cm) were evaluated as back contacts and compared to our standard Ti/Ag contact. The resistivity was controlled by varying the O_2 concentration in the sputtering gas (balance of Ar).

Table 27 shows the performance of three devices with different ZnO contacts compared to Ti/Ag. Over this wide range in ZnO thickness and resistivity, the ZnO properties had no

effect on V_{oc}, J_{sc}, or FF. Compared to our standard Ti/Ag back contact, the ZnO/Ag back contact has no effect on V_{oc} but increased J_{sc} by 1.5 mA/cm^2. The improvement in J_{sc} is due to the increased red response (QE at 700 μm) from about 0.33 to 0.50 independent of ZnO thickness or resistivity. Figure 33 shows the QE at -2V for cells from run 4320 having Ti/Ag or ZnO/Ag back contacts with 200 or 800 Å of ZnO. The significant improvement in red response with even just 200 Å of ZnO suggests that improved back contact reflection may be due to the ZnO preventing a reaction between the Ti/Ag and a-Si n-layer. The presence of such a layer could increase the parasitic absorption at the back contact.

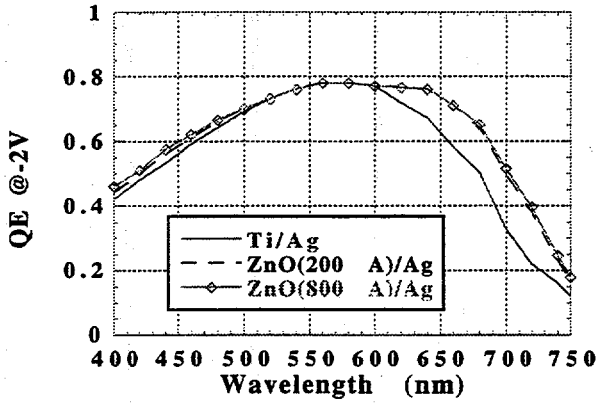


Figure 33. QE at -2 V comparing back contacts. Devices are from run 4320 having back contacts of Ti/Ag, or ZnO/Ag with 200 or 800 Å thick ZnO.

Table 27. Results with ZnO/Ag back contacts with different sputtered ZnO properties. 4320-22 had standard Ti/Ag back contact shown for comparison. ZnO/Ag on these cells was defined by photolithography. QE is at 700 μm.

	ZnO properties							
Piece #	Res., Ω-cm	Thickness, Å	V_{oc}, V	J_{sc}, mA/cm^2	FF %	Eff. %	R_{oc} Ω-cm^2	QE (700)
4320-22	n/a	n/a	0.84	12.4	72	7.5	6	0.32
4320-12	10^{-3}	200	0.84	13.6	67	7.7	14	0.50
4320-21	10^{-3}	800	0.83	13.9	65	7.5	23	0.51
4295-21	10^{-2}	1600	0.84	13.7	69	8.0	7.2	0.49

In fact, we have found that the best we can achieve is a 2-3% lower FF with ITO or ZnO compared to a metal contact. However, typically the FF is 5-12% lower. Cells with ZnO had lower FF independent of ZnO thickness or resistivity, indicating that ZnO bulk series resistance is not the dominant effect. Most other groups do not find a significant FF loss when using TCO back contacts. Since the ZnO bulk properties were not a major influence on FF, and the conditions of ZnO sputtering were typical of those used by others, other processing steps were investigated. We evaluated the following variables: ZnO vs ITO, Ag vs Ti/Ag, the effect of O_2 in the ZnO sputtering atmosphere, the effect of different n-layer conditions (low power with no H_2 dilution vs high power with high H_2 dilution), and the cell definition process (photolithography vs etching ZnO using the Ag as a mask vs no wet

etching at all). A post-process anneal of 30 minutes at 170°C was found to be sufficient to increase FF.

Twenty-four pieces from 10 runs were processed with ZnO or ITO back contacts to study this matrix of variables. Compared to the control piece from each run receiving Ti/Ag, it was found in general that V_{oc} was unaffected, J_{sc} increased 0.5 to 1 mA/cm^2, and FF decreased from 4 to 27% (i.e. from FF=72% to FF=45-68%). The decrease in FF was accompanied by a large increase in R_{oc}, including the appearance of curvature at V_{oc} suggesting a second junction. Since this second junction did not reduce V_{oc} and was apparent in the dark as well as in the light, it was not photovoltaically active. Rather, second junction was probably formed between the contact and doped layers.

A cell definition process was developed as a time-saving alternative to photolithography (PL). The new HCl etch step (10-20 s at 50°C in 6% HCl) uses the Ag dots directly as an etch mask instead of photoresist pattern. However, this etch step was very detrimental for both ITO or ZnO back TCO contacts. This was verified by dipping an already tested device with ZnO/Ag cells defined by PL (which involves etching in HCl with photoresist as a mask) in HCl for 20 s. Dipping in HCl significantly increased the double diode curvature and caused degradation of the FF from >70% to <60%. A piece from the same run with the standard Ti/Ag metal contacts showed no change after the same dipping step, indicating the HCl doesn't penetrate the Ag. This suggests that the HCl etch process degrades the ZnO or one of the ZnO interfaces, and is likely to be causing poor FF even on cells receiving PL since PL includes an HCl etch step. This key experiment lead to deposition of the ZnO and Ag directly through the same mask, eliminating any PL or wet etching steps. The results were the same, i.e., poor FF (<60%) and large R_{oc} (>40 Ω-cm^2), persisted.

Careful consideration of the data from the above 24 pieces suggested that the key variable affecting the decrease in FF relative to the initial control piece was the length of time between when the a-Si device was deposited, and when the TCO layer was deposited. The FF degrades with increasing time between deposition and contacting independent of whether the contact is Ti/Ag, ITO/Ag or ZnO/Ag. This aging is independent of the n-layer deposition conditions and whether the ZnO is defined with an HCl etch step or not. Future work on back reflectors will stress shorter delays between a-Si deposition and deposition of the back contact.

2.4.9 Deposition Conditions for best cell efficiency with different back contacts

The highest efficiency cells with Ti/Ag and ZnO/Ag contacts were obtained on pieces from run 4296. Deposition conditions for this run were very similar to those of 4295 and 4300 (Table 25) which also had cells around 8% efficiency. The deposition conditions for 4296 are given in Table 28. The substrates were baked under vacuum at 120°C for 48 hr (weekend), then at 325°C for 30 minutes and 250°C for 2.5 hr prior to deposition. Note that the n-layer was deposited at low power, and no layers had H_2 dilution.

Table 28. Deposition conditions for run 4296. PH_3 and B_2H_6 were diluted 2% in H_2. The SiH_4 flush was followed by a 30 minute turbo pump/purge cycle after buffer.

				Flow rate, sccm				
layer	T, °C	Pressure torr	Power, W	SiH_4	CH_4	PH_3	B_2H_6	t_s min
p	150	0.2	20	20	30	0	2.5	0.5
buffer	150	0.2	20	20	10	0	0	0.33
i	175	0.2	7	20	0	0	0	30
n	175	0.5	10	10	0	5	0	2

The performance of the best cell from this run with Ti/Ag and with ZnO/Ag contacts is shown in Table 29. The Ti/Ag (25 Å/5000 Å) was evaporated through a mask. The ZnO (1600 Å) was sputtered at room temperature in Ar/O_2, the Ag (5000 Å) was thermally evaporated, and the cells were defined by photolithography. If the FF of the ZnO/Ag piece 4296-21 had been the same as the Ti/Ag piece, the efficiency would have been 8.9%.

Table 29. Device properties achieved using films deposited as described in Table 28.

Cell	Contact	V_{oc}, V	J_{sc}, mA/cm^2	FF %	Eff., %	R_{oc}, Ω-om^2	QE (400)	QE (700)
4296-21-1	ZnO/Ag	0.84	14.6	69.4	8.5	7.5	0.49	0.49
4296-22-1	Ti/Ag	0.83	13.3	72.5	8.1	5.2	0.49	0.30

2.4.10 Multijunction Cell Modeling

A multijunction cell model is needed as a guide to help prioritize and clarify device and material research issues for the Multijunction Device Design Team. An optical model is being developed at IEC to calculate the current in each component of a multijunction cell based on the optically-limited QE. Detailed optical models have already been developed by others (52, 53) but are not generally available. The QE model used here accounts for glass reflection R_f, TCO absorption ATCO, p-layer absorption, generation in the i-layer, multiple passes (m) due to light trapping and back reflection (R_b). Measured values of R_f (7%) and ATCO are used. Literature values of m and R_b used. The optical thickness of each i-layer is (nD). Absorption losses in the TCO and p-layer limit the blue response and are important primarily for the top cell while optical enhancement of red response due to m and R_b are important only for the bottom cell. Absorption coefficients for a-Si (top cell i-layer) and a-SiGe (middle and bottom cell i-layers) have been provided by Solarex and USSC.

While the optical model is still evolving, certain conclusions are possible. For example, accounting for window layer losses affecting the top cell, we find: front reflection losses (0.7 mA/cm^2), absorption losses in Solarex SnO_2 (1.1 mA/cm^2), and p-layer losses (0.5-0.8 mA/cm^2). To generate 8 mA/cm^2 in the top cell requires 800 Å if the i-layer bandgap is 1.73 eV and 1100 Å if the i-layer is 1.80 eV. These bandgaps span the range currently used for non-alloyed a-Si top cells. To generate 8 mA/cm^2 in the middle cell requires about 1600 Å if the i-layer is 1.60 eV but over 4000 Å if the middle cell bandgap is 1.73 eV. Thus, selection of the middle cell bandgap should be based on stability considerations.

Significant effort has been made in modeling the electrical performance of multijunction cells. The goal is to develop a measurement-based model which requires a limited number of input parameters. Such a model would be complementary to detailed numerical simulations based on fundamental semiconductor physics such as AMPS. Previously we had used the SPICE circuit model program to analyze the multijunction device using lumped circuit models (1). However, SPICE was found to be incapable of accurately representing the voltage dependent photo current collection. A model of triple junction cells has been developed instead using the parametric JV analysis described in Section 3. A preliminary result confirms that current limiting the multijunction device with the top cell (having the highest FF and V_{oc}) yields a better FF than if all three components are current matched. This confirms modeling and experimental results from Solarex (54) where it is found that current imbalance always results in a higher FF for the triple junction. Presently, we are analyzing JV data of single junction component cells from Solarex and USSC to obtain the six parameters which characterize the JV behavior. These will be used as input parameters to calculate the triple junction JV behavior. Then, sensitivity of

performance to various parameters (collection length, built-in voltage, current mismatch) will be investigated to guide priorities in Team research.

3.0 SOLAR CELL MEASUREMENTS AND ANALYSIS

3.1 ABSTRACT

A procedure has been developed for accurately representing the current voltage (J-V) characteristics of polycrystalline and amorphous silicon solar cells. The measured J-V data is separated into a forward diode current (J_D) and a (possibly voltage dependent) light generated current (J_L). The forward diode current (J_D) is analyzed in terms of a set of standard diode parameters (A, J_0, J_{00} and E_G). The justification for applying these standard diode parameters is based on a model in which the forward diode current (J_D) is controlled by recombination within the active light absorbing material. The possibly voltage dependent light generated current (J_L) is characterized using a simple electric field dependent collection model derived for a-Si devices. Resistive losses are usually represented by a series resistance (R_S) and infrequently a shunt conductance (G_{SH}). Very good agreement is found between measured and calculated current voltage (J-V) characteristics from reverse to forward voltage bias in a variety of cells, illumination levels and temperatures.

In addition, another method is being developed to use standard spectral response and capacitance measurements in order to get a separate estimate of the total minority carrier collection width $(L_{eff} = w + L)$ due to the electric field collection width (w) and that due to diffusion length (L). This technique is demonstrated for $Cu(In,Ga)Se_2$ devices.

3.2 INTRODUCTION

Part of the program plan for 1993 and 1994 has been to develop a set of analysis tools that will provide the parameters, when coupled with simple modeling equations, needed to accurately represent the current voltage behavior of thin film polycrystalline and amorphous solar cells over the voltage, illumination and temperature ranges of interest. This was intended as an aid to help determine the mechanisms and quantify the losses that limit V_{oc} in these devices.

Because the parameters derived from the analysis can accurately describe the entire current voltage behavior, they are also useful in predicting the performance of a solar cell either under different operating conditions or as a component of a completed module or a multijunction structure. These parameters can also be used to determine the areas of solar cell development and processing where improvements will have the largest impact on performance. Finally, this parametric representation can be used to establish relationships of how changes in either material properties or processing and manufacturing can affect solar cell output.

These techniques are also beginning to be applied to spectral response and capacitance measurements in the case of $Cu(In,Ga)Se_2$ devices.

3.3 J-V ANALYSIS

The analysis is based on applying simple established models of device behavior. The applicability of these models is tested by the agreement between calculated and experimental data. The form of the forward diode current is assumed to be exponential with voltage $\left(J \propto e^{kV}\right)$ whose magnitude and temperature dependence is determined by recombination with an exponential density of gap states within the active light absorbing material (55, 56). Usually, the forward bias diode current is independent of light intensity. The light generated current is separated into a voltage independent

(i.e. constant) and a voltage dependent part. The voltage dependent part of the light generated current is analyzed by applying a model (57, 58) which uses an averaged electric field and photocarrier generation in the region of the device where voltage or electric field dependent photocarrier collection takes place. The light generated current is usually independent of temperature over the ranges of interest. The net current through the device is, ignoring series and shunt resistive losses, the difference between the dark and light generated currents.

$$J(V_D) = J_D(V_D) - J_L(V_D) \tag{3.1}$$

Small series and shunt resistive losses can be included with a resistive term (R_S) and a conductive term (G_{SH}) leading to the form:

$$J(V) = J_D(V - R_S J) - J_L(V - R_S J) + G_{SH} V \tag{3.2}$$

where the voltage (V_D) across the junction region is reduced from the terminal voltage (V) by the series resistance (R_S) and the output current is lowered by the shunt conductance (G_{SH}).

Like amorphous silicon based devices, it appears that most high efficiency polycrystalline thin film solar cells such as those based on CdTe and $CuInSe_2$ and its alloys operate with the diode current being controlled by recombination within the active light absorbing material (59 - 62). This is due to the material being inverted, (i.e. changing from p to n-type) near or within the active light absorbing material. This also helps in eliminating interface recombination as a loss mechanism in these devices.

The recombination is then controlled by states within the bandgap in this region. When these states are localized near the center of the bandgap, the diode or recombination current can be expressed as (63) :

$$J_D = J_{Recombination} = J_0 e^{\left(\frac{qV_D}{2kT}\right)} \tag{3.3}$$

where:

$$J_0 = J_{00} e^{\left(-\frac{E_G}{2kT}\right)} \tag{3.4}$$

For additional levels, the total recombination can be summed and expressed numerically. However, when the recombination is through an exponential distribution of recombination centers i.e. :

$$N_{Recombination}(E) \sim e^{\left[-\frac{(E_C - E)}{kT^*}\right]} \tag{3.5}$$

or;

$$N_{Recombination}(E) \sim e^{\left[-\frac{(E - E_V)}{kT^*}\right]} \tag{3.6}$$

Then, for T* >> T , the diode or recombination current can be expressed in closed form as (55, 56):

$$J_D = J_{Recombination} = J_0 e^{\left(\frac{qV_D}{AkT}\right)} \qquad (3.7)$$

where the diode quality factor (A) becomes slightly temperature dependent and not necessarily equal to one or two, i.e. :

$$A = \frac{2}{1+\frac{T}{T^*}} \quad \text{and} \quad 1 < A < 2 \qquad (3.8)$$

A plot of the temperature dependence of the diode quality factor for various T* is shown in Figure 34. The reverse saturation current remains the same as before (Equation 3.4). This means that the diode component of the solar cell current-voltage characteristic becomes:

$$J_D = J_0 e^{\frac{qV_D}{AkT}} \qquad (3.9)$$

This is the standard diode exponential behavior with a diode quality factor that has a slight temperature dependence.

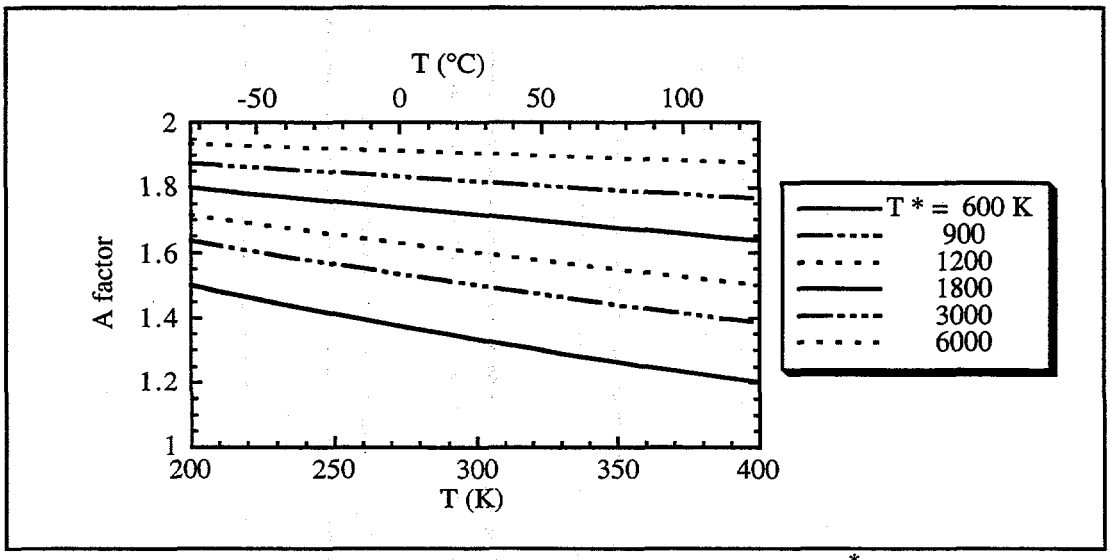


Figure 34. The temperature dependence of the diode A factor arising from T^*. (see Equation 3.8)

The light generated current (J_L) in a solar cell can be separated into two parts. One is due to the minority carriers collected by diffusion which is independent of the applied voltage (J_{L0}) and the other is due to minority carriers collected by drift or electric field which is voltage dependent $J_L(V)$. i.e. :

$$J_L = J_{L0} + J_L(V_D) \qquad (3.10)$$

The voltage dependent light generated current (J_{LV}) decreases with increasing forward voltage bias because of the reduction (and possible reversal) in the minority carrier collecting internal electric field. There is a simple closed form expression for the voltage dependent light generated current derived by Crandall for use with amorphous silicon based devices (57). In this case the voltage dependent light generated current can be expressed in the form:

$$J_L(V_D) = J_{LV}\, F(x) \tag{3.11}$$

with;

$$F(x) = x\left(1 - e^{\frac{-1}{x}}\right) \quad \text{and} \quad x = k_1\left(1 - \frac{V_D}{V_B}\right) \tag{3.12}$$

To get an idea of the behavior of the function expressed in Equations 3.10 and 3.11, a plot of the normalized form is shown in Figure 35 for various values of k_1.

Crandall derived the above form for the case assuming a region of thickness (D), with uniform optical carrier generation, a constant electric field given by:

$$F = \frac{(V_B - V_D)}{D} \tag{3.13}$$

and an electric field collection width (L_C) that depends on the mobility (μ) and lifetime (τ) in the form:

$$L_C = \mu \tau F \tag{3.14}$$

so that;

$$k_1 = \frac{L_C}{D} \tag{3.15}$$

The form of Equations 3.10 and 3.11 accurately represents the voltage dependent current behavior of amorphous silicon devices, as will be seen in Section 3.4. In addition, they can also be used, although with less physical justification, to represent the much smaller $J_L(V)$ effects in CdTe devices (see Section 3.6). Usually, the temperature dependence of the light generated current can be neglected.

Finally, the effects of possible parasitic shunting, such as conductivity along edges or defects, and resistive losses, due to contacting and sheet resistance, are taken into account with a shunt conductance term (G_{SH} V) and a series resistance term (R_S J) respectively. The value of the shunt conductance (G_{SH}) is usually assumed to be small (≤ 10 mS/cm^2). However, the series resistance term (R_S) can be significant and dependent on the value of the device current, $R_S(J)$, because of non-ohmic contact effects. When the major part of the series resistance is due to non-ohmic contact effects, it will vary significantly with temperature.

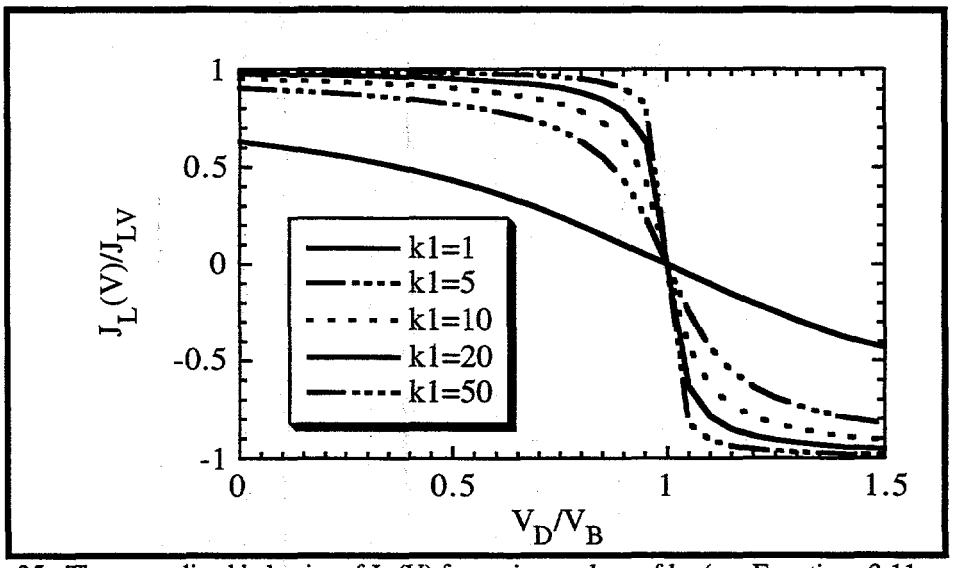


Figure 35. The normalized behavior of $J_L(V)$ for various values of k_1.(see Equations 3.11 and 3.12)

3.3.4 Methods of Analyzing J-V Measurements

The final set of equations used for the analysis of J-V measurements are:

$$J = J_0 e^{\frac{q(V_D)}{AkT}} - J_{L0} - J_L(V_D) + G_{SH} V_D \qquad (3.16)$$

with;

$$V_D = V - R_S J \qquad (3.17)$$

and;

$$J_L(V_D) = J_{LV} F(x) \qquad (3.18)$$

with;

$$F(x) = x\left(1 - e^{\frac{-1}{x}}\right) \quad \text{and} \quad x = k_1\left(1 - \frac{V_D}{V_B}\right) \qquad (3.19)$$

This means that, in the most complicated case, there will be eight parameters needed to represent the J-V behavior of a device (J_0, A, J_{L0}, J_{LV}, k_1, V_B, R_S and G_{SH}). The rest of this section will show (with examples) how these parameters are determined from the actual J-V measurements.

The J-V data is collected digitally in terms of pairs of current-voltage data. Usually the measurement is taken by sweeping the voltage both forward and reverse to check for any hysterisis effects. Because this data will be differentiated numerically, special care is taken to keep electrical noise out of the data. This can be done by paying extra attention to cabling, device contacts and the power supplies that provide the sweep voltage and the electrical power for the bulbs.

In order to simplify the analysis, the initial J-V measurements are made in a region of either sufficiently low light intensity or of large enough forward voltage bias so that the voltage dependent part of the light generated current, $J_L(V)$, can be neglected. i.e. :

$$J_0 e^{\frac{qV_D}{AkT}} - J_{L0} + G_{SH} V_D >> J_L(V_D) \qquad (3.20)$$

In the case of Cu(In,Ga)Se_2 devices, this is always true for all measured voltages and light intensities, because $J_L(V)$ is always small. In CdTe based devices, using the part of the J-V data in forward bias that is at least a few mA/cm^2 above J_{SC} will suffice for all light intensities, since $J_{L0} >> J_L(V_D)$. However, for amorphous silicon based devices, because $J_L(V_D) >> J_{L0}$, a lowered light intensity where the short circuit current (J_{SC}) can be neglected is used. In this case it is also assumed that the change in light intensity only affects the light generated current (J_L). In all cases the J-V equation can be written as (if $R_S G_{SH} << 1$) :

$$J - G_{SH} V + J_{SC} = J_0 e^{\frac{q}{AkT}(V - R_S J)} \qquad (3.21)$$

In reverse voltage bias or near short circuit current, the diode current on the right hand side of Equation 3.21 can be neglected, so that the shunt conductance can be determined from a simple straight line fit of the J-V data as shown in Figure 36.

If the forward voltage bias where $J >> G_{SH} V$ is examined, rearranging Equation (3.21) gives:

$$V = R_S J + \left(\frac{AkT}{q}\right)\left[\mathrm{Ln}(J + J_{SC}) - \mathrm{Ln}(J_0)\right] \qquad (3.22)$$

Differentiating with respect to current gives (if the series resistance (R_S) is a constant with respect to current) :

$$\frac{dV}{dJ} = R_S + \frac{AkT}{q}(J + J_{SC})^{-1} \qquad (3.23)$$

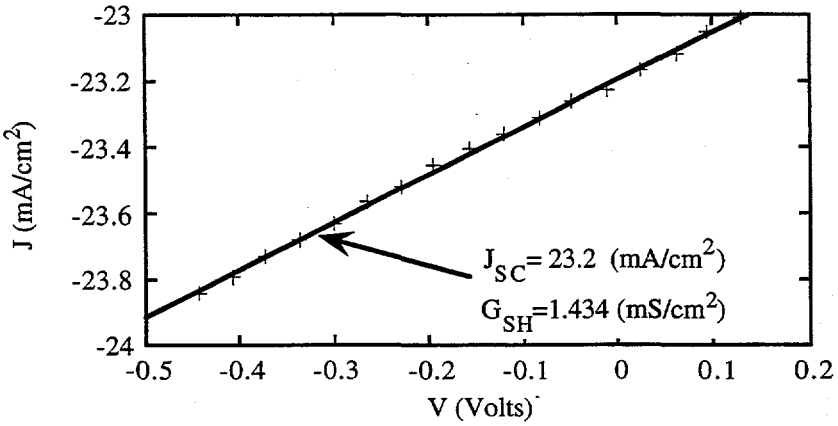


Figure 36. A plot of J vs. V near J_{SC} to demonstrate the effects of a shunt conductance (G_{SH}).

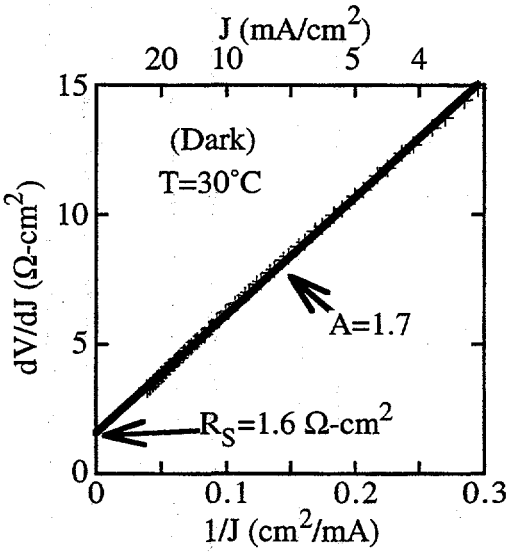


Figure 37. The slope of a dark J-V curve of an amorphous silicon device (IEC GD4326-22-1) as a function of the inverse current.

In this case a straight line fit to the slope of the J-V data at a given temperature T will determine the value of the series resistance (R_S) and the diode quality factor (A) as shown in Figure 37. With a value for the series resistance, the reverse saturation current, as well as a check on the diode quality factor (A), can be found from a plot of a rearranged form of Equation 3.22 i.e. :

$$(V - R_S J) = \left(\frac{AkT}{q}\right)\left[\mathrm{Ln}(J + J_{SC})\right] - \left(\frac{AkT}{q}\right)\mathrm{Ln}(J_0) \qquad (3.24)$$

as shown in Figure 38.

To completely characterize the J-V behavior of amorphous silicon (and infrequently CdTe) based devices it is still necessary to determine the behavior of the voltage dependent light generated current. After the parameters characterizing the diode and resistive losses have been determined, these components can be subtracted from the J-V data leaving the light generated current (J_L) as shown :

$$J_L = J - G_{SH} V - J_0 e^{\frac{q}{AkT}(V - R_S J)} \qquad (3.25)$$

This remainder is shown for an amorphous silicon device in Figure 39. As can be seen from equations 3.18 and 3.19, the parameter (J_{LV}) can be found from the limiting current in reverse bias and the built in voltage parameter (V_B) can be determined from the voltage at which the light generated current becomes zero. Finally, the curvature factor (k_1) can be fairly easily determined by a few trial and error attempts to fit the data (as shown in Figure 39).

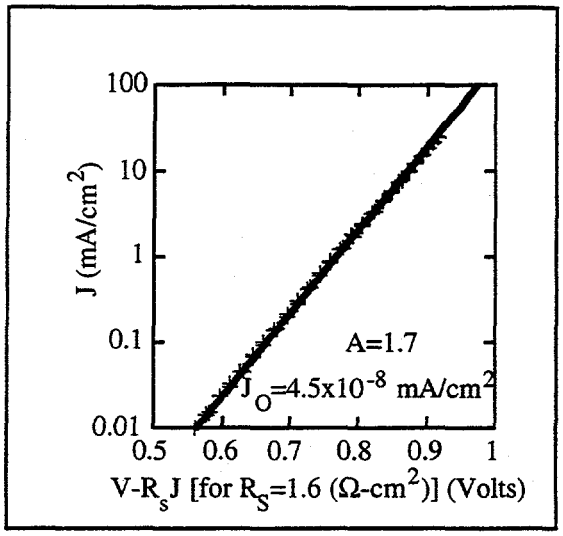


Figure 38. The dark J-V curve of an amorphous silicon device (IEC GD4326 22-1) as a function of the diode voltage.

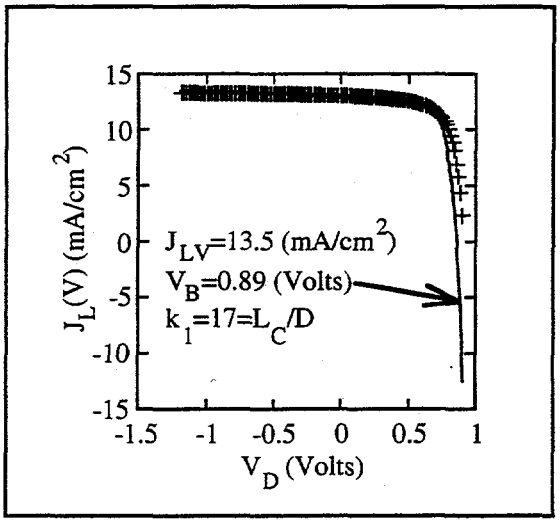


Figure 39. A graph of remaining J_L(V) of an amorphous silicon device (IEC GD4326-22-1) as a function of the diode voltage.

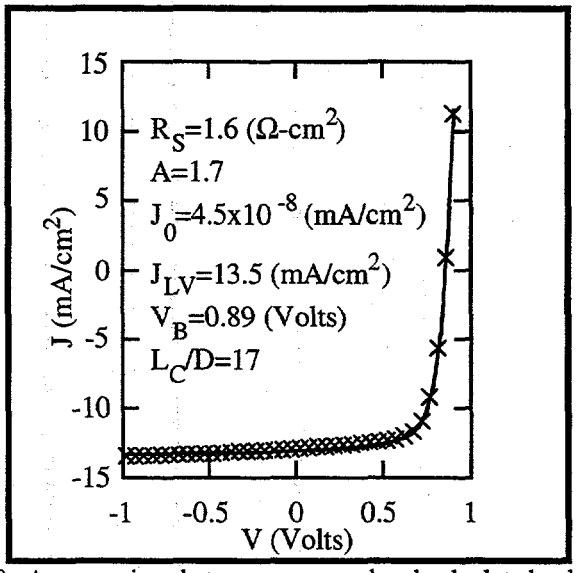


Figure 40. A comparison between measured and calculated values of the illuminated J-V curve of an amorphous silicon device (IEC GD4326-22-1).

The last thing to determine is how well these parameters represent the original J-V data. This can be done by comparing or subtracting the original data from that calculated by the parametric fit. This is an important step that will both show the quality or appropriateness (i.e. whether the assumptions made are correct for the case being examined) of the representation and catch most errors. An example is shown in Figure 40.

3.3.2 a-Si Devices

The examples of the analysis of $J_L(V)$ in the previous section show that the model expressed by Equations 3.18 and 3.19 are an excellent fit to the $J_L(V)$ behavior of amorphous silicon devices. However, to be useful the curvature fitting parameter (k_1) should be related to actual transport properties of the amorphous silicon i-layer. From Equations 3.13 to 3.15 it can be seen that :

$$\frac{L_C}{D} = \frac{\mu\tau F}{D} = \frac{\mu\tau(V_B - V_D)}{D^2} \qquad (3.26)$$

If the i-layer thickness (D) is varied while keeping the rest of the processing steps the same (i.e. the same V_B in all cases), it should be possible to measure the transport properties ($\mu\tau$) as a function of i-layer thickness. The analysis was applied to devices deposited at APS having D from 0.2 to 0.6 μm (64). Results are shown in Table 30. Note that as D increased, fill factor decreased from 74% to 63% and L_C/D decreased from 27 to 8.5. Figure 41 shows the $\mu\tau$ value determined using Equation 3.26, suggesting an improvement in i-layer quality with increasing D. This may be due to greater defect density in material grown near the substrate, or due to the relatively greater influence of interface recombination in thin i-layers. The technique presented here yields a single value of $\mu\tau$ for each device representing the average throughout the i-layer. Values of $\mu\tau$ for holes of 0.5-3x10^{-8} cm^2/V are commonly reported (65-68) while values of $\mu\tau$ for electrons are in the range from 10^{-7} to 10^{-6} cm^2/V. Thus, L_C as determined here is the hole collection length. These measurements support the "limiting carrier" argument (69), i.e. the carrier with the shorter collection length or $\mu\tau$ (ordinarily holes) limits the collection.

It is well known that light exposure increases the defect density in a-Si material and reduces the $\mu\tau$ product of electrons and holes. Therefore, it is expected that L_C/D should also change with light soaking. A device deposited at IEC was characterized in the annealed state and after 90 hours light exposure (see Section 2.4.4) as shown in Table 31.

The fill factor decreased from 69 to 49% corresponding to L_C/D decreasing from 14 to 3. The dark diode and photo current parameters also changed slightly with light exposure as shown in Table 31. To determine if the effect of light soaking could be described solely by changes in L_C/D, the AM1.5 illuminated JV data after light soaking were also fit with the same five parameters (A, J_0, R, J_{LV}, and V_B) as determined for the annealed case but with $L_C/D=3$ as found from light soaking. Figure 42 shows a very good fit to the light soaked data changing only L_C/D from 14 to 3. Clearly, the effect of light soaking can be represented primarily by changes in L_C/D.

The method presented here allows routinely measured amorphous silicon data J-V to be analyzed to yield parameters containing fundamental information about the i-layer material quality and its relation to the device structure and performance. Although the approach (58, 59) contains broad approximations and assumptions, good agreement is found between AM1.5 J-V measurements and calculation on cells with very good and very poor fill factors. The method is closely linked to experiment. Five parameters are obtained directly from the measured data, requiring only one parameter L_C/D to be fitted. The method has been successfully applied to cells with fill factors from 74 to 49% and with thicknesses from 0.2 to 0.6 μm. The $\mu\tau$ values ($2\text{-}4\times10^{-8}$ cm^2/V) are consistent with hole transport. Effects of light induced degradation can be modeled with only one parameter, L_C/D .

Table 30. Extracted device parameters with measured and calculated solar cell performance for APS solar cells having i-layer thicknesses 0.2<D<0.6μm.

D (μm)	R_S (Ω-cm^2)	A	J_0 (mA/cm^2)	J_{LV} (mA/cm^2)	V_B (V)	L_C/D
0.22	2.1	1.54	$7x10^{-9}$	10.4	0.837	26.8
0.25	2.4	1.48	$5x10^{-9}$	10.6	0.827	24.9
0.31	2.8	1.54	$8x10^{-9}$	12.6	0.863	22.5
0.38	3.5	1.54	$7x10^{-9}$	13.6	0.850	19.0
0.43	2.5	1.54	$9x10^{-9}$	11.1	0.853	17.2
0.48	2.6	1.67	$1x10^{-8}$	12.4	0.867	14.5
0.54	2.2	1.67	$1x10^{-8}$	12.1	0.880	9.8
0.57	3.5	1.67	$1x10^{-8}$	12.1	0.861	10.0
0.58	2.7	1.67	$1x10^{-8}$	12.1	0.883	8.5

D (μm)		V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Eff. (%)
0.22	calc	0.815	10.2	73.8	6.1
	meas	0.816	10.1	74.2	6.1
0.25	calc	0.803	10.3	74.1	6.1
	meas	0.803	10.3	73.5	6.1
0.31	calc	0.827	12.3	71.7	7.3
	meas	0.829	12.2	72.2	7.3
0.38	calc	0.823	13.2	69.5	7.6
	meas	0.826	13.2	69.5	7.6
0.43	calc	0.814	10.8	70.5	6.2
	meas	0.812	10.7	71.3	6.2
0.48	calc	0.851	12.1	68.5	7.1
	meas	0.853	12.0	69.5	7.1
0.54	calc	0.852	11.5	65.0	6.4
	meas	0.854	11.6	64.2	6.4
0.57	calc	0.840	11.5	63.8	6.2
	meas	0.844	11.6	63.2	6.2
0.58	calc	0.853	11.4	63.2	6.1
	meas	0.853	11.5	62.8	6.1

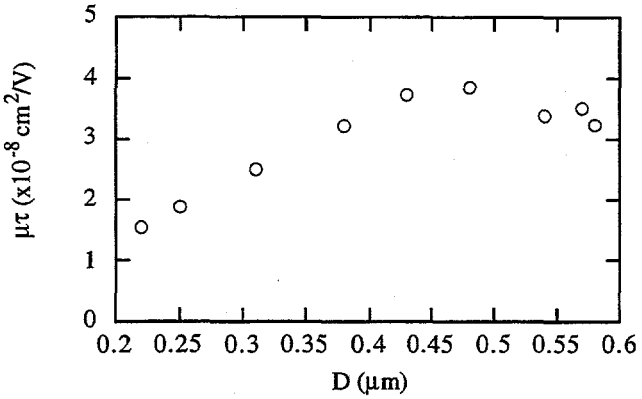


Figure 41. The behavior of μτ as a function of i-layer thickness for a group of APS amorphous silicon solar cells.

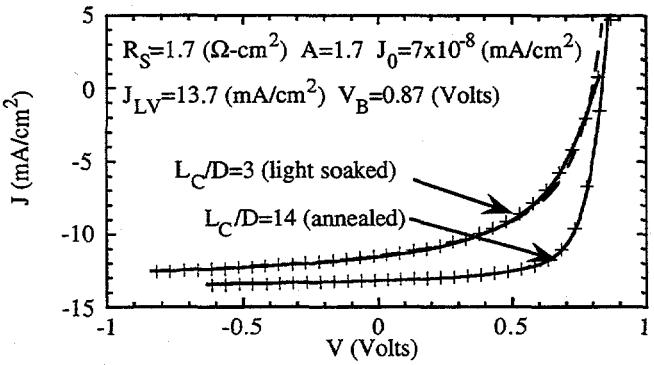


Figure 42. A comparison between measured and calculated values for a light soaked and annealed amorphous silicon device (IEC GD4304-22-2) using the same device parameters for both except L_C/D.

Table 31. Extracted device parameters for the a-Si device IEC GD4304-22-2 in both the annealed and light soaked states.

State	A	J_0 (mA/cm^2)	R_S (Ω-cm^2)	J_{LV} (mA/cm^2)	V_B	L_C/D
annealed	1.7	$7x10^{-8}$	1.7	13.7	0.87	14.1
light soaked	2.3	$2x10^{-6}$	2.6	13.6	0.83	3.1

3.3.3 Cu(In,Ga)Se_2 Devices

In the case of Cu(In,Ga)Se_2 solar cells, because the light generated current (J_L) is independent of voltage, the illuminated J-V analysis is simplified (1, 70). In this case, the light generated current

is the short circuit current (J_{sc}) and Equations 3.21-3.24 accurately represent the current voltage behavior of these devices. This is shown in Figures 43 and 44.

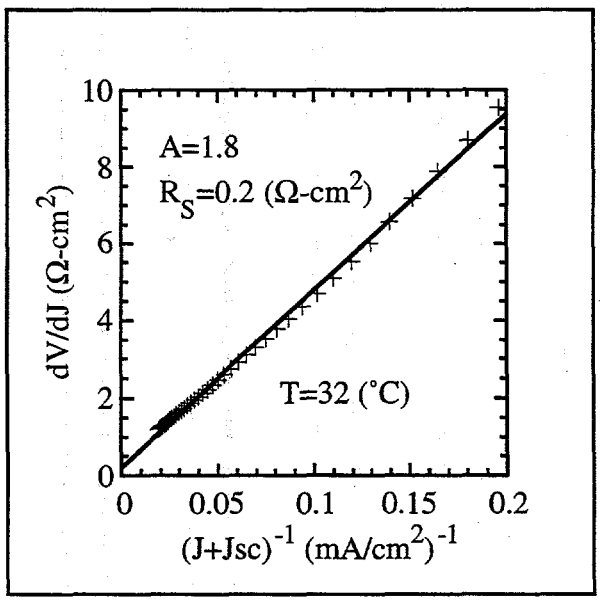


Figure 43. The slope of an illuminated J-V curve of a high efficiency $Cu(In,Ga)Se_2$ device (IEC 32535-33-10) as a function of the inverse current.

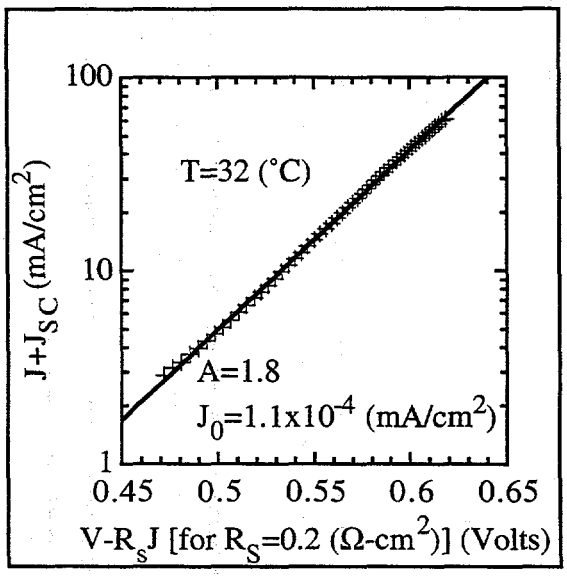


Figure 44. The illuminated J-V curve of a high efficiency $Cu(In,Ga)Se_2$ device (IEC 32535-33-10) as a function of the diode voltage.

At lower temperatures, most of these devices have a current dependent series resistance R_S (J) (1, 59, 61, 70) due to non-ohmic contacts (as shown in Figure 45). In this case, the analysis of V_{OC} and J_{SC} as a function of temperature and light intensity can be used to extract E_G, T* (and

therefore A) and J_{00} because the effects of the current dependent series resistance $R_S(J)$ are zero at open circuit voltage (i. e. J=0). From Equation 3.22:

$$V_{OC} = \left(\frac{AkT}{q}\right)\left[Ln(J_{SC}) - Ln(J_0)\right] \tag{3.27}$$

or using Equations 3.4 and 3.8;

$$V_{OC} = \left(1 + \frac{T}{T^*}\right)^{-1}\left[\frac{E_G}{q} + \left(\frac{2kT}{q}\right)Ln\left(\frac{J_{SC}}{J_{00}}\right)\right] \tag{3.28}$$

which can be rewritten in a form useful in determining E_G, J_{00} and T^* by linear regression techniques i. e.;

$$V_{OC} - \left(\frac{2kT}{q}\right)Ln(J_{SC}) = \frac{E_G}{q} - \left(\frac{2kT}{q}\right)Ln(J_{00}) - \frac{TV_{OC}}{T^*} \tag{3.29}$$

An example of the results of this type of analysis is shown in Figure 46.

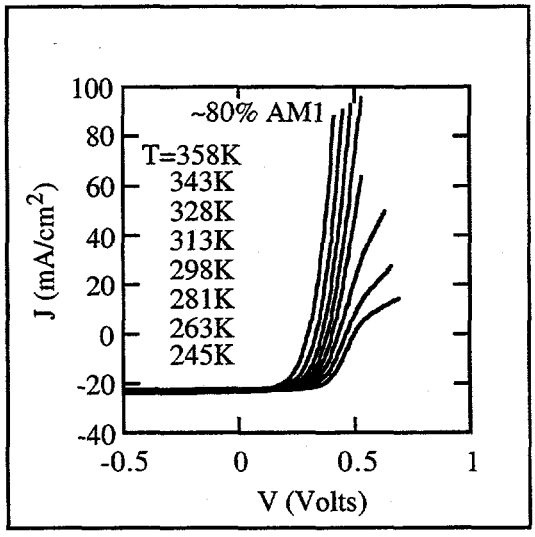


Figure 45. J-V data as a function of temperature for the $CuInSe_2$ device EC-32220-22-5 (note the non-ohmic behavior at lower T in forward bias).

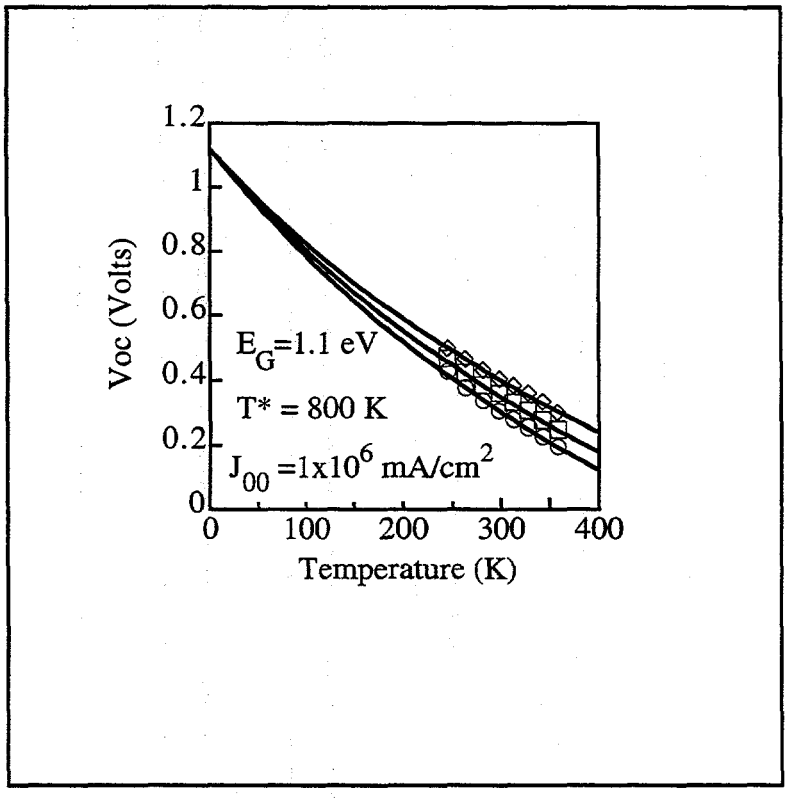


Figure 46. V_{oc} as a function of temperature and light intensity (~5% AM1, ~20% AM1 and ~80% AM1) for the $CuInSe_2$ device IEC-32220-22-5. The lines are calculated using the values for E_G, J_{00} and T* shown.

In determining whether this type of model can account for the observed J-V behavior in Cu (In,Ga)Se_2 polycrystalline thin film solar cells, ten different devices made by various processes and manufacturers have been examined (1, 61, 70). J-V data was taken over a range of temperatures (218K to 373K) and light intensities (dark, ~ 5% AM1, ~20% AM1 and ~80% AM1). This usually involved forty sets of J-V data for each device. The results of analyzing this data according to Equation 3.29 (i.e. V_{oc} as a function of temperature and light intensity) are presented in Table 32.

Table 32. A summary table of the diode parameters extracted from measurements of V_{oc} as a function of temperature and light intensity for various Cu(In,Ga)Se_2 devices.

$CuInSe_2$

Deposition Method	Manufacturer	E_G (eV)	T^* (K)	J_{00} (mA/cm^2)	Device I.D. #
elem. evap.	IEC	1.1	800	$1x10^6$	IEC-32220-22-5
elem. evap.	IEC	1.1	1300	$2x10^6$	IEC-32187-22-12
	EPV	1.1	2000	$4x10^6$	EPV-11133-21-5
	Stuttgart	1.2	1000	$6x10^6$	STU-M243-4
selen. Se	IEC	1.2	800	$6x10^6$	IEC-61079-23-5
selen. H_2Se	IEC	1.1	1700	$2x10^6$	IEC-89095-2-9

Cu(In,Ga)Se_2

Deposition Method	Manufacturer	E_G (eV)	T^* (K)	J_{00} (mA/cm^2)	Device I.D. #
	Siemens Solar	1.2	1200	$7x10^6$	SSI-16543-4-3
elem. evap.	IEC	1.3	2000	$4x10^6$	IEC-32356-33-5
elem. evap.	NREL	1.3	1000	$2x10^6$	NREL-S478-14-5
elem. evap.	NREL	1.4	1500	$2x10^6$	NREL-S416-23-5

In conclusion, the simple equations presented here appear to represent the J-V behavior of various Cu(In,Ga)Se_2 devices over a wide range of processing parameters, manufacturing methods and both illumination and temperature test conditions.

3.3.4 CdTe Devices

With most CdTe based solar cells, there is a small, but measurable voltage dependent light generated current. However, it is small enough so that the simplified analysis used for Cu(In,Ga)Se_2 devices and described in the previous section can be applied (at least in regions of the current voltage characteristic that are slightly removed from J_{SC}). This is shown by comparing the illuminated and dark characteristics as seen in Figures 47 and 48. Here the slight differences are due to a small $J_L(V)$ effect (1, 62).

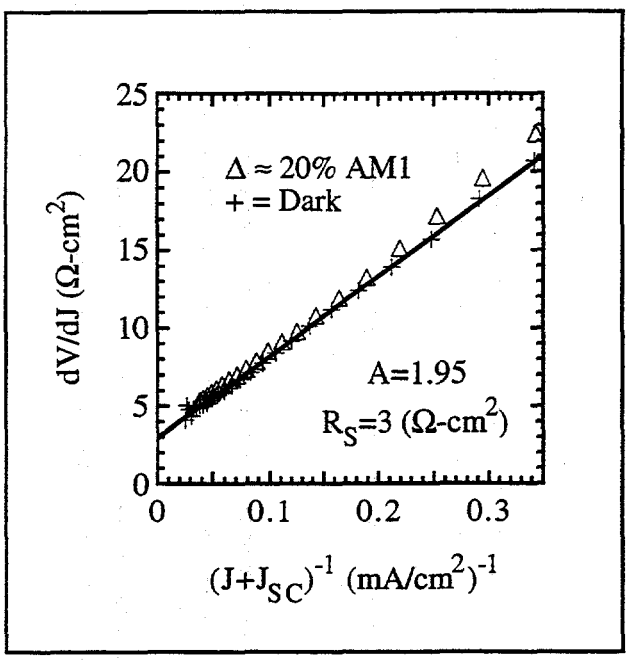


Figure 47. The slope of the illuminated and dark J-V curves of a CdTe based device (IEC 40803-22-8) as a function of the inverse current.

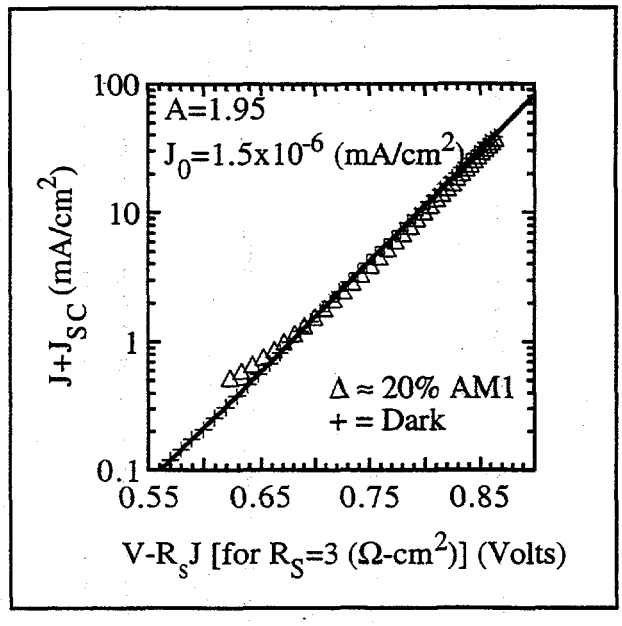


Figure 48. The illuminated and dark J-V curves of a CdTe based device (IEC 40803-22-8) as a function of the diode voltage.

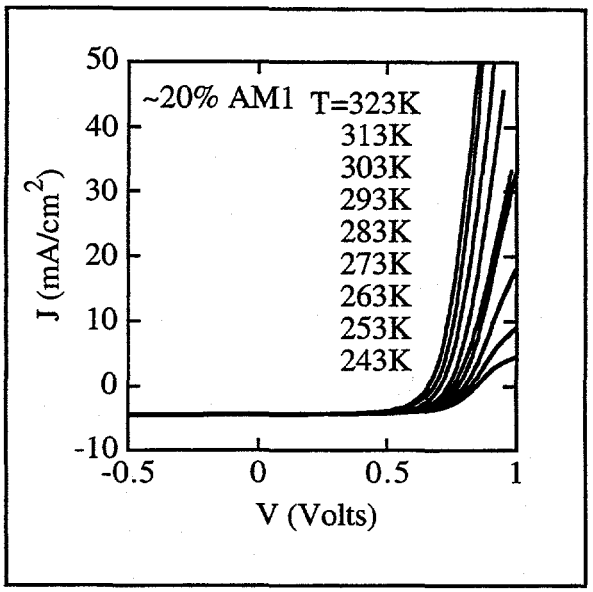


Figure 49. J-V data as a function of temperature for the CdTe device IEC-40803-22-8 (note the non-ohmic behavior at lower T in forward bias)

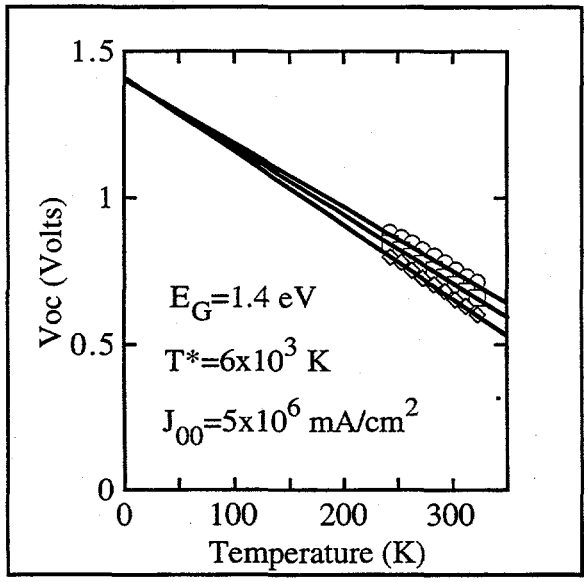


Figure 50. V_{oc} as a function of temperature and light intensity (~5% AM1, ~20% AM1 and ~80% AM1) for the CdTe device IEC-40803-22-8. The lines are calculated using the values for E_G, J_{00} and T^* shown.

Again, similar to Cu (In,Ga)Se_2 devices, CdTe based solar cells have a current dependent series resistance $R_S(J)$ (1, 62, 70) due to non-ohmic contacts (as shown in Figure 49). In this case, as before, the analysis of V_{oc} and J_{sc} as a function of temperature and light intensity can be used to extract E_G, T^* (and therefore A) and J_{00}. An example of the results of applying Equation 3.29 to these measurements is shown in Figure 50.

To determine whether this type of model can account for the observed J-V behavior in CdTe based devices, four different devices made by two different processes and manufacturers have been examined (70). J-V data was taken over a range of temperatures (240K to 340K) and light intensities (dark, ~ 5% AM1, ~20% AM1 and ~80% AM1). This usually involved forty sets of J-V data for each device. The results of analyzing this data according to Equation 3.29 (i.e, V_{oc} as a function of temperature and light intensity) are presented in Table 33.

Table 33. A summary table of the diode parameters extracted from measurements of V_{oc} as a function of temperature and light intensity for various CdTe based devices.

Deposition Method	Manufacturer	E_G (eV)	T^* (K)	J_{00} (mA/cm^2)	Device I.D. #
PVD.	IEC	1.4	6000	$5x10^6$	IEC-40803-22-8
PVD.	IEC	1.4	1400	$1x10^5$	IEC-40821-21-7
	Solar Cells Inc.	1.4	4000	$1x10^6$	SCI-L9808-24-4
	Solar Cells Inc.	1.5	1500	$2x10^5$	SCI-L10304-26-6

In conclusion, the simple equations used appear to account for the observed J-V behavior in CdTe based devices, of four different devices made by two different processes and manufacturers under a fairly wide range of both illumination and temperature test conditions.

3.4 SPECTRAL RESPONSE AND CAPACITANCE ANALYSIS

3.4.1 Introduction

Systematic studies and optimization of new solar cell materials require reliable numerical data obtained from film and/or device analysis. The diffusion length for minority carriers is an important parameter describing a semiconductor and is of direct relevance for the photovoltaic performance. A variety of techniques to measure the diffusion length is available. However, for polycrystalline thin films questions concerning the reliability of the obtained data arise. The main difficulty is caused by the fact that absorption length, space charge layer, film thickness, grain size and diffusion length may well be within the same order of magnitude. In many cases only an "effective" value can be derived from the measurement. It is therefore advantageous to use data that are as closely as possible related to the real photovoltaic performance of the cell.

3.4.2 Method of Approach

In our current work we have performed numerical fits of measured spectral quantum efficiencies (QE) to analytical approximations to estimate diffusion length (L) and width of the field zone (w) in the absorber. Analytical approximations for the quantum efficiency are derived by neglecting the influence of majority carriers and by assuming complete collection in the space charge layer. The derivation is well known from textbooks and is based on Gärtner's work (71).

According to this and assuming that the width of the quasi-neutral region (d), which is equal to the thickness of the absorber minus the thickness of the space charge layer (w), is much greater than the diffusion length (L), the internal quantum efficiency (IQE) is written as:

$$IQE = 1 - \frac{e^{-\alpha w}}{1+\alpha L} \qquad (3.30)$$

where α is the optical absorption coefficient in the absorber. The measured (external) QE differs from this expression due to e.g. reflection, absorption in the window, recombination at or near the interface. Those deviations are expected to depend on the photon energy only weakly, at least in the limited range used for the fit. They are therefore taken into account by allowing measured and calculated QE to differ by a constant factor k. In some cases, e.g. free carrier absorption in highly doped thick ZnO or when films are very smooth (interference fringes) this assumption may not be totally correct.

The absorption coefficient as a function of the wavelength of the incident light must be known in order to calculate the electronic parameters from the measured QE. In the case of $Cu(In,Ga)Se_2$, where the absorption varies strongly with the In/Ga ratio in the film, it is not very practical to use witness samples (without the Mo contact) and transmission measurements. Instead, it is assumed that the absorption can be described analytically by the following expression:

$$\alpha = \frac{k_2}{h\nu}\sqrt{h\nu - E_G} \qquad (3.31)$$

Where k_2 is taken from a transmission measurement and is assumed to be constant for all samples. Equation 3.31 holds only in a certain range of photon energies above E_G and the fit has to be restricted accordingly.

Combining Equations 3.30 and 3.31 and fitting to the measured QE the free parameters k_2, L, w and E_G may be obtained. However, as a consequence of abandoning absolute values by introducing the k factor, the values obtained for w and L are not reliable, i.e. different values are obtained depending on the initial guess of w and L supplied to the fit algorithm. Nevertheless, for a given measurement the sum of w + L is approximately constant for different fits. The problem arises because the functions $1-e^{-y}$ and $1-(1+y)^{-1}$ have a very similar shape in the wavelength region used for the fit. As long as other errors are bigger than the difference between these functions it is not possible to distinguish between the contributions of w and L to the current collection. It is therefore more appropriate to use the following function as a target for the fit:

$$QE = k_3\left(1 - e^{-\alpha L_{eff}}\right) \qquad (3.32)$$

The fit parameter L_{eff} will be equal to the sum of w + L within an error of less than ±30% if, in the wavelength range of the fit, the values of αL_{eff} are within $(1 \le \alpha L_{eff} \le 3.5)$. The lost information can be recovered by determining w independently from capacitance or by using QE data obtained at different voltages and assuming that $w \propto \sqrt{(V_B - V)}$. Since $E_G \approx 1.15$ eV in our samples, $V_B \approx 1.0$ V.

3.4.3 Results

To demonstrate the method Figure 51 shows the quantum efficiency of a 14.6% efficient solar cell, measured at three different voltage biases together with the fits. Fits have been restricted to the 900 to 1050 nm wavelength range but calculated curves are depicted in a bigger range to show where the calculation differs from the experimental data. The extracted parameters are given in Table 34. Using L_{eff} $(@\ V_{bias} = 0 \text{ and } -1V)$ to calculate L (without using the capacitance data) gives $L = 1.19\ \mu m$ and $w = 0.3\ \mu m\ (@\ V_{bias} = 0V)$ in good agreement with capacitance measurements.

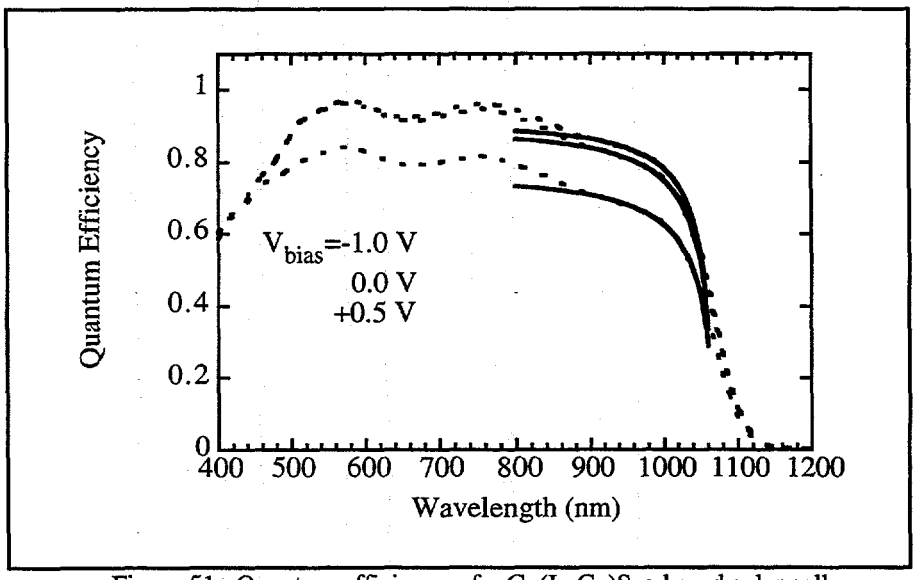


Figure 51. Quantum efficiency of a $Cu(In,Ga)Se_2$ based solar cell.

Table 34. Parameters extracted from the analysis of QE and capacitance data.

Bias (V)	k_3	L_{eff} (μm)	E_G (eV)	w* (μm)	L_{eff}-w (μm)
-1.0	0.91	1.49	1.17	0.34	1.15
0.0	0.90	1.37	1.17	0.23	1.13
0.5	0.77	1.26	1.17	0.08	1.19

* extracted from capacitance measurements

Several cells have been measured and evaluated in this manner. Diffusion lengths in the range of 0.2 - 1.5 μm have been found. The correlation between L and the cell efficiency is not as clear as might be expected. Partly this is because the efficiency is limited by V_{oc} rather than current collection. It has been claimed that the open circuit voltage of $Cu(In,Ga)Se_2$ based solar cells is limited by recombination in the space charge region, probably via band tails rather than midgap states. In this case there are two main parameters that determine V_{oc}, doping and carrier lifetime. Both parameters are accessible from QE measurements if it is assumed that minority (L) and majority carrier lifetimes are correlated. This would be true if the same recombination states (i.e.

from band tails) are also responsible for the space charge width. Since V_{oc} depends on the space charge width as shown by the relation (from Equation 3.27 and reference (63)):

$$V_{OC} = \left(\frac{AkT}{q}\right) Ln\left(\frac{J_{SC}}{J_0}\right) \propto Ln(J_0) \propto Ln(J_{00}) \propto Ln(w) \qquad (3.33)$$

Therefore, plotting V_{oc} vs. Ln (w) should give a straight line if all other parameters remain unchanged. A plot is shown in Figure 52 where w has been calculated from the QE at 0 and -1 V. Due to some variations in the bandgap of the absorber, the plot is not quite linear. However, the plot indeed shows a correlation between V_{oc} and w which, in addition to the previous evaluation of V_{oc} (T), indicates that generally cells prepared in our lab are limited by the same bucking current mechanism as the cells of other labs. It can be seen, that at some point there have been large variations in the doping and hence V_{oc} of the devices.

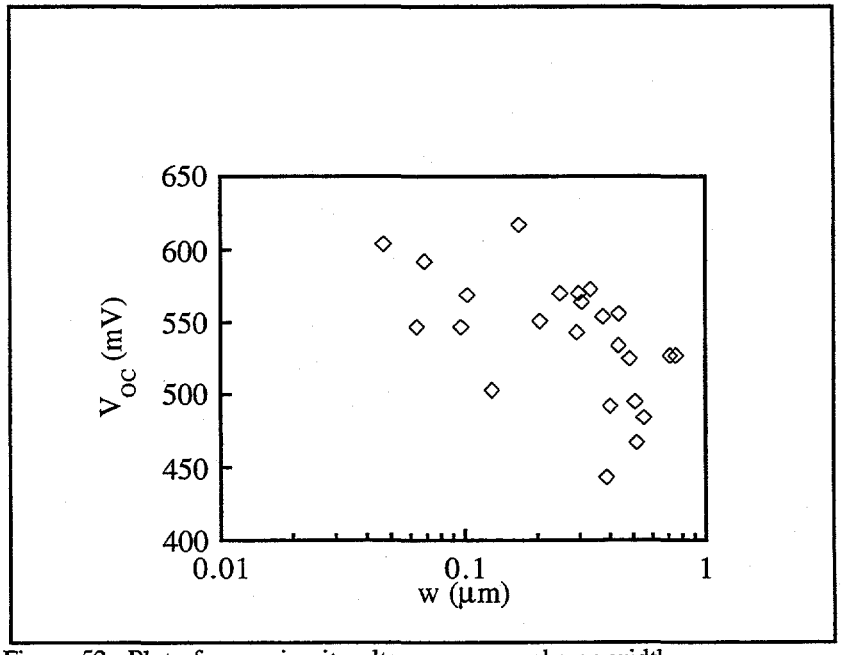
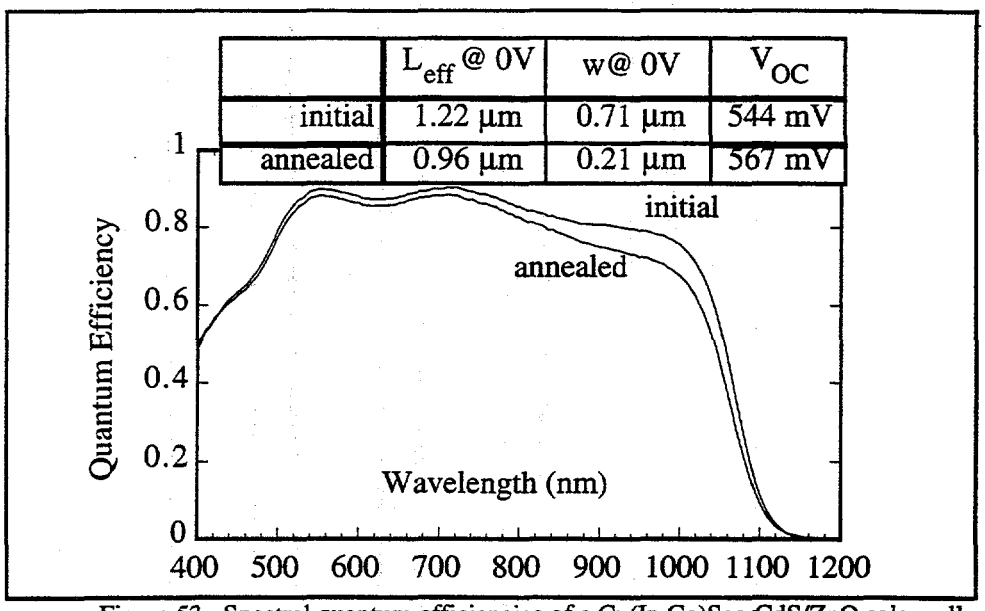


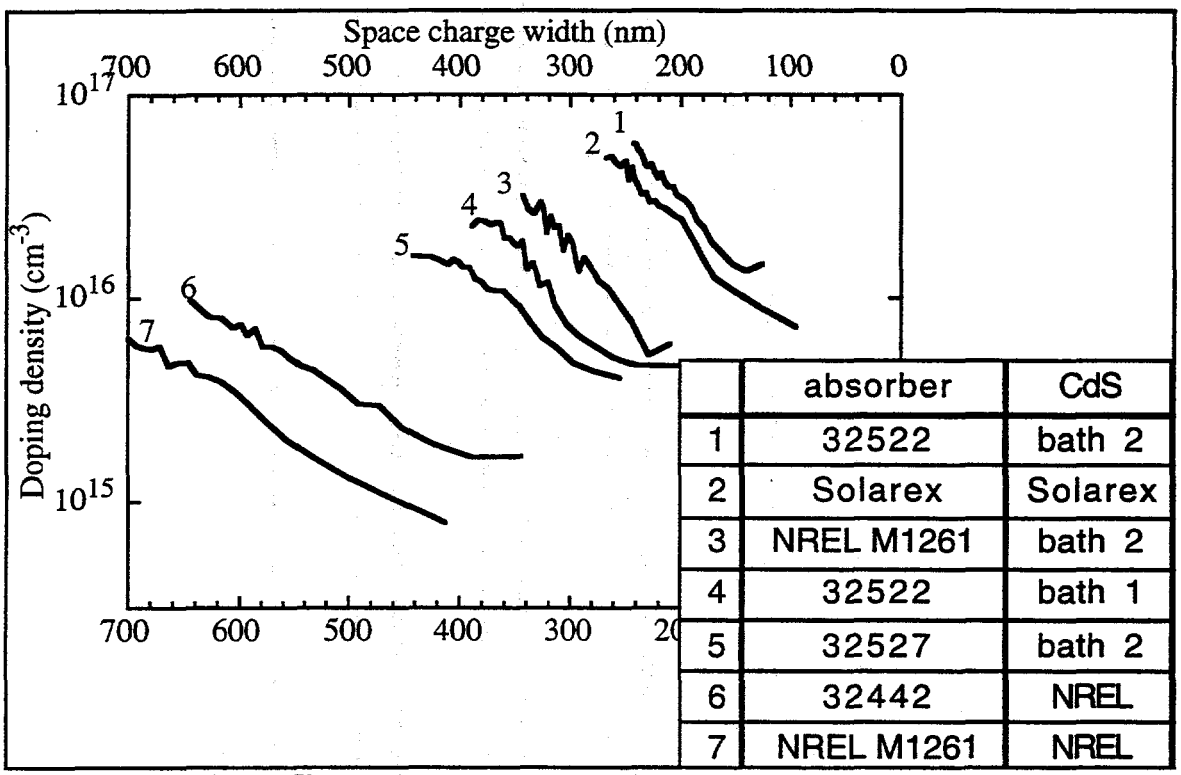
Figure 52. Plot of open circuit voltage vs space charge width.

The preparation of the CdS buffer layer has been identified as one important factor influencing the doping in the absorber (see Section 2.2). Another influence is the short post preparation heat treatment. Examples of quantum efficiencies in the initial and annealed state are shown in Figure 53. The heat treatment increases the doping and V_{oc} whereas the red response decreases due to the smaller extension of the field zone.



	L_{eff} @ 0V	w@ 0V	V_{OC}
initial	1.22 µm	0.71 µm	544 mV
annealed	0.96 µm	0.21 µm	567 mV

Figure 53. Spectral quantum efficiencies of a Cu(In,Ga)Se_2/CdS/ZnO solar cell before and after heat treatment.



	absorber	CdS
1	32522	bath 2
2	Solarex	Solarex
3	NREL M1261	bath 2
4	32522	bath 1
5	32527	bath 2
6	32442	NREL
7	NREL M1261	NREL

Figure 54. Doping profiles.

In most cases capacitance measurements have been found to roughly agree with the estimation of w from QE. However, if samples are compared, the difference in capacitance is often lower than would be expected from the difference in V_{oc} and L_{eff}. Examples of doping profiles calculated from the slope of $1/C^2$ vs. V are shown in Figure 54, including two samples with different CdS as mentioned above. Comparison with cells from other labs indicate similar doping levels.

3.5 SUMMARY & CONCLUSIONS

A procedure has been developed for accurately representing the current voltage (J-V) characteristics of polycrystalline and amorphous silicon solar cells. The measured J-V data is separated into a forward diode current (J_D) and a (possibly voltage dependent) light generated current (J_L). The forward diode current (J_D) is analyzed in terms of a set of standard diode parameters (A, J_0, J_{00} and E_G). The justification for applying these standard diode parameters is based on a model in which the forward diode current (J_D) is controlled by recombination within the active light absorbing material. The possibly voltage dependent light generated current (J_L) is characterized using a simple electric field dependent collection model derived for a-Si devices. Resistive losses are usually represented by a series resistance (R_S) and infrequently a shunt conductance (G_{SH}). Very good agreement is found between measured and calculated current voltage (J-V) characteristics from reverse to forward voltage bias in a variety of cells, illumination levels and temperatures.

In the case of a-Si devices, the method allows routinely measured J-V data to be analyzed to yield parameters containing fundamental information about the i-layer material quality and its relation to the device structure and performance. Effects of light induced degradation can be modeled with only one parameter, L_C/D .

There are strong indications, in the case of the $Cu(In,Ga)Se_2$ and CdTe based materials, that the diode characteristic can be described by recombination through a continuous exponential-like distribution of centers within the bandgap of the light absorbing material. Although not as pronounced, this behavior is quite similar to that of photovoltaic devices made from amorphous semiconductors. Possibly this is because the crystalline order in these polycrystalline thin films, with grain sizes on the order of about a micron in diameter, is part way between that of crystalline and amorphous material.

In addition, another method is being developed to use standard spectral response and capacitance measurements in order to get a separate estimate of the total minority carrier collection width $(L_{eff} = L + w)$ due to the electric field collection width (w) and that due to diffusion length (L). This technique is demonstrated for $Cu(In,Ga)Se_2$ devices.

4.0 RESEARCH AND DEVELOPMENT COLLABORATION

4.1 $CuIn_{1-x}Ga_xSe_2$

Florida Solar Energy Center - IEC has assisted FSEC in the development of $CuIn_{1-x}Ga_xSe_2$ film formation by Se vapor selenization by characterizing films deposited at FSEC and fabricating and characterizing completed solar cells on those films. Characterization of the films included film characterization of the morphology by SEM and composition by EDS. Devices were completed using the standard fabrication steps discussed in Section 2.2. The best cell from this work had $V_{oc} = 0.38V$, $J_{sc} = 35$ mA/cm^2, FF = 63%, and eff. = 8.2%.

University of Illinois - IEC has continued to assist the University of Illinois in the development of $CuIn_{1-x}Ga_xSe_2$ films deposited by hybrid sputtering by providing film characterization, and device fabrication and characterization. In addition to films deposited on standard glass/Mo substrates this work has included epitaxial layers grown on GaAs substrates.

ISET - X-ray diffraction measurements of glass/Mo substrates deposited by ISET for $CuInSe_2$ devices were completed to help in the evaluation of their substrate processing.

Martin Marietta - IEC has provided ongoing advice and guidance to Martin Marietta to assist in their process development. This has included guidance in the deposition of Mo, $CuInSe_2$, CdS and ZnO and in device measurements and analysis.

NREL- Samples were exchanged to evaluate CdS and ZnO used as window/ heterojunction layers in $CuIn_{1-x}Ga_xSe_2$ devices. This work is discussed in Section 2.2.1. IEC assisted NREL in the measurement and analysis of current-voltage characteristics versus temperature and illumination intensity of $CuIn_{1-x}Ga_xSe_2$ films.

Penn State University - IEC has provided data and guidance to Penn State in support of its program to model $CuInSe_2$ device behavior. Current-voltage data versus temperature and illumination intensity and quantum efficiency data on several $CuInSe_2$ and $CuIn_{1-x}Ga_xSe_2$ devices has been supplied. This is being used to model diode effects and current collection as well as non-ohmic contact effects.

Solarex - IEC has provided assistance to Solarex in their development of $CuIn_{1-x}Ga_xSe_2$ module fabrication. Specifically, IEC has provided assistance with deposition of $CuInSe_2$ by thermal evaporation, CdS, and ZnO deposition; deposited ZnO on Solarex films and 4" x 4" modules; completed detailed XRD analysis of $CuInSe_2$ films, and fabricated and characterized solar cells on $CuInSe_2$ and $CuIn_{1-x}Ga_xSe_2$ deposited at Solarex to help evaluate Solarex's in-house fabrication processes.

4.2 CdTe

In addition to both IEC's in house research activities and to teamed research, IEC scientists have devoted a significant effort toward supporting research activities of other PV researchers. The following are examples of those support activities.

Georgia Institute of Technology - Completion of CdTe/CdS films into devices by performing $CdCl_2$ treatment, Cu treatment, and contacting. Also deposited CdTe by PVD onto CdS provided by Georgia Tech. Contact method was effective, gave similar performance as that obtained by Georgia Tech with Cu/Au contact.

NREL - Fabricated CdTe based structures for SEM, XPS, and SIMS analysis to corroborate interpretation of processing steps used to form ohmic contacts. Submitted devices completed with contacting process on CdTe made at Solar Cells, Incorporated.

Solar Cells, Inc. - Completion of CdTe/CdS films in devices by performing $CdCl_2$ treatment, Cu treatment, and contacting. Diffused Cu process was effective, gave higher FF and similar overall performance as that obtained by SCI with their contact. Achieved fill factors ~75% at $V_{oc} > 820$ mV with Ni and carbon contacts.

A.D. Plating, Inc. - Provided detailed optical and structural characterization of CdTe/CdS films deposited under different electrochemical conditions. Completion of films into devices by performing $CdCl_2$ treatment, Cu treatment, and contacting. Based on these results, IEC made recommendations on deposition and post deposition treatment conditions to use.

University of South Florida - Completed CdTe/CdS devices using diffused Cu contact process, obtained similar performance as that obtained by USF with their contact.

4.3 a-Si

Advanced Photovoltaic Systems (Dr. Kampas, Dr. Xi) - IEC characterized a-Si/a-SiC n/p recombination junctions deposited at APS. This continues the effort described previously [Ref. 2.4.1] where IEC verified that the thin a-Si p+ layer between the n and p layers of a tandem significantly improves the recombination and reduces the voltage drop across the reverse biased n/p junction. During this year, APS supplied six devices having different types of n and p layers, including amorphous and microcrystalline. Results were presented in the APS Annual Report [Ref.4.1]. A microcrystalline n-layer improved the junction conductance even over that obtained with a microcrystalline p-layer.

NREL (Dr. McMahon) - Special a-Si test devices were made for Tom McMahon at NREL for shunting studies. Light induced shunting of triple junctions on textured SnO_2 is a problem which McMahon has been studying for 3 years using devices from Solarex. IEC made McMahon four sets of devices to test his theories as to the cause of the shunting. Devices were deposited with either much thinner (80 Å) or much thicker (500 Å) p-layers than usual (120 Å) on smooth ZnO and textured SnO_2 substrates. This allowed comparison of the effect of p-layer thickness and TCO texture on shunt formation. The devices were fully characterized at IEC before sending to McMahon. His results on these samples were published [Ref. 4.2]. He has concluded that metastable (reversible) shunting only occurs on devices having at least one contact of Al-doped ZnO suggesting Al diffusion. Also, smooth substrates show a continuous (smooth) increase in shunt current while textured substrates give discrete step-like increases or decreases in shunt current, suggesting current paths related to the sharp peaks in the textured TCO.

Energy Conversion Devices (Dr. Deng) - ECD is interested in alternatives to ITO for the top contact to a-Si based triple junctions. Previously, we described problems we had in obtaining good results from sputtering ZnO on their n-i-p devices and defining the cells by photolithography [Ref. 2.4.1]. This year, we attempted to use scribing to define the ZnO with Ni tabs. Both ITO or ZnO have been sputtered as a top window layer on 10 pieces of their ss/n-i-p cells, but the result as always complete shorts. This happens even before scribing. Further work will involve depositing the same contact on IEC n-i-p cells and sputtering IEC ZnO on pieces from ECD which are already covered with their ITO contact.

NREL (Dr. Sopori) - Bhushan Sopori (NREL) is developing an optical scattering model to be applied to optimize texture for multilayer thin film solar cells. IEC sent him data consisting of reflection and transmission measured at IEC on a-Si p, i, and n layers on glass and on textured SnO_2, and absorption coefficients for all three layers plus for the SnO_2 itself. In addition, SEM cross sectional photos and analysis were sent to allow NREL to characterize the physical texture of the SnO_2. SEM data on SnO_2 was also sent to Nagi Maley at Solarex who expressed interest in seeing the texture on their SnO_2. The goal is to verify the program by first modeling scattering in single layer films on textured SnO_2 before attempting p-i-n structures. Presently, the analysis requires excessive amounts of computer time.

University of Delaware Physics Dept. (Prof. Glyde) - IEC obtained a-Si samples for Henry Glyde in UD Physics for neutron scattering (NS) experiments. The goal is to determine if NS detects a change in H environment with light exposure. We determined the best type of sample structure based on his description of experimental geometry and scattering sensitivity. IEC obtained two 1 sq. ft. samples of a-Si i-layer on glass from APS and gave Glyde assistance in cutting samples, etching, etc. He plans to have NS measurements done at NIST and Cambridge, UK.

Harvard University Chemistry Dept. (Prof. Gordon) - We have deposited a-Si devices on several sets of textured TCO deposited by APCVD by Roy Gordon's group. This includes textured SnO_2, ZnO and ZnO/SnO_2 bilayers. Results are described in Section 2.4. Four p-i-n device substrates were sent to Roy Gordon at Harvard for deposition of ZnO by APCVD for the back reflector. He will return them to us for metallization and testing.

University of Hawaii Electrical Engineering Dept. (Prof. Rocheleau) - Richard Rocheleau has developed a numerical device model capable of analyzing JV data or QE data to determine recombination and generation profiles in i-layers of single or multijunction cells given layer thicknesses, optical absorption spectra, etc. It can also be used to optimize the multijunction cell design for a given illumination. IEC provided him with JV data measured at IEC on a number of pieces for his modeling effort. These included IEC light soaked devices, Solarex a-SiGe devices under white and red light, Solarex single and tandem cells, and APS devices with varying i-layer thickness.

United Solar Systems Company - Dr. Hoffman of USSC has supplied IEC with data for use in our modeling described in this report. USSC supplied absorption coefficients for their a-Si and a-SiGe i-layers used in triple junctions, and the JV data of the component single junction cells. The optical data will be used in the multijunction QE model. The JV data is being analyzed as described in Section 2.4 and Section 3, to obtain parameters of each single junction device, then the parameters will be used to simulate the triple junction JV behavior.

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6.0 ABSTRACT

This report describes results achieved during the second phase of a four year subcontract to develop and understand thin film solar cell technology related to a-Si and its alloys, $CuIn_{1-x}Ga_xSe_2$, and CdTe. Accomplishments during this phase include, development of equations and reaction rates for the formation of $CuIn_{1-x}Ga_xSe_2$ films by selenization, fabrication of a 15% efficient $CuIn_{1-x}Ga_xSe_2$ cell, development of a reproducible, reliable Cu-diffused contact to CdTe, investigation of the role of CdTe-CdS interdiffusion on device operation, investigation of the substitution of HCl for $CdCl_2$ in the post-deposition heat treatment of CdTe/CdS, demonstration of an improved reactor design for deposition of a-Si films, demonstration of improved process control in the fabrication of a ten set series of runs producing ~8% efficient a-Si devices, demonstration of the utility of a simplified optical model for determining quantity and effect of current generation in each layer of a triple stacked a-Si cell, presentation of analytical and modeling procedures adapted to devices produced with each material system, presentation of baseline parameters for devices produced with each material system, and various investigations of the roles played by other layers in thin film devices including the Mo underlayer, CdS and ZnO in $CuIn_{1-x}Ga_xSe_2$ devices, the CdS in CdTe devices, and the ZnO as window layer and as part of the back surface reflector in a-Si devices. In addition, collaborations with over ten research groups are briefly described.

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This report describes work performed under the second phase of the subcontract to continue to provide the thin-film PV community with a greater depth of understanding and insight into a wide variety of issues including (1) the deposition and characterization of $CuIn_{1-x}Ga_xSe_2$, CdTe, CdS, a-Si, and TCO thin films; (2) the relationships between film and device properties; and (3) the processing and analysis of thin-film PV devices. This was achieved through the analysis and quantification of the reaction chemistries involved in thin-film deposition and through the thorough and systematic investigation of all aspects of film and device production. This methodology has led to improved process control of the fabrication of a-Si solar cells, in-depth and device-specific modeling, reliable and generally applicable procedures for contacting CdTe films, and controlled fabrication of a 15%-efficient $CuIn_{1-x}Ga_xSe_2$ solar cell. Specific accomplishments are described in the report.

14. SUBJECT TERMS

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