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CHARGE-SENSITIVE POLY-SILICON TFT AMPLIFIERS FOR a-Si:H PIXEL PARTICLE DETECTORS

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ABSTRACT

Prototype charge-sensitive poly-Si TFT amplifiers have been made for the amplification of signals (from an a-Si:H pixel diode used as an ionizing particle detector). They consist of a charge-sensitive gain stage, a voltage gain stage and a source follower output stage. The gain-bandwidth product of the amplifier is ~ 300 MHz. When the amplifier is connected to a pixel detector of 0.2 pF, it gives a charge-to-voltage gain of ~ 0.02 mV/electrons with a pulse rise time less than 100 nsec. An equivalent noise charge of the front-end TFT is ~ 1000 electrons for a shaping time of 1 μsec.

I INTRODUCTION

Hydrogenated amorphous silicon (a-Si:H) diodes have been used in detecting single particles or fluxes of charged particles, X-rays or gamma rays for medical and physics applications.[1,2] Since signals produced in amorphous silicon detector diodes are generally small, even in ~ 30 μm thick diodes and especially in the case of single particle detection (~ 80 e-h pairs/μm)[1], pixel-level amplification is desired before the signal from a 2-d pixel detector array is readout by the external circuitry in order to minimize stray effects, such as transfer loss of signal, and noise pick-up at data lines crossing large-device area.

To implement these pixel amplifiers for a large-area 2-d pixel array of a-Si:H detectors, poly-Si thin-film-transistor (TFT) technology seems to be the most appropriate and natural choice because it has compatibility together with amorphous silicon in making large-area devices on the same substrate. Also it has better electronic characteristics than a-Si:H TFTs, such as higher field-effect mobility and lower threshold voltage etc. This technology is still under intensive development in the linear image sensor or active matrix LCD industry.[3,4] However in those applications, the TFTs are used principally as switching elements rather than as analog amplifiers, so it is important to investigate the analog characteristics of the TFTs and their limitations in making amplifiers.

A prototype amplifier circuit was designed, fabricated and tested in order to determine the feasibility of making charge-sensitive amplifiers for a-Si:H pixel detectors using the poly-Si TFT technology developed at Xerox Parc.[5] In actual pixel detectors, in addition to the amplifying stage, other signal processing units such as sampling, holding and readout switch are necessary but they were not implemented in this prototype.

II A POLY-Si TFT PIXEL AMPLIFIER

II(a) Design

General design requirements for the pixel amplifiers were; (a) small size limited to a pixel area (b) moderate amplifying gain in order to readout the signal through a large-area detector array without picking up extra noise, (c) enough bandwidth to respond to a fast rise of the input current

determined by the charge collection in the detector (~ μsec), (d) low noise to get a maximum signal-to-noise ratio, (e) low power dissipation, and (f) circuit simplicity for easy fabrication and high reliability.

The prototype pixel amplifier consists of three stages; the first stage is a low-noise charge-sensitive amplifier which integrates the signal charge from a detector. The second stage is a voltage amplifier to give an additional gain and the final stage is a source follower output stage with small output impedance to drive the readout lines. The circuit diagram of the test amplifier is shown in Fig. 1.

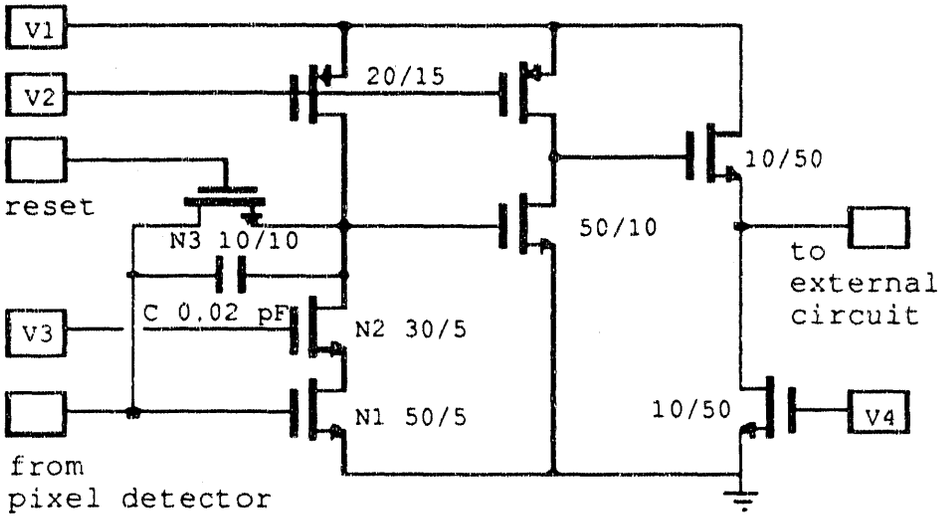

Fig. 1 A schematic circuit diagram of the prototype poly-Si TFT charge-sensitive pixel amplifiers for a-Si:H pixel detectors. Each square with node numbers represents a test pad. N and P stand for n-channel and p-channel TFTs respectively, and C stands for a capacitor.

The first charge-sensitive stage consists of an inverting voltage amplifier and a feedback capacitor. Two important design concepts for the first stage were; (a) for the maximum open-loop gain, the channel length L of the front-end TFT was chosen to be the minimum feature size (5 μm) and for minimum noise, the channel width W (50 μm) was chosen to make the input capacitance of the amplifier equal to that of an arbitrary pixel detector, 0.2 pF. This value is equivalent to the capacitance of an a-Si:H pixel detector of area 300 μm x 300 μm and thickness 50 μm. (b) for the maximum closed-loop charge gain, the feedback capacitance must be minimized. The capacitor was made using the same dielectric used as a gate insulator of TFTs, which was 100 nm thick SiO_2. We took, arbitrarily, as the capacitor's dimension, twice the minimum feature size, or 10 μm x 10 μm, which gave a C_F = 0.02 pF. Therefore the effective voltage gain, the ratio of the detector capacitance to the feedback capacitance, would be ~ 10 for a high open-loop voltage gain.

The voltage amplifier is implemented by an n-channel single-ended common-source poly-Si TFT N1, cascoded with a TFT N2, and a current-source load.[6] Although p-channel poly-Si TFTs have lower noise, an n-channel TFT was selected as the front-end because its threshold voltage is smaller and more stable than that of p-channel TFTs. A cascode configuration was used to minimize the Miller effect which causes the gate-to-drain (overlapping) capacitance to be effectively increased by the gain factor, thereby reducing the bandwidth. The load was designed as a p-channel TFT current source. This

complementary configuration was expected to give a higher gain and more reliability than a resistive load or n-channel TFT load. Finally another n-channel TFT N3 was connected in parallel with the feedback capacitor for biasing the input node and for reseting the amplifier by discharging the feedback capacitor.

The second stage is an extra voltage-gain stage which amplifies the signal further so that the amplified signal pulse will reach the external circuit with minimal addition of perturbation by the extra noise sources such as inter-communication, pick-up noise, etc. The final stage is simply a source follower stage, which has a unity gain and low output impedance.

Except for the front-end TFT N1, the dimensions of the other TFTs and operation biases (V_1 ~ V_4) required by the circuit as shown in Fig. 1 were determined using a circuit simulation program, PSPICE [7] in order to achieve (a) a moderate gain of the second stage (~ 10), (b) a maximum gain-bandwidth, and (c) a minimum power dissipation. In the simulation, a simple crystal-Si MOSFET model was used. Input data were taken from reference [8].

II(b) Fabrication

In order to test each stage, as well as the complete circuit, several combinations of test amplifiers were fabricated; first stage only, second stage only, and the complete amplifier with and without the cascode configuration. The complete amplifier, including interconnection lines occupied an area of 200 μm x 100 μm which is well within the target pixel of 300 μm x 300 μm. On the test chip, we also made individual TFTs having the same dimensions as TFTs used in the prototype amplifier to check the input parameters used in the design. The interconnections and test pads were drawn for convenience and easy identification of components. The test circuit was fabricated using the standard high temperature (900 °C) poly-Si TFT process at Xerox Parc.[5]

III TESTS AND RESULTS

III(a) Individual TFTs

Before the complete circuit was tested, the individual TFTs were separately tested in order to make sure the fabrication process was satisfactory, and to find the range of operating bias voltages for each node.(V_1 ~ V_4 in the figure 1)

Fig. 2 shows dc I-V characteristics of an n-channel TFT which has the same dimension as the front-end TFT N1 of the prototype amplifier. As seen in the figure, the TFT shows a well-defined linear and saturation region of I-V curve similar to that of crystal-Si MOSFET in the low bias (V_{ds}) region. In the high bias region, however, the short-channel effect makes a kink which has an onset (V_s) at 5 V and 6 V for n-channel TFTs of L = 5 μm and 10 μm respectively. For p-channel TFTs, V_s was 9 V for L = 15 μm.

Table 1 Measured circuit parameters of poly-Si TFTs

	L (μm)	K_p ($\mu A/V^2$)	μ_{fe} (cm^2/Vsec)	V_T (V)	V_s (V)
n-ch TFT	5	2.6	73	1.3	5
n-ch TFT	10	3.2	90	1.4	6
p-ch TFT	15	0.6	17	3.0	9

The measured values of some characteristics of individual poly-Si TFTs are shown in Table 1 where $K_p = \mu_{fe}\varepsilon_i/t_i$, ε_i and t_i is the dielectric coefficient and the thickness of the gate insulator respectively.

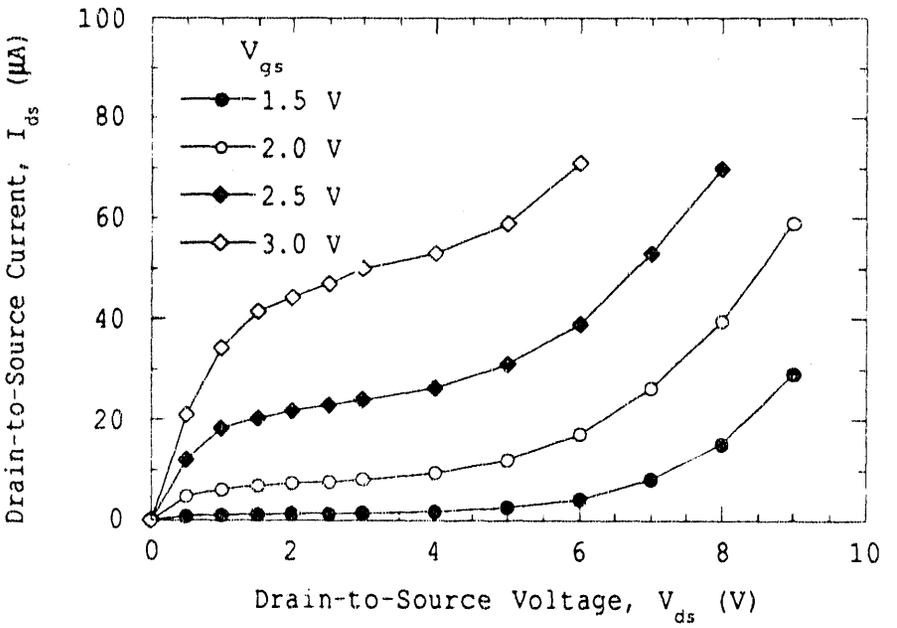

Fig. 2 I-V Characteristics of an n-channel poly-Si TFT. (W/L= 50/5 μm)

III(b) Front-End Charge-Sensitive Amplifying Stage

Because of short channel effects, which were not considered at the time of design and because of the difference between the design and measured values of the circuit parameters such as the threshold voltage, the input node dc bias was supplied separately with a probe during the test instead of through the reset TFT N3.

The measured dc voltage swing of the first stage with and without the cascode is plotted in Fig. 3. The dc gain A_1 which is the slope of the curves shown in the figure is ~ 11 and ~ 8 respectively with and without the cascode. The cascode configuration gives better linearity in the dc gain. The closed-loop gain, A_c, of the charge-sensitive amplifier would be reduced to ~ 7 and ~ 5.5 respectively when it is connected to a detector capacitance C_d of 0.2 pF.

The overall noise of the amplifier system is governed mainly by the front-end TFT. The frequency spectrum of noise from the same-sized n-channel TFTs as the front-end TFT at the same operation bias was measured using the set-up described in reference [9], and is shown in Fig. 4. 1/f noise was found to be the dominant noise source up to the measured range of 0.1 MHz. Thermal noise was calculated using the following equation, [10]

$$\langle V \rangle^2/\Delta f = 8\ kT/3\ g_m$$

where k is the Boltzmann constant, T is the temperature in Kelvin and g_m is the transconductance of the TFT. Assuming a CR-RC shaping network, the input equivalent noise charge (ENC) from the front-end TFT, a sum of 1/f noise and the channel resistance noise, was calculated. [11] For the range of shaping time > 0.1 μsec, ENC was independent of the RC shaping time and was ~ 1040 electrons in rms.

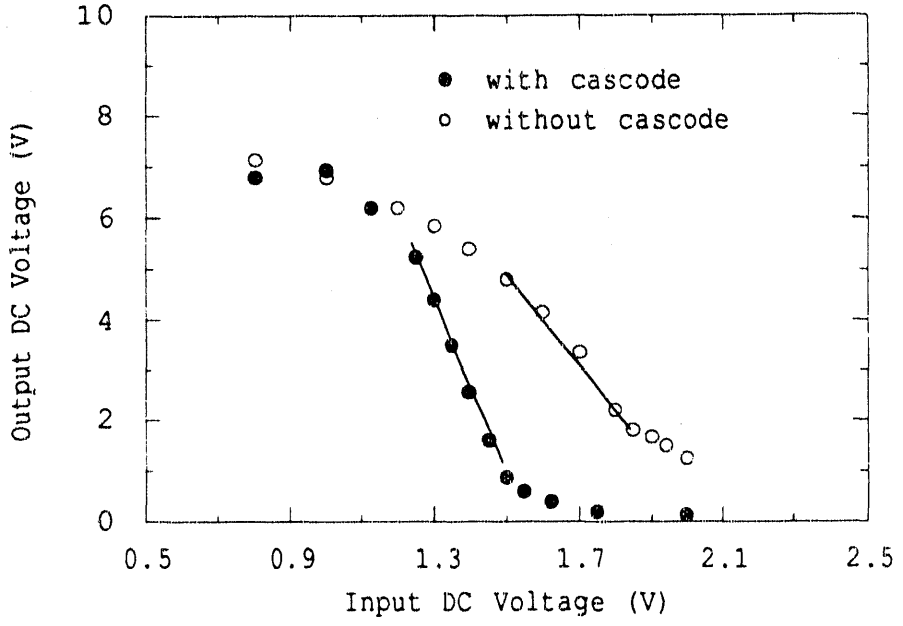

Fig. 3 DC characteristics of the first stage with and without cascode configuration. V_1 = 10 V, V_2 = 5 V and V_3 = 5 V.

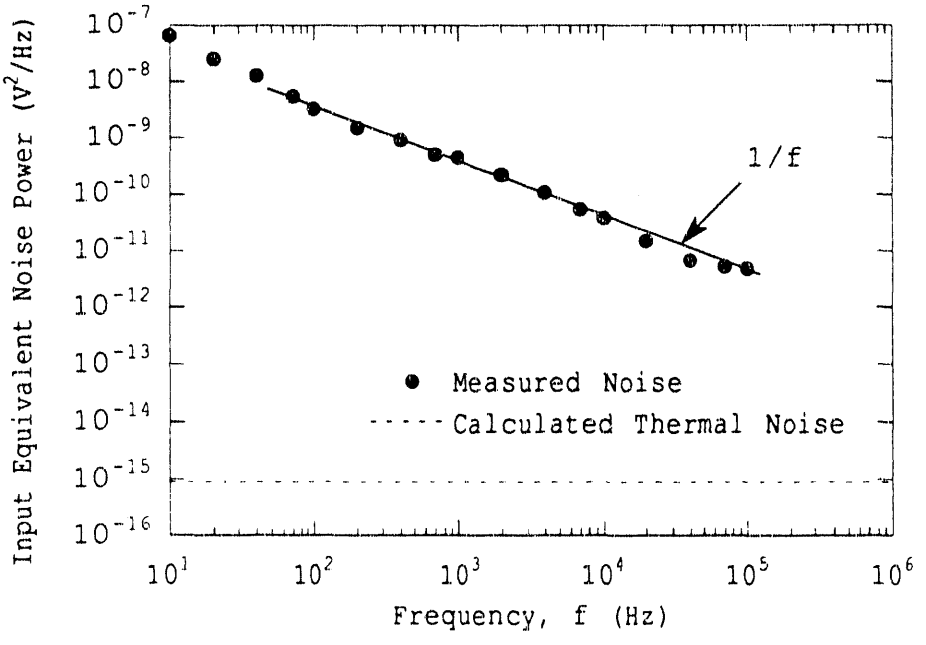

Fig. 4 Measured noise power spectrum of the front-end n-channel poly-Si TFT (W/L = 50/5 μm) at V_{gs} = 1.8 V, V_{ds} = 4 V (g_m = ~ 20 μA/V).

III(c) Overall Gain and Bandwidth

In order to find the frequency response, a sinusoidal wave with a magnitude 10 mV was introduced to the input node through an external coupling capacitor (~ 0.01 μF), and the output wave form was measured at the output node using an active probe. The measured frequency responses for the amplifier is shown in Fig. 5. The measured 3dB cut-off frequencies (f_{m3dB}) into the oscilloscope probe load (1 pF + 1 MΩ) are ~ 1 and ~ 0.5 MHz

respectively with and without the cascode. These values are equivalent to ~ 3 and ~ 1.5 MHz of the intrinsic cut-off frequencies after subtraction of the loading effect of the probe, assuming

$$f_{3dB} = f_{m3dB} \times (C_L + C_{probe})/C_L$$

where C_L and C_{probe} are the loading capacitance of the last stage (~ 0.5 pF) and that of the probe (1 pF) respectively. The frequency response was limited at the second stage which was loaded with large capacitance of the source follower stage. The linear gain of the second stage was determined to be ~ 10 and ~ 20 with and without cascode respectively assuming the third stage gain is about 1. This difference might be come from the difference of the dc bias for the second stages due to the presence of the cascode TFT N2. The pulse rise times are 100 and 200 nsec with and without the cascode using a relation, $f_{cut\text{-}off} \times T_{rise} \approx 0.35$, [12] The dynamic range of the amplifier is determined by the noise level, estimated previously for the case of CR-RC shaping amplifier, and the range of input voltage swing before the saturation of the output voltage. The lower limit is arbitrarily defined as the total equivalent noise charge in rms from the detector and the amplifier system and is ~ 1000 electrons. The upper limit is estimated by the maximum voltage swing at the input terminal and is $C_{tot} \times V_{swing} / q$ = 0.4 pF x 0.1 V / 1.6 x 10^{-19} Coul = 250,000 electrons. Therefore dynamic range is ~ 48 dB.

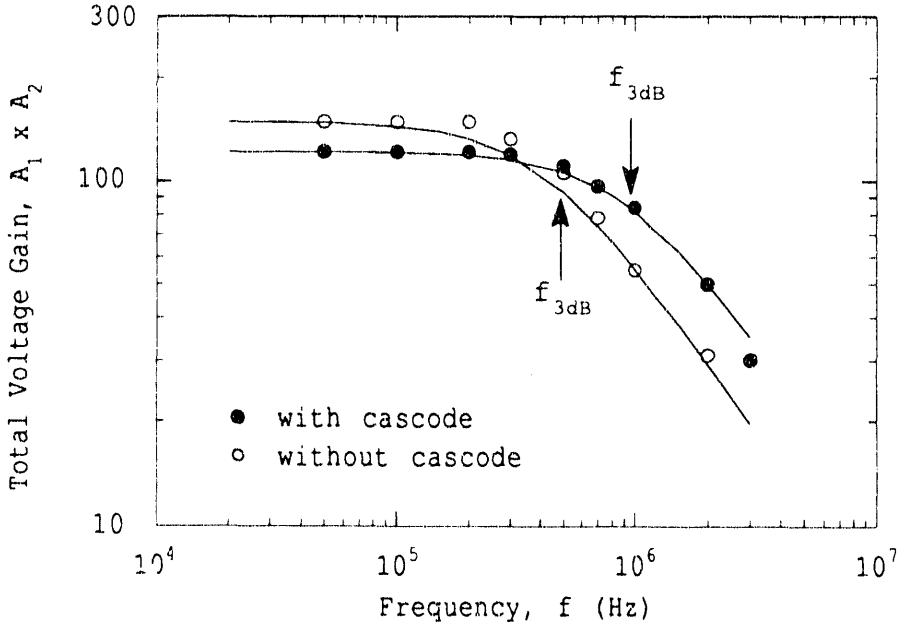

Fig. 5 Total voltage gain of the complete amplifier with and without the cascode configuration.

IV DISCUSSION

A prototype poly-Si TFT CMOS amplifier was designed and tested. It consisted of a charge-sensitive gain stage, a voltage gain stage and a source follower output stage. The open-loop gain A_1 of the first stage with the cascode was measured to be ~ 12 and of the second stage ~ 10. The overall gain-bandwidth product was ~ 400 MHz. When the amplifier is connected to a pixel detector of capacitance 0.2 pF, it would give a charge-to-voltage gain of ~ 0.02 mV/electron with a pulse rise time less than 100 nsec and a dynamic range of 48 dB. For large-area integrated electronic devices, the minimum feature size is usually limited by the thermal expansion of the substrate

material at the maximum process temperature.[5] For a glass substrate in the low temperature poly-Si technique, the minimum feature size is about 5 μm. If quartz is used as a substrate, the minimum feature size can be reduced to 3 μm or less because of the superior thermal property of the quartz. The smaller the minimum feature size, the larger gain that can be achieved.

From the measurement of the noise-power-spectrum of TFTs, 1/f noise was found to be dominant noise source up to 10 MHz when it was extrapolated to the point of intersection with the thermal noise. An equivalent noise charge of the front-end n-channel poly-Si TFT was estimated, based on the measured 1/f noise and the transconductance at the operation bias point, to be ~ 1000 electrons rms at a shaping time of 1 μsec for CR-RC filters. The 1/f noise can be reduced by decreasing the density of the interface states between silicon and gate oxide.

Amorphous and poly-silicon TFTs are relatively new devices of great importance to applications in large-area imaging and consequently they are the subject of intensive and extensive study worldwide. Currently, an analytical model of poly-Si TFTs for circuit simulation incorporated in PSPICE [13] is available at Xerox Parc and improvement in the design of poly-Si TFT amplifier is under study using the model.

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