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SiO_x Precipitation: Defect Density Correlation With The n+ Substrate Resistivity*

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Introduction:
The thermal budget of a CMOS process, which employs n/n+ epitaxial silicon, can constrain the SiO_x precipitation necessary for bulk gettering sites. This makes the control of both the precipitation and its distribution difficult. Little or no precipitation will occur when heat treatments are inadequate or the n^+ substrate O_2 concentration [O] is too low. Likewise, uncontrolled precipitation can lead to warpage, slip and the formation of surface stacking faults. Bulk precipitation in some CMOS processes using n/n^+ epitaxial silicon may not be feasible, because of the smaller thermal budgets. However; many CMOS processes using n/n+ epitaxial silicon rely on some form of gettering. Extrinsic and intrinsic gettering techniques [1,2] as well as pre-processed [3] gettered wafers can be employed with CMOS processes to develop the necessary internal SiO_x defects for effective gettering. An experimental strategy was designed to determine how the CMOS thermal budget interacts with the extrinsic gettering layers on n+ substrates with different [O]. Models for the defect densities and denuded zones developed from the strategy are reported for the polysilicon [Poly] and polysilicon/nitride [PN] extrinsic gettering layers. An unexpected correlation between the defect density and the n^+ substrate resisitivity with [O] also is discussed.

Experimental:
An experimental strategy was designed to obtain information concerning the possible interactions or nonlinear behavior between different extrinsic gettering layers, n^+ substrate [O] and the thermal budget of a CMOS process. The strategy employed was a 2-level fractional factorial design with center points. Two (2) duplicates were run at each coordinate, and at least five (5) at the center point. Special runs also were made to validate the empirical model developed from the strategy. Experimental variables and their ranges are defined in Table 1. The n+ substrates were obtained from two (2) separate silicon sources and the epitaxial silicon was grown internally or obtained from an external vendor. The experimental responses of this study are internal defect density (DD) and denuded zone width (DZ). The internal defect density (DD) in this study includes SiO_x precipitate density and stacking faults. A high-low-high thermal cycle was used, and the initial oxidiation (1100 °C, 1 hr., steam) remained constant in order to reduce the total number of experiments in this study. All n^+ substrates received the same epi growth process prior to the initial oxidation cycle. Only the nucleation [NT] and precipitation [PT] times of the thermal budget were varied. The substrate, epitaxial and gettering layer parameters are given in Table 2.
Secondary Ion Mass Spectrometry (SIMS) was used to obtain the initial and post processing substrate [O]. The initial [O] values given in Table 2 are

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averages of three measurements. Defect density and the denuded zone determinations were made by preparing cross-sections and then decoratively etching for 2 minutes with a Wright etch. The cross-sections were viewed at a magnification of 200X using optical microscopy.

Results and Discussion

Empirical models developed from this strategy predict the dependence for DZ and DD within the NT-PT parameter field. The models predict that the DD should increase as the either NT or PT increases, and DZ decreases with increasing NT or PT. Sources for epitaxial and bulk silicon exhibited no influence on DZ or DD. Denuded zone measurements agreed with previous results for Poly and PN gettering layers [4]. A comparison between the DD values predicted by the empirical model and other values obtained from the validation runs are given in Table 3. This comparison includes DD values for both Poly and PN. Good agreement is observed for the PN, but not so for the Poly. Analysis of the experimental Poly gettering DD values indicated that the substrate resistivity and [O] were the major contribution to the lack of agreement between the predicted and experimental Poly DD values.
The effect that resistivity and O_2 concentration has on the DD of the y gettered n+ substrates is presented in Fig. 1. The DD for the n+ substrate with the [O] = $7x10^{17}$ cm^{-3} shows a linear dependence with the substrate resistivity, lower curve Fig. 1. Although a backside poly gettering layer was used, very limited precipitation was observed even at the hi-hi point of the (NT-PT) parameter field. Tsuya's [5] reported DD dependence for n^+(Sb) substrates is shown in Fig. 1 for comparison, and Pearce [6] indicated a similar result. Both Tsuya and Pearce suggested a vacancy mechanism to explain their observations. Changing the n+ substrate [O] to $1x10^{18}$ cm^{-3} creates a strong DD dependence on the n+ substrate resistivity, solid triangles, Fig. 1. Below the 0.0125 Ω-cm threshold the DD coincides with data from the n^+, [O] = $7x10^{17}$ cm^{-3} substrate. Above this threshold a rapid increase of several orders of magnitude in DD is observed indicating an improved precipitation process. The DD was observed to be non-uniform across a wafer for many of the Poly gettered samples, and this agrees with other investigators [7,8]. The precipitation behavior for the n+ silicon with [O] = $1x10^{18}$ cm^{-3} and a PN gettering layer is represented by the upper curve, open circles. Little or no n+ resistivity dependence is observed, although some decrease is observed below 0.012 Ω-cm.
Uniform precipitation behavior of the Poly and PN samples with substrate resistivity > 0.014 Ω-cm is associated with the stress created by the polysilicon and/or nitride layers. A saturation of vacancies, which are effective nucleation sites for SiO_x precipitates, and for enhanced oxygen diffusion in silicon [9]. The OED is a necessary component for the SiO_x precipitation phenomena. The silicon interstitials I_{Si} generated during the formation of the precipitates are absorbed at the poly/silicon interface [10] by grain boundaries and dangling bonds.
Transition from a DD of 10^4 cm^{-2} to 10^2 cm^{-2} may result from a point defect-impurity donor interaction, either the Sb^+ reacts with I_{Si} to form a Sb^+I^- complex or the Sb^+ reacts with a V^- to form a Sb^+V^- complex. The second is more likely because it reduces the number of vacancies, which can lead to a saturation of I_{Si}.
Correspondingly, in the low DD region with the higher Sb^+ concentrations the formation of Sb^+V^- may be more favorable due to the excess of Sb^+. In the case of the n^+ substrate with [O] = 7 $x10^{17}$ cm^{-3} and Poly gettering a Sb^+V^- mechanism also is suggested. Impurity ion size effects and substrate carbon concentration have not been consideredin this discussion, but may contribute to the above observations. Further study is required in this area.

Summary:
Interactions between a CMOS process thermal budget for n/n^+ epitaxial silicon with n^+ substrates with different backside gettering layers and O_2 concentrations were examined. Substantial differences in DD are observed for the Poly gettered substrates with different [O] as well as for substrates with the same [O] but different gettering layers, Poly or PN. The DD for the Poly gettered n^+ substrates shows a strong dependence on resistivity below 0.0125 Ω-cm, which is attributed to a point defect-impurity (Sb^+V^-) interaction. Uniform SiO_x precipitation in the n^+ substrate with Poly and PN gettering results from a saturation of vacancies generated as a result of the stress from the Poly or PN layers. A point defect-impurity interaction also is suggested for the n^+ substrate with [O] = $7x10^{17}$ cm^{-3}.

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Table 1. Strategy Variables and Ranges

Variable		Range
Nucleation Time[a]	[NT]	0.5 to 3.0 hrs.
Precipitation Time[b]	[PT]	1.0 to 10.0 hrs.,
O_2 Concentration	[O]	High and Medium
Gettering Layers		Poly or PN
Substrate Source		Vendor A and B
Epi Source		Internal and External

[a]Nucleation temperature was 900 °C, atmosphere N_2.
[b]Precipitation temperature was 1100 °C, atmosphere N_2.

Table 2. Substrate and Epitaxial Parameters

<u>Substrate</u>:		
Type/Dopant	n+/Sb	
Orientation	<100>	
Resistivity	0.01 to 0.03 Ω-cm	
O_2 Conc.	High	$1x10^{18}$ cm^{-3}
	Medium	$7x10^{17}$ cm^{-3}
Diameter	100 mm	
Thickness	625 +/- 25 μm	
<u>Epitaxial Layer</u>:		
Thickness	10 to 12 μm	
Resistivity	3 to 4 Ω-cm	
<u>Gettering Layer</u>:		
Poly[a]	2.0 +/- 0.2 μm	
PN[b]	2.0 μm/0.06 μm	

[a]Deposition Temperature: 625 °C, 450 mT.
[b]Deposition Temperature: 750 °C, 350 mT.

Table 3. Comparison of Predicted and Experimental DD for Poly and PN Gettered Substrates

		Poly[a]		PN[a]	
NT[b]	PT[b]	Exp.	Model	Exp.	Model
1	8	6	1.7	30	28
2	8	2	2.2	30	29
1.5	4	2	1.2	20	18
2	4	5.5	1.4	20	18
3	5.5	2	1.9	20	22
1	2	2	0.9	10	12

[a] All defect density values are given as 10^4 cm^{-2}.
[b] The units of NT and PT are hours.

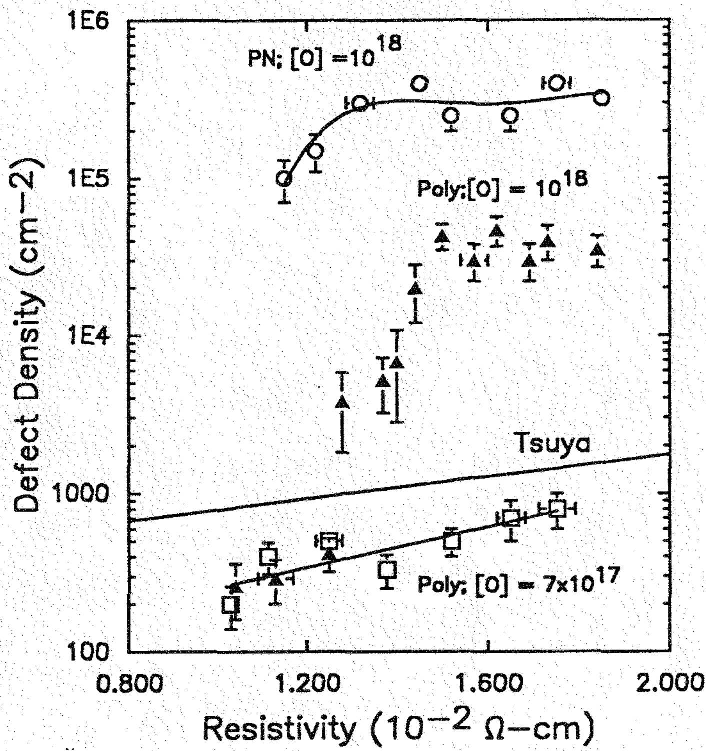

Fig. 1. The Effect of n^+ Substrate Resistivity on Defect Density
Lower: squares; [O] = $7x10^{17}$ cm^{-3};
Middle: triangles; [O] = $1x10^{18}$ cm^{-3};
Top: circles; [O] = 1 x 10^{18} cm^{-3}.