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FIRST LEVEL TRIGGER PROCESSOR FOR THE ZEUS CALORIMETER

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Abstract

This paper discusses the design of the first level trigger processor for the ZEUS calorimeter. This processor accepts data from the 13,000 photomultipliers of the calorimeter which is topologically divided into 16 regions, and after regional preprocessing, performs logical and numerical operations which cross regional boundaries. Because the crossing period at the HERA collider is 96 ns, it is necessary that first-level trigger decisions be made in pipelined hardware. One microsecond is allowed for the processor to perform the required logical and numerical operations, during which time the data from ten crossings would be resident in the processor while being clocked through the pipelined hardware. The circuitry is implemented in 100K ECL, Advanced CMOS discrete devices, and programmable gate arrays, and operates in a VME environment. All tables and registers are written/read from VME, and all diagnostic codes are executed from VME. Preprocessed data flows into the processor at a rate of 5.2GB/s, and processed data flows from the processor to the Global First-Level Trigger at a rate of 700MB/s. The system allows for subsets of the logic to be configured by software and for various important variables to be histogrammed as they flow through the processor.

Introduction

The ZEUS calorimeter first-level trigger processor (CFLTP) presents summary data on energy deposition in the uranium/scintillator sampling calorimeter to the global first-level trigger (GFLT). The summary data includes global and regional sums of electromagnetic and hadronic energy deposition, the number of isolated muons and isolated electrons, missing transverse energy, jet cluster information, and the likelihood of beam-gas background. The CFLTP receives data from 16 regional trigger pre-processors which digitize the calorimeter signals and perform regional energy sums and logical operations. The CFLTP is a pipelined processor that contains data from a number of crossing periods at any instant. It can capture input and output data from a sequence of up to 4096 consecutive beam crossings or first-level trigger events for detailed examination. All data variables are accessible for histogramming; the histograms are computed and evaluated by two 88000 RISC processors that reside in VME buses, embedded within the the CFLTP. Input or output data emulation capability is provided to allow the CFLTP to operate at full speed in a stand-alone mode. In addition, the design includes a number of utility functions to inspect the data flow and to assist in troubleshooting.

Overview

The ZEUS experiment at the HERA colliding electron-proton facility uses a sampling calorimeter with uranium as the showering medium interleaved with strips of plastic scintillator for energy sampling. It is designed to produce equivalent output for hadrons and electrons of identical energy. The

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calorimeter is divided into three sections: the barrel (BCAL), front (FCAL), and rear (RCAL). The inner portion of the calorimeter is called the electromagnetic calorimeter (EMC) and detects mostly electromagnetic showers. The outer portions, the hadronic calorimeter (HAC), detects mostly hadronic showers. The BCAL is composed of 32 wedge-shaped azimuthal modules. FCAL and RCAL are planar, and each is composed of 23 vertical modules. The EMC section is finely segmented, with a typical arrangement of four EMC towers in front of a HAC tower. (Typically BCAL and FCAL have two stacks of HAC behind the EMC's; RCAL has one HAC stack behind the EMC's). The BCAL EMC's are segmented (53 segments) in projective tower geometry. The 14 HAC towers are non-projective and are aligned perpendicular to the beam direction. The F/RCAL EMC's and HAC's are non-projective and are aligned along the beam direction. Typically there are four EMC towers in front of every HAC tower in FCAL and BCAL and two EMC towers in front of every HAC tower in RCAL. The calorimeter is described by "regions" and "supertowers" (ST) for the first-level calorimeter trigger. Typically, each region consists of 56 ST. The definition of an ST will vary depending on location in the calorimeter. The simplest definitions are near the beam pipe for F/RCAL and at 90° from the interaction region for the BCAL. In those places, an FCAL or BCAL ST consists of four EMC towers and the HAC towers directly behind them; an RCAL ST consists of two EMC towers and one HAC tower. The most complex definitions of ST's are near the periphery of F/RCAL and at the boundaries of BCAL with FCAL and RCAL. There are 16 regions of the calorimeter: the four quadrants of FCAL, four quadrants of RCAL, four 90° azimuthal sections of the front half and four sections of the rear half of the BCAL. The regions are shown in Fig. 1. Every 96 nsec the electron and proton beams cross in the interaction region of

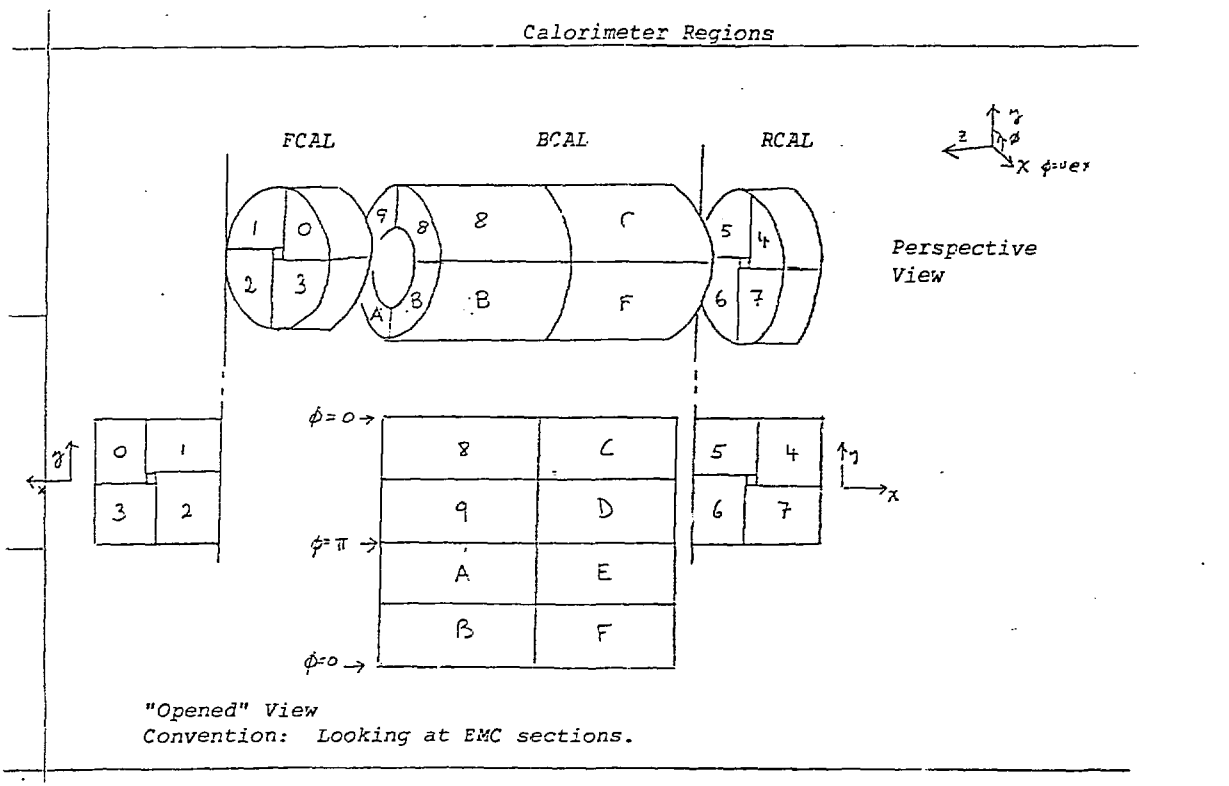


Fig. 1. Overview of CFLTP.

HERA. Scintillation light produced in the calorimeter by particles resulting from interactions is extracted by means of wavelength-shifter guides and presented to 13,000 photomultiplier tubes (PMT). The first-level trigger system receives 5% of the current produced in every PMT. The currents are routed from the "analog DAQ cards" to "trigger sum cards" (TSC), located on the calorimeter backing, to produce analog sums for EMC and HAC supertowers. The analog outputs from the TSC are transmitted over 60 m of cable to the electronics room for digital processing. The HAC and EMC signals for each ST are digitized and pre-processed by trigger encoder cards and adder cards that reside in customized VME crates[1]. Each VME crate contains 14 trigger encoder cards and 2 adder cards in 9U format for pre-processing data from one calorimeter region. Each crate performs three basic functions on the digitized data, yielding regional pre-processed data which is transmitted to the CFLTP. The functions of one custom VME crate are outlined below:

a) The regional values of energy (E), transverse energy (Et), x-energy (Ex), and y-energy (Ey) are summed for EMC and HAC separately..

b) The energy of each ST is compared to 6 different (and programmable) threshold windows. The number of ST's in a given energy window is determined for the entire region as well as for eight subsets of the region. In this way a crude determination of energy deposited in certain (programmable) portions of a calorimeter region is made. A region edge is one portion of particular interest.

c) The energy in each ST is tested to determine if it is predominantly electromagnetic. Also the energy in each ST is tested to determine if it is consistent with that deposited by a minimum-ionizing particle. The ST's in the immediate vicinity are tested to see whether the above-mentioned energy deposits are isolated. If so, the energy is presumed to have been deposited by isolated "electrons" (or photons) and isolated "muons". The number of isolated "electrons" and isolated muons contained in each region is reported. Potentially isolated energy deposits along the edge of a region and the position of the edge are reported so that the CFLTP can determine whether energy isolation is consistent with energy deposition on the edge of the neighboring region.

Note: The calorimeter can not distinguish photons from electrons. We refer to isolated electromagnetic energy deposition as isolated "electron" and not "electron or photon" only for the sake of brevity.

Calorimeter First-Level Trigger Processor

The CFLTP[2] implements the global algorithms, logic, and energy sums in order to provide the calorimeter information required by the global first level trigger (GFLT). The CFLTP receives 64 words (16 bits/word) of data from the regional adder cards every 24 ns for processing, so that in the 96 ns crossing period 4096 bits of information are provided. It also receives control and status data every 96 ns from the GFLT and status information from the data acquisition electronics, and distributes GFLT control information to the pre-processors. The CFLTP can capture sets of input and output data upon software or hardware command, up to a total corresponding to 4096 beam crossings. This may be data from a series of beam crossings or only data from interactions that have resulted in a first-level trigger (GFLT "ACCEPT"). Captured data are available via two embedded VME buses to the two Motorola 88000 RISC microcomputers that reside within the CFLTP. The CFLTP maintains histograms of input and output variables. Histograms are evaluated periodically by on-board microcomputers. Data that falls outside predetermined bounds of a histogram may be reported to the calorimeter equipment computer and to the DAQ computer via VME. In addition, the CFLTP can emulate input or output data for 4096 consecutive

beam crossings. Emulated data is programmable or may consist of previously-stored (real) data. Emulated data is available on the input cards or on the output cards of the CFLTP via software-controlled switches. The processed summary data consists of 32 words output at 96 ns. It includes the following information:

- global hadronic and electromagnetic energy deposition: scalar sum of energy, energy flow transverse to the beam direction, vector sum of transverse energy (missing energy);
- the number of isolated electrons and isolated muons;
- the likelihood of jet clusters;
- the likelihood of beam-gas interaction;
- regional information on energy and transverse energy deposition, the number of isolated muons and electrons, and the likelihood of jets;
- the error status of adder cards, CFLTP, and calorimeter DAQ.

Data Processing

The data from the adder cards is clocked differentially at ECL levels with a 24 ns period on ribbon twisted pairs to the CFLTP. Figure 2 shows a block diagram of the CFLTP input card which receives this regional data from 2 of the 16 pre-processor VME crates. Eight of these input cards serve the 16 regions of the calorimeter. Upon arrival, the data bits are latched, de-multiplexed, and synchronized with the local clock. The data are concatenated in pairs of words, and then clocked forward on a 48 ns clock. The data paths on the input card are configured by the contents of the on-board status register which is written/read from VME. In addition, a global address register exists on the input cards so that the cards may be addressed in subsets with global writes. There are two memories on the input card - the trigger FIFO, a dual-port SRAM which emulates a FIFO, and the main memory, 8K 256-bit words of fast CMOS SRAM. The main memory can accumulate crossing data directly, crossing data from the trigger FIFO, or simulated crossing data loaded from VME. Data may be stored in the trigger FIFO to be written into main memory on receipt of a first-level accept, which occurs approximately 35 crossings after the CFLTP has sent this data to the GFLT. VME may have access to the memories at the same time that data is flowing through the CFLTP to the backplane, where the cards are located which implement the global algorithms. Figure 3 shows an overview of the CFLTP "crate," which occupies essentially an entire rack. VME buses are embedded at the input and output, and can interact with the input cards, output cards, other VME modules on the buses, and the processor backplane. Data from the CFLTP input cards is routed via high density connectors to a multilayer (20 layers) processor backplane on 48 ns clock edges, and then as a 2048-bit wide bus to the algorithm cards. The electronics mounted on the backplane which performs the algorithms is implemented almost entirely in high-performance CMOS, and consists of alternate latches and banks of logic. Extensive use of lookup tables is made in the processing logic - there are somewhat over 300 tables, implemented as fast CMOS SRAM. Data bits are latched on 48 ns and/or 96 ns clock edges, propagate through logic, and valid output from each bank of logic is latched on the next set of latches on the next clock edge. In this way, eight sets of crossing data are resident in the CFLTP at any time, each set marching through latched on successive clock edges. When the data is fully processed, programmable switches located on the far end of the processor unit route either the actual processed data or emulated data (stored in FIFO's located on one of the processor unit's cards) from the far end of the processor backplane to the CFLTP output. The output section of the CFLTP is similar to the input section - data is received on high-density connectors from the backplane, formatted, and clocked to the GFLT at ECL levels. The output cards interact with the second embedded VME bus where a second 88000 RISC processor has the ability to histogram data, configure the data paths, read/write

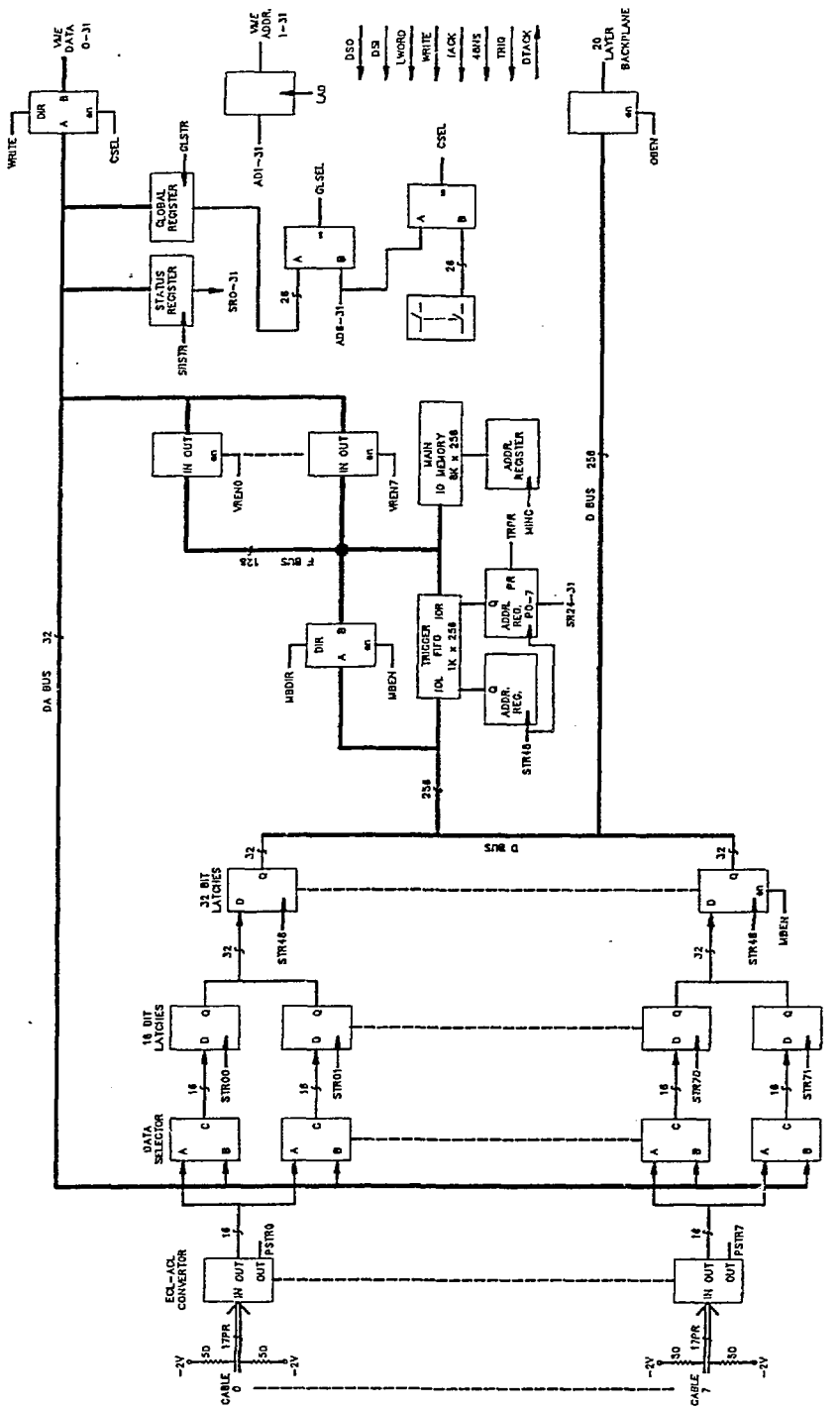
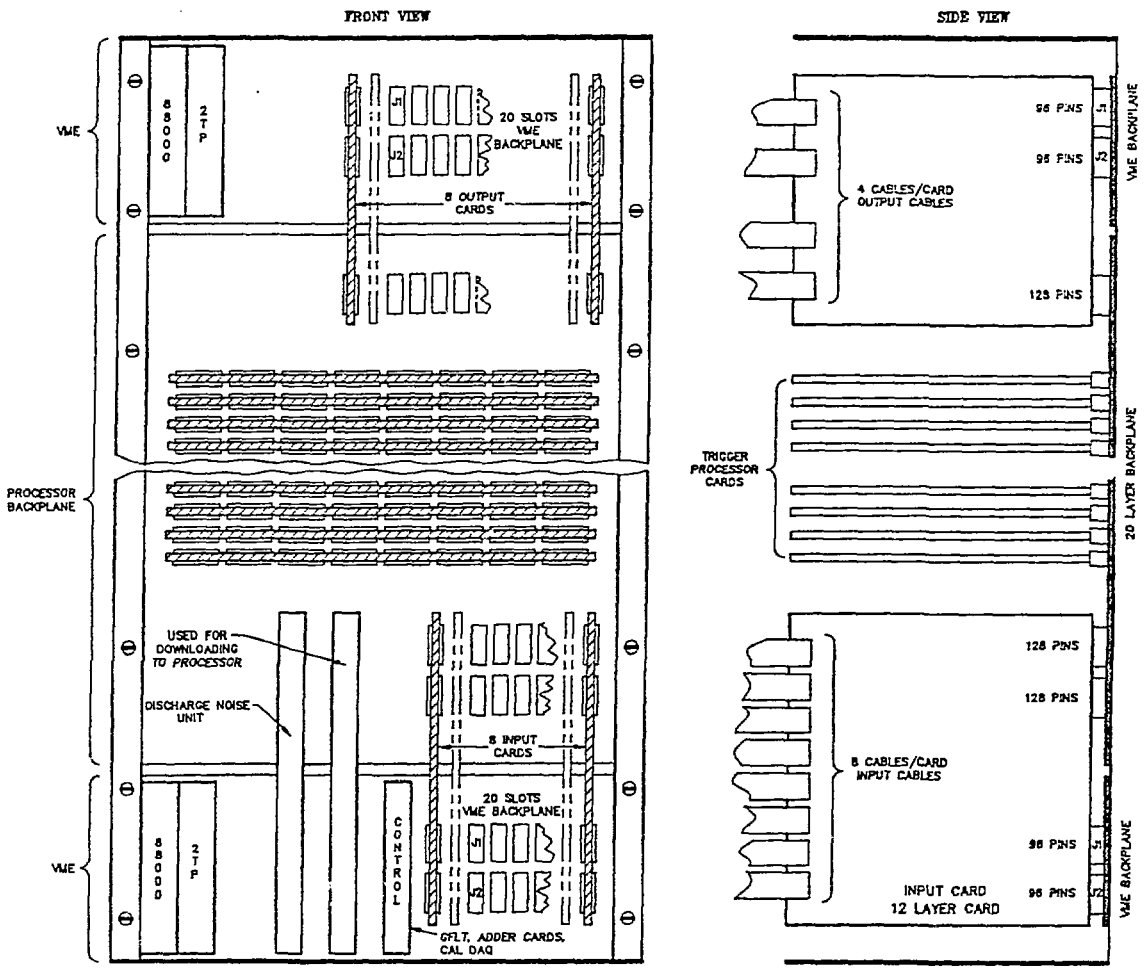


Fig. 2. CELTP input card block diagram.



ZEUS CALORIMETER FIRST LEVEL TRIGGER PROCESSOR MECHANICAL OVERVIEW

Fig. 3. Mechanical Overview of CFLTP.

registers and memory, execute diagnostics, etc.

Capture and Emulation

Data may be captured and transported to VME for histogramming on board the CFLTP or for forwarding to the host equipment computer. Two types of data capture are possible; the first captures input and output data that resulted in a GFLT first-level accept. This will happen with an approximate rate of 1000 Hz. The second type captures input and output data for 4096 beam crossings, which may be consecutive, in which case the captured data corresponds to 384 microseconds of real time. Input or output data can be simulated by loading data patterns under software control via the two embedded VME buses. Simulated crossing data for 4096 crossings may be downloaded from VME to main memory FIFO's and stored. On software command, the buffers feed data into the input or the output of the CFLTP at full speed. The FIFO's may be loaded either with software-generated data or with previously-captured data. Histograms are derived from data contained in FIFO's at the CFLTP input and output. Current histograms may be compared to benchmark histograms, and significant deviations reported to the equipment computer.

Current Status

Most of the algorithms have been definitized and are regarded as firm. A few algorithms, particularly those which recognize clusters for jet identification, are not entirely finalized. A trigger Monte Carlo has been written and the performance of the algorithms is being studied. The input card has been designed and prototypes are currently being manufactured as a 12U 400 mm VME card. This is a ten-layer card designed entirely in surface-mount technology. Aside from the input which receives the data at ECL levels, the circuit is designed in high performance CMOS discrete devices with a few EPLD's, and with F logic used at some points where propagation delays are critical. The conceptual specifications for the hardware are firm, and detailed design will proceed in step with finalization of the algorithms. Codes for the 88000 processors are being written in C to handle execution of diagnostics, initialization of lookup tables, histogramming variables, data transfer to the host, etc. Plans call for calorimeter modules to be calibrated in an on-going program in a test beam at Fermilab (E790). Subsets of the CFLTP hardware will be operated in the Fermilab test beam in conjunction with calorimeter module tests prior to the actual installation at HERA.

References

[1] W. H. Smith et al., ZEUS Note 89-085.

[2] R. L. Talaga, J. W. Dawson, ZEUS Note 89-086.