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# PHASE I OF THE AUTOMATED ARRAY ASSEMBLY TASK OF THE LOW COST SILICON SOLAR ARRAY PROJECT

Technical Quarterly Report No. 2

Motorola Report No. 2258/2

M. Coleman

July 1976

Work Performed Under JPL Contract No. 954363

Semiconductor Group
Motorola, Incorporated
Phoenix, Arizona

ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION
Division of Solar Energy

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By

M. Coleman

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## ABSTRACT

Phase I of the Automated Array Assembly Task, LCSSAP, is concerned with a comprehensive assessment of the improvements in existing technology that may be needed in order to develop, by 1985, an industrial capability for low cost, mass production of very durable silicon solar photovoltaic modules and arrays.

Both experimental, literature, and theoretical sources are being utilized to evaluate efficient solar cell design criteria and individual and synergistic process effects on the cost effective production and encapsulation of such efficient solar cells.

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## 1.0 Summary Statement

Studies on solar cell design improvement, process adaptation, process sequencing optimization, and encapsulation design and evaluation have progressed during this quarter according to plan.

A literature survey and evaluation of Schottky-type solar cells was performed. A metallization test pattern to study various line-widths in processing has been made with initial results available from photoresist and soldering processes. A study to investigate back surface reflectance from metallized back surface has been initiated. Studies are in progress to evaluate spin-on sources, printed metal contacts, plated contacts, and gettering. Cleaning by scrubbing has been investigated and found to enhance certain semiconductor device yields. Photoresist processing of textured surfaces has been modified as a result of a process sequencing study. A process selection criterion has been added to account for non-planar silicon surfaces. Early encapsulation design evaluations have been concerned with material selection and cell interconnection schemes.

## 2.0 Introduction

Phase I of the Automated Array Assembly Task, LCSSAP, is concerned with a comprehensive assessment of the improvements in existing technology that may be needed to develop, within a period of no more than 10 years, as industrial capability for low cost, mass production of very durable silicon solar photovoltaic modules and arrays.

This program incorporates solar cell design, process adaptation, process sequencing optimization, technology assessment, solar cell fabrication, encapsulation, and cost analysis in an interrelated way such that the final choice for particular solar cell automated process sequences will be realistic, and that any recommendations for specific additional studies to improve particular process steps will have an (estimated) high probability of success in a (promising) given process sequence.

## 3.0 Technical Discussion

### 3.1 Design Improvement

#### 3.1.1 Schottky Barrier Solar Cells

In Technical Quarterly Report No.1, it was stated that silicon solar cells using metal-semiconductor Schottky barriers are not currently considered to be the desired end products of a design model. While there are no present plans under this contract to fabricate Schottky cells with which to obtain empirical and theoretical correlations to strengthen the model, the statement needs expansion.

In order to obtain the LSSA Project goal of silicon solar cell panels which operate with at least 10% efficiency, it is necessary that the individual cells operate at greater than 10% efficiency. This is required since module optical transmission losses, thermal inertia, cell packing density, and space utilization will lower the overall efficiency.

A survey of the recent literature has been performed, and a list of references in chronological order follows this section. No reference has been found which reports large area silicon Schottky-type solar cells which exhibit greater than a 9.5% efficiency[9]. (Schottky-type cells with 15% efficiency have been reported on GaAs.[15]) Recent professional society conferences have given no indication that a breakthrough in the present state-of-the-art of silicon Schottky cell technology is imminent. In fact, although theoretical computations have been mentioned in the literature claiming that the upper limit on conversion efficiency is slightly better for a Schottky barrier cell than for a p-n junction cell,[7] the state of the technology is quite the opposite.

Metal-semiconductor solar cells reported to date exhibit inherently low output voltages. This effect is a consequence of high diode "saturation" currents (in the dark) and low metal-semiconductor barrier heights. Thus the possible high photo-generation current densities theoretically available with Schottky cells are offset by low output voltages.

Metal-oxide-semiconductor solar cells[5,12] have been fabricated, exhibiting open circuit voltages as high as 0.52 volts.[18] In such cells, current flow requires tunneling through the interfacial layer. The best such cells have shown only an 8% conversion efficiency, [8,16] indicating reduced current collection efficiency through the interfacial layer compared to the metal-semiconductor cells.

No experimental results have been shown to give credence to the possibility of obtaining increased Schottky cell voltages while maintaining high currents. On the other hand, the high generation current possibilities ascribed to such cells can be approached by p-n junction cells. In fact, high generation current densities along with high open circuit voltages have been reported for p-n junction solar cell structures fabricated incorporating violet-cell and textured surface techniques.

It is often stated (or implied) that Schottky cells are easily fabricated, giving an inherent processing simplicity (and cost) advantage over junction cells. This is a major misconception. Schottky cells require precise control of metal depositions in the thickness ranges of less than 100A in order to optimize trade-offs between conductivity and reflectance. Such control is difficult by evaporation, and more controllable sputtering techniques

have resulted in lower open circuit voltages, presumably due to penetration of the sputtered atoms through the interfacial layer into the silicon.[19] Yield efficiency, and cost problems can be expected to continually plague this fabrication step. Schottky-type solar cells require the same highly conductive metal collection grid and anti-reflection coating deposition as p-n junction cells. Rather than being simpler, the fabrication complexity for a good silicon Schottky solar cell would be about the same that of a good silicon p-n junction solar cell. It is Motorola's conclusion that the technological uncertainties that must be resolved in order to demonstrate the (slight) theoretical advantages of the silicon Schottky solar cell are much too great to permit considering it as a serious contender at this time.

3.1.1.1 Schottky Barrier Solar Cell Bibliography


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### 3.1.2 Metallization Test Pattern

A major factor in determining solar cell performance is the metallization pattern. The metallization must efficiently collect current while shadowing the minimum active area. In achieving optimum designs, thus, it is necessary to determine allowable contact metallization line widths, both from an achieveable fabrication feasibility standpoint and from a series resistance standpoint.

The limitations of metal contact pattern linewidths will vary with the surface flatness of the silicon. Accordingly, two types of surfaces are being studied: polished and texture etched. These two types of surfaces represent extremes in surface microscopic smoothness. Both, however, are on macroscopically plane surfaces and will not necessarily reflect the effects of surface warp or ripple possible from sheet or ribbon growth. The effects of these latter parameters must be evaluated when sufficient representative ribbon samples become available.

A test pattern photoresist mask has been designed with linewidths ranging from 0.0003 inch to 0.0500 inch. Dielectrics (or metals) can be patterned on the desired surfaces by standard photolithographic techniques.

The evaluation technique, on both polished and textured test wafers, will include the formation on the surface of a dielectric, either silicon dioxide

or silicon nitride, and the patterning of the dielectric with the test pattern. The patterns will be visually inspected and evaluated. The patterned wafers will then be electroless nickel plated and solder coated. Optical inspections will indicate minimum linewidth limitations due to photoresist procedures, and electrical continuity measurements will determine line resistance after soldering. Sheet resistance will be tabulated versus metal linewidth for both textured and polished surfaces to determine the relative advantages of using a small number of wide lines versus a large number of narrow lines for solar cell current-collecting patterns.

Preliminary results to date indicate, exactly as expected, that there is no problem in obtaining the smallest (0.0003 inch) line width on polished wafer surfaces using our standard photolithographic techniques and equipment. To the contrary, textured surfaces present a special problem. In order to maintain the integrity of the dielectric covering the peaks of the textured surface pyramids in areas where no preohmic pattern is to appear, a much more viscous photoresist must be used (240 cp versus the standard 44 cp, as discussed in Section 3.3.3). The application of this viscous resist produces a much thicker layer of resist in the "troughs" of the textured surface, and this, in combination with the optical properties of the textured surface itself, seems to set a practical lower limit on preohmic line width resolution. Patterns were formed by contact printing from the mask. Inspection has shown that line widths smaller than 0.001 inch have not been clearly and consistently opened. Textured surface pyramids may have base widths on the order of 10 microns; therefore line widths of 0.0005 inch (12.7 microns) may encompass only a single pyramid. Pyramid heights on the order of 10 microns prevent true contact printing. Thus, light scatterning among the pyramids may inherently limit the line width resolution. A more columuated light source for exposure, such as is used with projection or proximity printing, might help minimize this problem.

The wafers used for the photolithographic studies above, as well as a comparable set of polished test wafers, will be plated with nickel and solder-dipped to obtain maximum metal build-up for a given line width. These lines will then be measured for sheet conductance/resistance.

Early experiments with textured surface wafers which were coated with silicon dioxide and prepared using standard viscosity (44 cp) photoresist have indicated that solder build-up on metal lines between 0.0003 inch and 0.0500 inch in width is less than a hemicylindrical bead. For line widths less than or equal to 20 mils, soldered line sheet resistance $\rho$ (in $\Omega$/sq.) is given by

$$\log \rho = -1.09 - 0.75 \log W$$

where W is the line width in mils. This means $\rho$ is proportional to $W^{-3/4}$. If the solder bead build-up were hemicylindrical, then $\rho$ would be proportional to $W^{-1}$.

For line widths greater than 20 mils the capillary effect of fine lines tends to become suppressed and the sheet resistance become independent of line width. However, the relation between sheet resistance and line width given above for lines less than 20 mils wide implies that, for a given area of metal line coverage, one wide contact finger will introduce more series resistance than two contact fingers, each half as wide. Thus, for soldered contact systems of equal total area, many narrow fingers are more efficient than few wide fingers, as long as the thinnest lines are at least 0.001 inch wide to preserve physical and electrical continuity.

This work is continuing, and more definitive results will be presented in later reports.

### 3.1.3 Back Surface Reflectance Experiments

Two back surface reflectance experiments have been initiated to determine if any cell performance advantages can exist with patterned back metallization. The first experiment is a reflectance/absorption experiment on non-device wafers. The second experiment is a spectral response measurement on active cells both with and without back metal at the illuminated region. While wafers are in process for these experiments, no results are as yet available.

### 3.2.1 Spin-on Sources

Spin-on application of diffusion sources is commonly used in areas of the semiconductor industry today as an alternative to the more conventional gaseous carrier method. Further, spin-ons can be utilized to provide antireflection coatings on photosensitive devices such as solar cells. Evaluation of this technology is a necessary portion of the technology assessment for this contract.

Most present uses are on round wafers which are readily spun at high speeds during application. Such spinning application may not be transferrable to rectangular ribbon or very large sheet geometries, but may require spray-on or roll-on technology to be developed. Other than the exact application method, however, the remainder of the technology should be directly applicable to future geometries.

A bibliography of Motorola authored papers and patents follows this section. A more comprehensive literature survey is not contemplated at this time.

Typical spin-on sources consist of a solution of an organic silicate, an alcohol, and a small proportion of an organic compound of the desired dopant element. The solution is usually filtered and is in the form of a liquid, not a suspension. It is applied to the wafers using standard photoresist spinners. Subsequent heat treatment forms a doped silicon oxide layer on the surface of the wafers, the organic components being driven off.[21] This densified layer acts as the dopant source during diffusion.

Spin-on diffusion sources can be formulated for specific dopants and dopant concentrations.[22,23,24] In addition, as is the case for gaseous diffusion sources, sheet resistivity and junction depth can be controllably varied by varying the diffusion temperature and time. Dopant surface concentrations have been varied up to solid solubility and have been established experimentally to be controlled by the dopant concentration in the spin-on film.[24]

Wafer-to-wafer dopant uniformity has been shown to be excellent. A lot of 52 wafers, for example, boron diffused from a spin-on source showed a mean standard doping deviation of 3%.[25] Production performance has also been tested on small signal pnp transistors manufactured solely from spin-on sources. Such transistors met all the DC electrical specifications for devices manufactured from conventional gaseous diffusion sources.[26]

Since diffusion occurs from a doped oxide film, simultaneous diffusion of different dopants and/or concentrations can be performed simultaneously on opposite sides of the wafer without concern for cross-contamination. This feature could allow, for example, p-n junction formation simultaneous with back surface field diffusion.

Spin-on sources to deposit antireflection coatings of silicon, tantalum, or titanium oxides have been formulated. As an example, a single application of spin-on gave a $TiO_2$ film which can be patterned in the as-deposited conditions. Following a 925°C densification, it had a thickness ranging from 800 to 1100A was resistant to HF etching, and had an index of refraction of approximately 2.0. Application following metallization would require much lower temperature annealing steps; no data have been taken as yet on lower temperature densification.

Textured silicon surface, as well as ribbon or other surfaces with irregularities in the macroscopic range, may cause some problems with spin-on diffusion sources. It is possible, for example, that the pyramids of a textured surface might cause uneven film thickness, being thicker than average in the valleys between pyramids and being correspondingly thinner at the tips of the pyramids. These comments have an impact on diffusion spin-ons, but have an even greater impact on spin-on coatings designed as anti-reflection coatings. Thickness variations in an AR coating will have a first order effect on cell performance. These considerations, as well as similar considerations for large or irregular surfaces and for photoresist application, indicate the need for studies of alternate application methods.

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### 3.2.2 Printed Metal Contacts

Screening-on contacts for solar cells for large scale arrays has considerable appeal due to the possible lower cost of this approach when compared with more conventional methods of contacting silicon, such as metal evaporation, sputtering, or even plating through holes patterned in a dielectric on the cell surface. The screening-on process itself is not only faster, but the capital cost of equipment may be lower. The line widths required for solar cells are close to the limits of resolution of silk screening, however, and may limit its use to plane polished surfaces.

An experimental investigation has been intiated to evaluate silk screened or printed metal contacts to solar cells. Samples of several formulations from two vendors have been ordered. The formulations of the conductive inks from these vendors are based on either copper or silver. Both formulations may be applied directly to silicon for contacts, but both require a high temperature "firing" to form ohmic contact to the silicon.

It is not apparent, without actual experimental evaluation at this time, that such application and firing will be without problems. It is anticipated, in fact, that low temperature firing of these contacts will result in poor contact adherence and poor interconnection reliability, while high temperature firing will generate yield and efficiency losses due to alloying, shorting, or lifetime degradation when applied over shallow p-n junctions.

The nature of the contact between silicon and a sintered screened-on contact is not known since most of the applications for these materials relate to ceramic substrates. If the contact actually forms a (shallow) compound, such as a metal - silicide, the contact may be expected to capable of exhibiting reliable performance. However, if the screened-on contact interface to silicon is merely physically adherent, then there is a high probability that the action of temperature cycling, particularly in the presence of moisture, will cause the contact interface to gradually increase in resistance and eventually become open. A study of the nature of sintered screened-on contacts to silicon is considered an important part of this phase of the study.

### 3.2.3 Silicon Nitride Deposition

Silicon nitride could constitute an excellent choice for the anti-reflection coating on silicon solar cells. In addition to its useful refractive index, it is the best passivant for silicon known to the semiconductor industry. It is extremely stable and inert, but possesses the ability of being deposited by low temperature CVD processes in a "soft" state, being easily patterned by standard $SiO_2$ processes, and subsequently being densified by a modest thermal cycle to its high density state. The CVD deposition process could be much cheaper than a vacuum deposition process, and comparable to (or cheaper than) a spinning process if the reactor capacity can be made large.

Silicon nitride has been deposited at 600°C in a hot wall, quartz lined furnace. The nitride is deposited from the reaction of silane ($SiH_4$) and ammonia ($NH_3$) in a nitrogen carrier gas. Deposition cycles of approximately 50 minutes have resulted in silicon nitride layers of 1050A° ± 100A°, this excellent uniformity applying to both variations within a run and variation from run-to-run. As established, the process deposits the nitride on wafers placed horizontally in the furnace; as a result this deposition system is capable of processing only five 3" wafers per run. This low throughput would be unacceptable for long range LSSA project goals.

As an alternative deposition approach, increased area throughput has been reported if deposition occurs at a reduced (less than 1 atmosphere) pressure. Such a system has been constructed in our laboratory. Preliminary shakedown experiments have shown ±5% thickness uniformity over runs of 50 wafers with total deposition times approximating the previous horizontal system for five wafers. Further results will be presented in later reports.

### 3.2.4 Cleaning by Scrubbing

A technique relatively new to the semiconductor industry is cleaning of silicon wafers by the mechanical scrubbing of their surfaces with brushes. Until recently, such scrubbing was avoided to eliminate possible mechanical damage to the silicon surface. Studies have shown, however, that removal of tightly adhering (and otherwise difficult to remove) dirt particles can be achieved through scrubbing without silicon damage.

Numerous vendors now have automatic and semi-automatic scrubbing equipment available. Yield increases of several semiconductor lines within Motorola (precise data is considered proprietary by those lines) indicate that scrubbing is technically advantageous. A cost study will be performed to evaluate its ultimate inclusion in an automated solar cell factory.

## 3.3 Process Sequencing Optimization

### 3.3.1 Plated Contacts

A preliminary process for plating contacts to solar cells has been established. Early results from the process indicate a high reproducibility, good ohmic contact, good metal adherence, and ready solderability.

The initial process investigated in our laboratory was electroless nickel plating. As had been the apparent industry experience in the past, this system first showed both reprodicibility and adhesion variations which were deemed unacceptable. Further work in our laboratory produced an advanced nickel plating process which minimized these fluctuations but did not eliminate them.

The new process utilizes the advanced electroless nickel plating process. Rather than plating directly onto silicon, however, the nickel is plated

onto a previously plated layer of another base metal, palladium. The palladium is plated with excellent reproducibility and can be made to form an excellent bond with silicon. Further discussion of this process will be presented as the study progresses.

### 3.3.2 Gettering Processes

A major concern in many semiconductor devices is the minority carrier lifetime. As a result, many techniques have been identified which are claimed to either preserve or improve minority carrier lifetimes. A program to evaluate some of these techniques and their interaction with other processing steps has now been initiated on this contract.

Initial experiments will be limited to two techniques: heavy phosphorus diffusions and temperature ramping experiments. Planned follow-up experiments will study the effects of HCl leaching during high temperature process steps, and surface damage gettering.

A literature survey on these and other techniques is being performed and will be presented in a future report.

### 3.3.3 Textured Surface Processing

A process sequencing study has investigated photoresist coverage of textured surfaces. The study has resulted in modifications to the photoresist procedure.

In our laboratory, normal photoresist procedure for polished wafers utilizes thin, 44 cp (0.044 $N \cdot s/m^2$) photoresist and spin speeds of 5000 rpm. This procedure was applied to patterning silicon nitride layers deposited on textured surfaces. Figure 3-1 is a scanning electron microscope (SEM)

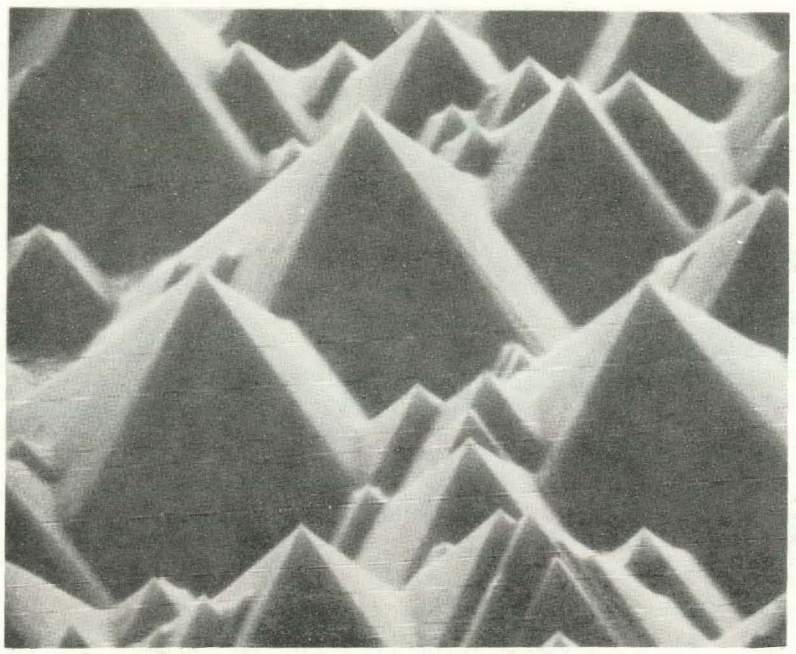


FIGURE 3-1: SEM Photomicrograph of textured silicon surface following removal of deposited silicon nitride surface layer. 5000X, $60^{o}$ tilt.

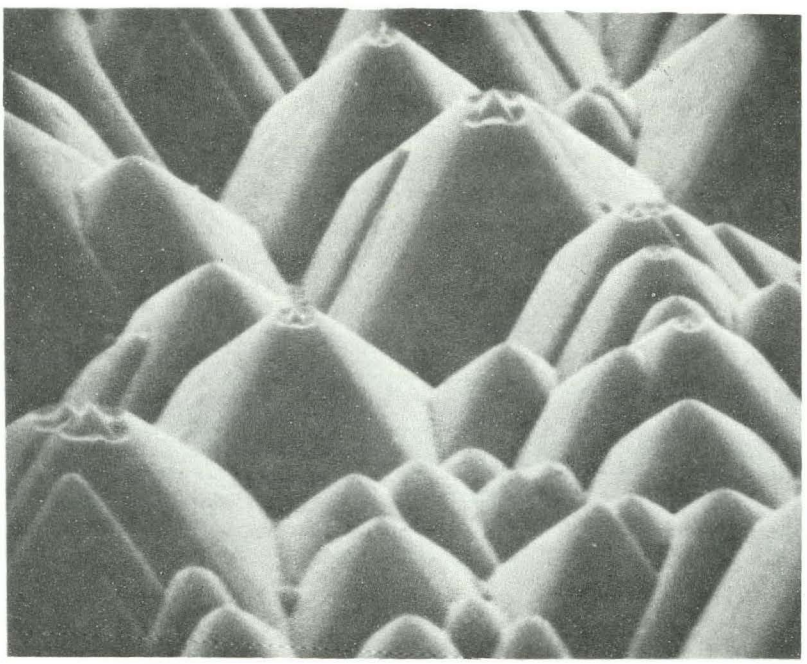
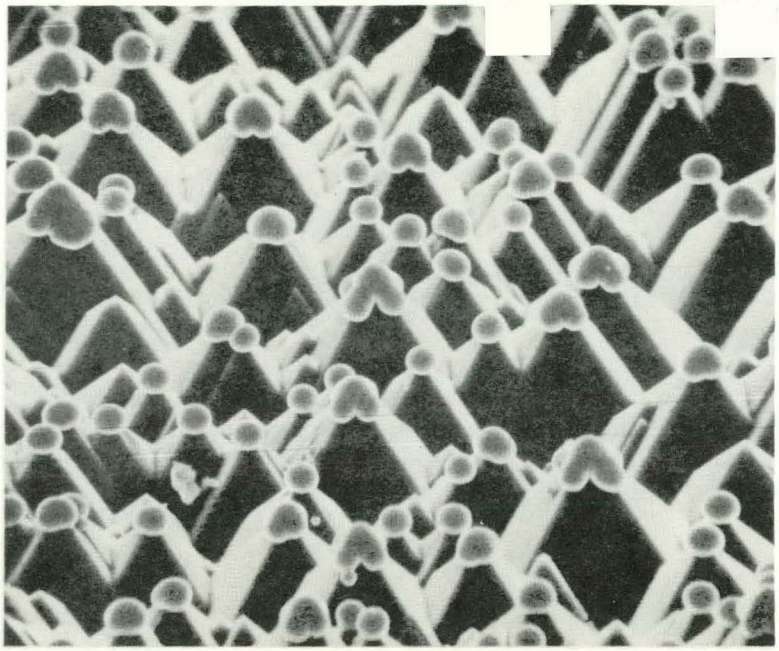
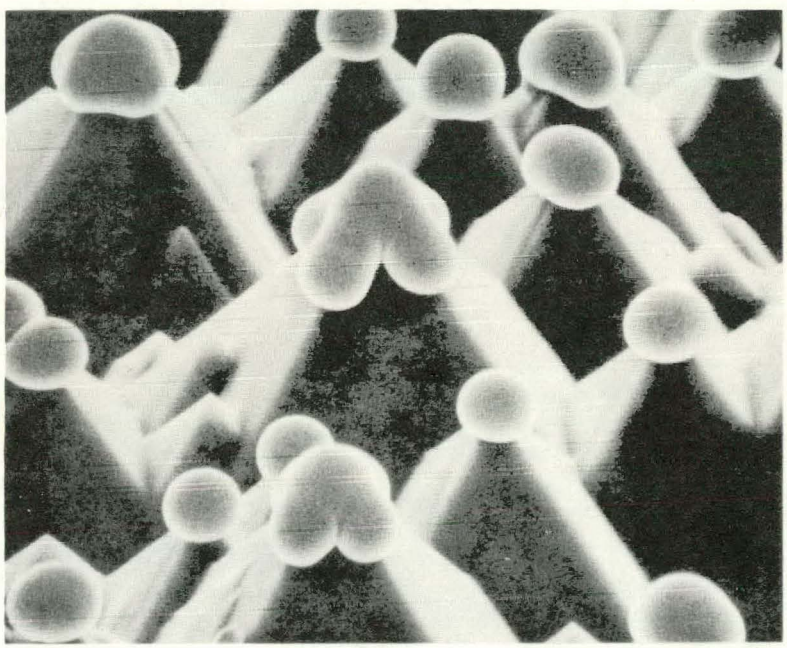


FIGURE 3-2: SEM Photomicrographs of silicon nitride covered textured surface with nitride etched from some pyramid peaks. 5000X, $60^{o}$ tilt.



(a)



(b)

Figure 3-3: SEM photomicrographs of electroless nickel plated surfaces of unprotected pyramid peaks. (a) 2000X, 60° tilt; (b) 5000X, 60° tilt

photomicrograph (5000X) of an area on the textured surface with the silicon nitride removed. Figure 3-2 is another SEM photograph (5000X) of an area on the same wafer, protected during nitride etching by photoresist.

Note that the tips of some of the pyramids have the nitride missing, and bare silicon protrudes. Examination of the nitride around the exposed silicon points indicates that etching, not fracture, is the cause of nitride removal, eliminating mask contact during photoresist or wafer handling techniques as the cause. This conclusion is substantiated by two observations. First, the general appearance of the remaining nitride is regular, unlike a glass or concoidal fracture. Second, the nitride has been removed from the peaks of pyramids of varying heights with no apparent damage to the sharp silicon peaks of the higher pyramids. To substantiate this last observation, the wafer was electroless nickel plated. Results are shown in Figure 3-3(a), (2000X), and 3-3(b), (5000X). Here, nickel has plated on exposed silicon at pyramid peaks of varying heights.

Following identification of this phenomenon as a photoresist problem, the photoresist technique has been modified. Complete photoresist protection appears to be achieved by increasing photoresist viscosity to 240 cp (0.24 $N \cdot s/m^2$) and reducing spin speeds to 3000 rpm.

### 3.3.4 Effects of Non-Planar Surfaces

At this point in time, it is not known which of the various large area sheet growth techniques will be successful in providing large quantities of sheet at prices capable of being processed into solar cells arrays at $0.50 per peak watt in the 1985 target time frame. It is becoming obvious, however, that sizes, shapes, and uniformity can vary widely within some proposed processes, and from process to process. Some processes may be capable of producing

smooth, flat surfaces over large areas. Other processes may have extreme surface variations including ripple, bending, and warp, all of which may occur to varying degrees within any given area.

The geometrical variations in silicon sheet can greatly influence the usefulness of some solar cell processing, fabrication, and encapsulation choices. It must be made clear at this point in time that two separate philosophies may be pursued. The first simply states that the large area sheet must conform to certain geometrical limits in order to allow solar cell processing and encapsulation to be performed by essentially conventional silicon wafer processing methods. The second, the converse of the first, states that whatever the shape that results from the sheet growth method, it will be used, forcing solar cell processing and encapsulation to conform to the delivered geometry.

The most likely ultimate choice will be a compromise between the two extreme philosophies. The compromise may, however, provide non-planar and rough surfaced sheets as compared to today's surface texture and flatness standards for wafers. Accordingly, processes which are recommended under this Task IV study must have the flexibility of handling such future material, or must be clearly labeled as applicable only to optimum surfaces. Motorola is thus adding a "process tolerance of irregular sheet geometries" as a criterion in recommending process choices.

## 3.4 Encapsulation

### 3.4.1 Module Materials

Materials must be chosen for solar cell modules, both for interconnection and for encapsulation, on the basis of functional compatability, long term reliability, and cost.

A tentative set of materials for encapsulation has been chosen for early studies. The configuration will include a metal back plate and a glass cover plate. A transparent silicone compound will fill the volume between the glass and the solar cells, while a copper-kapton laminate forms the cell interconnection paths and primary electrical insulation system between the cells and the metal back plate. A thermally conductive silicone completes the electrical insulation while providing a thermal path for heat removal from the cells. A metal bezel will provide both mechanical strength and an area for placing moisture barrier gasketing.

A primary module failure mechanism is anticipated to be interconnect corrosion, possibly greatly aggravated by moisture penetration. Accordingly, tests and test structures to observe moisture penetration are being evaluated to provide design criteria.

### 3.4.2 Solar Cell Interconnection Schemes

Increased solar cell performance and improved module reliability can be achieved through the use of multiple contacts on each cell, as discussed in our first quarterly report. Solar cell interconnection schemes within the package will have further significant bearing on performance and reliability.

If all solar cells within a module are connected in series, the module is highly vulnerable to catastrophic failure modes. If the contact to either polarity of any single cell fails electrically open, the entire module fails. Multiple redundant contacts to each cell will reduce the chances of such cataclysmic failure, but failure of one contact may still reduce power by an undesireable amount. Modules with cells in series are susceptable to total failure not only from internal connections, but by having one cell shadowed externally by relatively small objects such as leaves, debris, or wildlife.

The effect of such failure mechanisms may be minimized or, for all practical purposes, alleviated by incorporating internal module redundancy through the use of parallel or series parallel cell interconnection schemes. Such schemes increase module reliability while ensuring at least equivalent total system performance. The use of parallel oriented interconnections in solar cell modules is recommended for enhanced reliability in operation. Efforts have been, and are continuing to be, expended to develop efficient parallel and series-parallel interconnection schemes which can help meet the long range project goals.

## 4.0 Conclusions

The suitability of Schottky barrier solar cells has been evaluated and deemed unlikely to be a preferred (or even equal) contender with p-n junction cells for successful achievement of LSSA Project goals. A metallization test pattern has indicated that photoresist patterned lines on textured surfaces must be at least 0.001 inch wide. Similarly, a thick viscosity photoresist must be used to adequately protect pyramid peaks on textured surfaces. Based upon experience internal to Motorola and upon claims from vendors, silicon cleaning by scrubbing is a viable technical process capable of increasing semiconductor device yields. This process will be considered for potential incorporation in recommended process sequences, dependent on costs. Potential ribbon geometry variations and irregularities will have significant impact on process choices; this criterion has been added to the technology assessment study. Modules with parallel or series-parallel cell interconnections appear to have improved reliability over modules with series interconnected cells. Efforts must be made to design efficient parallel interconnection schemes.

## 5.0 Recommendations

It would be beneficial for TASK IV to have preliminary data and expectations on geometrical features of the various sheet growth approaches funded in TASK II in order to make meaningful decisions on process and encapsulation approaches.

## 6.0 Current Problems

No specific problems have occurred to the date of this report.

## 7.0 Work Plan Status

The work plan is on schedule.

## 8.0 List of Action Items

No items requiring unusual action have come to light during this report period.

## 9.0 Program Expenditures

The following are the man hours and costs expended in the performance of the program:

1. MANHOURS

| Previous Expenditures | Current Month Expenditures | Cumulative Expenditures |
|---|---|---|
| 3794 | 1234 | 5028 |

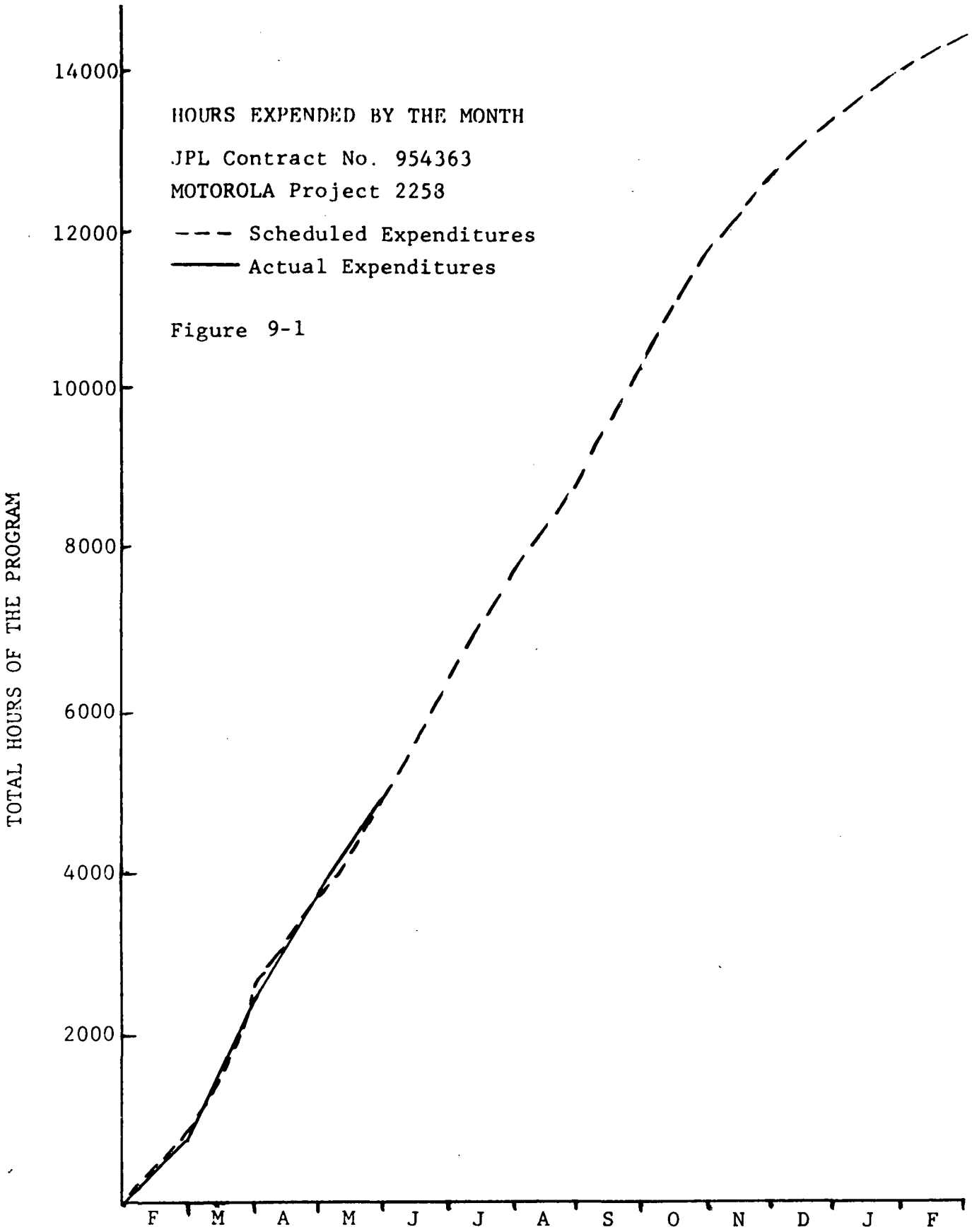
2. FUNDS

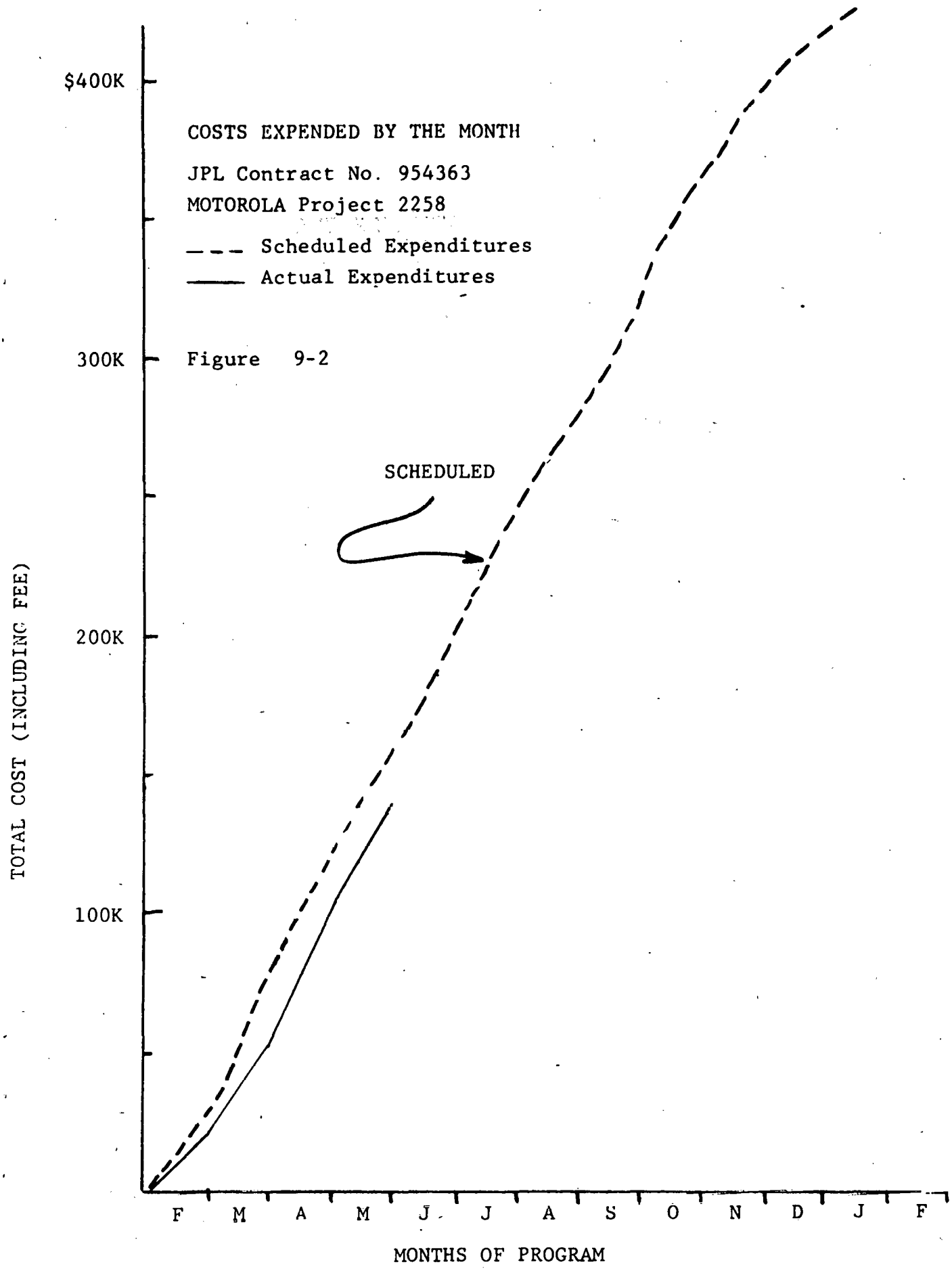
| Previous Expenditures | Current Month Expenditures | Cumulative Expenditures |
|---|---|---|
| 102,322 | 37309 | 139,631 |

Figures 9-1 and 9-2 depict graphically the hours and costs expended by month.

## 10.0 Milestones

Status of the program is shown on the Milestone Prediction and Accomplishment Chart, Figure 10-1.


HOURS EXPENDED BY THE MONTH
JPL Contract No. 954363
MOTOROLA Project 2258
--- Scheduled Expenditures
——— Actual Expenditures
Figure 9-1
TOTAL HOURS OF THE PROGRAM
14000
12000
10000
8000
6000
4000
2000
F
M
A
M
J
J
A
S
O
N
D
J
F
MONTHS OF PROGRAM


COSTS EXPENDED BY THE MONTH
JPL Contract No. 954363
MOTOROLA Project 2258
Scheduled Expenditures
Actual Expenditures
Figure 9-2
SCHEDULED
$400K
300K
200K
100K
TOTAL COST (INCLUDING FEE)
F M A M J J A S O N D J F
MONTHS OF PROGRAM

MILESTONE PREDICTION AND ACCOMPLISHMENT CHART

MOTOROLA PROJECT No. 2258 JPL CONTRACT No. 954363

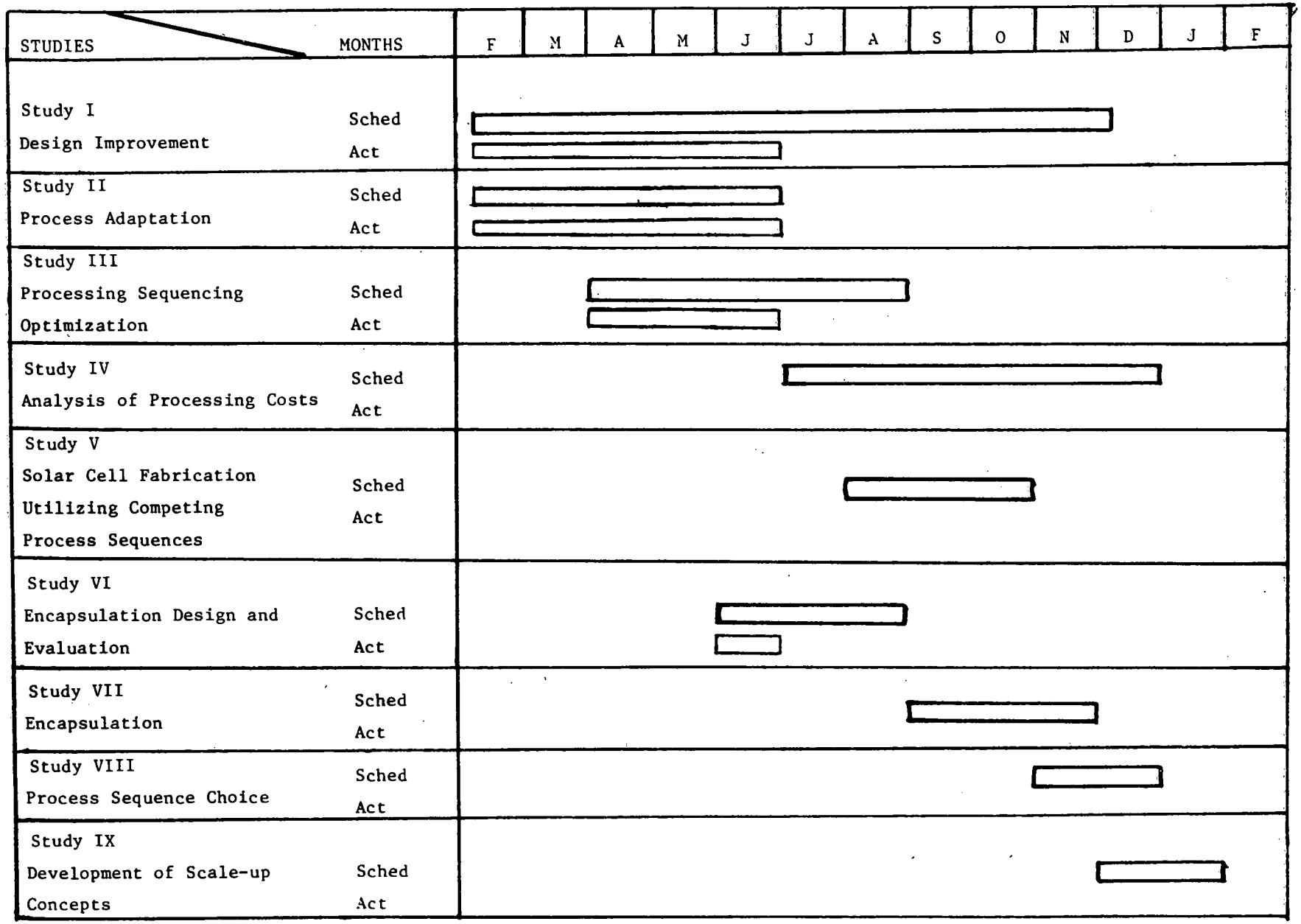
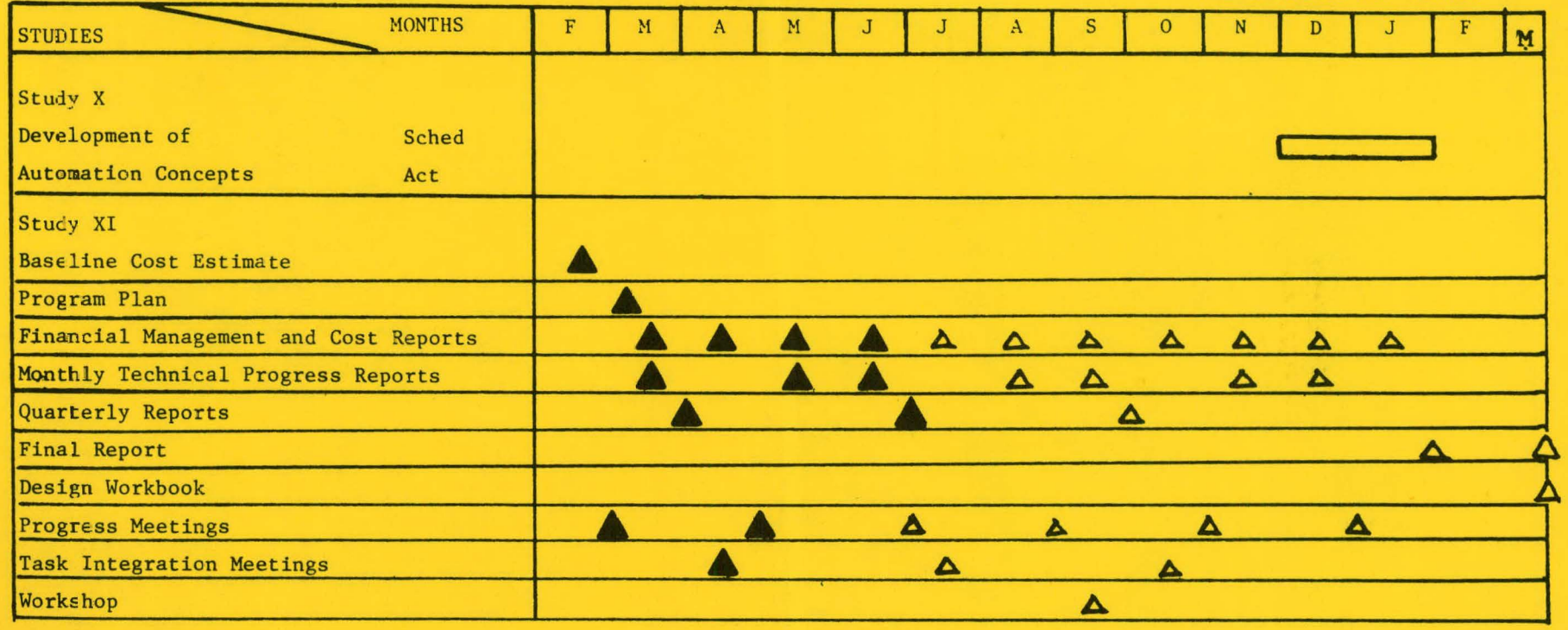



FIGURE 10-1

MILESTONE PREDICTION AND ACCOMPLISHMENT CHART

MOTOROLA PROJECT No. 2258 JPL CONTRACT No. 954363




Legend: Scheduled △ Completed ▲ Date: May 31, 1976

FIGURE 10-1