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PHASE I OF THE AUTOMATED ARRAY ASSEMBLY TASK OF THE LOW COST SILICON SOLAR ARRAY PROJECT

Motorola Report No. 2258/1

Technical Quarterly Report No. 1

M. Coleman

April 1976

Work performed under JPL Contract No. 954363

Semiconductor Group
Motorola Incorporated
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ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION
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By

M. Coleman

PREPARED BY

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"The JPL Low-Cost Silicon Solar Array Project is funded by ERDA and forms part of the ERDA Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays."

ABSTRACT

Phase I of the Automated Array Assembly Task, LCSSAP, is concerned with a comprehensive assessment of the improvements in existing technology that may be needed in order to develop, by 1985, an industrial capability for low cost, mass production of very durable silicon solar photovoltaic modules and arrays.

Design criteria for efficient solar cells are discussed, emphasis being given to front metal surface pattern and texture etched front surfaces. A generalized processing matrix, containing competing methods for solar cell manufacturing steps, is outlined. The steps in this processing matrix are discussed and characterized according to immediate and potential usefulness. Representative steps have been chosen for empirical evaluation.

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1.0 Summary

This report features the results of an abbreviated first quarter. The program was initiated during February and is proceeding according to plan.

A preliminary process matrix, with initial ratings, was set up as an aid to the continuing technology assessment study. Work on solar cell design has pointed to the desirability of multiple contacts on a solar cell for improved performance. The use of a textured surface can have a large effect on optical absorption; in addition, it interacts with other parameters to affect the internal cell design for optimal performance. A group of eight processes has been selected for initial process adaptation study. These processes are texture etching, photolithography, silicon nitride, diffusion, ion implantation, electroless nickel plating, solder coating, and phosphorus gettering.

2.0 Introduction

Phase I of the Automated Array Assembly Task, LCSSAP, is concerned with a comprehensive assessment of the improvements in existing technology that may be needed to develop, within a period of no more than 10 years, an industrial capability for low cost, mass production of very durable silicon solar photovoltaic modules and arrays.

Mass production may utilize continuous processing if the starting single crystal silicon substrate material is in the form of continuous ribbon. Alternatively, it may prove desirable to cut a continuous silicon ribbon into segments and utilize either continual (i.e., each substrate segment follows the preceding one through the process sequence) or batch processing. The final fabrication sequence need not be designed around any single process strategy, but indeed may employ continuous, continual, or batch processing for different parts of the fabrication sequence. Of course, if the starting single crystal silicon is in the form of large (but not continuous) sheets, then continuous processing for solar cell fabrication is excluded. If the starting single crystal silicon is deposited on an insulating substrate, continuous or continual/batch processing may all be considered; however, in this case, the process sequence (and solar cell design) must be adapted to one-sided fabrication and metallization.

Considerations like these emphasize the interdependence of the Automated Array Assembly and Large Area Silicon Sheet Tasks of LCSSAP. Similarly, Automated Array Assembly and Encapsulation Tasks are highly interdependent. For example, the shape and area of a solar cell, and whether contacts are made to both surfaces or only one, will have important ramifications in package design and processing. Consequently, this study will require utilization of information gained via frequent interactions with other

LCSSAP task groups; in some cases, where clear-cut directions are not available, evaluation of alternate choices, with an attempt to determine their relative probability of success, will be necessary.

This program is structured on the thesis that improvements in solar cell module cost/performance/reliability through process (and concomitant materials selection) improvement will, in the final analysis, require demonstration. Further, a given process step must be demonstrated as part of a complete sequence if its true value is to be accurately assessed. In additon, solar cell design is a variable that must be considered anew with each process modification. Accordingly, solar cell design improvement is a study that starts at the beginning of the program and continues throughout most of it. The process adaptation study has the objective of testing the suitability to solar cell fabrication of certain new processes, as well as selected processes common to the silicon semiconductor component industry but not widely applied to solar cell production. This study starts at the beginning of the program; after a few months it branches into process sequencing optimization which emphasizes that the sequence in which processes are performed can be just as important as process selection.

Technology assessment will be a continuing part of the program, and a processing matrix has been set up to assist in this study. It will identify processes (and concomitant materials) for further study, while, on a continuing basis, rejecting certain technologies based on analysis of information available at the time.

Solar cells will be fabricated and encapsulated during the latter part of the program. Final cost analyses and process sequence selection (including recommendations for future work) will be based upon all of the studies performed --- design improvements, process adaptation and process sequencing optimization, solar cell fabrication, and technology assessment.

3.0 Technical Discussion

3.1 Study I - Design Improvement

A rational means of determining which elements of the "Processing Matrix" are feasible, which are highly desirable, and which are not likely to be useful for the mass production of low cost silicon solar cells must be based on a solar cell design model which reflects current state-of-the-art practices as well as additional concepts not currently incorporated in solar cells but envisioned as likely to contribute to future solar cell improvement. The prime directive for the Design Improvement Study is to develop a solar cell design model (or design models) which effectively characterize the highest efficiency silicon solar cell capable of being produced utilizing current or anticipated semiconductor processing techniques, subject to the major constraint that the estimated cost in dollars per watt of the final assembled and installed array of silicon solar cells be minimized. In ruling against (or in favor of) various design elements which could be incorporated in such a model, consideration must be given not only to the feasibility and cost of processes in the "Processing Matrix" but also to the degree of control available over each process and the consequent control of performance variations for the solar cells being fabricated.

3.1.1 Baseline Design Model Considerations

This section presents what, in effect, is a "wish-list" of the desirable features of a high performance silicon solar cell which may be reflected in the components of a design model. This selection of features is based on current state-of-the-art solar cells as well as on developments which are known to be desirable. The list is subject to updating and revision as the work progresses and inputs are obtained from the other tasks of the LSSA Project.

The silicon solar cell should have an antireflective coating which:

(i) optimizes the transmission of incident photons into the silicon material;

(ii) promotes the lowest concentration of surface-state recombination centers at the coating-silicon interface;

(iii) aids in establishing an electric field within the silicon (near the surface) which retards minority carrier flow toward the front surface and recombination at the front surface;

(iv) passivates and isolates the P-N junction perimeter.

The antireflective coating may be single layered or multilayered.

The silicon solar cell should possess a silicon front surface condition which:

(i) minimizes surface defects and maximizes minority carrier lifetime near the silicon surface;

(ii) minimizes surface recombination velocities;

(iii) maximizes the absorption of incident photons by the silicon;

(iv) refracts the incident light to optically enhance the possible photon path lengths through the silicon substrate;

(v) promotes the adhesion of metal ohmic contacts.

The preparation of such a surface could involve chemical and/or mechanical manipulation of silicon substrates. Chem-etching, lapping, and polishing have been used traditionally. It has recently become apparent that texturing the silicon surface with an orientation-dependent chemical etch may provide a highly controllable, cost-effective way of obtaining most of the properties listed above while accruing additional benefits for solar cell design. A model for a textured front surface is discussed in further detail in a following section of this report.

The silicon solar cell must have a thin, front surface region with an electrical conductivity opposite that of the substrate (e.g., N type surface region on a P type substrate which:

(i) forms a metallurgical P-N junction;

(ii) is amenable to ohmic contact without degrading solar cell performance;

(iii) has low surface recombination velocities or is compensated to effectively minimize surface recombination effects (e.g., has built-in drift fields);

(iv) has sufficiently high minority carrier lifetime;

(v) maximizes the collection efficiency for short wavelength photons;

(vi) has a sufficiently low value of sheet resistance.

Property (v) implies that the P-N junction depth below the front surface be as shallow as can be allowed, subject to the other five properties. Traditionally, only junction depths of about 0.5 micron or less have been used and the best (violet-type) cells have junction depths closer to 0.1 micron. This requirement makes attainment of property (vi) more difficult. The possibility of silicon solar cells utilizing Schottky barrier junctions or field-induced junctions is not currently being considered for the design model. If it can be shown that these types of cells can produce solar cell panels of better than 10% efficiency, then they will be reconsidered.

The solar cell must have a silicon substrate which:

(i) has high minority carrier lifetime for maximum photo-current generation;

(ii) has high impurity doping level for high open circuit voltages and low electrical resistance;

(iii) is thick enough to efficiently absorb an appreciable fraction of incident long wavelength photons but is thin enough to conserve silicon;

(iv) has a low minority carrier recombination velocity at the back surface or is compensated (producing a drift field) to effectively minimize back surface recombination effects.

Minority carrier lifetime is of supreme importance to efficient solar cell performance; however, lifetime values eventually may be dictated by silicon purification processes. Under more immediate control and of particular interest insofar as a design model is considered is the optimum thickness of the silicon substrate. Special attention will be paid to this topic as the design model is developed and utilized.

The solar cell should have a silicon back surface condition which:

(i) minimizes surface defects and maximizes minority carrier lifetime near the silicon surfaces;

(ii) minimizes surface recombination velocities;

(iii) reflects unabsorbed incident radiation passing through the substrate and reaching the back surface.

By reflecting photons reaching the back surface the optical thickness of the substrate can be at least twice as great as the physical thickness. Moreover, unusable infrared wavelength photons can be re-radiated from the front of the solar cell rather than be absorbed by encapsulation materials beneath the cell.

Finally, the solar cell must have a front surface metal pattern which:

(i) provides ohmic electrical connection to the front side of the P-N junctions;

(ii) allows reliable, low-loss interconnection with other solar cells and with external circuits;

(iii) minimizes solar cell internal series resistance;

(iv) covers and therefore shadows a minimum of the cell front surface area.

Another possibility which must be considered is the use of transparent conductive layers to either augment or replace a standard metal pattern. Some preliminary conclusions on the nature of front surface metal patterns will be discussed in the following section.

3.1.2 Front Surface Metal Patterns

The front surface metal pattern of a silicon solar cell will affect the performance of solar cell modules in three ways: 1) the pattern must provide an interface point or points for electrical connection to other cells; 2) the pattern will shadow a portion of the active front surface of the cell; and 3) the metal pattern itself, as well as the cell below, will have an internal series resistance. Some preliminary conclusions regarding constraints on metal pattern design and on solar cell size can quickly be drawn by considering the interaction of these three effects.

Assume that a silicon solar cell is available with any desired surface area or shape but is constrained to have a fixed, minimum value of surface sheet resistance above the P-N junction. The series resistance of the cell will then depend on the amount of metal used for the front ohmic contact pattern and the resistivity of that metal. If the metal pattern coverage is limited to a reasonable percentage of the front surface area (say, 5 to 10%) and a particular metal system (and thereby thickness and resistivity) is adopted, then series resistance depends on pattern topology. The metal "current collection" fingers on the cell surface may contribute appreciably

to series resistance. As the cell surface area becomes larger, and the metal current-conducting paths become longer, a point will be reached where series resistance has increased beyond an acceptable value. In effect, the permissible surface area of the solar cell has been limited.

This is not true if more than one external electrical contact can be made to the cell. In this case only one lateral dimension of the solar cell surface will be limited. For example, a solar cell fabricated on a rectangular ribbon substrate may be infinitely long if electrical contacts are made along its edges at small intervals, but there must be a practical limit on the width of the cell if acceptably low internal voltage loss (i.e., series resistance) is to be maintained. The same principle holds for circular solar cells. Constrained to a fixed area of front surface metal, a circular cell may require multiple contact points around the perimeter to maintain a low series resistance, and a larger diameter cell would require more contacts than a smaller diameter cell. In the limit, as cell diameter becomes larger and still larger, overall cell efficiency must suffer.

The net effect of using multiple electrical contacts at the perimeter of a solar cell is to shift some of the burden of summing the photo-current generated by the active surface of the cell away from the metal pattern on the cell surface to external electrical busses. When such a solar cell is assembled in an array of cells, an additional benefit is the increased reliability achieved through the partial redundancy of the multiple cell contacts.

Studies of the front surface metal pattern component of the design model and of the effects discussed in this section are continuing with the hope of providing some firmer guidelines to the limits (on solar cell size and shape, and on pattern design) which are introduced by considering some attractive metal systems.

3.1.3 Textured Front Surface

A textured front surface, consisting of a uniform distribution of minute pyramids as shown schematically in Figure 1, causes light reflected from the first impingement on the solar cell surface to strike the solar cell at least a second time (assuming initial normal incidence). This second impingement increases the amount of light absorbed in the solar cell, improving cell efficiency by reducing the total amount of light reflected from the cell. Incoming, reflected, and refracted ray traces of light normally incident to the overall solar cell, Figure 2 show the multiple reflection features of this surface topography.

Another major effect is that, since light is refracted into the silicon at an angle to the normal of the overall solar cell plane, more light is absorbed within a given thickness of silicon than would occur with normally incident sunlight on a smooth-surfaced solar cell. This effect can be separated into two regions, a microscopic region involving the volumes immediately adjacent to the p-n junction, and a more macroscopic effect involving the bulk of the silicon below the junction region.

In the microscopic region near the junction, it is first assumed that the surface relief of the pyramidal structures is large (averaging greater than 1μ) compared to the p-n junction depth (less than 0.5μ). Light normally incident to a textured surface solar cell strikes the surface facets at an angle near 55^{o}. Figure 3 diagrammatically demonstrates the refracted paths of both a normal incidence light beam on a smooth surface cell and an analogous beam on a textured surface facet. The optical path length of the refracted beam within the region of the junction is greater than the normal path length by a factor of $\frac{1}{\cos\phi}$ in the case of the textured surface. This increased path length has an effect equivalent to increasing the absorption coefficient of light in the silicon by the same factor (over

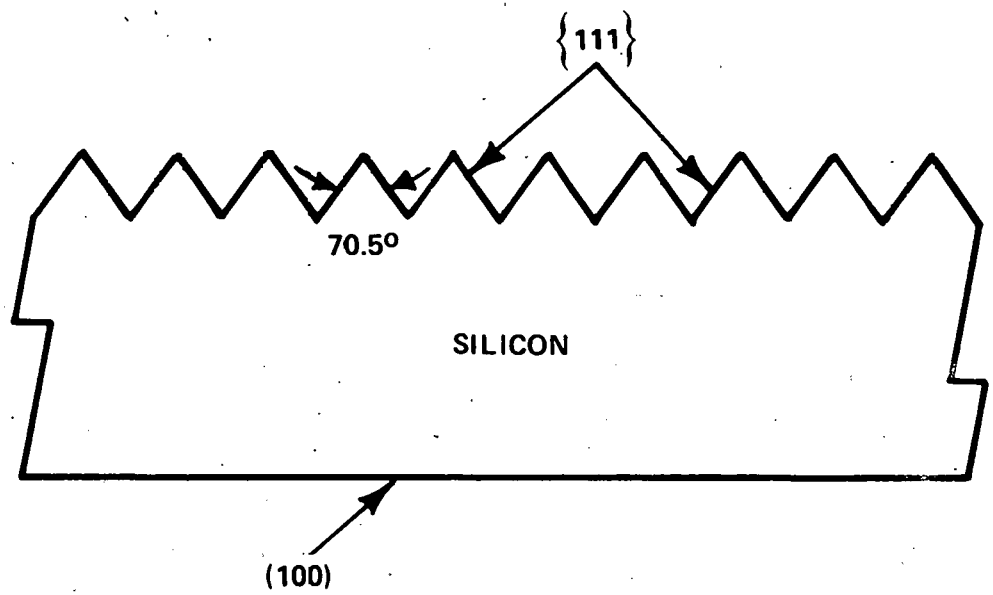


Figure 1 CROSS-SECTIONAL DIAGRAM OF SILICON (100) WAFER SHOWING GEOMETRY OF TEXTURED SURFACE HAVING {111} FACETED PYRAMIDS

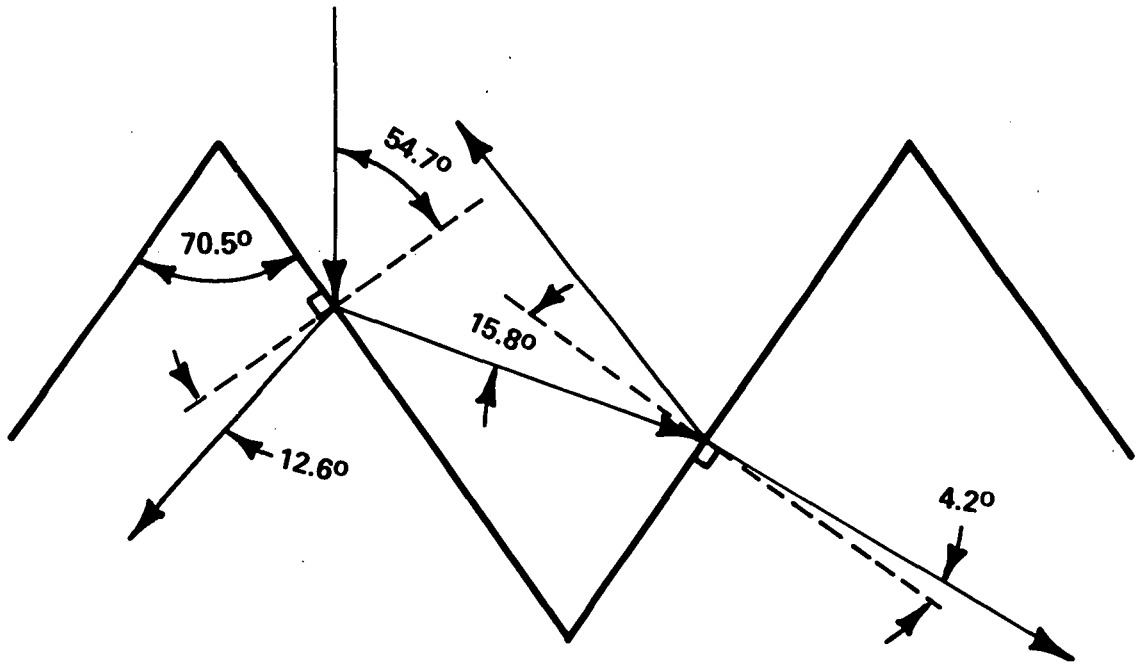


Figure 2 DIAGRAM OF REFLECTED AND REFRACTED RAY TRACES AND ANGULAR RELATIONS FOR LIGHT NORMALLY INCIDENT TO THE SUBSTRATE (100) PLANE OF A TEXTURED SURFACE SOLAR CELL.

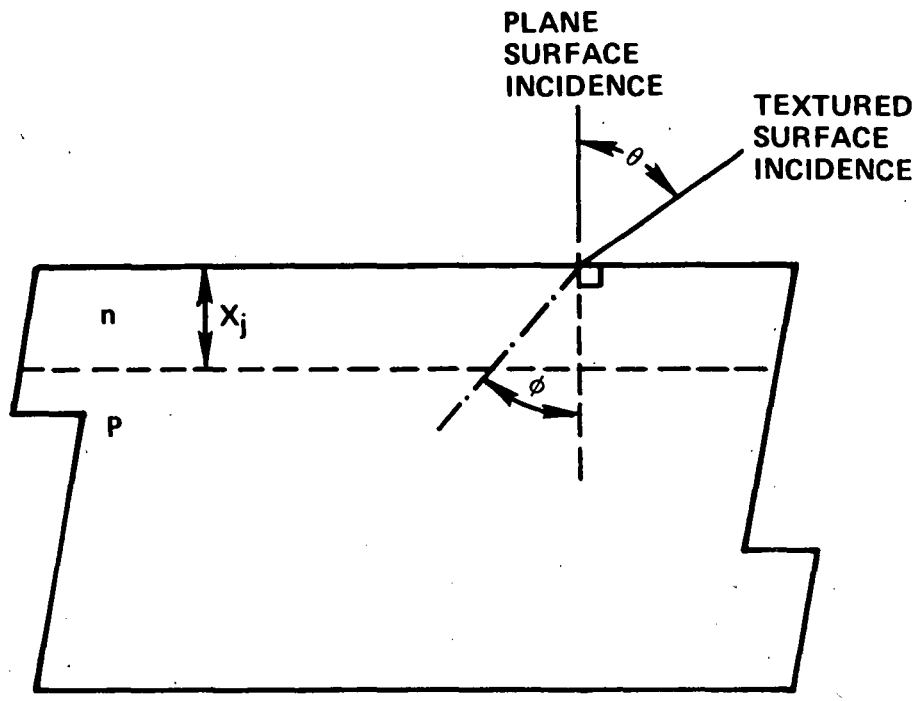


Figure 3 REPRESENTATION OF INCREASED ABSORPTION PATH LENGTH OF TEXTURED SURFACE LIGHT RAY TRACE COMPARED TO TRACE NORMAL TO A PLANE SURFACE.

the smooth cell normal incident beam). Thus, within the region near the junction, more light is absorbed, creating more carriers, and increasing cell efficiency. Assuming that the index of refraction is 3.75, the angle ϕ is approximately 12.6^{o} and $\frac{1}{\cos\phi}$ is approximately 1.025. This is effective throughout the solar spectrum, but is most significant in absorption of the shorter wavelength portion of the solar spectrum, where absorption coefficients are highest.

A larger effect is seen in the macroscopic region within the bulk of the cell below the microscopic junction region. Light incident normal to the plane of the overall cell is refracted by the textured surface through an angle 12.6^{o} from the normal to the facet. (Figure 3.2). This is equivalent to an angle of 42.2^{o} from the normal of the overall cell, i.e., $\phi=42.2^{o}$, Figure 3, so that the path length through the bulk is increased by a factor of $\frac{1}{\cos 42.2^{o}}$, equal to 1.35. This is the equivalent of increasing the path length through the bulk by 35%, making each three units of solar cell thickness look like four units of thickness. Restated, the number of carriers created in an optical path length of four thickness units is generated within three thickness units of the front surface and the p-n junction. This makes the cell far more responsive to the longer wavelengths of incident sunlight, which have smaller absorption coefficients in silicon than the short wavelengths.

A further effect of the angle of travel of the refracted beam through the bulk is at the back surface of the cell. If the back surface of the cell is a plane, all light refracted through the front textured surface can be shown to strike the back surface of the cell at an angle exceeding a critical angle, resulting in total reflection from the back surface toward the front surface. (The condition for total internal reflection

$$n_{Si} \sin \varepsilon = n_{ext}$$

yields angles of about 15.5° for air and near 24° for most plastics and SiO_2.) Total internal reflection occurs when the angle ϕ exceeds the angle ε, Figure 4. The internally reflected beam will be further absorbed on its second pass through the material, again creating more carriers and increasing cell efficiency. Alternately, a thinner cell (conserving silicon) could be made to display the same efficiency as a thicker standard cell. The magnitude of the effect of the second pass absorption will be, of course, a function of the total cell thickness.

More subtle advantages also occur with a textured surface. The textured surface, formed by etching, leaves a surface which is relatively free of work damage. A plane surface, on the other hand, is often achieved by polishing, leaving a finite degree of work damage in the crystal surface layer. Such damage is known to adversely affect both carrier lifetimes and surface recombination velocity; it can propagate during high temperature processing, aggravating the damage. This additional advantage of textured surface etching will not apply to solar cells fabricated from silicon ribbon (if it is directly grown to have smooth, damage-free surfaces), or from chem-etched wafers.

For any unit area in the plane of the substrate, the (100) plane, the corresponding area of the textured surface described above will be a factor of $\sqrt{3}$ times larger. When ohmic metal contacts are applied, this increased surface area will serve to reduce the magnitude of the contact resistance. Furthermore, the textured surface itself can promote better metal adhesion to the silicon surface.

Finally, the mechanism causing reduced reflection of incident light discussed at the outset of this section will also lessen the requirements

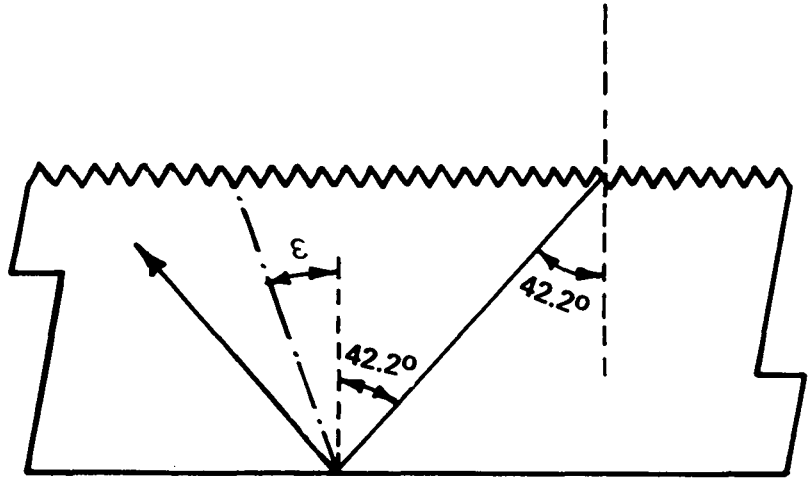


Figure 4 PATH OF BEAM REFRACTED FROM TEXTURED SURFACE ILLUSTRATING TOTAL INTERNAL REFLECTION FROM BACK SURFACE IF THE BREWSTER ANGLE $\varepsilon < 42.2^{\circ}$.

on antireflection coatings chosen for the solar cell surface. For example, the differences in total reflection obtained when using a perfectly matched antireflection coating and when using a somewhat less than perfect one will be much less pronounced, perhaps allowing coatings to be chosen for increased cost-effectiveness and convenience of processing.

The implications of incorporating textured surfaces into high efficiency silicon solar cells are continuing to be considered. Studies of the interaction of metal systems and textured surfaces, of the effects of antireflection coatings, of the angular dependence of incident radiation, and of the nature of junction formation in such a surface are anticipated.

3.2 Technology Assessment

This is an ongoing part of the program and pervades each of the studies outlined in the program plan. To formalize this study, a matrix of possible processing functions for manufacturing solar cells is being assembled and will be continually updated. Evaluation of each processing function will involve many factors, including the following:

- Performance
- Controllability
- Amenability to automation
- Cost
  - Labor
  - Material
  - Capital Equipment
- State of readiness
- Reliability considerations.

Items in this generalized matrix fall into four categories.

(1) Processes which are judged unlikely to be utilized in any recommended process sequence.

(2) Processes which appear potentially promising, but which require for their first-hand evaluation equipment not available within the time-frame of this program. Also included in this category are processes which appear to require major technological advancement to ensure usefulness. Information reported on this contract in these areas will rely heavily on the literature, information from equipment vendors, and inputs from other contract participants.

(3) Processes common to the semiconductor industry and utilized regularly for manufacturing devices and integrated circuits. Some selected processes from this category will be set up for study where it is deemed necessary to support or observe interactions with other processes. In most cases, however, processes in this category will be evaluated through observation and corroboration of existing expertise within Motorola. They are, or relate closely to, processes utilized in the production of solar cells.

(4) State-of-the-art semiconductor device and integrated circuit processes which have had little or no application to process sequences for manufacturing solar cells and which can be empirically evaluated on this contract.

The initial generalized process matrix follows; it includes a first approximation of categorization ratings and discussion of these ratings.

Processing Matrix

A. Starting Condition of Silicon Surface

The starting condition of the silicon surface plays a critical role in subsequent processing steps and in cell efficiency.

1. Sawed Surfaces (1)

   Material will not be utilized in the as-cut condition. Although this form of silicon is the cheapest available today, near-surface damage and contamination from the saw blade and coolant can badly degrade the crystal properties upon subsequent processing. Heating of the sawed surface can result in polyganization or recrystallization, converting the area in which the p-n junction is to be formed into a polycrystalline region. Heating may also propagate surface damage and mobile impurities far into the bulk, resulting in a heavily dislocated, low lifetime material. All of these factors will degrade efficiency in a severe, uncontrolled manner.

   All three types of sawing - wheel (O.D. or I.D.), blade and wire - result in comparable depths of damage of the order of 25 μm, depending upon speed, size of cutting particles, etc. This is the thickness of material that must be removed to eliminate deterioration of silicon crystallographic perfection upon heating to a high temperature, ~1000°C. If sawing is done carefully, the surface has a "lapped" appearance with depth of damage comparable to that of a lapped surface.

2. Sawed and Etched Surfaces (3)

   This is the best candidate broadly available today. Etching is utilized to remove the sawing damange and contamination. Etching

wafers can leave surfaces that contain only gradual undulations of a magnitude so small that no pattern having linewidths of interest to solar cell production should experience any masking difficulties because of surface non-planarity. With sawing and etching, a nominally 1 Ω-cm, 76 mm diameter wafer about 0.5 mm thick can be purchased today for less than $3.50. Much thinner, larger area sheets could conceivably meet longer range cost goals; such work is included as part of Task II of the LSSA Project.

3. Lapped Surfaces (1)

Lapping produces a matte appearing surface on a silicon wafer. It will be a flat surface, and, if done carefully, both sides of a wafer can be made plane and parallel by lapping them both. Lapping doesn't necessarily produce a better surface than careful sawing, but a sawed surface will not be as flat as a lapped surface. This process is slow, batch oriented, and labor intensive, and hence, is too expensive for ultimate solar cell use. Lapping is discussed in more detail along with polishing in the following section.

4. Polished Surfaces (1)

Polishing is a process like lapping in which successively finer grit media are used to end up with a mirror-flat scratch-free surface. This degree of smoothness is necessary in order to obtain, by photographic means, the very fine line geometries utilized on many semiconductor devices and integrated circuits. However, solar cell geometries are about an order of magnitude coarser, so polished surfaces are not required for solar cell processing even where patterning is done photographically. Furthermore, polished

surfaces typically contain more mechanical crystal damage than etched surfaces, making them potentially less satisfactory for solar cell use.

Polishing would be too costly for incorporation into a process sequence to make inexpensive solar cells. The typical sawed and etched wafer price of ~<$3.50 escalates to about $5.75 when the wafer is lapped and polished on one face.

5. Cleaved Surfaces (2)

Direct cleaving of silicon wafers or sheets from crystals would eliminate kerf losses and could produce smooth surfaces. To date, however, no process has been developed for cleaving wafers from a boule with anything approaching a satisfactory yield. If a major breakthrough in this area could be realized, it would be very cost competitive. No work appears to be currently underway in this area, however.

6. As-Grown Sheet Surfaces (2)

This is the responsibility of several contractors in LSSA Task II. Breakthroughs in technology are still required to make as-grown sheet practical in the large scale necessary. However, judging by the progress made to date and the potentialities of the process, it must be assumed that the probability of success is at least 50%. The various processes being studied all have the possibility of providing as-grown surfaces suitable for efficient solar cell processing. Also, since the as-grown sheet processes have the inherent possibility of providing silicon with little or no waste, they must be considered as prime contenders for the ultimate source of silicon solar cell substrates.

7. Texture Etched Surfaces (4)

There are several optical advantages to having a texture etched top surface on a solar cell. The costs of texture etching on present wafers should be only marginally above those on sawed and etched wafers, provided that texture etching can be done repeatably and uniformly. The textured surface is dramatically different in nature from the polished or etched surfaces normally used in the semiconductor industry. This process, and its integration into process sequences, will be investigated experimentally on this contract.

B. In-Process Surface Cleaning or Etching

Any solar cell manufacturing process will require cleaning steps at some stages. Further, most manufacturing sequences will require etching steps.

1. Wet Chemical Cleaning or Etching (3)

Processes in this category are widely utilized in the semiconductor industry. Those appropriate to process sequences investigated experimentally on this contract will be evaluated. Generalization of such process results, and impacts on other possibilities in this class, will then be made.

2. Plasma Cleaning or Etching (3)

This is a dry process incorporating an RF field to excite a plasma. The energetic plasma is then used to remove material from the surface, either by bombardment of inert energetic plasma ions (e.g., A) or by ions liberated from molecules injected into the plasma (e.g., F). While plasma processing technology and equipment have been available for several years, only limited acceptance has

been granted by the semiconductor industry. Costs, control, and uniformity of results do not seem presently adequate for completely automated processing. Future improvements may reverse the present status.

3. Vacuum Baking and Reverse Sputter Etching (3)

   Isolated vacuum steps can be highly expensive, both from the standpoint of equipment and labor. Little justification for an isolated vacuum cleaning (baking or sputter etching) step can be seen. However, when integrated into a total vacuum processing sequence, such as is being investigated under Task IV contract, vacuum cleaning and etching steps can hold advantages over non-vacuum processes. Vacuum system technology is now adequate for such evaluation.

4. Texture Etching (4)

   This is a specialized portion of wet chemical cleaning and etching. The resulting surface roughness requires particular consideration since it will be prone to contamination adherance. Unique cleaning and etching problems are expected.

5. Brushing (3)

   Brushing, usually in a liquid stream, has gained recent acceptance in the semiconductor industry as a viable cleaning technique. In addition to removal of fine particles, brushing is thought to remove adsorbed surface films which could cause later contamination.

6. Gas Stream Drying (3)

   Wet chemistry steps require a subsequent drying operation. Drying by a gas flow has been one of the standards in the industry.

7. Gravity (Centrifuge) Drying (3)

   For round wafers, centrifuge or "spin" drying has become another

of the semiconductor industry standards. In that industry, wafers are thicker and smaller than those likely to be utilized for future solar cells. This technique may require special adaptation for very large area, thin solar cell substrates such as long ribbons.

C. Lifetime Enhancement and Preservation

Solar cell processing may require minority carrier lifetime improvement of the starting material, and must incorporate special precautions (and possibly specific techniques) to preserve lifetime during processing.

1. Complexing and Removal (3)

   A heavy surface diffusion, typically with phosphorus, has been known to "getter" mobile lifetime killing impurities. Removal of the diffusion glass and the phosphorus diffused silicon region removes the gettered impurities from the wafer, permitting subsequent processing while maintaining high lifetime (provided the wafer is not re-contaminated). In some cases, a heavily phosphorus-diffused region may be left in place through all (or part) of the process sequence, keeping most of the lifetime degrading impurities tied up in a region remote from the active device regions.

2. Temperature Profile (3)

   During high temperature processing, silicon wafers can be subjected to large temperature gradients which can create crystal damage and thus degrade lifetime. Thermal gradients can be appreciably reduced by slowing the heating and cooling rates of silicon cells in the high temperature region where plastic deformation can occur.

3. Leaching (3)

   Introduction of reactive chemicals, such as HCl, during high temperature process cycles has been widely utilized to leach impurities

from the surface of a wafer. In some cases, e.g., Cl_2 introduction during oxide growth, some of the leaching species actually becomes incorporated into the device.

4. Precipitation (2)

Some rapid-diffusing lifetime-degrading impurities can be precipitated at defects, reducing their concentration throughout the crystal lattice and hence improving bulk lifetime. The precipitate regions, however, can cause appreciable disturbances in the field distribution of a neighboring P-N junction, creating excess current which is perhaps even more undesirable than reduced lifetime. The value of this technique will depend on the future material characteristics resulting from LSSA project Tasks I and II.

D. Junction Formation

The most complex and critical steps in solar cell processing involve junction formation. In order to stay within the design requirements of an efficient solar cell, the junction depth must be controlled to be consistently in the vicinity of 0.2 micrometers.

1. Epitaxy (1)

Long experience has been obtained in silicon epitaxy by chemical vapor deposition at temperatures in exess of 1000°C. Presently, even though chemical vapor deposition epitaxy is performed in highly automated facilities, accurate deposition control in the 0.25 micrometer range is deemed impractical. This follows both from deposition dynamics and diffusion between substrate and epitaxial layer at the elevated deposition temperature. Today, a large run-rate 76mm epitaxial wafer, having far less stringent requirements than applicable for solar cells, costs nearly $20.00. Such costs

preclude current epitaxy processes as viable contenders for junction formation.

Epitaxy at lower temperatures in vacuum utilizing a thermal silicon source has been employed in an attempt to establish control over thinner layers. This technique has been reported to work, but the expense is expected to be far greater than that for chemical vapor deposited epitaxial layers.

Liquid phase epitaxy is commonly used in P-N junction formation for III - V compound semiconductors. While this process probably could be developed for use in growing thin silicon layers, its expense would be prohibitive.

2. Diffusion

   a. CVD Source (3)

   b. Spin-on Source (3)

   c. Vapor Transport Source (3)

   d. Vacuum Deposition of Source (3)

   e. Plasma Deposition of Source (2)

These diffusion-from-a-source techniques can all be viewed as similar, having source deposition followed by (or simultaneous with) a high temperature anneal. All diffusion processes have the feature of rather isotropic diffusion of dopant into exposed surfaces, with first order junction depth control being accomplished by time and temperature. Control of surface concentration is commonly obtained by utilizing solid solubility of an impurity in silicon to establish a controlled impurity source in the silicon, and then, with the external source removed, diffusing further from the "constant

quantity" source in the silicon surface region. Several of these processes will be studied experimentally during this contract.

3. Ion Implantation (4)

Ion implantation of the dopant, unlike diffusion, is not isotropic, but is unidirectional, with depth dependent upon implantation energy. Ion implantation can be performed with extremely pure, mass analyzed dopants, avoiding any undesired contamination. Surface concentration can be controlled by ion dose. Machine technology has progressed to the point of producing sufficiently high dopant ion beam currents to be a serious contender for solar cell processing. Still greater beam currents appear feasible; this could help meet the longer range LSSA Project cost goals. Ion implantation technology will be empirically evaluated during this contract. Ion implantation as a diffusion source is another potentially advantageous process sequence.

4. Alloy (1)

This original technique for P-N junction formation was largely discarded by the industry due to lack of control and its intractability for anything but simple patterning. For solar cell use, the alloying material would have to be removed, exposing the (liquid phase epitaxy) regrown region below. Since the surface region is grown from solution, its impurity profile may not be controlled as desired to produce a drift aiding field. There appears to be no new development on the horizon to create renewed interest in alloying for solar cell P-N junction formation.

E. Metallization (Contact, Conductor)

Solar panel reliability will be determined primarily by metallization (and interconnection) failures. Active area is sacrificed to the metal current collection pattern in order to reduce series resistance and thereby improve cell efficiency; the optimal compromise in metal coverage vs cell efficiency is determined by innovative cell design.

1. Vacuum (Total Surface or Selectively Masked) (3)

   a. Evaporation (Resistance, E-Beam)

   b. Sputtering

   Vacuum deposition is the predominant metallization method utilized in the semiconductor industry. A metal (or layers of metals) for most semiconductor devices and integrated circuits is deposited by evaporation or sputtering onto the entire wafer surface and subsequently patterned into small geometries in a photolithography (photoresist) step. Solar cell metallization, on the other hand, employs a large geometry pattern with coarse lines (by comparison). Such patterns can usually be made amenable to evaporation through a mask, thus eliminating the photoresist step. Both technologies are used for solar cell metallization. Vacuum deposition of solar cell metallization tends to be an expensive isolated vacuum step, however, and should receive lowest priority on further contractual developmental scale-up efforts for solar cells. Development of high throughput (including continuous) machines for evaporation and sputtering by the vacuum equipment industry will determine the competitive practicality of vacuum metallization processes.

   Practically any metal, or sequence of metals, can be deposited by modern vacuum equipment.

2. Plating from Solution (3)

   a. Electroless

   b. Electrolytic

   c. Displacement

   Plating, particularly electroless nickel, has been utilized in numerous semiconductor metallization applications. Such processing, however, has shown variable results, and it has been largely supplanted by other metallization techniques, particularly for shallow junction devices. Variations are prevalent in plating uniformity and adherance. If a plated contact system for solar cells can be developed to display a high degree of control, and superior reliability, the cost advantages would be very large. Such a program will be pursued under this contract.

3. Chemical Vapor Deposition (1)

   Chemical vapor deposition of metal contacts requires the decomposition of a metal-bearing gaseous compound. Primary candidates are all metal-organic compounds, which are generally highly expensive. It is doubtful that cost savings over established vacuum technology can be realized. Metallization by means of chemical vapor deposition will be considered only via an evolution of potentially useful new systems and raw material costs.

4. Paint-on (Silk Screen) (2)

   A metallization capable of being painted directly onto the solar cell surface could be the long term cheapest metallization technique. Several commercial candidates used for printed circuit boards and hybrid integrated circuits exist, but none has been applied to silicon devices or solar cells. Contamination of the silicon is

a primary concern in these cases, particularly since the starting materials contain components that must be driven off in a heating process after deposition. Also, contact resistance to the silicon, and depth of penetration into the silicon during the sintering step, are unknowns. Further developments and studies are required in this area.

5. Lamination (2)

   The attachment of pre-shaped metallization patterns by lamination is also potentially attractive. Again, further developments are necessary before it can be considered viable. Potential problems are similar to those facing paint-on metallization.

6. Solder Coating (3)

   In many cases, solar cell metallization systems will be composed of a base metal system for electrical and mechanical contact to the silicon surface, and a solder coating which will be thick enough to act as the primary current-carrying metal. Sophistication of processing already exists in the solder coating areas, and little developmental work is required provided that the surface of the underlying metallization is amenable to controllable solder coating.

F. Antireflection (AR) Coating

A necessity for achieving the maximum efficiency from a solar cell is a high quality antireflection coating system. In some cases, this antireflection coating can be used for p-n junction passivation.

1. Vacuum Deposition (3)

   The same basic comments made for metal vacuum deposition apply here, except that it is seldom required to pattern the AR film

since it is generally applied after metallization (a mask is used to prevent AR film deposition on the bonding pad areas). Film thickness control is critical. While suitable technology is now available, other methods may be cost preferable.

2. Chemical Vapor Deposition (CVD) (4)

   Little attention appears to have been given by the solar cell industry to chemical vapor deposition of AR layers. Several suitable candidates exist, both insulating and conductive, which may offer advantages over traditional vacuum deposited films. This area will be explored experimentally during the contract.

3. Growth (3)

   A less effective, but very cheap, AR coating is SiO_2 which may be grown directly on silicon. This coating also has excellent p-n junction passivation qualities. Performance and cost effectiveness trade-offs will be evaluated under this contract.

4. Plasma Deposition (2)

   Deposition of antireflection dielectric coatings can be performed by plasma-aided CVD reactions at much lower temperatures than are possible by thermally activated CVD. This area needs technological advancement prior to serious consideration for the LSSA Project.

5. Spin-on Deposition (3)

   Antireflection coating compounds can be applied in the same manner as photoresist, followed by a bake cycle to either complete chemical reactions and/or to drive off solvents. This technology merits serious consideration at this time.

G. Annealing

All solar cell manufacturing process sequences require some high temperature annealing.

1. Resistance Furnace Heating (3)

   This is the almost universal semiconductor industry tool. The major problem in operation is energy consumption. In a continuous, automated environment, however, the energy dissipation per unit area of silicon should be capable of appreciable reduction from current practices. Uniformity and control exist now, even for large area sheets, and the technology is proven.

2. Direct Radiant Heating (1)

   This technique has had only limited application in semiconductor technology, and has several inherent problems. The life of high intensity radiant sources is short, and output is somewhat variable during that lifetime. Uniformity of heating requires reflective surfaces which can also degrade with use. Direct radiant heating of silicon to relatively low temperatures is inefficient since absorption over much of the IR spectrum is low. Even when used for high temperature (where radiant energy absorption is good) heating of silicon, direct radiant heating of large areas to a specific temperature is hard to control. Because of these limitations, radiant heating will be dropped from consideration.

3. Laser and Electron-Beam Heating (2)

   These emerging technologies show promise of excellent control and good efficiency. Application to semiconductor technology has been, however, limited, and requires further study before conclusions can be drawn. E-beam heating is being explored by another contractor under LSSA Task IV.

4. RF Heating (1)

RF heating is broadly used in silicon epitaxy, since high temperatures can be achieved in a "cold-wall" (and thus noncontaminating) system. Heating of the silicon is indirect, however, in that a conducting susceptor is first heated by the RF field; this susceptor, in turn, conductively heats the silicon. This process is energy inefficient. A cold-wall system is not considered necessary for solar cell processing, so RF heating will be eliminated from further study.

H. Patterning

Metallization, antireflection coatings, and dielectric layers for diffusion masks may require patterning in any given solar cell fabrication process.

1. Photolithography (photoresist) (3)

   a. Contact

   b. Out-of-contact

   c. Projection

   This technology is mature and suitable for future use. Mask alignment to the silicon substrate should be primarily mechanical, as opposed to optical, and re-alignments should be avoided if possible because they tend to be expensive. For the large production volumes anticipated for solar cells, projection printing is a necessity to eliminate excessive mask costs. Exposure will continue to be by ultraviolet or visible light unless some technological breakthrough occurs in either laser, E-beam, or X-ray exposure.

2. Shadow (Mechanical) Masking (3)

   This technique will continue to be useful in metal depositions.

Similarly, masking during vacuum dielectric depositions can be achieved. Mechanical masking during ion implantation can be accomplished by means of a suitably designed wafer support holder. Shadow masking technology will be explored under this contract, but no fundamental innovation is forseen as necessary in order to improve performance.

I. Interconnection

Interconnections of solar cells into modules pose some stringent requirements for performance and reliability. The interconnection scheme must not contribute a substantial series resistance, or potential performance of the cells can be seriously degraded. Experience derived from the semiconductor industry would suggest that metallurgical interactions are the most likely failure mechanisms. These can lead to reduced output, for example, as a result of increased series resistance, or interference with the optical path, or, perhaps more commonly, opened circuit connections.

1. Solder Reflow (3)

   a. Flux

   b. Neutral or Reducing Ambient

   c. Ultrasonic

   The most widely used and probably the most cost effective solar cell interconnection scheme utilizes solder reflow. Little technology development is required here.

2. Thermal Compression Lead Bonding (1)

   Though widely used in the semiconductor industry, thermal compression bonding is useful mainly on small diameter (less than about 100 μm) wires where compression deformation requires low pressures

compared to the fracture strength of silicon. Where millimeter sized bonds are required, this process is expected to be too damaging to the substrate to warrant further consideration.

3. Ultrasonic Lead Bonding (3)

   Ultrasonic bonding is a low pressure process which utilizes ultrasonic energy to smear metal surfaces together, thereby establishing intimate contact for a metallurgical bond. It is not area limited, as is thermal compression bonding, and is a viable contender for future use.

4. Welding (1)

   Welding will require localized temperatures which can damage the solar cell. It is unlikely as a future candidate for this reason alone.

5. Filled Adhesives (2)

   Metallic filled adhesives to bond wires to solar cell metallizations have had little or no application. Filled adhesives are used in the semiconductor industry for relatively large area bonding (e.g., die attach). These materials have poorer electrical conductivities than metals, and the better ones (e.g., gold filled) are expensive. In a solar panel, where thermally or mechanically induced tensile stresses on the interconnect wires may be expected, the reliability of filled adhesive bonds is questionable. However, this field is continually changing, and so it should be monitored.

6. Clamped Connectors (2)

   A direct clamping to the cell metallization is possible, especially if metal smearing at the contacts can be achieved without damage

to the cell itself and pressure can be maintained in the package. Without such smearing, moisture ingression to the contacts would increase resistance and reduced module reliability. This area requires further investigation and application prior to recommendations.

3.3 Study II - Process Adaptation

The following processes have been selected for initial laboratory evaluation for applicability to solar cell processing.

1. Texture etching - formation and effects on subsequent processing.
2. Photolithography - patterning of dielectrics.
3. Silicon nitride - CVD deposition of antireflection coatings.
4. Diffusion from CVD sources (as typical of diffusion) - lifetime preservation.
5. Ion implantation - lifetime preservation and large area junction characteristics.
6. Electroless nickel plated contacts - reproducibility and reliability.
7. Solder coating - ultrasonic vs. flux.
8. Gettering - heavy phosphorus diffusion and removal.

These processes are considered representative of the present state-of-the-art. Each process will be judged on its ability to fulfill design considerations, controllability, reliability, and cost effectiveness. Following initial evaluations and adaptation to desired solar cell parameters, these processes will be applied through process sequencing studies for actual solar cell fabrication. These studies will aid in the selection of the best automated process sequence.

4.0 Conclusions

A generalized processing matrix is presented, and initial categorization of processes has been completed. A number of process steps have been eliminated from further consideration based on presently established criteria. A second group has been flagged for future attention, pending technology development or advances. From the remaining process steps, representative and state-of-the-art processing steps have been chosen for evaluation in process sequence studies. Those steps removed from further consideration are as-sawed surfaces, lapped surfaces, polished surfaces, junction formation by either epitaxy or alloying, metallization by chemical vapor deposition, annealing by radiant or RF heating, and interconnection by thermal compression lead bonding or welding. Those processes placed "on hold" are cleaved surfaces or as-grown sheet surfaces; plasma cleaning, etching, or deposition; lifetime improvement by precipitation; metallization by silk-screening or lamination; laser and E-beam annealing; and interconnection by filled adhesives or clamped connectors.

5.0 Recommendations

Active interaction across Task interfaces is an important aspect of the LSSA program. Some considerations pertinent to Automated Solar Array Assembly interfaces with other LSSA Tasks are presented below.

Silicon Material Task

The basic requirement of this task is to reduce the cost of the silicon which serves as the starting material for sheet gorwth, while maintaining purity adequate for fabricating solar cells meeting the efficiency goal. For a square foot of 4 mil thick solar cells, the silicon weighs 22 gm. The cost of the silicon per square foot of solar panel is $0.22 if the $10/kg objective for solar cell grade silicon is met. The sheet growth techniques being investigated under Task 2 will have various efficiencies of silicon utilization; using 50% as a rather worst case number, then the cost of silicon per square foot of solar panel is $0.44.

A tradeoff which needs to be explored as part of the Task 1 - Task 4 interface activity is then as follows: If purer silicon results in higher lifetime and permits the fabrication of higher efficiency solar cells, what is the allowed raw silicon cost as a function of lifetime? For example, 15% efficient solar cells may support considerably more than $0.66 per square foot of silicon cost, assuming 1) that defects introduced into the silicon during sheet growth don't negate the increased lifetime obtainable with the purer silicon and 2) processing costs per unit area to make the 15% cells aren't appreciably higher than for 10% cells. Alternatively, if lifetime can be improved (by removing some of the impurities present in the raw silicon) during the sheet growth or solar cell fabrication, then these technologies can be permitted a commensurate increase in cost. Restated,

a study is needed to determine final lifetime vs. purification costs.

Large Area Silicon Sheet Task

The ability to automate the fabrication and packaging of solar cells will, in considerable measure, be determined by parameters of the ribbon starting material.

Of first concern are geometrical factors. Shape and size interact directly with solar cell design. Reproducability will affect automation techniques. Solar cell efficiency will place practical limits on surface dimensions of sheet silicon. Surface roughness will determine usable processes. Sheet thickness interacts equally as importantly on both cell efficiency and processing yield losses due to broken substrates. Either degradation or improvement of lifetime is possible during sheet growth; and again, both are possible during processing.

Orientation of the silicon sheet surface will influence the fabrication of solar cells, since some processes are orientation - dependent. If crystallographic orientation changes during sheet growth, solar cell processes that are relatively insensitive to orientation will have to be used.

If the sheet-growth process employs a substrate, design and process considerations will be drastically different than for the case of a self-supporting sheet. An insulating substrate will require one-sided solar cell design and processing, and special considerations for the possible inclusion of a back surface field. Effects of the substrate on solar cell processing, particularly the high temperature steps, will require special investigation. Interface studies are needed to define acceptable limits on both geometries and material properties.

Encapsulation Task

The encapsulation system must provide, for the materials utilized in the solar cells and their interconnections, an environment that will guarantee long term reliability; internal materials can be selected to enhance reliability for a given degree of package integrity. Cost of packaging must be small compared to that of the solar cells; higher efficiency solar cells permit the use of more expensive packaging. Allowable encapsulation costs vs solar cell costs vs efficiency need to be better defined.

6.0 Current Problems

No specific problems have occurred during this period of the program.

7.0 Work Plan Status

The work plan is on schedule

8.0 List of Action Items

No items requiring unusual or unplanned action have come to light during this period.

9.0 Program Expenditures

The following are the man hours and costs expended in the performance of the program through the month of February.

1. MANHOURS

Previous Expenditures	Current Month Expenditures	Cumulative Expenditures
0	893	893

2. FUNDS

Previous Expenditures	Current Month Expenditures	Cumulative Expenditures
0	22185	22185

Figures 5 and 6 depict graphically the hours and costs expended by month.

10.0 Milestones

Status of the program is shown on the Milestone Prediction and Accomplishment Chart, Figure 7.

11.0 New Technology

There have been no reportable "New Technology" items uncovered during this period.

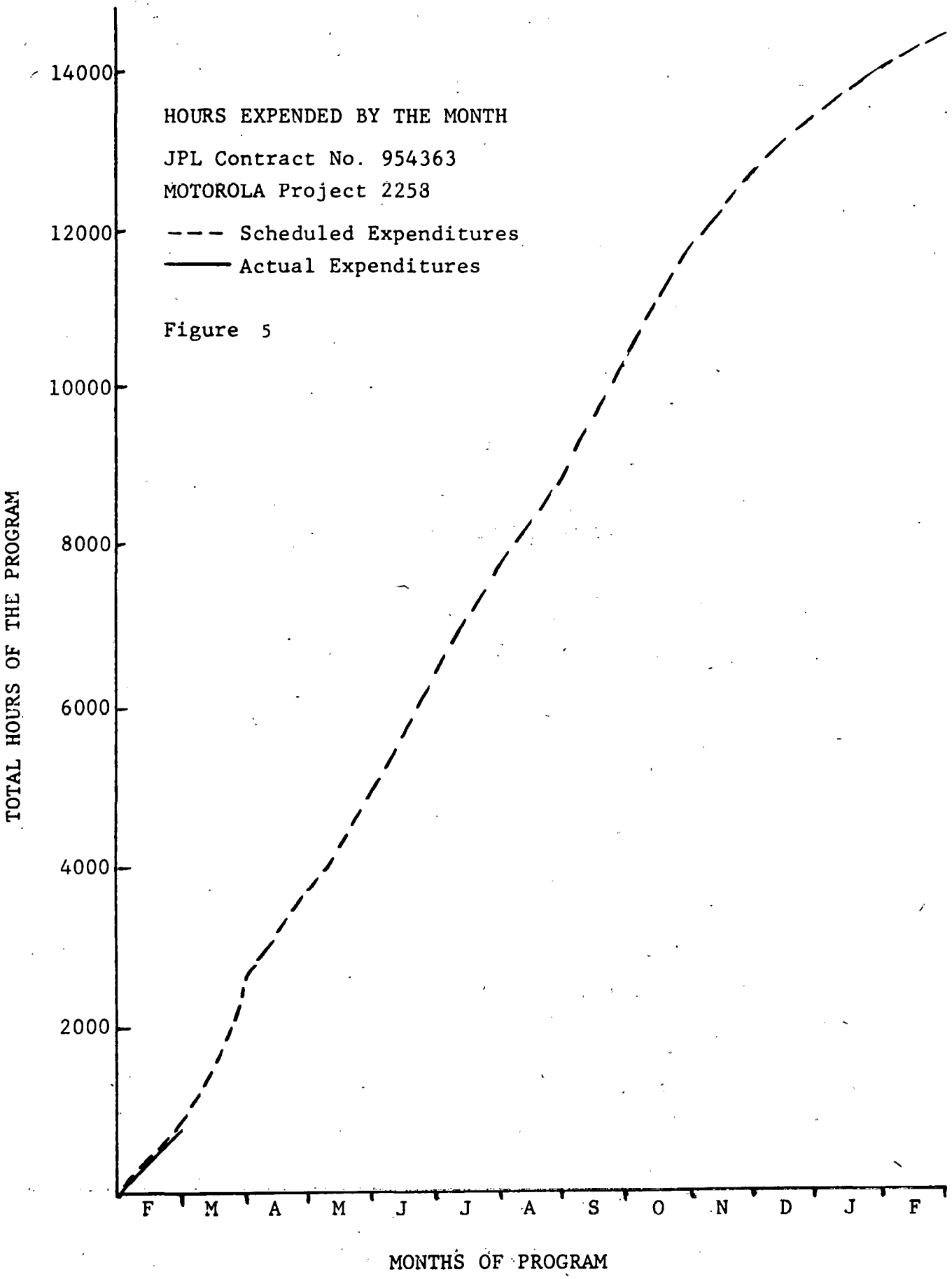
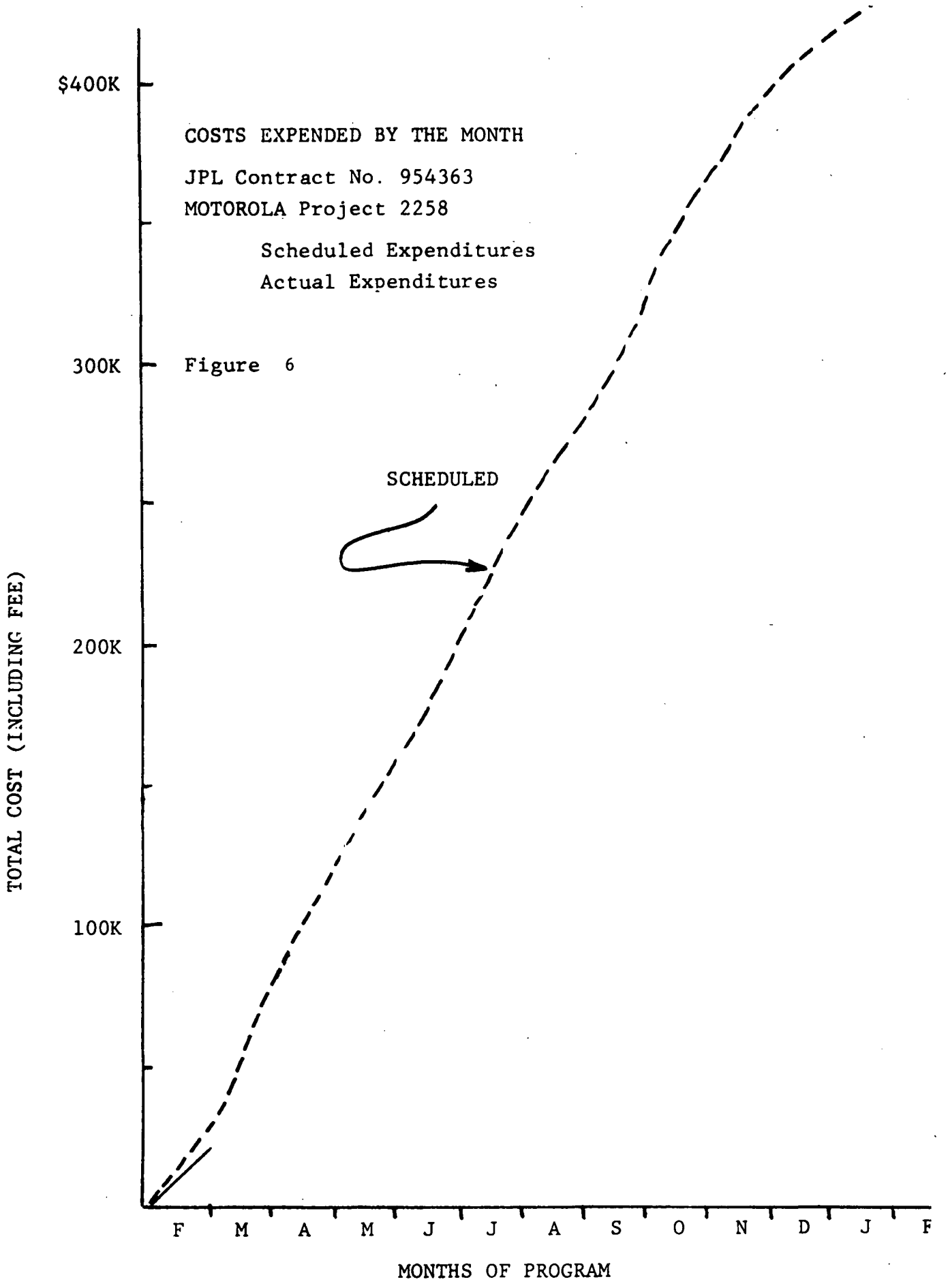

HOURS EXPENDED BY THE MONTH
JPL Contract No. 954363
MOTOROLA Project 2258
Scheduled Expenditures
Actual Expenditures
14000
12000
10000
8000
6000
4000
2000
TOTAL HOURS OF THE PROGRAM
F
M
A
M
J
J
A
S
O
N
D
J
F
MONTHS OF PROGRAM

Figure 5


COSTS EXPENDED BY THE MONTH
JPL Contract No. 954363
MOTOROLA Project 2258
Scheduled Expenditures
Actual Expenditures
Figure 6
SCHEDULED
$400K
300K
200K
100K
TOTAL COST (INCLUDING FEE)
F M A M J J A S O N D J F
MONTHS OF PROGRAM

MILESTONE PREDICTION AND ACCOMPLISHMENT CHART

MOTOROLA PROJECT No. 2258 JPL CONTRACT No. 954363

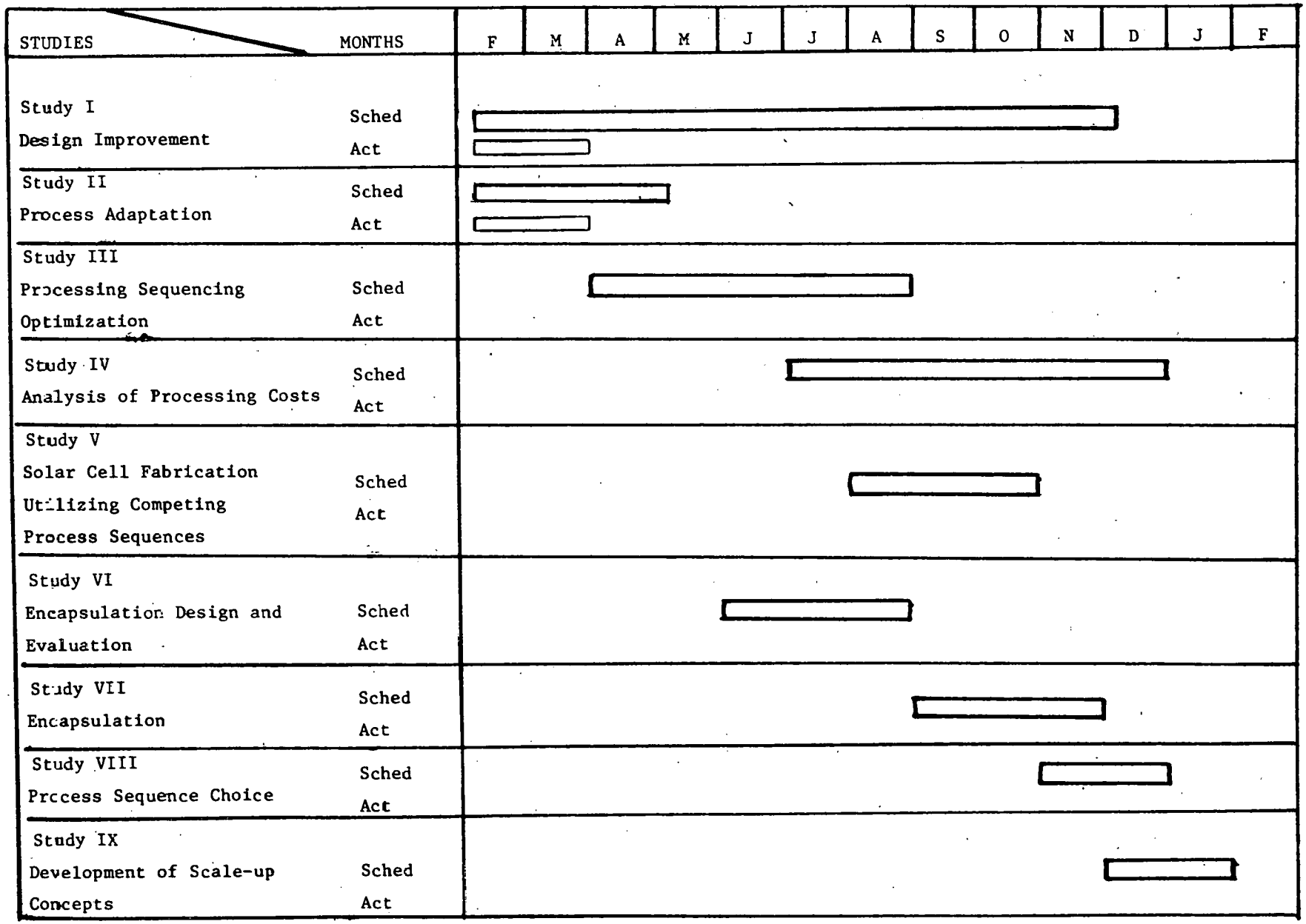
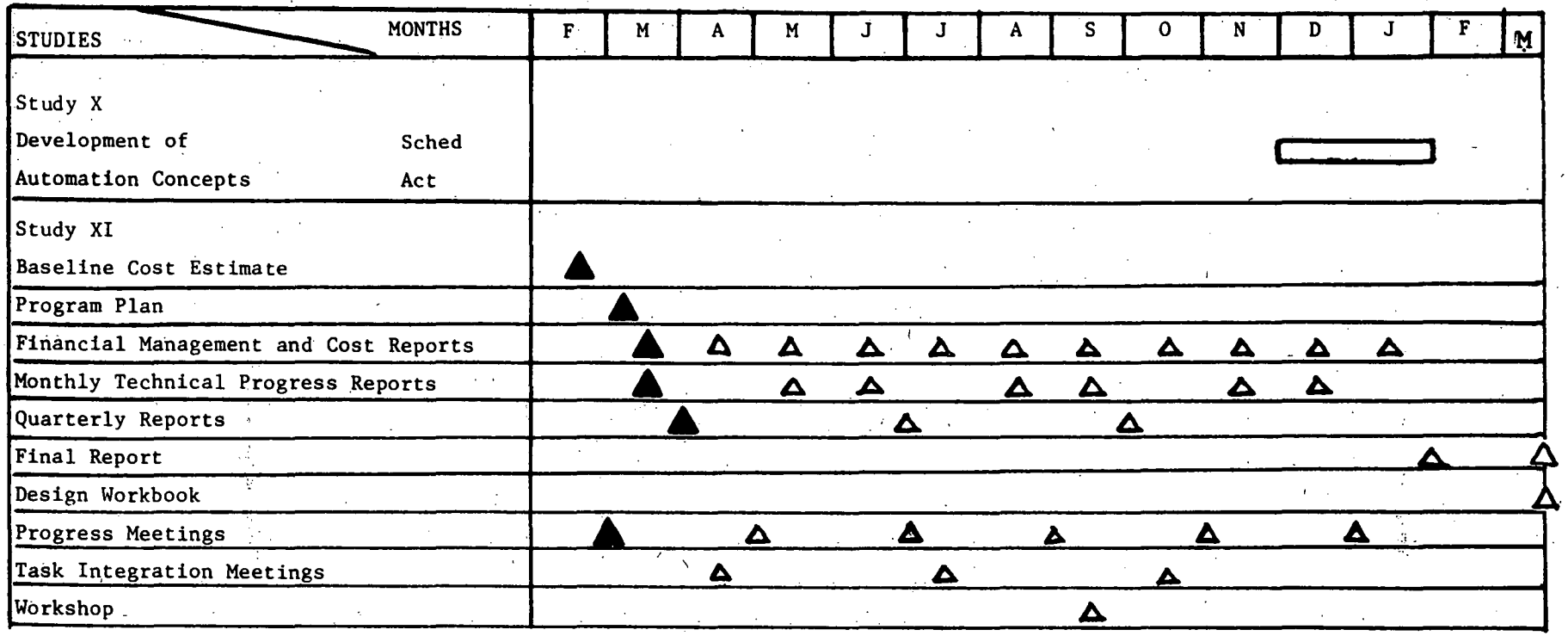


FIGURE 7

MILESTONE PREDICTION AND ACCOMPLISHMENT CHART.

MOTOROLA PROJECT No. 2258 JPL CONTRACT No. 954363



Legend: Scheduled △ Completed ▲ Date: March 31, 1976

FIGURE 7