DR-0193-7

DOE/JPL/955902-83/11
(DE84011716)

Energy SOLAR

PROCESS RESEARCH ON POLYCRYSTALLINE SILICON MATERIAL

Final Technical Report

By
J. S. Culik

Work Performed Under Contract No. NAS-7-100-955902

Solarex Corporation
Rockville, Maryland

Technical Information Center
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DOE/JPL/955902--83/11

DE84 011716

DRL No. 156
DRD Line Item No. 5

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(PROPSM)

FINAL TECHNICAL REPORT

CONTRACT NO. 955902

The JPL Flat-Plate Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE.

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ABSTRACT

The performance-limiting mechanisms in large-grain (greater than 1 to 2 mm in diameter) polycrystalline silicon solar cells were investigated by fabricating a matrix of $4cm^2$ solar cells of various thicknesses from 10cm x 10cm polycrystalline silicon wafers of several bulk resistivities. The analysis of the illuminated I-V characteristics of the cells of this thickness-resistivity matrix strongly suggest that bulk recombination is the dominant factor limiting the short-circuit current in large-grain polycrystalline silicon, the same mechanism that limits the short-circuit current in single-crystal silicon. The average open-circuit voltage of the polycrystalline solar cells is 30 to 70 mV lower than that of co-processed single-crystal cells; the fill-factor is comparable. Both open-circuit voltage and fill-factor of the polycrystalline cells have substantial scatter that is not related to either thickness or resistivity. This implies that these characteristics are sensitive to an additional mechanism that is probably spatial in nature.

Further investigation of the performance-limiting mechanisms consisted of fabricating a set of "mini-cell" wafers from a selection of 10cm x 10cm polycrystalline silicon wafers. A mini-cell wafer contains an array of small (approximately $0.2cm^2$ in area) photodiodes that are isolated from one another by a "mesa" structure. Measurement of the illuminated I-V

characteristics of the individual mini-cells showed that the average short-circuit current on different wafers was 3 to 14 percent lower than that of single-crystal Czochralski silicon. The scatter was typically less than 3 percent. The average open-circuit voltage was 20 to 60 mV less than that of single-crystal silicon. The scatter in the open-circuit voltage of most of the polycrystalline silicon wafers was 15 to 20 mV, although two wafers had significantly greater scatter than this value. The fill-factor of both polycrystalline and single-crystal silicon cells was equivalent, although several polycrystalline silicon wafers had fill-factor averages that were somewhat lower and had a significantly larger degree of scatter. Lower average values of open-circuit voltage and a greater degree of open-circuit voltage and fill-factor scatter were correlated with the presence of inclusions, which was also correlated with significantly greater values of shunt conductance.

Measurement of the dark I-V characteristics of mini-cells from several wafers with few inclusions indicates that spatial variations in quasi-neutral recombination current are the dominant cause of open-circuit voltage variations. Only a small number of cells, usually isolated mini-cells, suffer from excess space-charge recombination current.

A damage-gettering heat-treatment was investigated and was found to improve the minority-carrier diffusion length in low lifetime polycrystalline silicon. However, extended high temperature heat-treatment did not further improve, but rather degraded, the lifetime. Hence, while the minority-carrier diffusion length in polycrystalline silicon may improve, it is also sensitive to high temperatures, in a manner that is probably identical to single-crystal Czochralski silicon.

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I. INTRODUCTION

Work on JPL Contract 955902 was initiated in November, 1980. The original contract was a technical readiness demonstration program entitled "Module Experimental Process System Development Unit (MEPSDU)". In February, 1982 the program was completely restructured to determine the mechanisms affecting the conversion efficiency of large-grain polycrystalline silicon solar cells and, once knowing these mechanisms, to develop solar cell fabrication processes that take full advantage of its potential as a photovoltaic material. The primary emphasis of this work was on cast polycrystalline silicon as supplied by Semix, Inc.

A Summary Technical Report of the work completed on the MEPSDU is included as Appendix I. The remainder this final report summarizes the research effort on the efficiency-limiting mechanisms in large-grain polycrystalline silicon solar cells. A major portion of this effort was devoted to evaluating two sets of test devices - one set of solar cells, $4cm^2$ in area, which comprised a matrix of polycrystalline silicon cells that varied in base thickness and resistivity, and a second set of devices, about $0.2cm^2$ in area, fabricated on $100cm^2$ polycrystalline wafers. This second set was used to evaluate this material, using illuminated and dark I-V characteristics, with a higher spatial resolution. Section II discusses these results

in determining the fundamental mechanisms limiting the performance of polycrystalline cells.

Section III reviews the effort to investigate a process - damage gettering - to improve the minority-carrier diffusion length in polycrystalline material.

Section IV highlights the conclusions resulting from these efforts, and Section V discusses some recommendations for further work.

There are two appendices. As previously noted, the first contains the Final Technical Summary of the MEPSDU, which was the original goal of this program. The second appendix contains the publications that were produced under this program.

II. MECHANISMS LIMITING THE PERFORMANCE OF POLYCRYSTALLINE SILICON SOLAR CELLS

A. Thickness-Resistivity Matrix

The investigation of the performance-limiting mechanisms in polycrystalline silicon was begun by fabricating a matrix of $4cm^2$ solar cells of various thicknesses from polycrystalline p-type silicon wafers of several resistivities as supplied by Semix, Inc.

The process sequence that was used to fabricate the $4cm^2$ solar cells is shown in Figure 1 [1]. The wafers were thinned to the nominal thickness - 50, 100, 150, 200, 250 and 300 microns - using a CP-type etch, then diffused with phosphorus to a nominal 70 ohms/ to form a thin n^+ layer and junction on both sides. The rear junction was compensated by an aluminum paste alloy to form a thick p^+ layer. Front and rear contacts were Ti/Pd/Ag; the front pattern was defined photolithographically. Finally, the wafers were sawn into 2cm x 2cm cells, and a Ta_2O_5 anti- reflection coating was applied. Single-crystal control wafers were included with each group of polycrystalline wafers to monitor process variations.

Due to the fragility of the 50 micron thick polycrystalline wafers, none survived the processing intact, and therefore no

Figure 1. Thickness-resistivity matrix test cell process sequence.

1.	THINNING ETCH:	CP-type, final thicknesses: 50, 100, 150, 200, 250, 300 microns.
2.	DIFFUSION:	Phosphine, tube diffusion; 70-80 ohms/□.
3.	BACK ALLOY:	Englehard A-3484 aluminum paste, tube alloy, 30 seconds at 850°C; HCl post-alloy etch.
4.	FRONT METALLIZATION:	Evaporated Ti/Pd contacts, photolithographically defined.
5.	REAR METALLIZATION:	Evaporated Ti/Pd contacts.
6.	ELECTROPLATE:	Silver, 10-15 microns.
7.	AR COATING:	Evaporated Ta_2O_5.

results are reported for 50 micron thick cells. Overall the yield increased with thickness, and some results for 100 micron thick wafers were obtained.

Table 1 shows the number of $4cm^2$ polycrystalline solar cells for each thickness and resistivity category by lot number. The resistivity of the polycrystalline silicon wafers fell into three ranges: "low resistivity", 0.4 to 0.6 ohm-cm; "medium resistivity", 1.0 to 1.9 ohm-cm; and "high resistivity", 4.2 to 6.5 ohm-cm.

The variation of short-circuit current with thickness and resistivity is shown in Table 2. The short-circuit current of the polycrystalline cells decreases as the resistivity decreases, just as it does with single-crystal (control) cells, as shown in Table 3. The dependence of the short-circuit current of the single-crystal cells on resistivity is attributed to the dependence of the minority-carrier diffusion length on the dopant concentration. This behavior, though not well understood, is at least well known for Czochralski single-crystal silicon [2,3,4]. The variation of the short-circuit current of the single-crystal cells with base thickness is also related to minority-carrier diffusion length. For very narrow base widths, the number of photogenerated carriers, and therefore the short-circuit current, will be small because long wavelength photons are not absorbed. The amount of light absorbed and the short-

Table 1. Sample size: number of $4cm^2$, AR-coated, polycrystalline silicon solar cells in each thickness-resistivity category, by lot.

		THICKNESS (microns)				RESISTIVITY
	LOT NO.	100	150	200	250	300	(ohm-cm)
LOW RESISTIVITY	6		20	26	20		0.4 - 0.6
MEDIUM RESISTIVITY	1		6	20	19		1.3 - 1.7
	2	7	5	12	13	19	1.0 - 1.9
	7	9	14	11	8		1.2 - 1.8
HIGH RESISTIVITY	3	5	9	19			5.5 - 6.5
	5		10	18	22	10	4.2 - 6.2

Table 2. Short-circuit current of $4cm^2$, AR-coated, polycrystalline solar cells in each thickness-resistivity category, by lot (measured at AMO, 135 mW/cm^2, 25°C).

		THICKNESS (microns)				
	LOT NO.	100	150	200	250	300
LOW RESISTIVITY	6		126(4)	127(4)	127(4)	
MEDIUM RESISTIVITY	1		132(6)	128(6)	126(15)	
	2	104(33)	132(2)	127(3)	135(7)	131(5)
	7	143(2)	146(2)	140(3)	142(2)	
HIGH RESISTIVITY	3	141(3)	141(2)	143(2)		
	5		145(4)	147(5)	146(6)	145(7)

Mean (standard deviation about mean), in mA.

Table 3. Short-circuit current of $4cm^2$, AR-coated, single-crystal (control) solar cells in each thickness-resistivity category (measured at AMO, 135 mW/cm^2, 25°C).

	THICKNESS (microns)						RESISTIVITY
	50	100	150	200	250	300	(ohm-cm)
LOW RESISTIVITY		145(2)	149(2)	148(2)			0.7
		145(1)	146(2)	147(3)	148(2)		0.7
	145(3)	154(2)	159(1)	155(2)	159(1)	159(2)	1.7
MEDIUM RESISTIVITY			155(2)	155(4)	155(1)		1.7
		153(3)	159(3)	162(3)	164(1)	163(1)	7-22
HIGH RESISTIVITY	146(3)	151(4)	151(2)	150(3)			13-18
			156(3)	164(5)	161(2)	159(3)	10-16

Mean (standard deviation about mean), in mA.

circuit current will increase with cell thickness until the base width is approximately equal to the minority-carrier diffusion length. When the base width is greater than the minority carrier diffusion length, even though additional carriers may be generated deeper in the bulk, they will not be collected. Therefore, at some base thickness approximately equal to the minority-carrier diffusion length, the short-circuit current will asymtotically approach a maximum value. This current saturation with thickness is clearly seen for the single-crystal (control) cells. As the resistivity increases, the cell thickness at which the short-circuit current saturates also increases. This same type of behavior, though less clearly seen, is nevertheless also present for the polycrystalline cells. However, the short-circuit current of all polycrystalline cells appears to have saturated for cell thicknesses greater than 100 microns. This fact, together with short-circuit currents for polycrystalline cells that are five to ten percent lower than those of single-crystal cells of similar resistivity, indicates that the minority-carrier diffusion length of the polycrystalline material is less than that of the single-crystal silicon wafers.

It does not appear that the reduced short-circuit currents are the result of recombination at the grain boundaries. If this were the case, then there should be even more scatter in the data since no attempt was made to control the grain size,

which varied from about 1 to 10 mm in diameter. With the exception of the cells from Lot 1 and the 100 micron thick cells of Lot 2, the scatter in the short-circuit current of the polycrystalline cells is equivalent to that of the single-crystal control cells, that is, three to four percent. This result is consistent with earlier work - both theoretical [5] and experimental [6] - which indicates that the light-generated current is not substantially affected by recombination at the grain boundaries when the grain diameter is several times larger than the minority-carrier diffusion length. For a diffusion length of 100 to 150 microns, as indicated by the behavior of the short-circuit current with thickness and resistivity, this dimension would be on the order of 1 to 2 mm. In most present examples of cast polycrystalline silicon (Semix, Wacker, HEM) the grain size is consistently equal to or greater than this dimension. Hence, the short-circuit current of these materials should be dominated by bulk properties, rather than grain boundary recombination. This also implies that forming polycrystalline silicon with grain diameters larger than several diffusion lengths, or even passivating the grain boundaries of smaller-grain (grain diameter equal to minority carrier diffusion length) polycrystalline silicon, will not result in any substantial increase in short-circuit current. Improvements in the short-circuit current of large-grain polycrystalline silicon, at most five to ten percent, will be mainly due to elimination of the sources of recombination in the grain bulk.

The results for the open-circuit voltage of the polycrystalline cells in the thickness-resistivity matrix are shown in Table 4. Although there is some indication that the open-circuit voltage increases as the resistivity decreases, it is very difficult to conclude that dopant concentration is the dominant factor because the scatter in the data ranges from less than one percent to more than fifty percent. Likewise, it is difficult to establish any clear dependence of open-circuit voltage on thickness.

For comparison, Table 5 gives the results of the open-circuit voltage of the single-crystal (control) cells. As expected, the open-circuit voltage increases as the resistivity decreases and, because of the back surface field, is not very sensitive to thickness. The average open-circuit voltage of the single-crystal cells is 30 to 70 mV greater than that of the polycrystalline cells in the same thickness-resistivity category. For most single-crystal control groups the scatter is within 10 mV of the mean, that is, less than two percent. In the worst case the scatter is about five percent of the mean. The scatter in the open-circuit voltage of the polycrystalline cells was significantly greater than that of the single-crystal (control) cells.

Most of the thickness-resistivity groups of polycrystalline cells which showed very large amounts of open-circuit voltage

Table 4. Open-circuit voltage of $4cm^2$, AR-coated, polycrystalline solar cells in each thickness-resistivity category, by lot (measured at AMO, 135 mW/cm^2, 25^oC).

		THICKNESS (microns)				
	LOT NO.	100	150	200	250	300
LOW RESISTIVITY	6		577(24)	583(8)	580(8)	
MEDIUM RESISTIVITY	1		559(5)	559(19)	559(14)	
	2	333(158)	539(36)	538(67)	555(16)	553(11)
	7	587(4)	586(3)	573(10)	582(4)	
HIGH RESISTIVITY	3	573(8)	570(4)	570(5)		
	5		570(13)	552(30)	566(16)	559(19)

Mean (standard deviation about mean), in mV.

Table 5. Open-circuit voltage of $4cm^2$, AR-coated, single-crystal (control) cells in each thickness-resistivity category, by process group (measured at AM0, 135 mW/cm^2, 25^oC).

	THICKNESS (microns)					RESISTIVITY
	100	150	200	250	300	(ohm-cm)
LOW RESISTIVITY	601(4)	607(4)	602(5)			0.7
	607(4)	612(3)	612(6)	609(2)		0.7
	601(8)	608(2)	606(3)	604(3)	606(1)	1.7
MEDIUM RESISTIVITY	606(2)	599(10)	600(9)	603(3)		1.7
	580(15)	590(5)	598(3)	596(4)	600(3)	10-20
HIGH RESISTIVITY	598(3)	599(2)	593(26)			13-18
		602(2)	607(3)	601(5)	590(15)	10-15

Mean (standard deviation about mean), in mV.

scatter also had a very high average shunt conductance, as shown by the shunt conductance data in Table 6. In these groups the low open-circuit voltage, and also the scatter, were most likely the direct result of excessive shunt conductance. However, one group, the 150 micron thick cells of Lot 2, had shunt conductances which could in no way account for the low average or the scatter in the open-circuit voltage. In addition, polycrystalline cells with moderate amounts of open-circuit voltage scatter ($\pm$5 to $\pm$20 mV) invariably had values of shunt conductance that were so low as to have no significant effect on the open-circuit voltage.

The lower average open-circuit voltages (20 to 50 mV lower than single-crystal control cells) and the scatter in the open-circuit voltages of the non-shunted polycrystalline cells appear to indicate that there is a voltage-controlling mechanism, not present in the single-crystal (control) cells, which is limiting the open-circuit voltage of polycrystalline cells.

A comparison of the fill-factor of the polycrystalline cells to that of the single-crystal (control) cells is shown in Table 7. As with the open-circuit voltage, most of the groups with large amounts of fill-factor scatter were also found to be shunted; the shunts were very likely the cause of the low fill-factors as well as the low open-circuit voltages. The average fill-factor of most of the groups of non-shunted

Table 6. Shunt conductance of $4cm^2$, AR-coated, polycrystalline solar cells in each thickness-resistivity category, by lot.

		THICKNESS (microns)				
	LOT NO.	100	150	200	250	300
LOW RESISTIVITY	6		19.70(41.5)	2.49(4.59)	3.31(3.74)	
MEDIUM RESISTIVITY	1		1.12(1.72)	7.59(4.58)	2.25(3.33)	
	2	110.(63.0)	2.47(2.11)	33.2(88.7)	26.5(51.6)	3.89(3.67)
	7	0.35(0.28)	0.56(0.58)	1.69(1.78)	0.99(1.00)	
HIGH RESISTIVITY	3	21.9(27.7)	5.58(5.16)	7.50(9.81)		
	5		4.31(6.63)	63.7(86.1)	0.56(1.23)	1.73(1.66)

Mean (standard deviation about mean), in mmho.

Table 7. Comparison of fill-factor (in %) of polycrystalline and single-crystal (control) solar cells in each thickness-resistivity category, by lot.

		THICKNESS (microns)				
	LOT NO.	100	150	200	250	300
LOW RESISTIVITY	6		68(11) 80(1)	73(3) 77(6)	71(5) 79(1)	
	1		76(2) 75(1)	75(2) 76(1)	75(4) 76(1)	
MEDIUM RESISTIVITY	2	32(8) 74(7)	70(10) 80(1)	70(14) 80(1)	68(13) 78(2)	74(3) 78(1)
	7	76(1) 76(1)	76(1) 77(2)	75(1) 78(2)	76(2) 79(1)	
	3	70(7) 75(5)	64(4) 78(1)	64(4)) 77(1)		
HIGH RESISTIVITY	5		75(2) 77(1)	64(15) 77(3)	75(1) 77(3)	75(1) 71(11)

Mean (standard deviation about mean), polycrystalline.

Mean (standard deviation about mean), single-crystal.

polycrystalline cells was not significantly different from that of the single-crystal (control) cells. However, the average fill-factor of four polycrystalline groups (Lot 6 - 250 microns; Lot 2 - 150 microns; and Lot 3 - 150 and 200 microns) was much lower than that of their single-crystal controls, and not because of shunting. This indicates that, while there does not appear to be any fundamental limit to fill-factor in large-grain polycrystalline silicon, there is a mechanism, not present in single crystal silicon, which can reduce the fill-factor in some polycrystalline samples.

B. Mini-Cell Wafer Evaluation

The scatter in both the open-circuit voltage and the fill-factor of the polycrystalline cells in the thickness-resistivity matrix indicates that there is an additional performance-limiting mechanism that is not associated with bulk properties - specifically, base thickness or resistivity. The degradation of both the open-circuit voltage and the fill-factor seems to have a spatial nature because each group contains individual cells with very good I-V characteristics (as shown by the sum of the mean plus one standard deviation) even though the average open-circuit voltage or fill-factor might be low. Since the location of any particular cell on a wafer was not controlled, this position-dependent scatter is implicit. Therefore, an experiment was designed to determine, first, the location of cells

with degraded I-V characteristics, and, second, the fundamental cause of the degradation. To achieve these objectives an array of up to 400 small (approximately 0.20cm^2 in size) photodiodes ("mini-cells") were fabricated on a selection of 10cm x 10cm polycrystalline silicon wafers.

1. Mini-Cell Wafer Fabrication

A set of mini-cell wafers was fabricated using a mesa etch isolation process sequence described below and shown in Figure 2. The wafers were chemically polished using a CP-type etch to a thickness of 250 microns, then diffused with phosphorus to a surface resistivity of 80 ohms/□. Individual test cells were isolated from one another by etching away several microns of silicon between the cells, resulting in a mesa diode structure. A p^+ layer on the back side of the wafer was formed by alloying aluminum into the wafer. Front contact pads were deposited by evaporating Ti/Pd over photoresist which had been photolithographically patterned. Undesired metal was removed using a lift-off technique. The back contact consisted of a full-coverage Ti/Pd layer. Silver was then electroplated onto the Ti/Pd metallization, and the contacts were sintered. No anti-reflection coating was applied.

Figure 2. Process sequence for mesa etch isolation test cells.

1.	THINNING ETCH:	250 $\pm$ 10 Microns Final Thickness
2.	DIFFUSION:	80 ohm/□
3.	MESA ETCH MASK:	Spin Photoresist Open Window Frame In Resist
4.	MESA ETCH:	CP-type, $\sim$ 2 Microns Removed
5.	STRIP RESIST	
6.	BACK ALLOY:	Aluminum Paste Bake Alloy HCl Etch
7.	FRONT METALLIZATION:	Spin Photoresist Open Windows For Contact Pads Evaporate Ti/Pd Liftoff
8.	REAR METALLIZATION:	Ti/Pd
9.	ELECTROPLATE:	Silver
10.	SINTER	

The set of mini-cell wafers consisted of five polycrystalline wafers supplied by Semix, a Wacker Silso polycrystalline wafer, and a single-crystal control wafer. Three of the Semix wafers were from the central portion of an ingot (No. 71-01E) near the bottom, in the middle, and near the top. The remaining two Semix wafers are from the middle of two additional bricks (Nos. C4-108 and C4-116B). The single-crystal control wafer was Czochralski-grown with a resistivity of 1.2 ohm-cm, which was approximately the same as that of the polycrystalline wafers.

2. Variation of Resistivity With Position

The dopant concentration in the base of an abrupt, one-sided p-n junction may be experimentally determined by measuring the junction capacitance (C) as a function of reverse bias (V), then determining the slope of a curve of $1/C^2$ versus V [7]. Assuming the base is p-type, the dopant concentration, N_A, is given by the relation

$$N_A = 2/q\varepsilon_{Si}\varepsilon_o\alpha$$

where q is the electronic charge, ε_{si} is the relative dielectric constant of silicon, ε_o is the permittivity of free space, and α is the slope of the $1/C^2$ versus V curve. Knowing the acceptor dopant concentration, the bulk resistivity is found by

use of a curve of resistivity as a function of boron concentration in silicon [8].

While the above technique is rather straightforward, it is also very tedious, particularly if one anticipates evaluating 400 cells per 10cm x 10cm wafer. In order to make it possible to determine the spatial variation of resistivity for the mini-cell wafers, a simpler technique for determining the resistivity from junction capacitance data was necessary. This technique involved the measurement of the junction capacitance with no bias, then using a calibration curve of junction capacitance (at V=0) as a function of resistivity to uniquely determine the resistivity. Such a calibration curve can be developed by using the above equation with the previously mentioned resistivity versus dopant concentration curve, and by assuming: (1) an abrupt p-n junction; (2) no deviation of the value of C at V=0 from the $1/C^2$ versus V curve; and (3) carrier mobilities in polycrystalline silicon which are equal to those in single-crystal silicon. The resultant calibration curve of junction capacitance (at V=0) versus resistivity is shown in Figure 3. Using this curve, a single capacitance measurement, rather than several, is adequate to determine the base resistivity with good accuracy.

The junction capacitance measurement was made using a General Radio 1672-A Automatic Capacitance Bridge whose oscil-

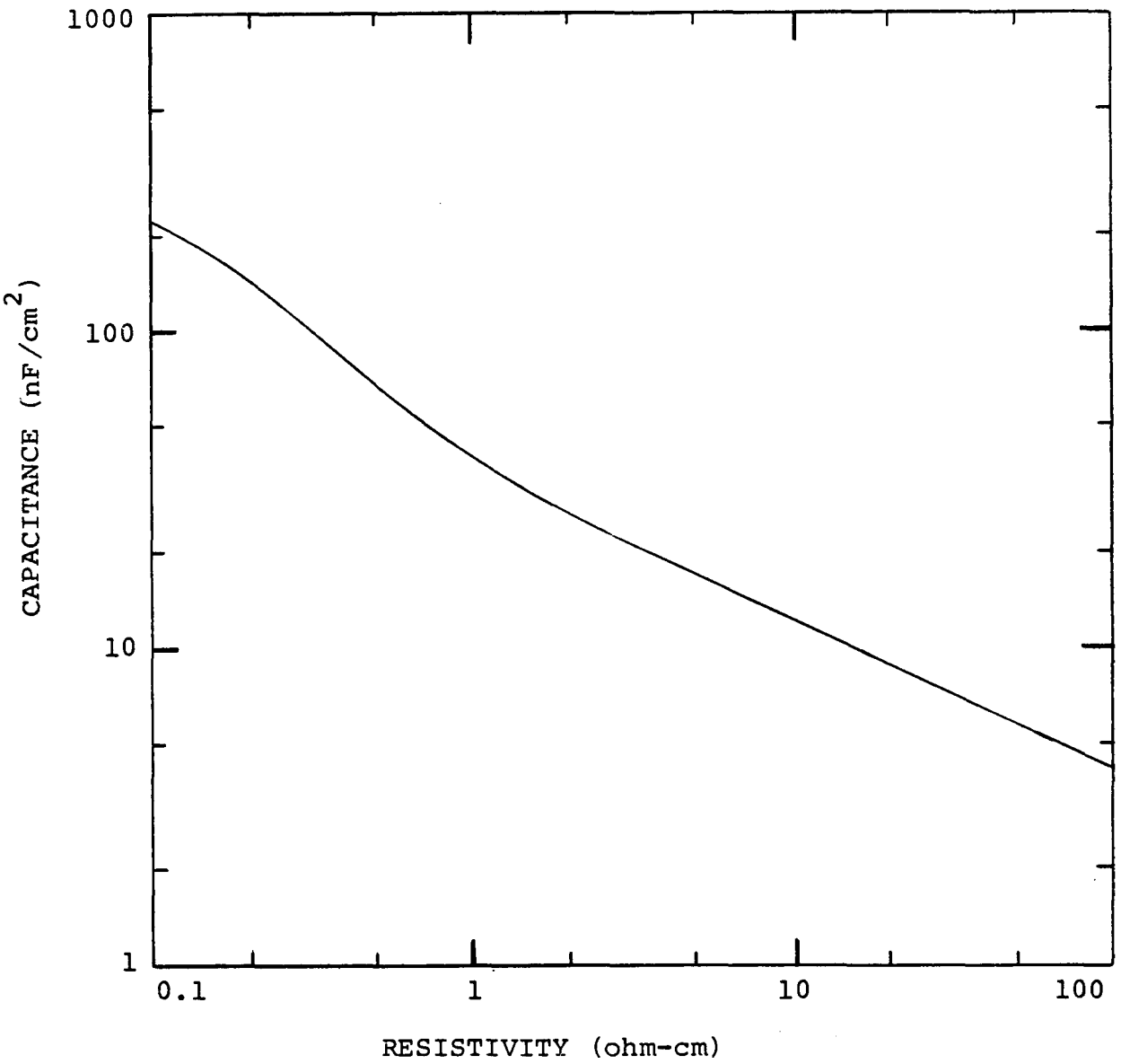

Figure 3. Junction capacitance as a function of resistivity; bias voltage = 0 V.

lator voltage is 100 mV with the cell in the dark and with no bias. The results for several of the mini-cell wafers showing the derived base resistivity as a function of position are given in Figures 4 to 6. Resistivity values that are missing in these figures indicate areas where the test cell shunt conductance is too high (greater than 1 mmho) to make a meaningful measurement of junction capacitance from which to determine resistivity. These shunted areas may possibly, though not necessarily, be due to some defect in the wafer; however, they may also be due to interaction between the silicon and the processing. The cause of higher values of shunt conductance in any particular cell can only be determined by additional measurements and observations.

Figures 4, 5, and 6 show the spatial variation of resistivity from wafers near the bottom, in the middle, and near the top of brick 71-01E, respectively, all of which were cut from the central portion of an ingot. The resistivity varies from 1.5 to 1.9 ohm-cm near the bottom, from 1.4 to 1.7 ohm-cm in the middle, and from 1.3 to 1.7 ohm-cm near the top. There is a slight trend toward lower resistivity from bottom to top. There is a much higher incidence of cells with shunt conductances greater than 1 mmho for cells from the bottom than for cells from the middle or from the top. This makes analyzing the spatial variation of resistivity difficult for the wafer near the bottom. However, the resistivity data of these and the remaining three polycrystalline wafers indicates that there is no particular pattern to the spatial variation of resistivity.

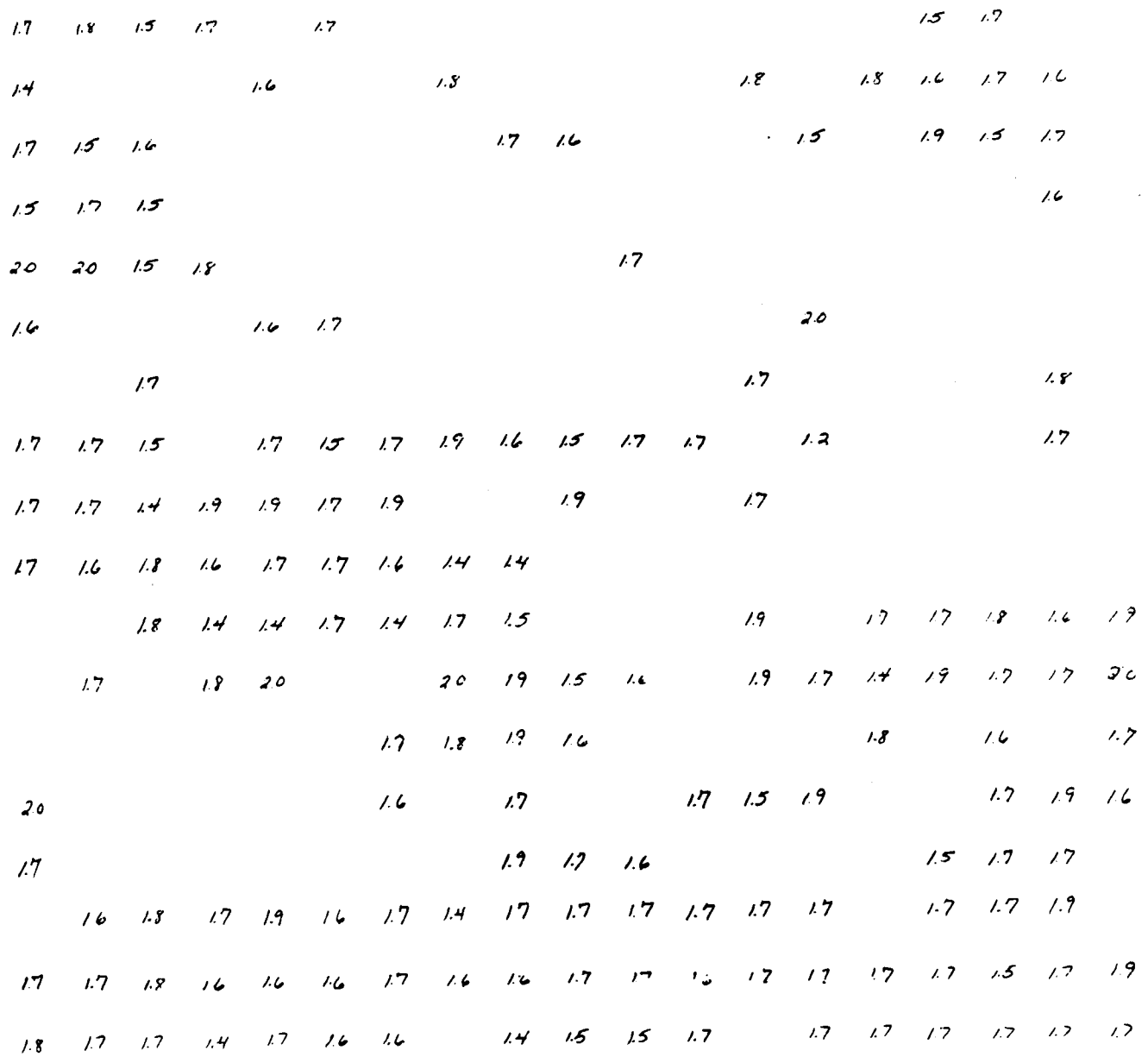

Figure 4. Resistivity (in ohm-cm) as a function of position: bottom wafer from Semix brick 71-01E.

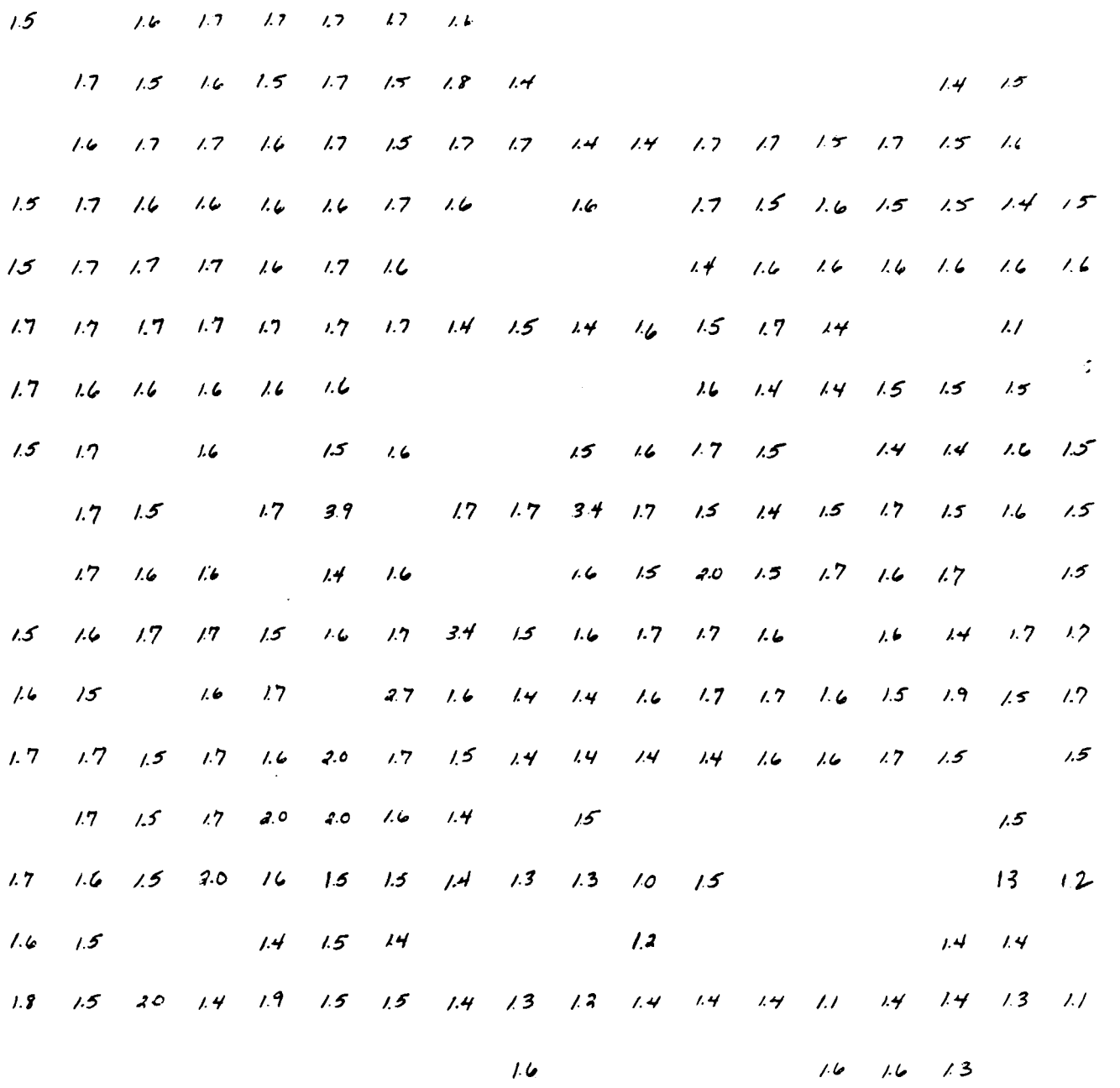

Figure 5. Resistivity (in ohm-cm) as a function of position: middle wafer from Semix brick 71-01E.

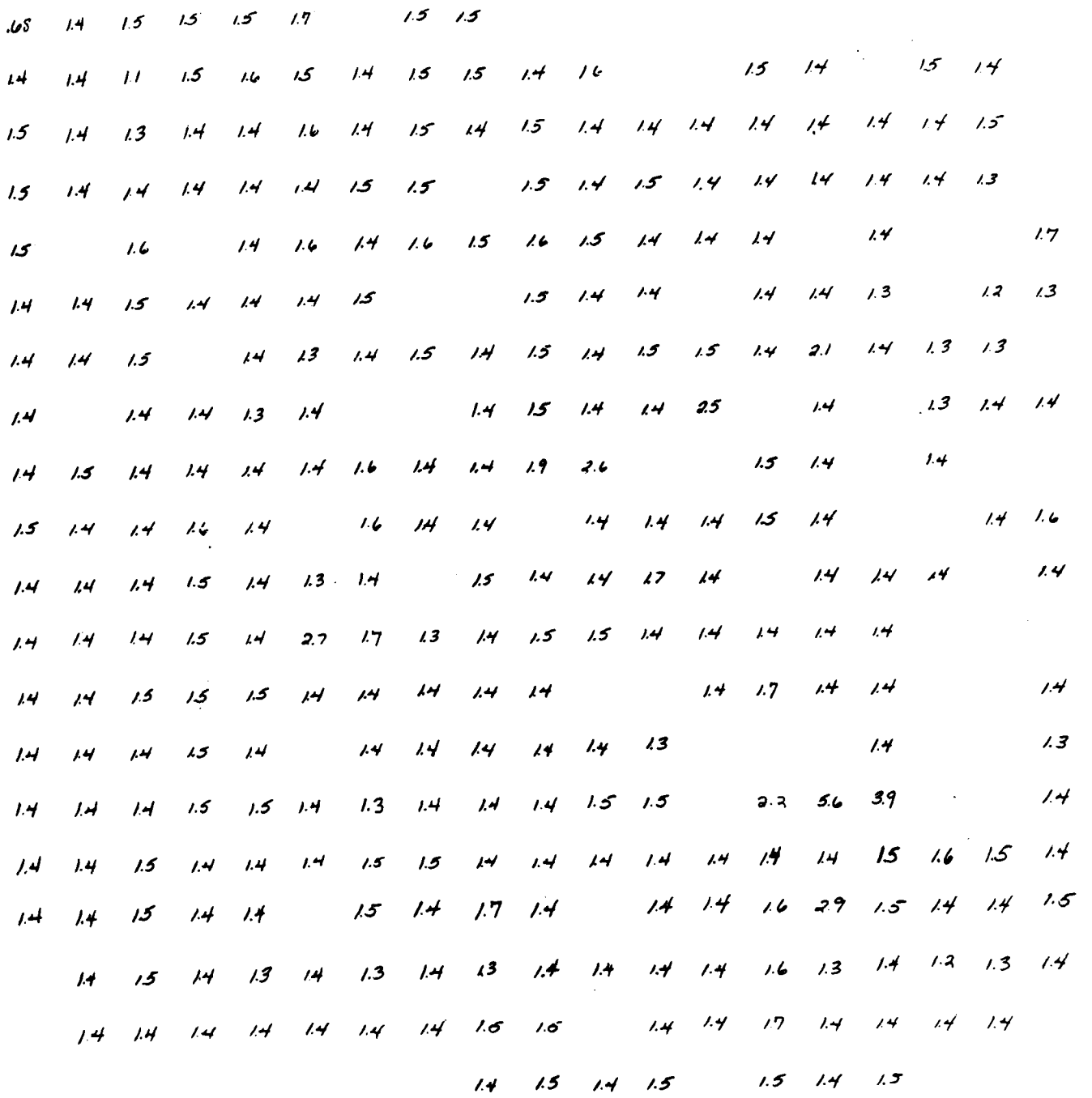

Figure 6. Resistivity (in ohm-cm) as a function of position: top wafer from Semix brick 71-01E.

Table 8 summarizes the results from the mini-cell wafer set. In general, these results show that, since the standard deviation about the mean is very small, the resistivity does not vary significantly across a wafer. The average resistivity does appear to decrease slightly from the bottom to the top of an ingot.

3. Illuminated I-V Characteristics

The illuminated AM0, red-filtered, and blue-filtered I-V characteristics (short-circuit current, open-circuit voltage, fill-factor) of all mini-cells were measured under an AM0, 135 mW/cm^2, CW, filtered-xenon light source at 25°C. The average, standard deviation, coefficient of variance, and range of the characteristics for each wafer are shown in Table 9.

The average short-circuit current density (J_{sc}) of the polycrystalline cells was always less than that of the single-crystal control wafer (SC11-1). In the best material (C4-116B), the difference was only 3 percent; the bottom wafer of brick 71-01E was about 14 percent lower. The scatter for the wafers from brick 71-01E and for the Wacker wafer was less than 3 percent; the scatter in the short-circuit current of the wafers from brick C4-116B and C4-108 was significantly greater, 5.6 and 6.7 percent, respectively.

Table 8. Resistivity (in ohm-cm) of the mini-cell wafer set, as determined from junction-capacitance data. Wafer SC-11 is the single-crystal control.

WAFER	AVERAGE	STANDARD DEVIATION
SC-11	1.14	0.07
71-01E/TOP	1.51	0.11
71-01E/MIDDLE	1.56	0.15
71-01E/BOTTOM	1.70	0.13
C4-116B	2.24	0.15
C4-108	1.69	0.10
WACKER SILSO	1.61	0.12

Table 9. Illuminated I-V characteristics of the mini-cell wafer set. Wafer SC-11 is the single-crystal control. Measured at AMO, 135 mW/cm^2, 25°C.

WAFER		J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	J_R (mA/cm^2)	J_B (mA/cm^2)	G_S (mmho/cm^2)
SC11-1	AVG	30.3	580	61.7	16.3	8.5	1.78
	STD DEV	0.4	15	4.2	0.2	0.2	2.85
241 CELLS	COEF VAR	1.3	2.6	6.9	1.5	2.2	-
	RANGE	29.2-31.0	500-598	45.3-68.2	15.8-16.7	7.5-8.9	0.01-23.55
71-01E/TOP	AVG	27.9	562	66.3	14.6	8.2	1.85
	STD DEV	0.6	16	5.7	0.4	0.1	4.58
294 CELLS	COEF VAR	2.1	2.9	8.6	2.9	1.6	-
	RANGE	26.3-29.3	512-583	46.0-73.3	12.8-15.4	7.7-8.6	0.00-55.91
71-01E/MID	AVG	27.9	560	63.9	14.6	8.0	6.83
	STD DEV	0.8	19	7.2	0.5	0.2	13.02
255 CELLS	COEF VAR	2.8	3.4	11.2	3.4	2.7	-
	RANGE	25.9-30.3	414-585	29.6-73.7	13.6-15.6	7.1-8.6	0.01-90.83
71-01E/BOT	AVG	26.1	520	55.5	13.2	7.9	10.02
	STD DEV	0.5	42	9.6	0.3	0.2	15.70
271 CELLS	COEF VAR	2.0	8.1	17.2	2.5	2.5	-
	RANGE	24.0-27.6	263-554	28.4-70.4	11.8-14.0	7.0-8.3	0.00-100.80
C4-116B	AVG	29.4	559	64.6	15.2	8.7	1.51
	STD DEV	1.6	14	3.3	1.2	0.2	2.40
329 CELLS	COEF VAR	5.6	2.5	5.2	7.9	1.9	-
	RANGE	26.2-31.9	522-588	50.4-70.2	12.9-17.0	8.2-9.2	0.00-19.24
C4-108	AVG	28.2	540	56.9	14.4	8.3	13.83
	STD DEV	1.9	55	11.0	1.2	0.4	20.77
287 CELLS	COEF VAR	6.7	10.1	19.3	8.5	4.4	-
	RANGE	15.2-30.9	169-586	26.0-71.2	10.7-16.4	6.5-9.0	0.00-154.09
WACKER	AVG	27.5	551	63.6	14.0	8.3	3.31
	STD DEV	0.8	14	5.2	0.7	0.2	4.82
308 CELLS	COEF VAR	2.7	2.6	8.1	4.7	2.2	-
	RANGE	25.4-29.6	434-582	36.2-70.9	12.0-17.6	7.8-9.7	0.00-41.90

The average open-circuit voltage (V_{OC}) of the polycrystalline cells is about 20 to 60 mV lower than the average of the single-crystal control cells, which was 580 mV. The scatter for the cells from the top and middle wafer of brick 71-01E, from C4-116B, and from the Wacker wafer, is similar to that of the single-crystal control - about 15 to 20 mV. However, the cells from the bottom wafer of brick 71-01E and from the wafer from brick C4-108 have an open-circuit voltage scatter that is significantly greater - 42 and 55 mV, respectively. These two wafers also have cells whose average open-circuit voltage is significantly lower than that of the single-crystal controls or the other polycrystalline wafers.

With the exception of the wafers from the bottom of brick 71-01E and from brick C4-108, the average fill-factor (FF) of the cells from the remaining polycrystalline wafers and from the single-crystal control wafer are similar and do not show excessive scatter. The average fill-factor is low (62 to 66 percent) for these wafers, including the single-crystal control wafer, due to the series resistance resulting from the lack of a fine front grid metallization. The average fill factor of the wafers from the bottom of brick 71-01E and from brick C4-108, 56 and 57 percent, respectively, is lower than that of the other wafers; in addition, their scatter is substantially greater.

The red-filtered short-circuit current density is sensitive to the minority-carrier diffusion length. The red filter (Corning filter 2408) transmits only these wavelengths longer than about 620 nm; this light would have an absorption coefficient in silicon of less than $4x10^3$ cm^{-1} and would be able to penetrate deeply into the bulk. Hence, carriers generated far from the junction by this long-wavelength light will be collected only if the minority-carrier diffusion length is sufficiently long. The blue filter (Corning filter 9788) transmits those wavelengths shorter than 600 nm. This light is able to penetrate only about 2 microns into silicon; therefore, the blue-filtered short-circuit current density is most sensitive to changes in the junction and near-junction regions.

The red-filtered short-circuit current density (J_R) of the polycrystalline cells was less than that of the single-crystal control cells, indicating shorter minority-carrier diffusion lengths in the polycrystalline silicon. The scatter in the red-filtered short-circuit current density of the cells from brick 71-01E was greater than that of the single-crystal control cells, but was substantially less than the scatter of the cells from the other polycrystalline wafers. The blue-filtered short-circuit current density (J_B) was fairly constant although it was somewhat greater for the single-crystal control wafer and for the wafer from brick C4-116B.

The average shunt conductance (G_S) varied substantially from wafer to wafer and within each wafer. It was low, less than 2 mmho/cm^2, in the single crystal control wafer, in the top wafer from brick 71-01E, and in the wafer from brick C4-116B. It was very high, greater than 5 mmho/cm^2, in the wafers from the middle and bottom of brick 71-01E and from the middle of brick C4-108. The average shunt conductance of the Wacker wafer was intermediate at 4.8 mmho/cm^2. Shunt conductance tended to increase from the top to the bottom of brick 71-01E. The ranges of the shunt conductance of the cells from the wafers from the middle and bottom of brick 71-01E and from brick C4-108 were 91, 100, and 154 mmho/cm^2, respectively, which are significantly greater than those of the remaining polycrystalline wafers (19 to 55 mmho/cm^2).

4. Shunt Conductance

Of particular interest in the data from the mini-cell wafers is the wide variation in shunt conductance of the mini-cells from wafer to wafer and, especially, within any wafer. The average shunt conductance varied by more than an order of magnitude from wafer to wafer, from a low of 1.5 mmho/cm^2 for wafer C4-116B to a high of 20.8 mmho/cm^2 for C4-108. Shunt conductances on the order of 1 mmho/cm^2 have little effect on cell performance. However, shunt conductances greater than 10 mmho/cm^2 will reduce the theoretical fill-factor by more than 20

percent. Thus, shunt conductances that are consistently greater than 10 mmho/cm^2 are a serious impediment to achieving a high efficiency solar cell.

Figures 7, 8 and 9 show histograms of shunt conductance for the top, middle, and bottom wafers, respectively, from Semix brick 71-01E. The top wafer had a nearly flat distribution from about 0.01 mmho/cm^2 to 10 mmho/cm^2, with one peak at 0.2 to 0.5 mmho/cm^2 and one peak at 2 to 5 mmho/cm^2. The middle wafer, in contrast, had only one peak, at 2 to 5 mmho/cm^2, with a normal-looking distribution about the maximum. The distribution for the bottom wafer is skewed toward higher values of shunt conductance, with a maximum at 20 to 50 mmho/cm^2. There is also a peak at 2 to 5 mmho/cm^2. Only about 4 percent of the cells of the top wafer had values of shunt conductance greater than 10 mmho/cm^2. However, more than 18 percent of the middle wafer's cells, and nearly 30 percent of the bottom wafer's cells, had shunt conductances greater than 10 mmho/cm^2. Microscopic examination of these cells revealed that in many cases inclusions were present in those cells with large shunt conductances.

This observation was repeated with wafer C4-108, whose histogram, shown in Figure 10, has a peak at 10 to 20 mmho/cm^2 as well as 2 to 5 mmho/cm^2 and is skewed toward higher shunt conductances. About 40 percent of the cells had values of shunt conductances greater than 10 mmho/cm^2. Many inclusions were

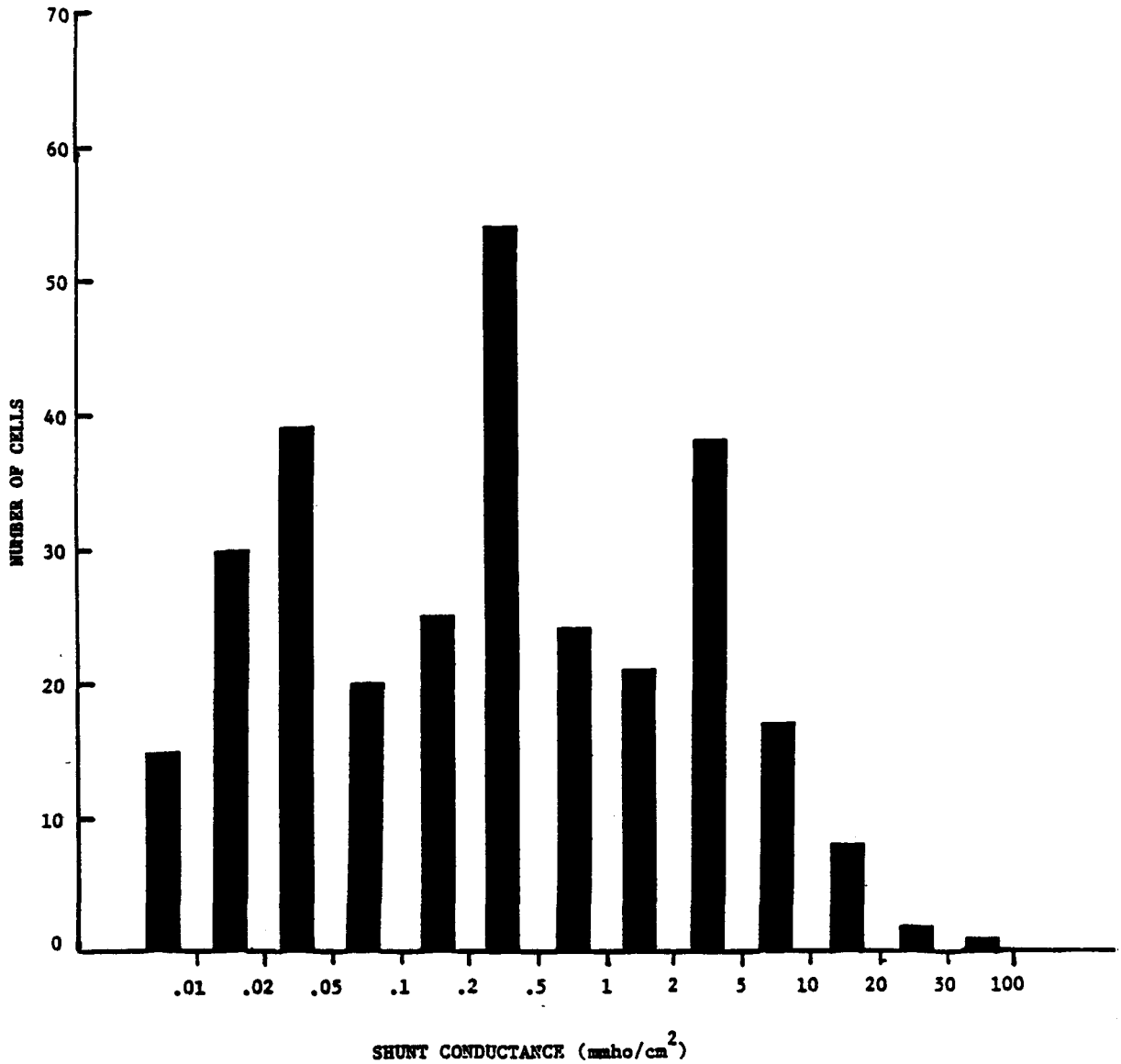

Figure 7. Histogram of shunt conductance: top wafer from Semix brick 71-01E.

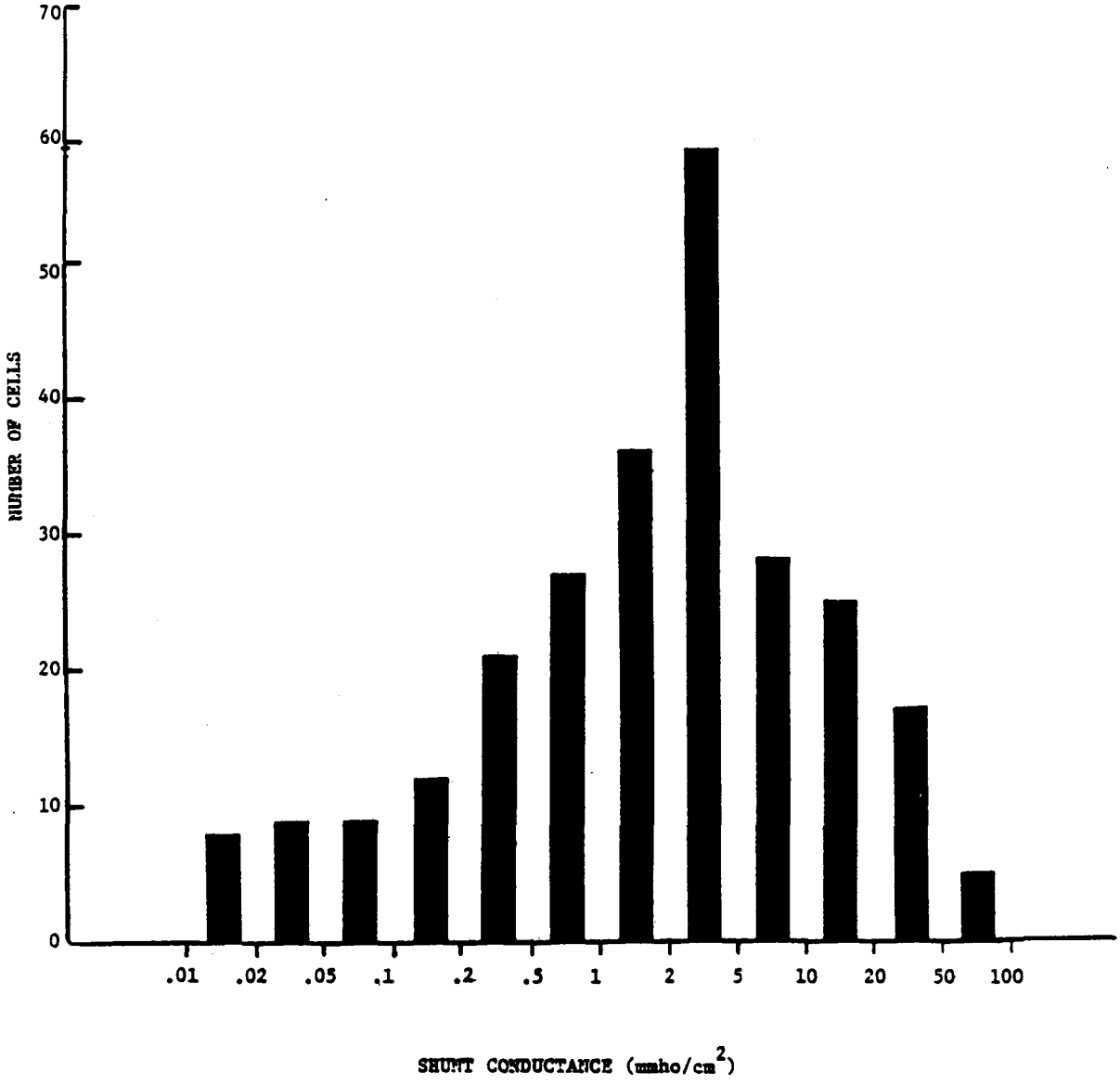

Figure 8. Histogram of shunt conductance: middle wafer from Semix brick 71-01E.

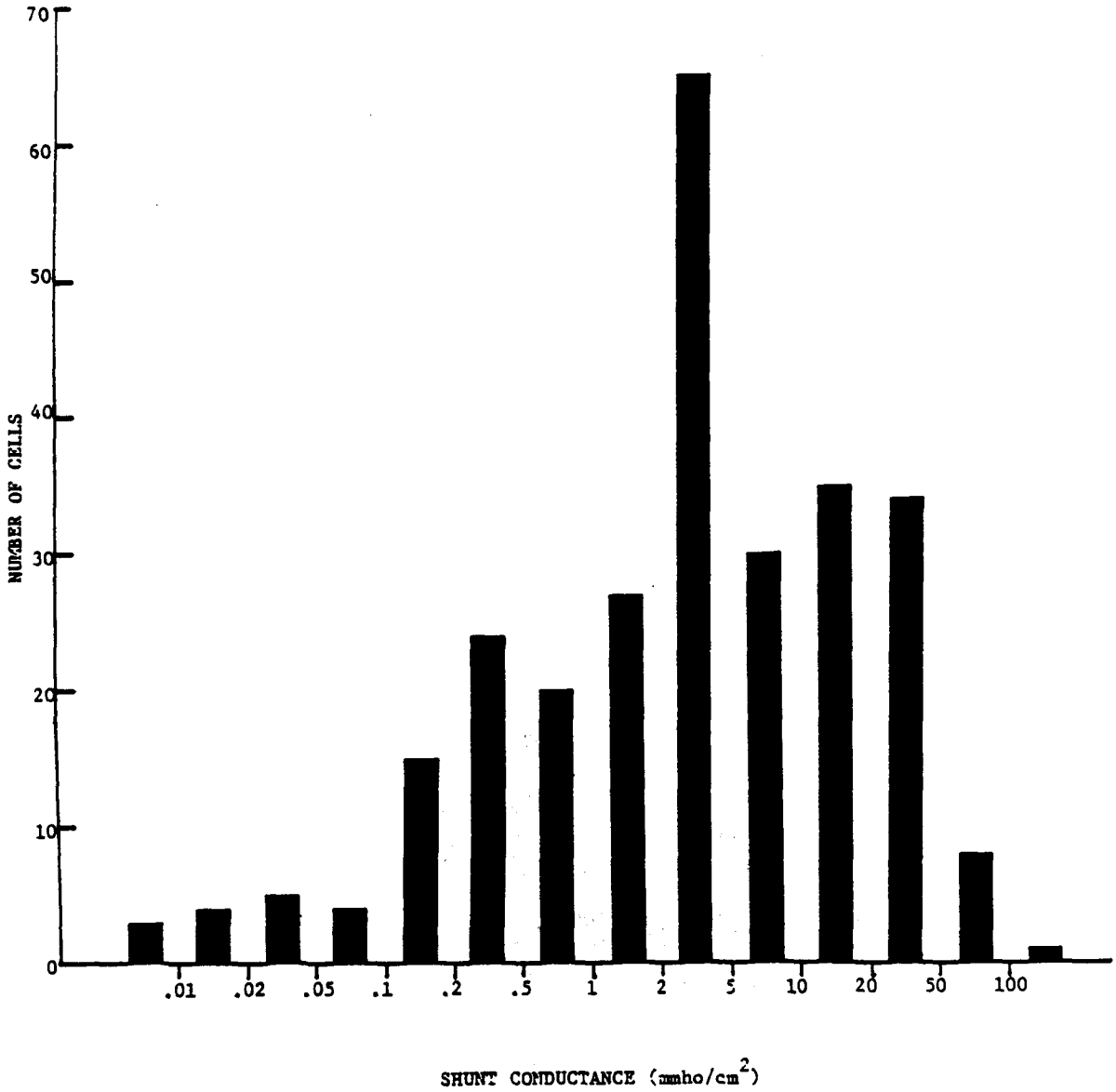

Figure 9. Histogram of shunt conductance from the bottom wafer from Semix brick 71-01E.

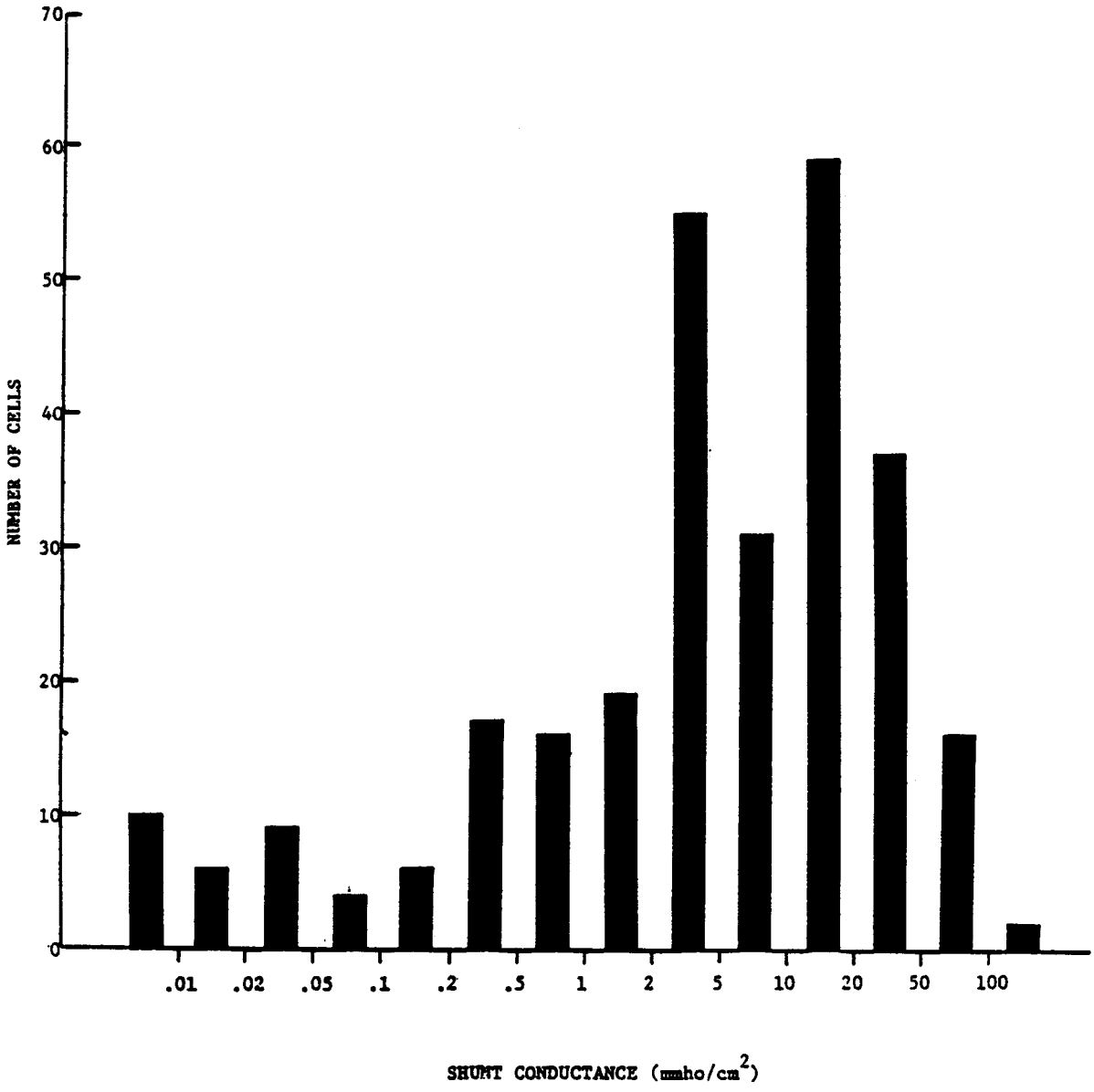

Figure 10. Histogram of shunt conductance: Semix brick C4-108.

present in these cells. Two SEM photographs of inclusions in this material (from a Secco-etched wafer next to the wafer used to fabricate the mini-cells) are shown in Figure 11.

In contrast to wafer C4-108, wafer C4-116B has a distribution, Figure 12, which, while skewed toward higher shunt conductances, has a peak in the 0.5 to 2.0 mmho/cm^2 range. Very few inclusions were observed in this wafer, and only about 1 percent of the cells had values of shunt conductance greater than 10 mmho/cm^2.

Finally, the distribution for the Wacker Silso wafer is shown in Figure 13. This is also skewed toward high shunt conductances with a maximum in the range of 2 to 5 mmho/cm^2. Some inclusions were present in this wafer. About 7 percent of the cells had values of shunt conductances greater than 10 mmho/cm^2.

While several interpretations of this data can be made, of significance is the fact that, for the wafer from the bottom of brick 71-01E and from brick C4-108, large numbers of high shunt conductance cells correlated strongly with the presence of many inclusions. These two wafers were also characterized by a large amount of scatter in open-circuit voltage and fill-factor, and large average values of shunt conductance, as shown in Table 10. Therefore, the degradation in open-circuit voltage and fill-factor, for these two wafers, was due to inclusions, which acted as resistive shunts.

Figure 11. SEM photographs of inclusions in polycrystalline wafer from Semix brick C4-108.

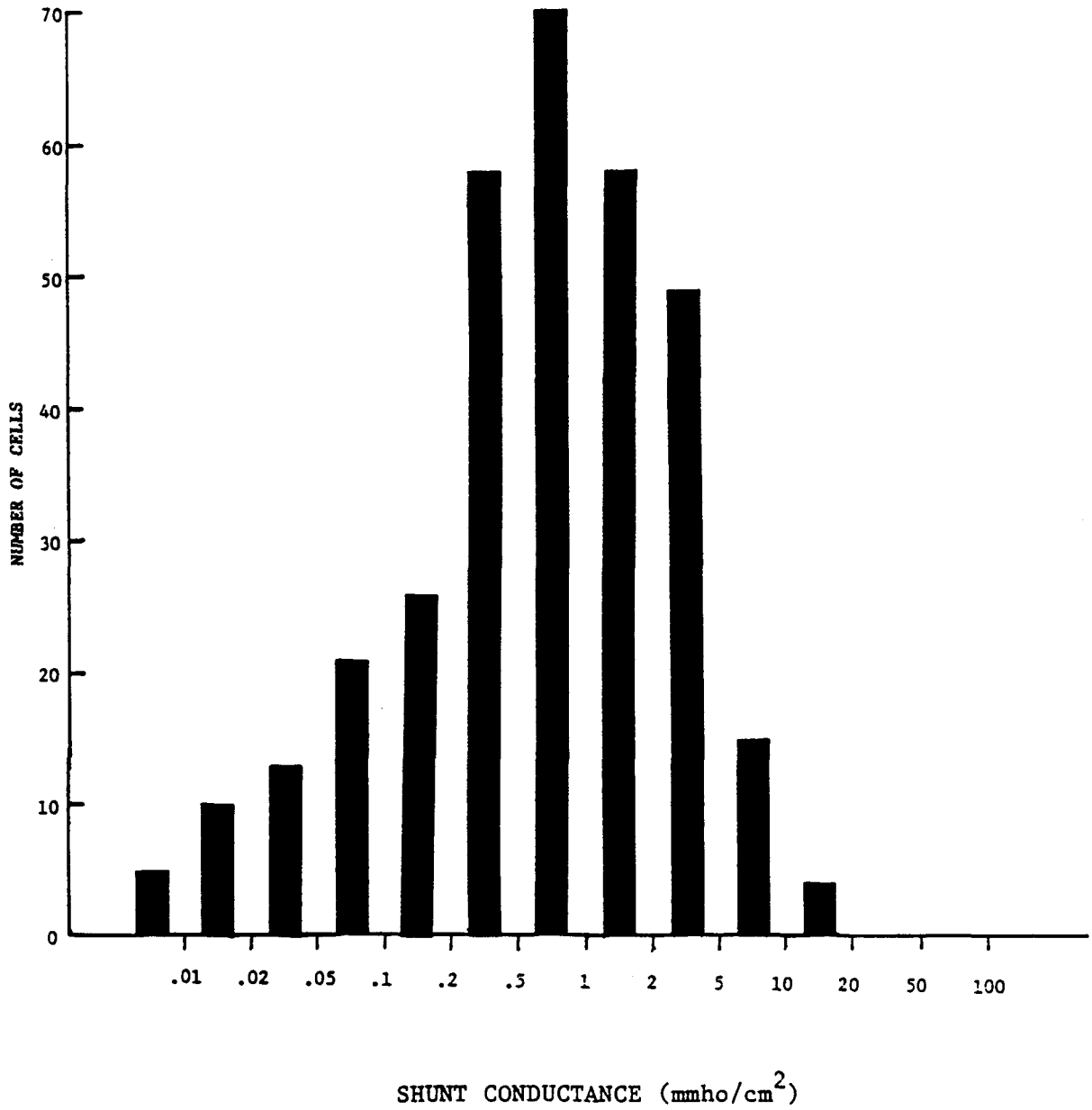

Figure 12. Histogram of shunt conductance: Semix brick C4-116B.

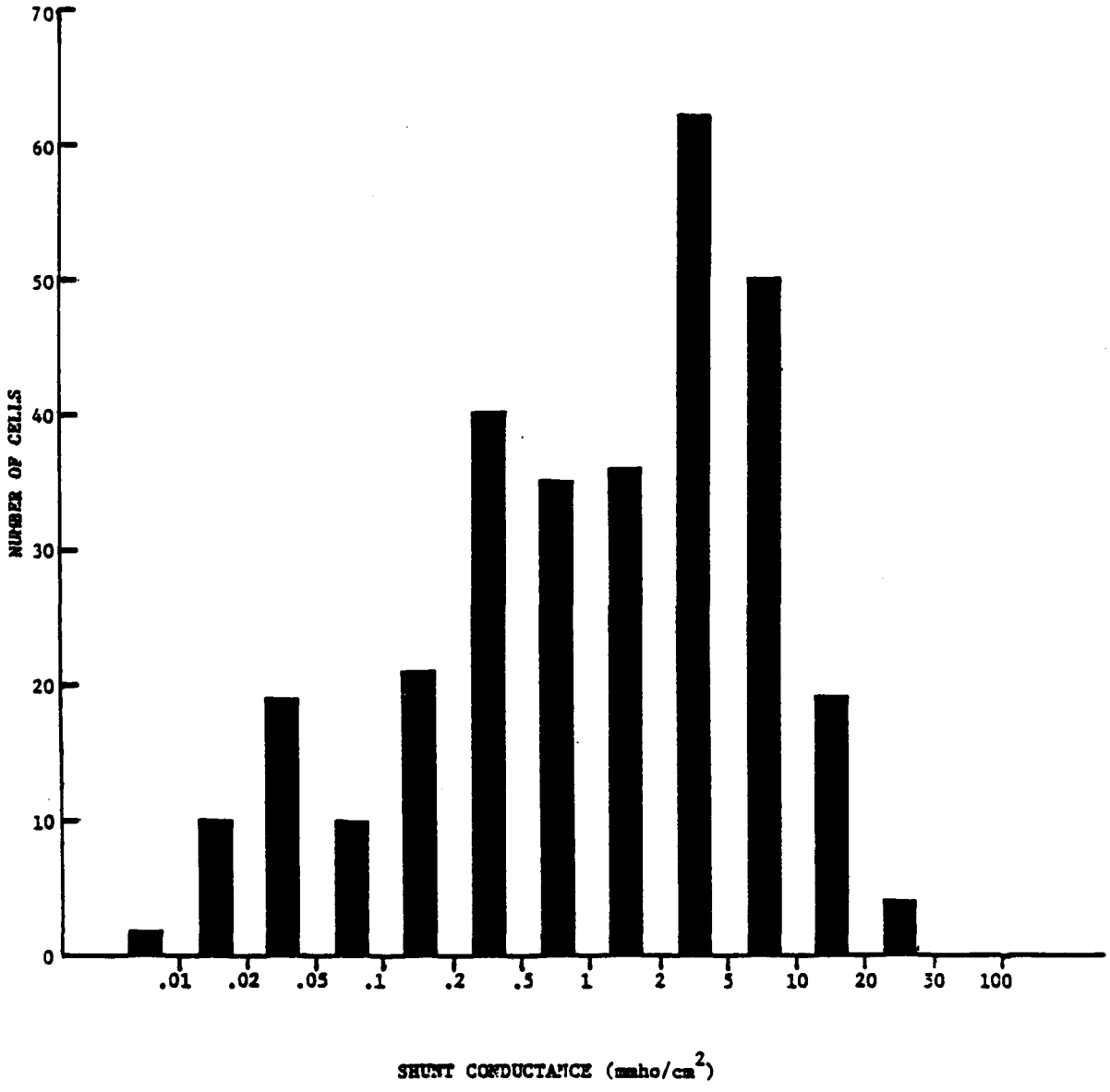

Figure 13. Histogram of shunt conductance: Wacker Silso wafer.

Table 10. Average and range of open-circuit voltage, fill-factor, and shunt conductance for the mini-cell wafer set. V_{OC} tested at AMO, 135 mW/cm^2, 25°C.

	V_{OC}(mV)		FF(%)		G_S(mmho/cm^2)	
WAFER	AVERAGE	RANGE	AVERAGE	RANGE	AVERAGE	RANGE
71-01E, TOP	562	512-583	66.3	46.0-73.3	1.9	0.0- 55.9
71-01E, MIDDLE	560	414-585	63.9	29.6-73.7	6.8	0.0- 90.8
71-01E, BOTTOM	520	263-554	55.5	28.4-70.4	10.0	0.0-100.8
C4-108	540	169-586	56.9	26.0-71.2	13.8	0.0-154.1
C4-116B	559	522-588	64.6	50.4-70.2	1.5	0.0- 19.2
WACKER SILSO	551	434-582	63.6	36.2-70.9	3.3	0.0- 41.9

5. Dark I-V Characteristics

Although the low open-circuit voltage of many mini-cells with excessive shunt conductance can be accounted for by inclusions, there were still many other mini-cells whose open-circuit voltage is low even though they were not shunted. Further characterization of these cells to determine the cause of the open-circuit voltage degradation was begun by determining their dark I-V characteristics.

The current-voltage (J-V) curve of a solar cell can be modelled approximately by the two-exponential equation

$$J = J_{QNO} \exp (V/\beta) + J_{SCO} \exp (V/n\beta) + G_s V - J_L$$

where J_{QNO} is the recombination current density (at zero bias) in the quasi-neutral (bulk) region, J_{SCO} is the space-charge (depletion region) recombination current density (at zero bias), n is the so-called ideality factor of the second diode (space-charge), G_s is the shunt conductance per unit cell area, and J_L is the light-generated current density, which in the dark is identically equal to zero. The factor β is equal to kT/q, which have their usual meanings; it is assumed in the approximation that the voltage, V, is much greater than β (approximately equal to 26 mV at 25°C).

The dark I-V characteristics, J_{QNO}, J_{SCO}, and n, are determined by making a series of measurements of J as a function of V. The shunt conductance, G_S, is determined by the behavior of the J-V curve for small bias (V 200 mV). A computer program was then used to choose simultaneous values of J_{QNO}, J_{SCO}, and n such that the calculated J-values are equal to the measured J-values. The measured values of J as a function of V are determined by the I_{SC}-V_{OC} technique (varying the illumination level), which eliminates one particularly large source of error, series resistance. For the mini-cells, this is especially important since the series resistance is large due to lack of a fine line metallization on the front.

The I_{SC}-V_{OC} characteristics of mini-cells in four regions of wafer C4-116B were measured. This wafer was chosen because the average short-circuit current density is nearly equal to that of the single-crystal Czochralski mini-cells, indicating long average minority-carrier diffusion length, and there did not appear to be an excessive number of inclusions, which act as resistive shunts. The I_{SC}-V_{OC} data was then reduced to the "dark I-V" or junction characteristics that are summarized in Figures 14 through 17, which show the open-circuit voltage, fill-factor, J_{QNO}, J_{SCO}, n-factor, open-circuit voltage loss (Δ V) and fill-factor loss (Δ FF) due to space-charge recombination current. These last two factors are derived by calculating the effect of J_{SCO} on the open-circuit voltage and

fill-factor that were theoretically obtained by assuming the cell can be represented by an ideal diode with a saturation current equal to J_{QNO} and a light-generated current density equal to the short-circuit current density.

Figure 14 shows the case where the open-circuit voltage is dominated by recombination in the bulk. The open-circuit voltage of the cells in column 18 is about 15 to 20 mV lower than that of the cells in column 17. The quasi-neutral recombination current of the cells in column 18 is approximately a factor of two greater than that of the cells in column 17. Theoretically, for an ideal solar cell (n-factor = 1), doubling the quasi-neutral recombination current will decrease the open-circuit voltage by about 18 mV. Therefore, even though the space-charge recombination current may increase, most of the open-circuit voltage loss is due to J_{QNO}; the open-circuit voltage loss due to J_{SCO} is only 1 to 7 mV.

From Shockley's analysis [9], the quasi-neutral recombination current of a p-n junction is given by the expression

$$J_{QNO} = \frac{q n_i^2 D_n^2}{N_A L_n}$$

for the case when $N_D >> N_A$. In this expression n_i is the intrinsic carrier concentration, D_n is the minority-carrier

	17	18
12	567 68 7.9 x 10^{-9} 1.2 x 10^{-3} 2.9 2 2	544 69 16.0 x 10^{-9} 2.2 x 10^{-4} 2.2 3 2
13	556 67 9.5 x 10^{-9} 5.2 x 10^{-5} 1.9 6 3	540 68 14.0 x 10^{-9} 2.4 x 10^{-4} 2.1 7 4
14	554 65 11.1 x 10^{-9} 1.2 x 10^{-2} 3.5 5 6	540 66 18.1 x 10^{-9} 3.5 x 10^{-2} 4.2 6 7

KEY

V_{OC}	FF
J_{QNO}	
J_{SCO}	
n-factor	
ΔV	ΔFF

Figure 14. Dark I-V characteristics: mini-cell wafer C4-116B.

diffusion coefficient, N_A is the boron concentration in the bulk, and L_n is the minority-carrier diffusion length. Assuming that the dopant concentration is homogeneous, then J_{QNO} is seen to be inversely proportional to L_n. That is, doubling the minority-carrier diffusion length will decrease J_{QNO} by a factor of two. The above experimental results showing that J_{QNO} increases by a factor of two indicates that L_n for the cells in column 18 is only half as long, on average, as those in column 17. If the diffusion length decreases, then the light-generated current should also decrease since less photogenerated carriers will be collected by the junction. In fact, the short-circuit current density of the cells in column 18 is significantly lower (by about 3 to 5%).

A different type of behavior is seen in comparing cell 13-4 to cell 13-2 in Figure 15. Most of the open-circuit voltage loss in cell 13-4 is due to excessive recombination in the space-charge region, which is more than an order of magnitude greater. For this cell, the theoretical loss in open-circuit voltage due to space-charge recombination is about 23 mV greater than in cell 13-2; the actual difference in open-circuit voltage is about 18 mV. The loss in fill-factor due to J_{SCO} is about 8 percent greater in cell 13-4. The remaining cells in Figure 15, cells 13-3, 14-2, 14-3, 14-4, 15-2, 15-3, and 15-4, have approximately the same quasi-neutral recombination current, 7.1 to 9.6 x 10^{-9} mA/cm^2. In general, the open-circuit voltage

	2	3	4
13	579 66 4.9×10^{-9} 9.2×10^{-5} 2.1 4 2	563 65 8.8×10^{-9} 7.0×10^{-5} 2.1 3 1	561 62 4.5×10^{-9} 1.1×10^{-3} 2.2 25 10
14	568 66 7.2×10^{-9} 9.3×10^{-5} 2.0 5 3	556 60 8.4×10^{-9} 1.2×10^{-1} 4.7 12 15	566 63 7.1×10^{-9} 6.8×10^{-5} 1.9 6 3
15	563 68 9.5×10^{-9} 8.5×10^{-4} 2.6 3 3	567 68 9.3×10^{-9} 1.5×10^{-2} 4.4 2 3	561 63 9.6×10^{-9} 9.9×10^{-3} 3.6 4 5

Figure 15. Dark I-V characteristic: mini-cell wafer C4-116B.

tracks J_{QNO}, but cell 14-3, which has the lowest open-circuit voltage, has space-charge recombination current that is nearly an order of magnitude greater than any of the others, and more than three orders of magnitude greater than the best.

To summarize, cells 13-3, 14-2, 14-4, 15-2, 15-3, and 15-4 have low open-circuit voltage due to high J_{QNO}; cell 13-4 has low open-circuit voltage due to high J_{SCO}; and open-circuit voltage of cell 14-3, the lowest of the group, is low due to both high J_{QNO} and high J_{SCO}.

Figure 16 shows a group of cells where much of the loss is due to space-charge recombination. Only in cells 12-16 and 12-17 is the open-circuit voltage loss due to space-charge recombination fairly small. The cell with the best open-circuit voltage, cell 10-16 at 575 mV, also has the most loss in open-circuit voltage due to space-charge recombination, even though the actual value of J_{SCO} is very low. This means that sensitivity to space-charge recombination current increases as the quasi-neutral recombination current decreases. This is also suggested by cells 11-15, 11-16, and 11-17. Even though both J_{QNO} and J_{SCO} increase, the loss in open-circuit voltage due to J_{SCO} decreases.

The last map, Figure 17, shows an area where J_{QNO} varied widely, from as low as 2.5×10^{-9} mA/cm^2 (cell 13-9) to a high

	15	16	17
10	560 65 7.7×10^{-9} 1.1×10^{-3} 2.4 9 7	575 65 3.7×10^{-9} 5.4×10^{-5} 1.8 14 5	565 67 7.5×10^{-9} 8.4×10^{-5} 2.0 5 3
11	554 64 7.6×10^{-9} 2.4×10^{-4} 2.0 15 6	544 64 9.6×10^{-9} 2.8×10^{-3} 2.5 15 9	539 63 10.8×10^{-9} 5.4×10^{-3} 2.8 14 9
12	545 65 10.1×10^{-9} 5.1×10^{-3} 2.6 19 11	567 66 8.0×10^{-9} 1.1×10^{-3} 2.6 4 3	567 68 8.1×10^{-9} 9.9×10^{-4} 2.7 3 2

Figure 16. Dark I-V characteristics: mini-cell wafer C4-116B.

	6	7	8	9	10	11	12
			566 67 7.8×10^{-9} 5.0×10^{-5} 1.9 6 3	569 69 7.1×10^{-9} 2.4×10^{-5} 1.8 4 2	576 68 5.5×10^{-9} 1.4×10^{-5} 1.8 4 2	562 64 8.4×10^{-9} 9.4×10^{-3} 3.7 3 4	568 67 5.0×10^{-9} 1.9×10^{-5} 1.7 11 3
10							
		570 60 4.0×10^{-9} 2.8×10^{-4} 2.0 17 7	575 65 4.7×10^{-9} 2.3×10^{-5} 1.7 10 3	568 65 5.8×10^{-9} 2.0×10^{-4} 2.0 11 5	557 67 11.4×10^{-9} 3.9×10^{-3} 3.1 4 4	557 53 5.3×10^{-9} 4.5×10^{-2} 3.6 22 17	568 61 3.0×10^{-9} 5.9×10^{-4} 2.1 25 9
11							
	557 66 9.5×10^{-9} 4.3×10^{-4} 2.2 8 5	506 65 34.9×10^{-9} 1.7×10^{-2} 2.9 21 13	530 64 26.2×10^{-9} 1.4×10^{-2} 3.2 9 8	574 68 6.0×10^{-9} 2.6×10^{-5} 1.9 3 2			
12							
	569 66 8.1×10^{-9} 1.2×10^{-2} 4.0 3 4	571 64 5.0×10^{-9} 5.9×10^{-4} 2.2 14 7	540 52 12.7×10^{-9} 2.0×10^{-3} 2.3 19 9	570 56 2.5×10^{-9} 8.5×10^{-4} 2.2 27 10			
13							
			570 66 6.0×10^{-9} 1.2×10^{-4} 2.0 8 4				
14							

Figure 17. Dark I-V characteristics: mini-cell wafer C4-116B.

of 3.5 x 10^{-8} mA/cm^2 (cell 12-7). An order of magnitude increase in J_{QNO} for the ideal solar cell theoretically results in a 60 mV decrease in open-circuit voltage, which is confirmed by the 68 mV difference between these cells. J_{SCO} also shows substantial scatter, from 1.4 x 10^{-5} mA/cm^2 (cell 10-10) to 4.5 x 10^{-2} mA/cm^2 (cell 11-11). The open-circuit voltage loss due to space-charge recombination varies from 3 to 23 mV; the loss in fill-factor due to J_{SCO} ranges from 2 to 17 percent. In particular, the lowest open-circuit voltage cells, 12-7 and 12-8, are degraded mainly due to excessive quasi-neutral recombination current, even though space-charge recombination current is large and also contributes to V_{OC} loss. Cells 10-8, 10-9, 10-11, 11-10, 12-6, 13-6, 13-8, and 14-8 have losses also due to excessive J_{QNO}, though not as great. Cells 10-12, 11-7, 11-9, 11-11, 11-12, 13-7, and 13-9 have losses due to space-charge recombination. The best cells of this group, 10-10, 11-8, and 12-9, have J_{QNO} equal to about 5 x 10^{-9} mA/cm^2, J_{SCO} less than 2 x 10^{-5} mA/cm^2, and n-factors less than two; the open-circuit voltage is about 575 mV.

The quasi-neutral current of most (24 out of 43) of the measured mini-cells on this wafer, C4-116B, varies from about 5 x 10^{-9} mA/cm^2 to around 1 x 10^{-8} mA/cm^2. At the extremes, the quasi-neutral current appears to vary by about an order of magnitude across the wafer, which would imply at least a 60 mV variation in open-circuit voltage. The space-charge

recombination current of only four out of 43 measured mini-cells is sufficiently large to account for more than a 20 mV open-circuit voltage loss. For the majority (27 out of 43) of the sampled cells, the open-circuit voltage loss due to excess space-charge recombination is less than 10 mV. Hence, the scatter (standard deviation) in the open-circuit voltage of the mini-cells of this wafer, $\pm$ 14 mV, is roughly composed of two parts, $\pm$ 10 mV due to quasi-neutral recombination variations, and $\pm$ 5 mV due to space-charge recombination variations. Recombination in the bulk is the predominant loss mechanism, although there are mini-cells on this wafer, C4-116B, that suffer from recombination in the space-charge region.

An additional mini-cell wafer was evaluated for dark I-V characteristics in order to further substantiate the above conclusions. The wafer from the top of Semix brick 71-01E was tested since this wafer had few apparent inclusions, as suggested by the large number of contiguous cells with values of shunt conductance less than 1 mmho/cm^2.

Figures 18 through 21 show the junction I-V characteristics in four areas of this wafer. Figure 18 shows an area in the upper left corner; the open-circuit voltage varies from 573 mV to 552 mV and tracks the quasi-neutral current, which varies from 5.5 x 10^{-9} mA/cm^2 to 10.0 x 10^{-9} mA/cm^2; the loss due to space-charge recombination is 10 mV or less. Therefore, the

	2	3	4
2	572 72 5.4×10^{-9} 5.1×10^{-5} 2.2 2 1	561 71 7.4×10^{-9} 7.8×10^{-3} 3.0 11 9	568 66 6.9×10^{-9} 1.3×10^{-1} 5.9 5 9
3	556 65 7.6×10^{-9} 7.5×10^{-2} 4.5 10 13	573 69 5.5×10^{-9} 1.9×10^{-3} 2.9 4 4	566 70 6.4×10^{-9} 1.5×10^{-4} 2.0 8 4
4	570 69 6.6×10^{-9} 3.6×10^{-4} 2.4 3 2	552 69 10.0×10^{-9} 2.0×10^{-4} 2.0 8 4	566 69 7.0×10^{-9} 5.0×10^{-5} 2.0 4 2

Figure 18. Dark I-V characteristics: mini-cell wafer 71-01E/top.

	9	10	11	12	13
2			549 66 9.5×10^{-9} 1.0×10^{-3} 2.3 12 7	515 57 9.5×10^{-9} 4.1×10^{-2} 3.1 50 20	
3	562 69 8.9×10^{-9} 6.4×10^{-3} 3.3 4 5	565 66 5.8×10^{-9} 1.6×10^{-3} 2.5 13 8	574 70 5.8×10^{-9} 1.5×10^{-4} 2.1 5 3	554 62 8.1×10^{-9} 8.8×10^{-3} 2.9 19 12	572 67 5.6×10^{-9} 1.2×10^{-3} 2.5 7 5
4	575 67 6.2×10^{-9} 1.3×10^{-2} 3.8 4 5			574 70 5.3×10^{-9} 1.5×10^{-3} 2.8 4 3	580 70 4.5×10^{-9} 1.6×10^{-3} 2.9 3 3
5	562 64 7.0×10^{-9} 1.8×10^{-1} 5.5 11 15		555 62 8.1×10^{-9} 3.5×10^{-1} 6.3 12 18	562 63 6.7×10^{-9} 1.6×10^{-1} 5.3 11 15	577 72 5.4×10^{-9} 1.3×10^{-4} 2.1 5 3
6	576 67 6.3×10^{-9} 7.7×10^{-2} 5.7 3 6	531 47 10.7×10^{-9} 9.4×10^{-1} 6.7 31 31	556 58 8.4×10^{-9} 2.7×10^{-1} 5.6 16 19	573 71 7.0×10^{-9} 2.3×10^{-4} 2.3 4 2	579 71 4.6×10^{-9} 1.4×10^{-5} 1.8 3 1
7	566 68 8.4×10^{-9} 1.8×10^{-2} 4.2 3 4	572 68 6.0×10^{-9} 6.2×10^{-3} 3.3 5 5	567 65 6.6×10^{-9} 1.4×10^{-1} 5.8 7 10	569 72 7.0×10^{-9} 8.9×10^{-5} 2.2 3 2	582 71 4.4×10^{-9} 3.5×10^{-5} 2.0 3 1
8	526 48 13.0×10^{-9} 1.0×10 7.2 27 31	568 64 4.0×10^{-9} 7.7×10^{-4} 2.2 18 8	580 71 4.4×10^{-9} 8.5×10^{-6} 1.7 4 2	582 71 4.0×10^{-9} 1.2×10^{-5} 1.8 3 1	581 70 4.1×10^{-9} 1.3×10^{-5} 1.8 2 1

Figure 19. Dark I-V characteristics: mini-cell wafer 71-01E/top.

	16	17	18	19
2	572 69 5.6×10^{-9} 4.0×10^{-3} 3.1 6 5	524 48 12.0×10^{-9} 9.8×10^{-1} 6.7 32 32	576 69 5.4×10^{-9} 5.9×10^{-5} 2.0 4 2	572 68 5.4×10^{-9} 1.7×10^{-3} 2.7 6 5
3	560 70 8.9×10^{-9} 6.4×10^{-4} 2.4 5 4	567 68 5.2×10^{-9} 1.4×10^{-4} 2.0 10 5	564 69 6.2×10^{-9} 1.1×10^{-3} 3.0 2 2	576 68 5.4×10^{-9} 1.2×10^{-4} 2.2 2 2
4	576 70 4.8×10^{-9} 4.3×10^{-4} 2.4 4 3	544 72 14.0×10^{-9} 4.2×10^{-5} 1.8 4 2	569 69 5.8×10^{-9} 1.2×10^{-4} 2.0 6 3	
5		564 70 8.2×10^{-9} 1.2×10^{-3} 2.9 2 2		

Figure 20. Dark I-V characteristics: mini-cell wafer 71-01E/top.

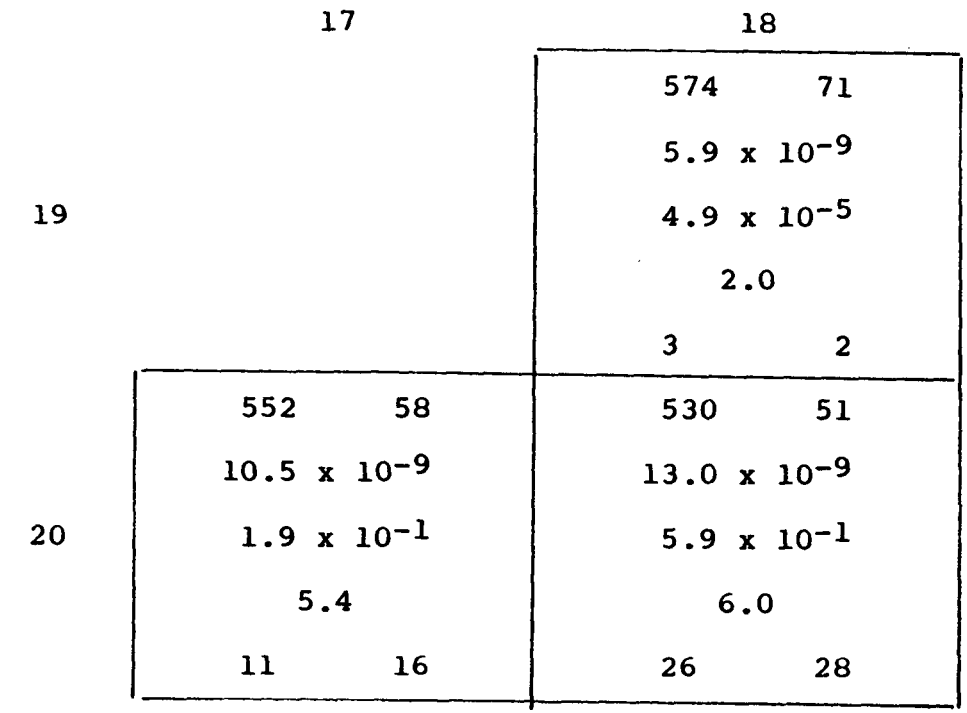

Figure 21. Dark I-V characteristics: mini-cell wafer 71-01E/top.

variation in open-circuit voltage in this area is primarily due to variations in J_{QNO}.

Figure 19 shows a large area in the upper middle of this wafer. In this area, cells suffer from both quasi-neutral recombination and space-charge recombination. For example, cell 2-12 (V_{OC} = 515 mV) has excessive J_{QNO} (the majority of the cells in this area have values of J_{QNO} near 5 x 10^{-9} mA/cm^2) but also significant loss, 50 mV, due to space-charge recombination. Cells 3-21 (V_{OC} = 554 mV), 5-11 (V_{OC} = 555 mV), and 6-11 (V_{OC} = 556 mV) are similar, although not degraded to the same extent by either. Cells 6-10 (V_{OC} = 531 mV) and 8-9 (V_{OC} = 526 mV) have values of J_{QNO} that are more than double the average value (loss = 20 mV) and space-charge recombination losses of about 30 mV. It is clear that space-charge recombination can substantially reduce the open-circuit voltage in isolated locations that appear to be less than 0.2 cm^2 in area.

Figure 20 then shows an area in the upper right section of this wafer. The cells in this area corroborate the behavior observed in the other two areas. Most of the cells have values of J_{QNO} around 5 x 10^{-9} mA/cm^2. Cell 2-17 (V_{OC} = 524 mV) is degraded by both excess J_{QNO}, accounting for about 20 mV loss, and excess J_{SCO}, a 32 mV loss. The cells surrounding 2-17, with little loss due to space-charge recombination, have values of open-circuit voltage near 570 mV. Cell 4-17 (V_{OC} = 544 mV),

too, is surrounded by cells whose open-circuit voltage is near 570 mV. The excess quasi-neutral recombination current measured in this cell easily accounts for the loss.

Finally, Figure 21 shows a small area near the bottom right corner, where cell 20-17 (V_{OC} = 552 mV) is degraded mainly by excess J_{QNO}, and cell 20-18 (V_{OC} = 530 mV), besides being degraded by J_{QNO}, suffers an additional loss due to space-charge recombination.

The results seen in this wafer are very similar to those obtained for wafer C4-116B. Namely, for the majority of those cells tested (38 out of 53), the quasi-neutral recombination varies by about a factor of two, from 5 x 10^{-9} mA/cm^2 to 1 x 10^{-8} mA/cm^2. The variation in J_{QNO} at the extremes is about a factor of five. Therefore, quasi-neutral current could account for about 40 mV of V_{OC} loss. Only five out of the 53 cells have more than 20 mV loss due to space-charge recombination; nearly three-quarters (39 out of 53) of the cells have an open-circuit voltage loss due to space-charge recombination that is less than 10 mV. Hence, like wafer C4-116B, the scatter (standard deviation) in the open-circuit voltage of the mini-cells from this wafer, $\pm$ 15 mV, appears to be dominated by variations in quasi-neutral recombination.

III. PROCESSES TO IMPROVE THE PERFORMANCE OF POLYCRYSTALLINE SILICON SOLAR CELLS - DAMAGE GETTERING

Results from the thickness-resistivity matrix indicated that the short-circuit current of the thicker polycrystalline cells is consistently five to ten percent lower than that of the cells fabricated from Czochralski single-crystal silicon that were used as controls for this experiment. In looking at the effect of thickness on cell I-V characteristics, the short-circuit current of the polycrystalline cells was found to saturate at a thickness that was less than that of the single-crystal (control) cells. These results indicate that large-grain polycrystalline silicon is presently characterized by a minority-carrier diffusion length that is shorter than that of Czochralski single-crystal silicon.

The cause of the shorter minority-carrier diffusion lengths in polycrystalline silicon has not been unequivocably identified, but one possibility is that this degradation is due to a minority-carrier lifetime-killing impurity. It may be possible, if this indeed is the case, to improve the short-circuit current of polycrystalline cells by removing some of this impurity. This type of improvement has been observed for the case of metallurgical grade silicon upon annealing wafers at a temperature high enough to allow the degrading impurities to diffuse to a surface with a high dislocation density. The

procedure, called damage gettering, was reported by Saitoh, et.al. [10], to result in a minority-carrier diffusion length increase from 11 microns to 16 microns in twice-pulled Czochralski single-crystal wafers that had metallurgical grade silicon as the starting material.

An experiment to investigate the usefulness of damage gettering to improve the short-circuit current of cast polycrystalline silicon was designed. For this experiment, a number of closely-matched 10cm x 10cm polycrystalline silicon wafers from Semix brick C4-87E were quartered and thinned using a CP-type etch to a nominal thickness of 300 $\pm$ 10 microns. Each quarter wafer was sandblasted on the back side only using a 320 mesh aluminum oxide (Al_2O_3) powder in order to introduce damage. Each quarter was paired with a 5cm x 5cm single-crystal wafer (ostensibly serial wafers from one ingot) of the same thickness that was also damaged on the back side.

Groups of polycrystalline and single-crystal wafers were heat-treated for 1, 5 and 25 hours at 1000°C in flowing nitrogen. One group, the controls, was not heat-treated. After the heat-treaments were completed, all wafers, including the controls, were CP-etched to remove surface damage, and then lightly diffused in order to measure the photoconductivity decay time constant.

The microwave reflectance photoconductivity decay technique was used to monitor the change, if any, in the minority-carrier lifetime as a result of the heat-treatment. This technique has been previously shown [11] to be useful in determining the variation in an approximate value of minority-carrier lifetime across a 10cm x 10cm polycrystalline silicon wafer. The exact relationship between the measured modulated microwave photoconductivity decay time constant and the minority-carrier lifetime has not been determined, and the two are not necessarily equivalent. Because the photoconductivity decay time constant is sensitive to a number of intrinsic and extrinsic parameters,. absolute values of time constant are not meaningful. However, if all test and sample conditions are maintained constant, the technique can be validly used to evaluate changes in minority carrier lifetime.

Solar cells were fabricated from these wafers using a high efficiency process [1]. Particular attention was focused on avoiding any process that would result in a textured surface, since this would tend to enhance the light-generated current. The solar cells have a surface texture that is characteristic of a CP-type etch, and they are not AR-coated, to avoid variations due to that process. The cells were tested under an AM0, 135 mW/cm^2 light source at 25^oC. These results, along with the photoconductivity decay time results, are shown in Tables 11 and 12 for the single-crystal controls and polycrystalline cells, respectively.

For the single-crystal samples, Table 11, the average short-circuit current, open-circuit voltage, and peak power decreased as a result of any heat-treatments. On average, the red-filtered short-circuit current tended to decrease with time at 1000°C. More significantly, however, the scatter in the red-filtered short-circuit current increased substantially from ± 1 mA to more than ± 3 mA for the cells that were heat-treated for 5 hours. This behavior indicates that the minority-carrier diffusion length is being degraded by these high temperature heat-treatments. The short-circuit current tends to track the photoconductivity decay time, τ_D.

In contrast, the short-circuit current of the poly-crystalline cells, Table 12, does not track the photo-conductivity decay time constant, which decreased significantly with time at 1000°C. The short-circuit current, red-filtered short-circuit current, open-circuit voltage, and peak-power of the cells fabricated from material heat-treated at 1000°C for 5 hours are significantly greater than those of either the non-heat-treated control cells, or those cells that were heat-treated for either 1 or 25 hours. The changes in short-circuit and red-filtered short-circuit current indicate that the minority-carrier diffusion length has increased after 5 hours at 1000°C, perhaps due to gettering of fast-diffusing impurities. The red-filtered short-circuit current decrease after 25 hours is probably due to a competing process - the same process

Table 11. Illuminated I-V characteristics of damage-gettered, single-crystal, $4cm^2$ so cells as a function of anneal time at 1000°C. No AR-coating. Measured at AMO, mW/cm^2, 25°C.

ANNEAL TIME (HOURS)		τ_D (μsec)	I_{sc} (mA)	V_{oc} (mV)	PP (mW)	FF (%)	I_R (mA)	I_B (mA)	G_S (mmho)
0	AVG	21.9	108	589	47.4	74.1	51	36	0.43
	STD DEV	0.8	1	8	3.1	4.0	1	1	0.55
(16 CELLS)	COEF VAR	3.7	0.8	1.4	6.4	5.3	-	0	-
	RANGE	20.5-23.5	106-109	573-598	42.4-51.4	68.0-79.6	50-52	35-36	0.05-2.
1	AVG	15.8	104	564	43.4	73.9	48	36	0.62
	STD DEV	2.3	2	7	2.6	4.7	2	1	1.00
(16 CELLS)	COEF VAR	14.6	1.9	1.3	6.0	6.3	-	-	-
	RANGE	12.4-19.0	101-108	546-575	37.5-47.1	63.4-79.1	45-51	35-36	0.03-3.
5	AVG	9.3	101	557	43.1	76.0	46	36	0.18
	STD DEV	4.8	4	11	3.0	4.3	3	1	0.17
(13 CELLS)	COEF VAR	51.6	3.5	2.0	7.0	5.7	-	-	-
	RANGE	5.0-19.5	98-107	541-581	37.6-49.0	64.9-79.3	43-50	35-36	0.04-0.
25	AVG	13.0	103	558	41.9	72.8	47	36	0.99
	STD DEV	3.8	2	13	3.6	4.0	1	1	0.84
(11 CELLS)	COEF VAR	29.2	1.7	2.4	8.6	5.4	-	-	-
	RANGE	8.8-21.0	100-105	535-581	35.9-48.1	65.7-78.4	45-49	35-36	0.03-2.

Table 12. Illuminated I-V characteristics of damage-gettered, polycrystalline, 4cm^2 solar cells as a function of anneal time at 1000°C. No AR-coating. Measured at AMO, 135 mW/cm^2, 25°C.

ANNEAL TIME (HOURS)		τ_D (μsec)	I_{sc} (mA)	V_{oc} (mV)	PP (mW)	FF (%)	I_R (mA)	I_B (mA)	G_S (mmho)
0	AVG	5.8	83	520	31.8	73.1	31	34	0.19
	STD DEV	1.8	3	4	1.1	1.2	2	1	0.12
(8 CELLS)	COEF VAR	31.0	3.2	1	3.4	1.6	-	-	-
	RANGE	3.5-10.6	78-87	516-527	30.6-33.8	71.0-73.8	27-33	33-35	0.09-0.46
1	AVG	4.3	78	503	27.9	70.8	28	32	0.53
	STD DEV	0.7	2	6	1.4	2.0	1	1	0.16
(20 CELLS)	COEF VAR	16.3	2.8	1.1	5.2	2.7	-	-	-
	RANGE	3.2-5.9	74-83	492-516	25.5-31.3	66.3-73.2	26-31	32-34	0.32-0.94
5	AVG	3.0	98	530	36.6	70.2	43	35	0.60
	STD DEV	0.8	2	4	1.1	2.0	2	1	0.22
(16 CELLS)	COEF VAR	26.7	2.2	0.8	3.0	2.9	-	-	-
	RANGE	1.7-4.6	95-101	522-535	34.4-38.2	65.8-73.5	41-46	35-36	0.38-1.13
25	AVG	1.0	88	514	32.0	70.4	36	34	0.66
	STD DEV	0.4	4	4	1.3	0.8	3	1	0.52
(14 CELLS)	COEF VAR	40.0	4.0	0.8	4.1	1.2	-	-	-
	RANGE	0.6-2.7	82-93	507-519	30.1-34.0	69.3-71.9	32-40	33-35	0.30-2.29

causing the degradation of minority-carrier diffusion length in the single-crystal samples.

Measurements of the dark I-V characteristics were obtained for two sets of selected polycrystalline cells and one set of single-crystal cells. The polycrystalline cells were chosen to be spatially close to one another on the original wafer. The results are shown in Table 13. For both sets of polycrystalline cells, the quasi-neutral recombination current increases after only one hour at 1000°C causing a drop in open-circuit voltage and short-circuit current. After a five hour heat treatment, however, the quasi-neutral recombination current has decreased, relative to the starting value, and the open-circuit voltage and short-circuit current have increased. However, longer times do not continue to decrease the quasi-neutral recombination; after 25 hours at 1000°C, the quasi-neutral recombination is the same or greater than with no annealing. These results showing significant changes in the quasi-neutral recombination current, together with the changes in the short-circuit current and open-circuit voltage, indicate that the effective minority-carrier diffusion length is being modified by the damage-gettering heat-treatments.

The contrast, the quasi-neutral recombination of the single-crystal cells appear to be only degraded by the damage-gettering heat-treatments. A factor of five increase in quasi-

Table 13. Dark and illuminated I-V characteristics of damage-gettered, 4cm^2 solar cells as a function of anneal time at 1000°C. No AR-coating. Measured at AMO, 135 mW/cm^2, 25°C.

CELL NO	ANNEAL TIME (Hours)	J_{QNO} (mA/cm^2)	J_{SCO} (mA/cm^2)	n-Factor	I_{sc} (mA)	V_{oc} (mV)	FF (%)
POLYCRYSTALLINE							
31A - 3	0	2.0×10^{-8}	5.2×10^{-4}	2.0	83	517	72.2
31B - 4	1	2.7×10^{-8}	2.8×10^{-4}	1.9	78	510	73.5
31C - 1	5	1.3×10^{-8}	1.2×10^{-3}	2.3	96	535	72.5
31D - 2	25	2.6×10^{-8}	1.7×10^{-3}	2.2	90	515	69.5
36A - 3	0	2.0×10^{-8}	6.6×10^{-4}	2.0	82	517	73.3
36B - 4	1	3.8×10^{-8}	5.5×10^{-4}	2.0	77	502	71.6
36C - 1	5	1.2×10^{-8}	3.3×10^{-4}	1.9	101	533	70.8
36D - 2	25	2.0×10^{-8}	6.0×10^{-4}	2.0	91	515	69.9
SINGLE-CRYSTAL							
3 - 0 - 4	0	2.1×10^{-9}	8.8×10^{-4}	2.5	108	592	74.6
3 - 1 - 4	1	5.4×10^{-9}	6.3×10^{-5}	2.2	101	571	79.1
3 - 5 - 3	5	11.0×10^{-9}	2.8×10^{-4}	2.7	98	554	79.3
3 -25 - 4	25	7.8×10^{-9}	4.4×10^{-3}	3.0	101	556	74.7

neutral recombination current, perhaps due to a factor of five decrease in minority-carrier diffusion length, will theoretically result in a 42 mV loss of open-circuit voltage and some loss in short-circuit current. This type of behavior was observed; both the open-circuit voltage and short-circuit current decreased after heat-treatment for 5 hours. The quasi-neutral recombination current increased by about a factor of five, the open-circuit voltage decreased by about 38 mV, and the short-circuit current decreased by about 10 mA.

The improvements in the polycrystalline samples may also be due to annealing of damage introduced by the sandblasting operation, particularly since the short-circuit current of the non-heat-treated cells appear to be very low when compared to that more typically obtained with this polycrystalline material. Therefore, an additional experiment was begun to investigate the effect of various sandblasting agents.

Four additional 10cm x 10cm polycrystalline silicon wafers, from the same section of Semix brick C4-87E, were quartered and thinned using a CP-type etch to a nominal thickness of 275 microns. One quarter (A) was not sandblasted; one quarter (B) was sandblasted in the previous manner on the back side only with 320 mesh aluminum oxide (Al_2O_3) powder; a third quarter (C) was sandblasted with 320 mesh silicon dioxide (SiO_2) powder; and the fourth quarter (D) was sandblasted using glass beads. Each

quarter was paired with a 5cm x 5cm single-crystal wafer of the same thickness and back-side damaged with the same material. The surface finish of the wafers sandblasted with the glass beads was much smoother than the surfaces of the wafers damaged with either aluminum oxide or silicon dioxide powders, which were very rough. Solar cells were fabricated from these back-side damaged wafers using a high efficiency process [1]. A summary of the results is shown in Table 14.

Wafers 30 and 37 can be used to compare Al_2O_3 and glass bead sandblasting to undamaged wafers. There is no substantial difference. The B quarters (Al_2O_3) are slightly worse than the controls (non-damaged A quarter), and the D quarters (glass beads) are slightly better than the controls. More significantly, the short-circuit current, open-circuit voltage, and peak-power of the cells fabricated from the undamaged wafers are very low, which confirms that the material used in this series of experiments has a very short minority-carrier diffusion length.

Wafers 38 and 40 show the difference between Al_2O_3, SiO_2, and glass beads as the sandblasting agent. The performance of the cells damaged with Al_2O_3 and SiO_2 is similar, which indicates that there is no degradation mechanism associated with contamination by Al_2O_3. The quarter damaged with glass beads is better than the others in both cases. This may be due to the

Table 14. Illuminated I-V characteristics of back-side damaged, $4cm^2$ solar cells. No heat-treatment or AR-coating. Measured at AMO, 135 mW/cm^2, 25^oC.

WAFER/QTR	N (Cells)	I_{sc} (mA)	V_{oc} (mV)	P_p (mW)	FF (%)
POLYCRYSTALLINE					
30 / A	4	74 ± 2	522 ± 4	28.6 ± 1.0	73.4 ± 0.3
B	4	68 ± 2	511 ± 5	26.2 ± 0.7	74.6 ± 0.6
C	-				
D	4	78 ± 1	529 ± 3	30.7 ± 0.6	73.8 ± 0.3
37 / A	4	72 ± 2	519 ± 6	27.7 ± 1.7	73.2 ± 1.3
B	4	67 ± 1	509 ± 2	25.6 ± 0.3	74.9 ± 0.4
C	-				
D	4	74 ± 1	526 ± 2	29.4 ± 0.4	74.7 ± 0.2
38 / A	-				
B	3	83 ± 2	537 ± 6	33.4 ± 1.8	74.9 ± 0.9
C	4	84 ± 6	537 ± 11	34.2 ± 3.0	75.7 ± 0.9
D	3	94 ± 1	558 ± 2	39.8 ± 0.9	75.7 ± 0.0
40 / A	-				
B	4	79 ± 2	529 ± 3	31.3 ± 0.6	74.5 ± 0.9
C	1	74	520	28.6	74.3
D	4	94 ± 2	558 ± 2	39.7 ± 0.8	75.7 ± 0.3
SINGLE-CRYSTAL					
A	12	116 (1)	600 (2)	54.4 (0.7)	78.2 (0.9)
B	12	115 (1)	596 (7)	53.8 (1.2)	78.4 (1.8)
C	12	115 (1)	596 (9)	52.9 (3.1)	76.6 (3.6)
D	8	116 (1)	596 (6)	52.2 (3.0)	75.0 (3.4)

Quarter A - no damage
Quarter B - damaged with 320 mesh Al_2O_3 powder
Quarter C - damaged with 320 mesh SiO_2 powder
Quarter D - damaged with glass beads.

texture of the damaged surface which was very rough for Al_2O_3 and SiO_2, but smooth for glass beads.

Damage to the single-crystal cells apparently results in no impact on short-circuit current, a slight decrease in open-circuit voltage, and an increase in open-circuit voltage scatter. With single-crystal silicon, damaging the back-side by sandblasting degrades the overall performance due to lower open-circuit voltage, but it does not appear to matter what material - Al_2O_3, SiO_2 or glass beads - is used to cause the damage.

As a result of this second experiment, it appears that the minority-carrier diffusion length in low lifetime polycrystalline silicon can indeed be increased somewhat by a damage-gettering heat-treatment. However, the improvement in the diffusion length, by about a factor of two for the particular conditions and materials in these experiments, was insufficient to achieve the open-circuit voltages and short-circuit current densities that were obtained with un-treated polycrystalline silicon earlier in this program. In addition, heat-treament for an extended period degrades, rather than continues to improve, the minority-carrier diffusion length. This behavior, lifetime degradation at high temperature, is identical to that observed in single-crystal Czochralski silicon.

The open-circuit voltage of about 1 out of 10 non-shunted mini-cells is degraded by excess space-charge recombination current. These areas of high space-charge recombination appear to be less than $0.2cm^2$ and isolated, since these low open-circuit voltage mini-cells are usually surrounded by cells whose space-charge recombination current is several orders of magnitude lower. The majority of non-shunted mini-cells have less than 10 mV of open-circuit voltage loss due to excess space-charge recombination. This means that only a very small improvement in performance will be realized by eliminating space-charge recombination, particularly by grain boundaries, without first reducing the quasi-neutral recombination.

Several mini-cell wafers that had, on average, lower values of open-circuit voltage, a greater degree of scatter in both open-circuit voltage and fill-factor, and significantly greater values of shunt conductance were found to contain many inclusions. Therefore, the scatter in the open-circuit voltage and fill-factor of presently-fabricated cast polycrystalline solar cells is due, to some extent, to inclusions, which act as resistive shunts. However, this defect is not intrinsic, since several other polycrystalline wafers show no indication of excessive shunt conductance or inclusions.

IV. CONCLUSIONS

The performance of large-grain polycrystalline silicon solar cells is limited by essentially the same mechanisms limiting the performance of single-crystal Czochralski silicon solar cells. Namely, the short-circuit current is dominated by the base minority-carrier diffusion length; the open-circuit voltage is dominated by the base majority-carrier concentration (resistivity) as well as the minority-carrier diffusion length. The scatter in the open-circuit voltage measured across several polycrystalline wafers with few inclusions is about $\pm$ 15 mV; a factor of two decrease in quasi-neutral current (from doubling the minority-carrier diffusion length or the majority-carrier concentration) will theoretically yield an 18 mV increase in open-circuit voltage; this magnitude of quasi-neutral recombination current variation was observed. Since the resistivity across a wafer is fairly constant, the effective minority-carrier diffusion length must vary with position on a wafer. The cause of this variation in minority-carrier diffusion length and quasi-neutral recombination current, whether impurity or structurally-related, has not been identified. However, a significant improvement in polycrystalline silicon solar cell performance will be realized by eliminating, or at least reducing, the cause of this excess quasi-neutral recombination.

The open-circuit voltage of about 1 out of 10 non-shunted mini-cells is degraded by excess space-charge recombination current. These areas of high space-charge recombination appear to be less than $0.2cm^2$ and isolated, since these low open-circuit voltage mini-cells are usually surrounded by cells whose space-charge recombination current is several orders of magnitude lower. The majority of non-shunted mini-cells have less than 10 mV of open-circuit voltage loss due to excess space-charge recombination. This means that only a very small improvement in performance will be realized by eliminating space-charge recombination, particularly by grain boundaries, without first reducing the quasi-neutral recombination.

Several wafers whose mini-cells had, on average, lower values of open-circuit voltage, a greater degree of scatter in both open-circuit voltage and fill-factor, and significantly greater values of shunt conductance were found to contain many inclusions. Therefore, the scatter in the open-circuit voltage and fill-factor of presently-fabricated cast polycrystalline solar cells is due, to some extent, to inclusions, which act as resistive shunts. However, this defect is not intrinsic, since several other polycrystalline wafers show no indication of excessive shunt conductance or inclusions.

V. RECOMMENDATIONS

The major mechanism limiting the performance of currently-produced, cast polycrystalline silicon solar cells appears to be variation of the effective minority-carrier diffusion length, which results in localized variations in quasi-neutral recombination. This has a significant impact on solar cell efficiency by limiting the open-circuit voltage and peak power. A substantial improvement in performance may be realized by eliminating, or at least reducing, this excess recombination.

A damage gettering process was investigated for improving the bulk properties. However, while there was some improvement with this process, the effect of heat-treatment is mixed. For short anneal times, the cell performance improved as the bulk recombination decreased. However, additional high temperature heat-treatment increased, rather than continued to decrease, the bulk recombination. Therefore, the cell performance worsened.

If the excess quasi-neutral recombination is due to the presence of grain boundaries, then their impact may possibly be reduced by "passivating" the electrically active recombination sites. The most likely passivant is hydrogen in its atomic (ionic) form.

Very few mini-cells suffered from excess space-charge (junction) recombination. Therefore, processing schemes that seek to reduce or eliminate excess space-charge recombination will have a minimal impact when used with this material until the quasi-neutral recombination is reduced.

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ACKNOWLEDGEMENTS

The results reported here are mainly due to the efforts of K. Grimes and S. Roncin, who fabricated and tested literally thousands of cells. The author is indebted to them for their dedication and persistence. The thickness-resistivity matrix work was organized and begun by G. Johnson.

Throughout this contract, the guidance of J. Wohlgemuth was instrumental, and the author would especially like to thank him and the JPL technical monitor, P. Alexander, for their help and patience.

The author would also like to thank C. Wrigley, S. Johnson, and G. Storti for many helpful comments, and he is particularly grateful to P. Fazio for preparing all of the documentation.

The polycrystalline silicon wafers used for this work were kindly supplied by Semix, Inc. (now a part of Solarex).

DRL No. 156
DRD No.

APPENDIX 1:

A MODULE EXPERIMENTAL PROCESS SYSTEM DEVELOPMENT UNIT (MEPSDU)

Summary Technical Report

November 26, 1980 to February 23, 1982

BY: J. H. WOHLGEMUTH

Contract No. 955902

The JPL Low-Cost Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initial a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE.

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ABSTRACT

This is a Summary Technical Report for the MEPSDU Program. The purpose of the program was to demonstrate the technical readiness of a cost-effective process sequence for the fabrication of flat-plate photovoltaic modules. The initial plan called for Solarex to design, develop, fabricate and operate a Module Experimental Process System Development Unit (MEPSDU). Due to DOE budget cutbacks and change in emphasis of their programs the MEPSDU program was discontinued before completion. This report summarizes the technical accomplishments at the time the program was discontinued.

At the time of the stop work order the following had been accomplished:

1. Identification of a cost effective process sequence.

2. Laboratory verification of the cell process sequence.

3. Design of the equipment required for the cell process sequence.

4. Performance of an IPEG cost analysis of the process sequence.

This process sequence was based on four significant program developments:

1. Hot Spray TiO_x AR Coating.
2. Glass Bead Back Clean-Up.
3. Wave-Soldering for Front Contacts.
4. Ion Milling for Edging.

The preliminary cost analysis indicated that the 6.6 MW pilot line of this contract could achieve a cell add-on cost of $0.56 per peak watt. The selling cost of the cells from a full scale 50 MW line would be consistent with the DOE module cost goal of $0.70 per peak watt.

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1.0 INTRODUCTION

The purpose of the MEPSDU program was to demonstrate the technical readiness of a cost-effective process sequence that has the potential to produce flat-plate photovoltaic modules which meet the 1986 price goal of less than $.70 per peak Watt. To achieve this goal, Solarex was to design, develop and fabricate a Module Experimental Process System Development Unit (MEPSDU) and to utilize the unit to produce a quantity of modules using the proposed process sequence. This effort was to include:

1. Design of a detailed cost effective process sequence.

2. Completion of a detail design of the MEPSDU.

3. Fabrication and assembly of the MEPSDU.

4. Preparation of a process instruction manual, including in-line process control information.

5. Performance of a minimum of three technical demonstrations which will include the production of sufficient modules and production data to permit validation of the contract goal.

6. Performance of a cost analysis of the process sequence, including a study of the cost impact and changes required in the MEPSDU to allow the use of different types of input material.

Due to DOE budgetary cutbacks and change in emphasis of their efforts, the MEPSDU program was discontinued before completion. At the time of the stop work order (February 23, 1982) considerable progress had been made in the areas of:

1. Design of a detailed cost effective process sequence.

2. Completion of a detail design of the MEPSDU.

6. Performance of a cost analysis of the process sequence.

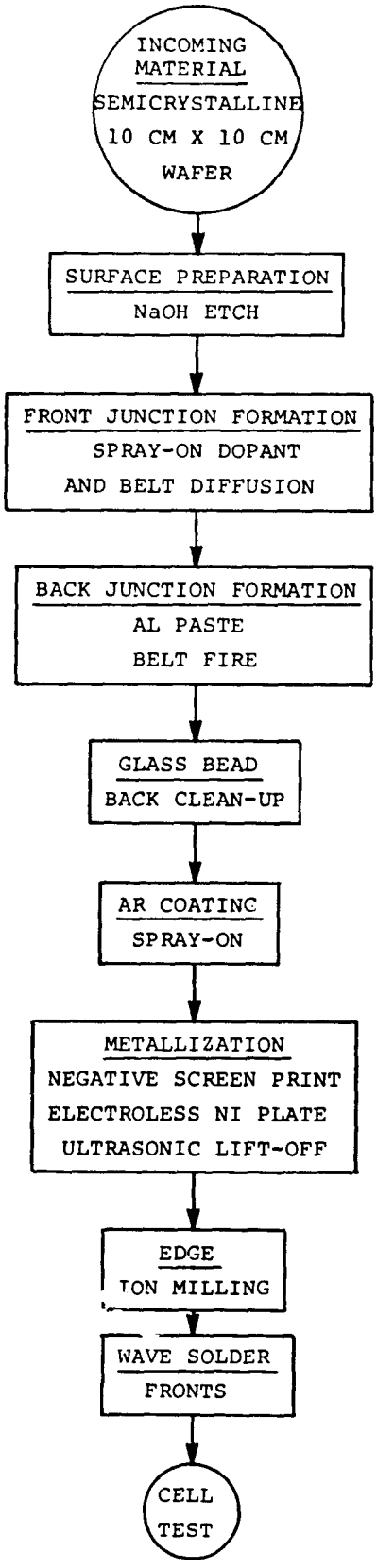
This report is to summarize the technical accomplishments of the MEPSDU effort and to present the preliminary cost analysis performed during the effort. The process sequence that was developed for the MEPSDU program is shown in Figure 1. This process sequence includes the following features:

- Semicrystalline silicon (10 cm x 10 cm) as the silicon input material.

- Spray-on dopant diffusion source.

FIGURE 1

GENERAL PROCESS DESCRIPTION (FINAL)



- Belt diffusion.
- Al paste BSF formation.
- Glass bead back clean-up.
- Spray-on AR coating.
- Electroless Ni plate-solder metallization.
- Edging - Ion Milling.

This process sequence evolved during the course of the program. The four most significant developments were:

1. AR Coating - A new technique involving the spraying of pure titanium isopropoxide onto heated wafers resulted in a significant improvement in AR coating uniformity especially for less smooth surfaces. This technique should be less expensive than previous spray methods because the use of solvents has been eliminated.

2. Glass Bead Back Clean-Up - The use of glass bead back clean-up not only eliminated the need for costly chemicals, but also allows the Al to serve as the prime current carrier on the back of the cell, saving

the cost of having to apply additional metal (such as solder) to provide for current collection.

3. Wave-Soldering - Using wave-soldering to apply the front pattern solder allows more control of the process, reduces the amount of solder utilized and makes the solder step more adaptable to automation.

4. Ion Milling - Stacking several hundred wafers and ion milling the edges promises to be a very useful edge isolation technique. Materials usage and breakage should be negligible and the need for elaborate diffusion masking or edge following is eliminated entirely.

A cost estimate has been completed for the 6.6 MW per year automated MEPSDU cell pilot line. Module costs were not included because effort in this area was halted in September, 1981 due to preliminary budget cutbacks. There was no attempt to estimate wafer cost because this effort is the subject of numerous other programs. This cost analysis led to a projected cell add-on cost of $0.56 per peak watt. The full scale 50 MW per year production line analysis was not completed before termination of that effort. However the pilot line cost add-on for a near term technology indicates significant improvement over present processes, with a high likelihood of being able to

achieve the final goal of $0.70 per peak watt module cost.

Section 2.0 presents the preliminary process sequence and the reasoning behind its selection. It also includes a discussion of developments during the program and how they led to the present process sequence. Section 3.0 describes the experiments conducted during the program. Section 4.0 describes the equipment requirements for the MEPSDU pilot line. Section 5.0 gives the details of the Cost Analysis. Finally Section 6.0 contains conclusions and recommendations concerning the technology developed during this program.

2.0 PROCESS DESCRIPTION

2.1 Preliminary Process Sequence

The preliminary process sequence as it was presented in the First Quarterly Report (1) is shown in Figure 2.

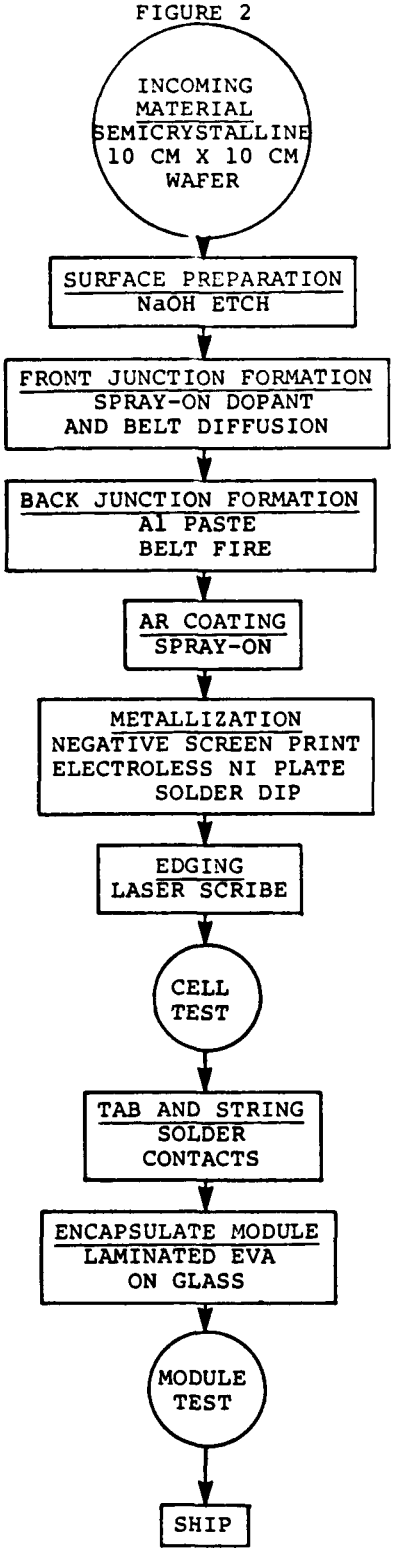
In selecting this process sequence, we emphasized the following considerations:

- Economics.
- Status of verification.
- Availability of equipment for automation.
- Ease of integrating individual processes.
- Compatibility with the selected input material and a variety of other alternative silicon sheet materials.

A preliminary cost analysis was performed resulting in an estimated module price of $0.691 per peak Watt in 1980 dollars, within the goal of the program.

PRELIMINARY PROCESS DESCRIPTION

FIGURE 2



This preliminary process sequence was made up of process steps that had each been verified separately. This process sequence had not been verified as a unified process using the starting material proposed. The initial program efforts were to verify the process sequence utilizing semicrystalline silicon. During this phase it was discovered that several steps were not compatible with the general process sequence and module design. In addition several new technologies were investigated that led to significant improvements in performance and/or cost. This led to changes in the sequence reflected in the following discussions.

2.2 Incoming Material

Semicrystalline 10 cm x 10 cm wafers were chosen as the input material for our MEPSDU because:

- The material is available for use now.
- It is closely related to other advanced sheet materials presently in the development stage.
- Analyses indicate that it can be produced for a cost within the $.70/Watt goal. Wafer costs as low as 30.6¢/Watt have been calculated (2).

- Solarex has sufficient experience with the processing of this material to understand its behavior through the various process steps.

The semicrystalline wafers are p-type silicon with a resistivity between 0.5 and 10 Ω-cm. The wafers will have a thickness varying from .012 in. to 0.016 cm. The corners are cropped to reduce breakage and allow for improved automatic handling.

2.3 Detailed Module Design

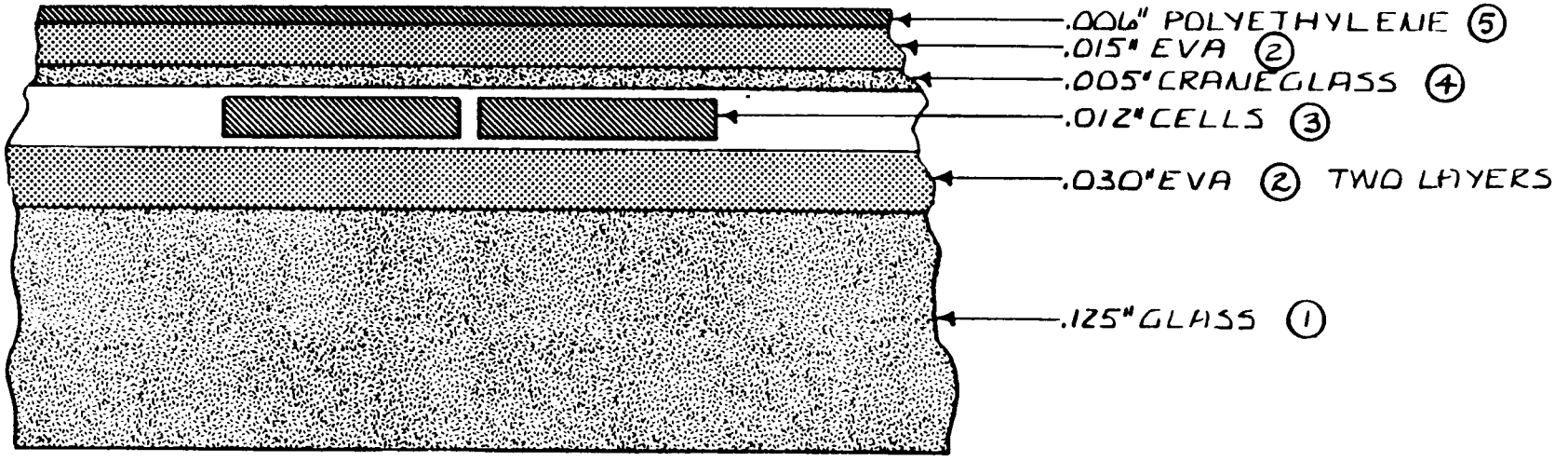
The module cross-section is shown in Figure 3. The components are described below.

A glass superstrate was selected because it:

- Filters out UV.
- Withstands oxidants, stains, etc.
- Withstands the effects of rain, wind and hail.
- Is readily cleanable.
- Serves as both a protective cover and structural support.

FIGURE 3

MODULE CROSS SECTION



NOTE:
TOTAL THICKNESS BEFORE LAMINATION .193"

SECTION A-A

- Is utilized extensively in the photovoltaic industry.

- Is compatible with the process and the other materials in the module.

We considered a variety of glasses, including tempered and annealed, 1/8 in. and 3/16 in. thick and a variety of iron contents: Sunadex (0.01% Fe), Solatex (0.05% Fe) and soda lime (0.2% Fe). A cost analysis indicated that for low cost modules (less than $2.00 per watt) soda lime glass is more economic than tempered low iron glass. However questions concerning the mechanical strength of the soda lime glass lead to our selection of 1/8 in. thick tempered glass as our baseline.

Ethylene vinyl acetate (EVA) was chosen as the encapsulant. Its main advantages are its low cost and ease of use in the lamination process. EVA has the following required properties:

- It does not degrade under UV exposure when protected by glass and the appropriate additives.

- It can withstand the necessary thermal cycling conditions.

- It can mechanically protect the solar cells.

- It and its processing are compatible with the other materials in the module.

- It is utilized by a number of PV manufacturers.

- Its behavior and environmental stability have been well characterized (3).

We used two sheets of 0.018 in. thick EVA between the glass and the cells and one sheet of 0.018 in. thick EVA behind the cells.

Craneglass was included in the module because it:

- Aids in the removal of bubbles during lamination.

- Improves the electrical insolation of the module.

- Lessens cell movement during lamination.

- Results in a smoother module back.

The very low cost of the Craneglass makes its use feasible wherever needed.

Linear low density polyethylene film was recommended as the vapor barrier because it:

- Has a low value of permeabilty to water vapor.
- Is tough and puncture resistant.
- Has demonstrated a long lifetime in outdoor applications (up to 30 years).
- Has sufficient dielectric strength to meet all codes.
- Is compatible with the processes and other materials.
- Has a very low cost.

A 0.006 in. thick black polyethylene film made with minimum memory was utilized.

The electrical output of the module was accomplished by use of a solarlok connector designed specifically for photovoltaic modules. The ease of installation, the ease of module interconnection in the field, and the low cost make this connector ideal for the MEPSDU module.

Rather than providing the module with a frame, we sealed and protected the edge of the module with a gasket. The gasket can save the cost of the integral frame and can be attached in the field as cost effectively as a hard frame.

The module utilizes seventy two 10 cm x 10 cm semicrystalline cells. Their electrical configuration is two cells in parallel with thirty six in series. The module is approximately 67.5 cm x 126.5 cm or 26.6 in. x 49.6 in. This size is large enough for economic production but small enough to be handled both in production and during installation.

The preliminary module design called for using six series strings of twelve cells each running along the four foot dimension of the module as shown in Figure 4. In this design the incorporation of internal bypass diodes could only be accomplished by running wires the length of the module. The additional cost and danger of shunting to these diode wires led to a redesign of the module lay-out. The new design is shown in Figure 5. The cells are now connected in six cell series strings along the two foot length. The diode tabs now span the short region between bus bars.

The electrical schematic of the module is shown in Figure 6. A complete drawing package was prepared for this module.

2.4 Detailed Process Descriptions

The following subsections describe each process step in detail including a description of the process, rationale for its selection, recommended changes in the process and the reason for such recommendations.

FIGURE 4

PRELIMINARY MODULE LAY-OUT

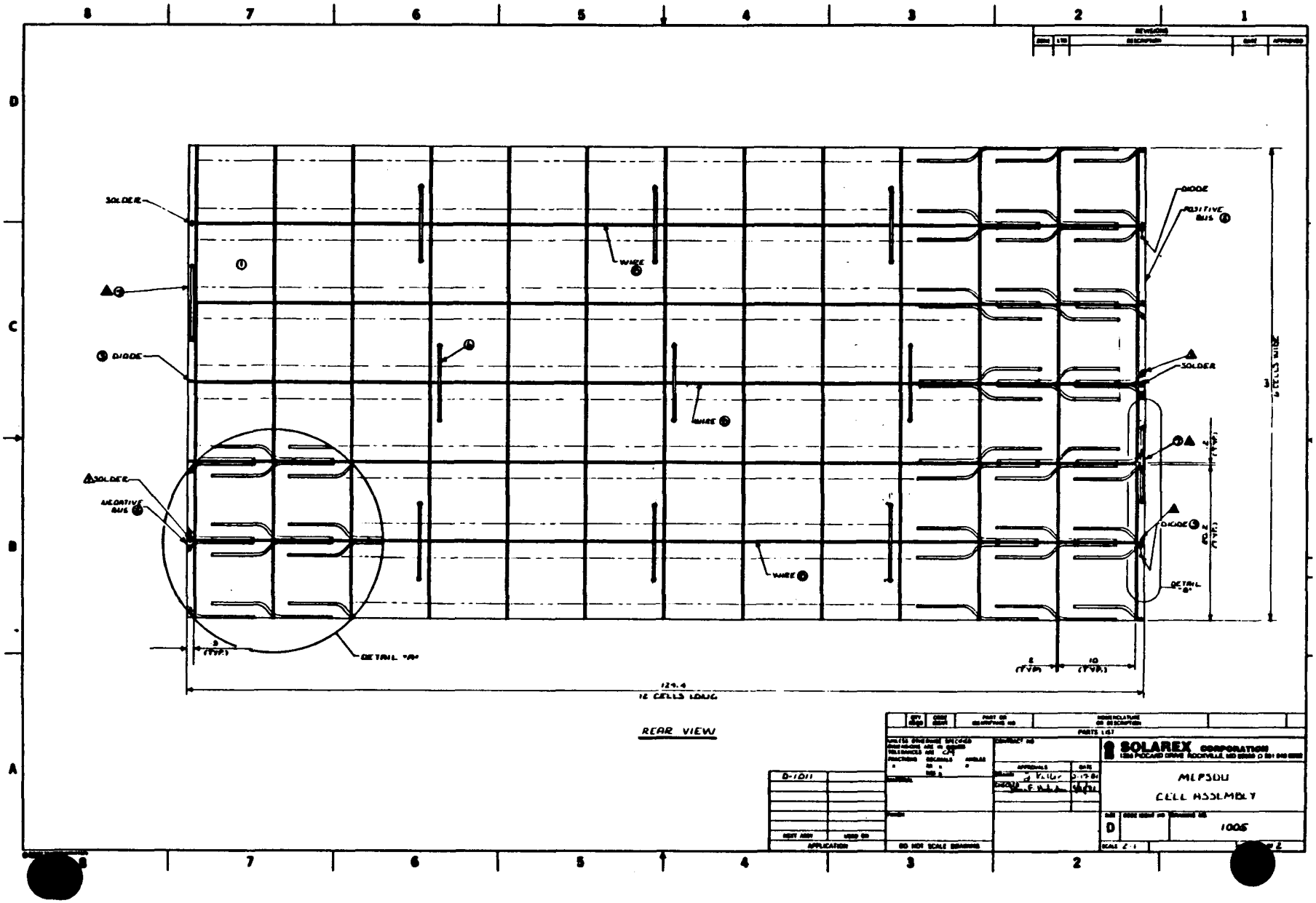


FIGURE 5

MEPSDU CELL ASSEMBLY

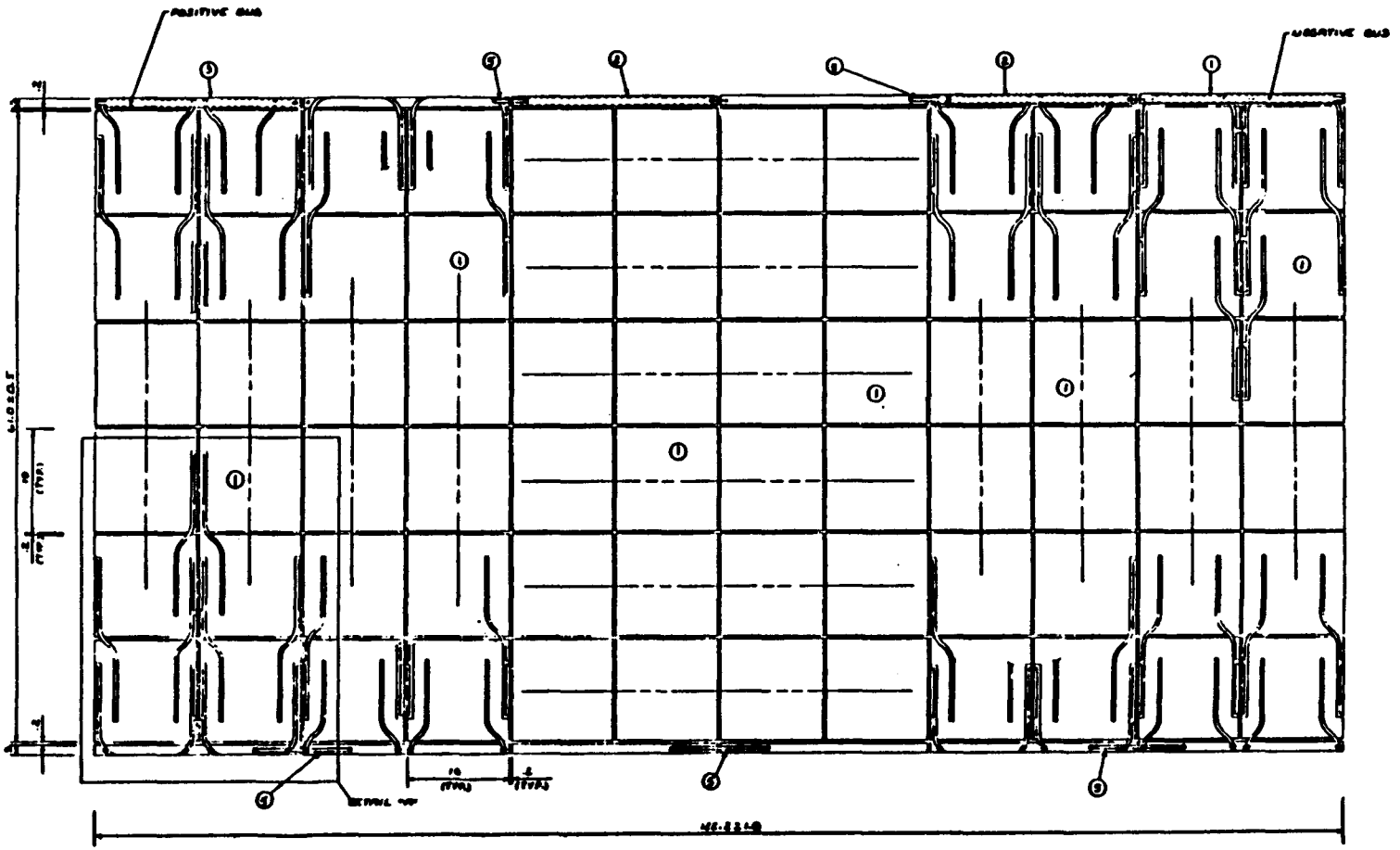
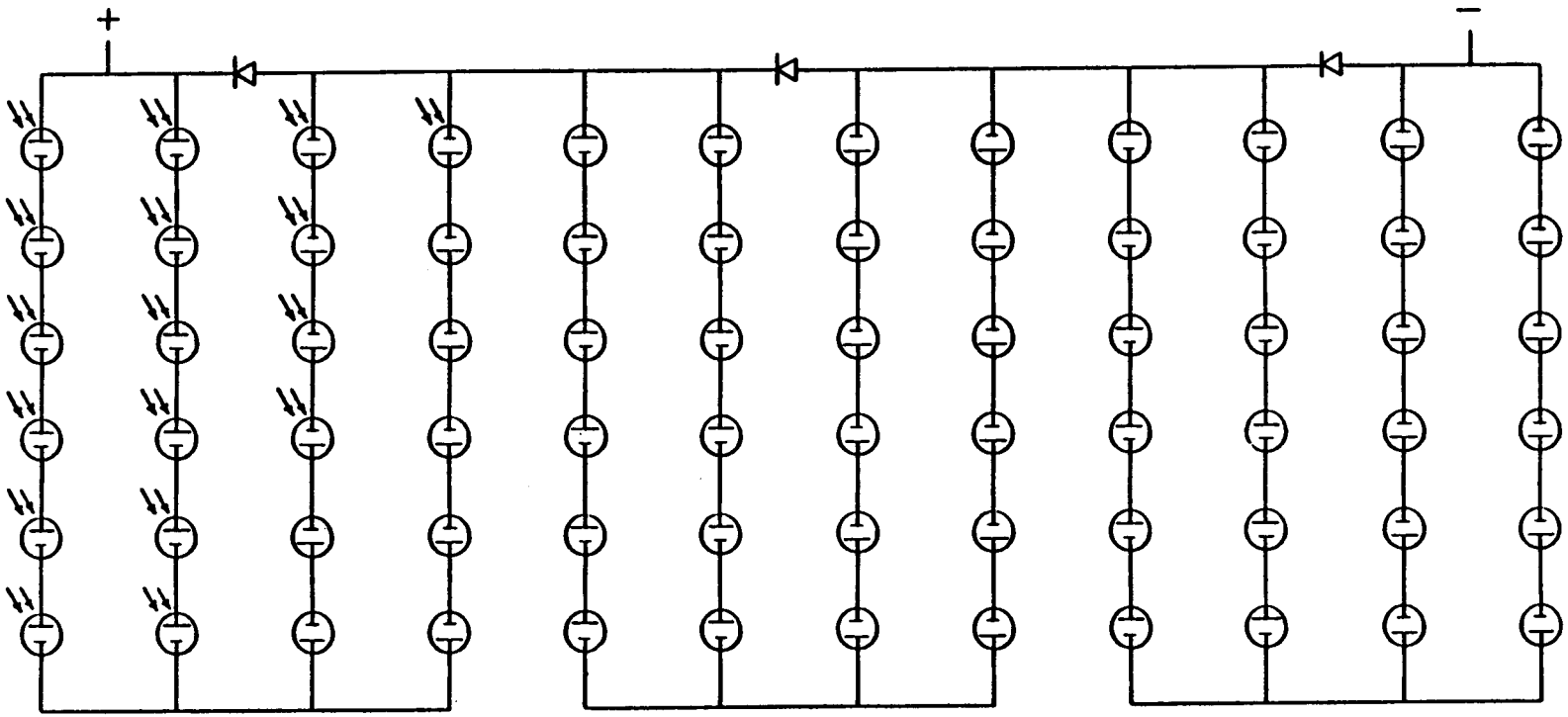


FIGURE 6

MEPSDU ELECTRICAL SCHEMATIC



2.4.1 Surface Preparation

Work damage is removed from the wafers by etching in a solution of sodium hydroxide. Texturing and grain boundary steps can be minimized by using a high concentration (30% by weight NaOH in water), high temperature (120°C) and short etch times (approximately two minutes). Due to high activity of the etch, a precleaning step is not necessary.

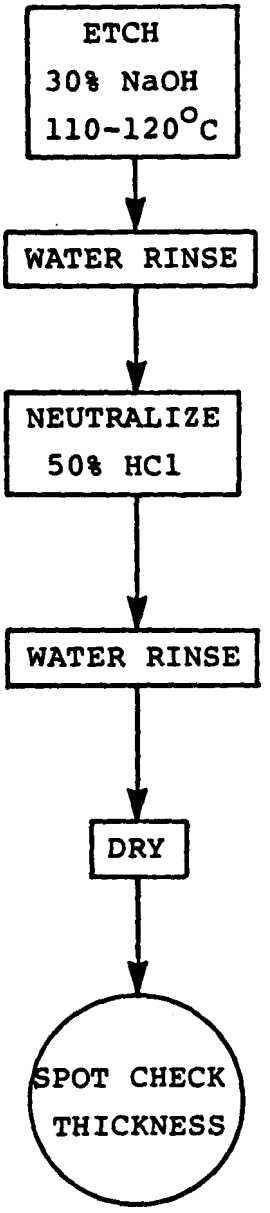
The process sequence for surface preparation is shown in Figure 7. After the etch itself, the wafers are rinsed in water, neutralized with hydrochlorine acid ($HCl:H_2O$), 1:1), rinsed in deionized water and dried.

Sodium hydroxide etching was chosen mainly on the basis of economy. The alternates investigated were:

- Acid etching, which has too high a materials cost, and
- Plasma etching, which has too high a capital equipment cost.

FIGURE 7

SURFACE PREPARATION



Sodium hydroxide etching is utilized extensively in production at Solarex. In addition, it has been verified by a number of contractors, including Solarex (4), Sensor Technology (5) and Lockheed (6).

No changes were made in this process sequence during the program. Care must be made that all work damage is removed without overtexturizing the surface. Additionally equipment design must take into account the violent reaction occurring during the etch.

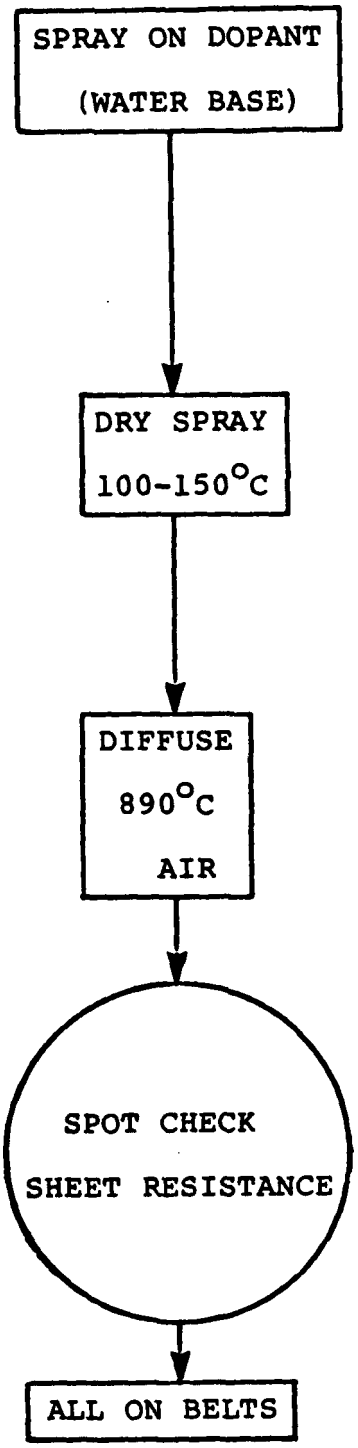
2.4.2 Front Junction Formation

A water base solution (phophorosilica film), available commercially from Emulsitone Corporation, has been formulated specially for spray-on application in the processing of solar cells. The process sequence is shown in Figure 8. Once the wafers are sprayed, they are dried at a low temperature (100-150^{o}C) for about twelve minutes. Diffusion is performed in a belt furnace at 890^{o}C for ten minutes in an air ambient, resulting in a sheet resistance of approximately 40 Ω /$\square$.

Spin-on and spray-on diffusion has been verified respectively by Spectrolab (7), Sensor Technology (8)

FIGURE 8

FRONT JUNCTION
FORMATION



and the manufacturer. The resultant diffusion oxides are readily removed as long as the diffusion is performed in the presence of oxygen. Belt diffusion has been verified by Solarex (9) and is used on a daily basis at Solarex.

The alternative front junction processes studied were:

- Gaseous diffusion, which is somewhat more expensive and requires extensive equipment clean-up without any performance advantages.

- Ion implantation, which requires expensive equipment without any performance advantages.

Spray doping worked well at times resulting in cells equivalent to gaseous diffused cells (1,10), as described in Section 3. However this material appears to have a short and inconsistent shelf life.

The shelf life problem manifests itself in the reduced ability of the dopant to wet the surface of the wafers. At that time the material begins to smell of acetic acid. A proposed hypothesis for this degeneration is an attack by the phosphoric acid on

the acetate groups which remain on the polyvinylalcohol from its original manufacture by hydrolysis (typically incomplete) of polyvinyl acetate. This attack of the acetate groups would produce acetic acid with its characteristic smell and a change in the wetting characteristics of the polymer.

The dopant material is clearly not ready for utilization in full scale production. Because of the advantages of this process and the lack of any low cost alternative we retained spray-on doping in the final process sequence, with the understanding that either a more stable material must be developed or the dopant must be prepared on site as needed.

2.4.3 Back Junction Formation

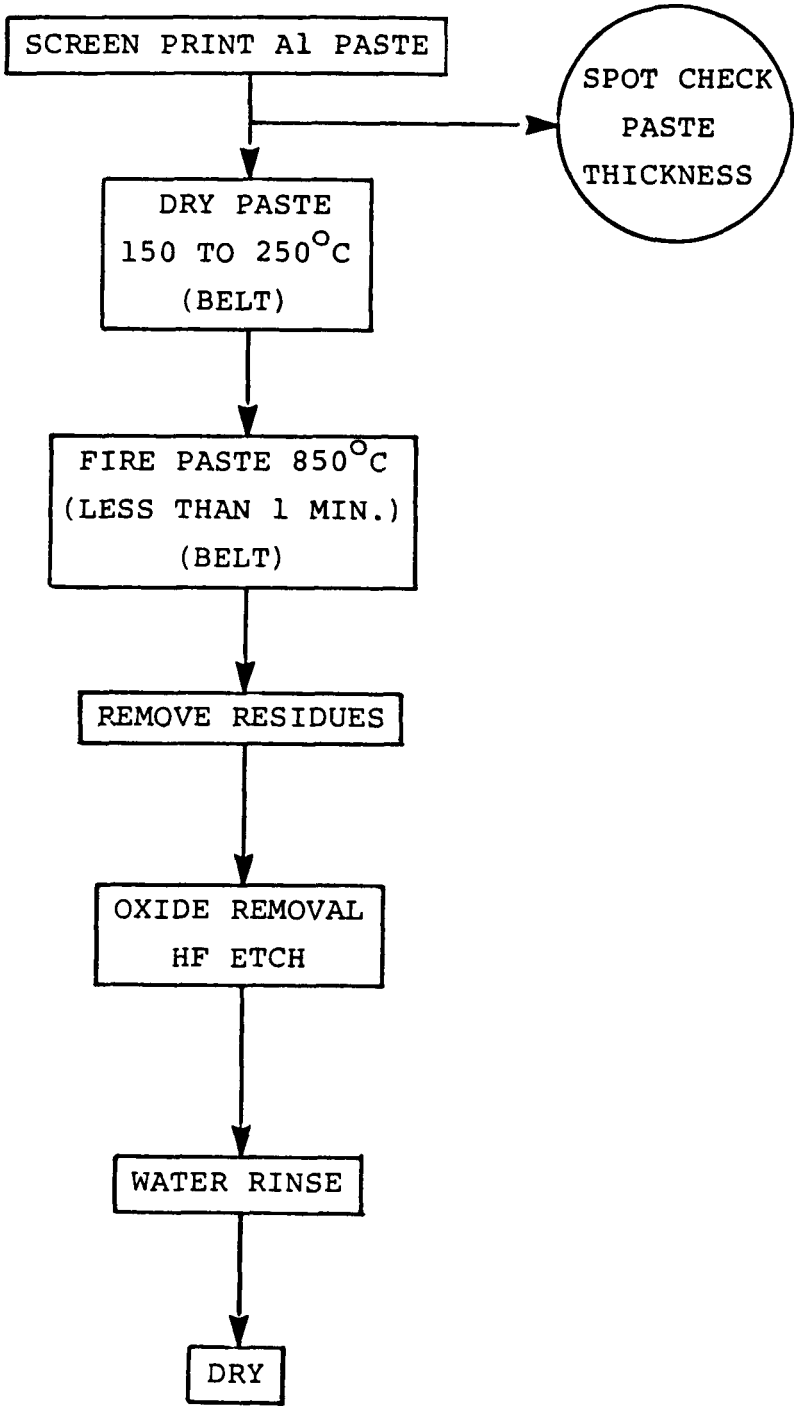
We elected to utilize screen-printed aluminum paste for BSF formation. Figure 9 shows the preliminary process sequence. A layer of Englehard A3484 aluminum paste is screened onto the back of the wafer. The wafers are then transferred to a belt furnace where the paste is first dried at a low temperature (150 to 250^{o}C) and then fired at a high temperature (850^{o}C) for a short time (less than one minute).

FIGURE 9

PRELIMINARY

BACK JUNCTION

FORMATION



The Al paste BSF process was chosen because.

- It is consistent with the production of high-efficiency solar cells (11,12).

- It is tolerant of variations in the incoming silicon resistivity.

- The required equipment is available and is consistent with volume processing.

- It is utilized extensively in production at Solarex.

The preliminary back clean-up process utilized an etch in hot HCl to remove the unalloyed Al.

After back clean-up, the wafers are etched in aqueous HF to remove oxides from both sides of the wafer. Finally, the wafers are rinsed and dried.

While the Al BSF formation process itself is an efficient and economic process the HCl clean-up process had several disadvantages:

- Warm HCl (60°C) degrades rapidly meaning that you either continually replace HCl or perform the etch at a lower temperature where the reaction is much slower.

- The amount of HCl utilized adds a significant cost.

- Using the HCl etch means that all of the Al is taken off the cell although only the firing residue really must be removed.

An economic problem related to the back clean-up question was that of utilizing solder on both sides of the cell. The typical procedure would be to fire the Al paste, etch off all of the excess Al in HCl, Ni plate and then solder dip the whole back. The cost of covering the whole back of the cell with solder is estimated to be greater than $0.10 per 10 cm x 10 cm cell which is not consistent with the $0.70 per peak watt price goals. Any back metallization process must then provide for sufficient back conductivity without applying solder over the whole back of the cell.

During this program we developed a new process sequence utilizing glass bead clean-up of the Al paste

residue leaving the bulk of the conducting Al in place. This Al can then provide the needed back metallization conductivity without addition of more metal, i.e., solder. The backs will still be Ni plated to allow them to be interconnected by soldering. However, no additional solder need then be added to the backs. The final Back Junction Formation Process Sequence is shown in Figure 10.

One additional change in the clean-up process has been the substitution of a fumic HF etch to remove the diffusion oxide rather than the aqueous HF etch. The fumic HF step was more adaptable to automation and was easier to control to assure complete removal of diffusion oxides.

2.4.4 AR Coating and Grid Pattern Definition

We selected a spray-on technique for applying the AR coating. The preliminary process sequence is shown in Figure 11. The wafers are sprayed with a titanium isopropoxide solution consisting of (13,14):

8.3%	Titanium Isopropoxide
25%	Butyl Acetate
33%	2 Ethyl 1 Hexanol
33%	Isopropyl Alcohol

FIGURE 10

BACK JUNCTION
FORMATION

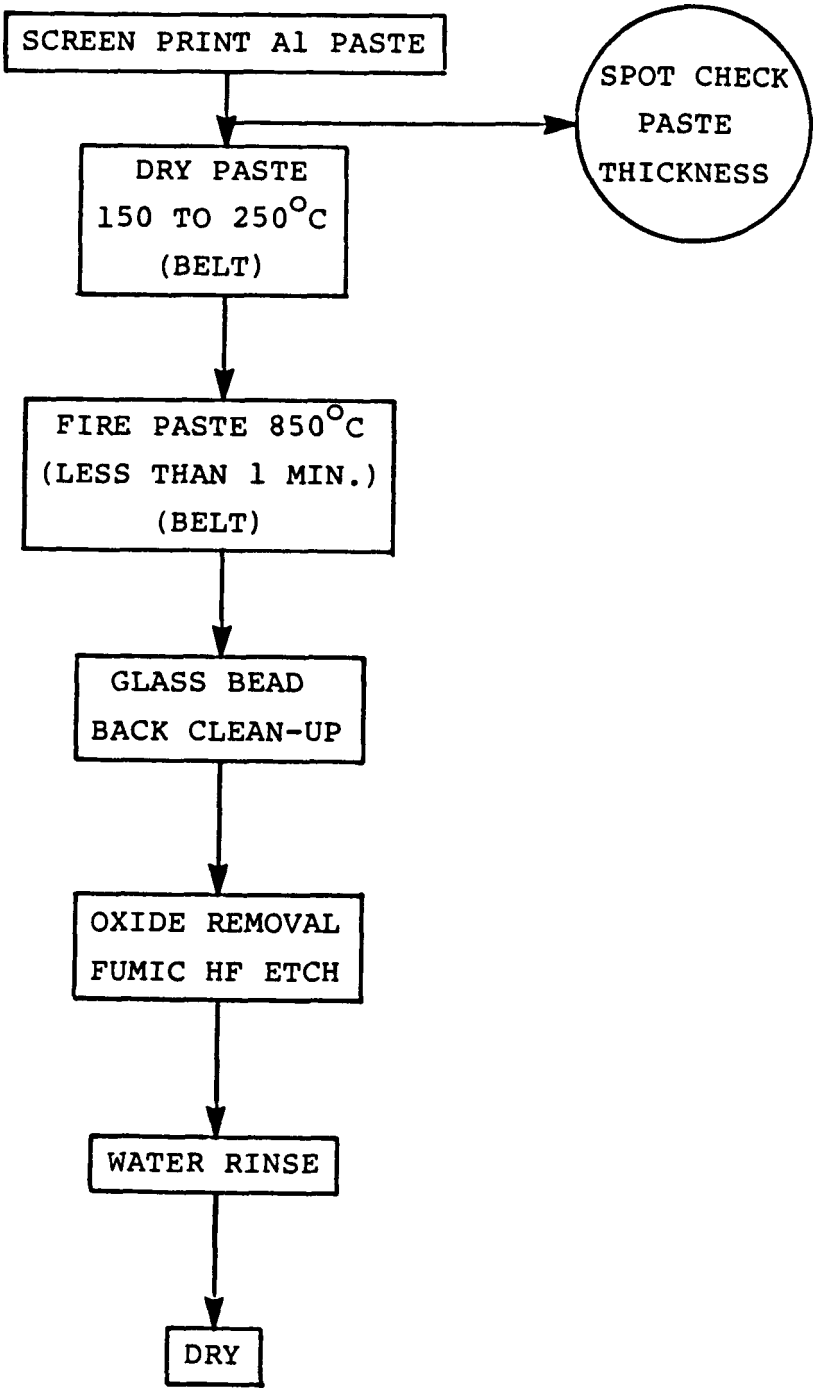
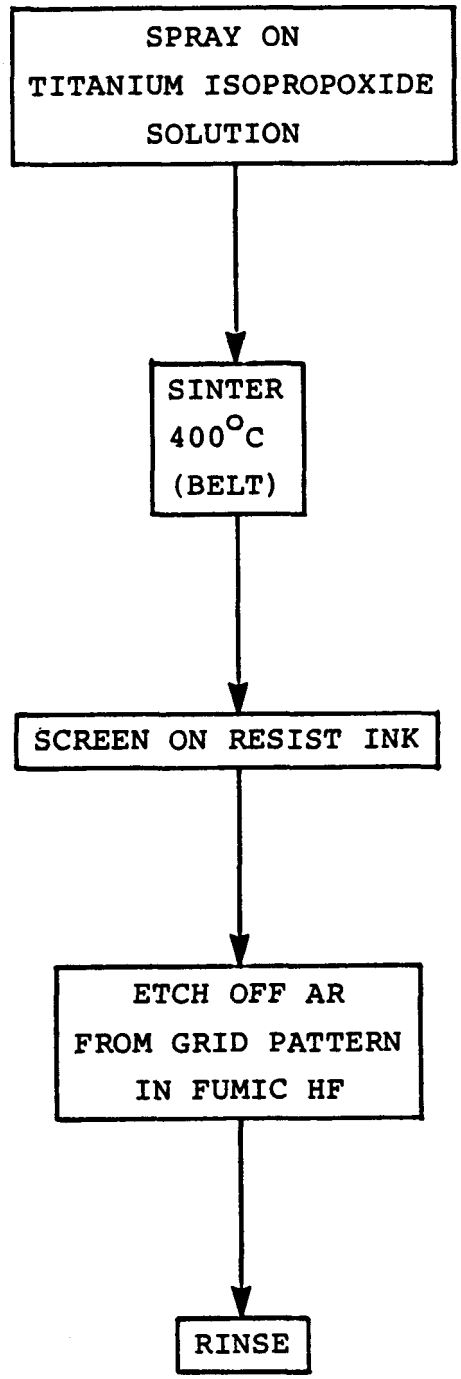


FIGURE 11

PRELIMINARY
AR COATING
AND
GRID PATTERN



The wafers are then transferred to a belt where the solution is dried at 125°C and then sintered at 450°C.

We elected to apply the AR coating before metallization because it simplifies the spraying process, protects the areas of the silicon surface that are not metallized, and can be sintered at high temperature without danger of metal penetration through the junction.

Other AR coating techniques evaluated were:

- Vacuum evaporation, which requires high capital equipment costs and has a low throughput
- Spin-on, which is not well suited to large square wafers
- Dipping, which is better suited for long, narrow cells, and
- CVD, which has high capital equipment costs and a low throughput.

This AR coating technique worked well for single crystal wafers, but the more textured semicrystalline wafers were not uniformly coated. Attempts at utilizing a prespray treatment were unsuccessful. However we found that spraying just the titanium isopropoxide onto heated wafers (400 to 410°C) resulted in extremely uniform AR coatings with an index of refraction of 2.1 to 2.2, as expected for TiO_x AR coatings. This led to the use of the revised process sequence shown in Figure 12. More details of the process procedure and verification of its results are given in Reference 15 and Section 3 of this report.

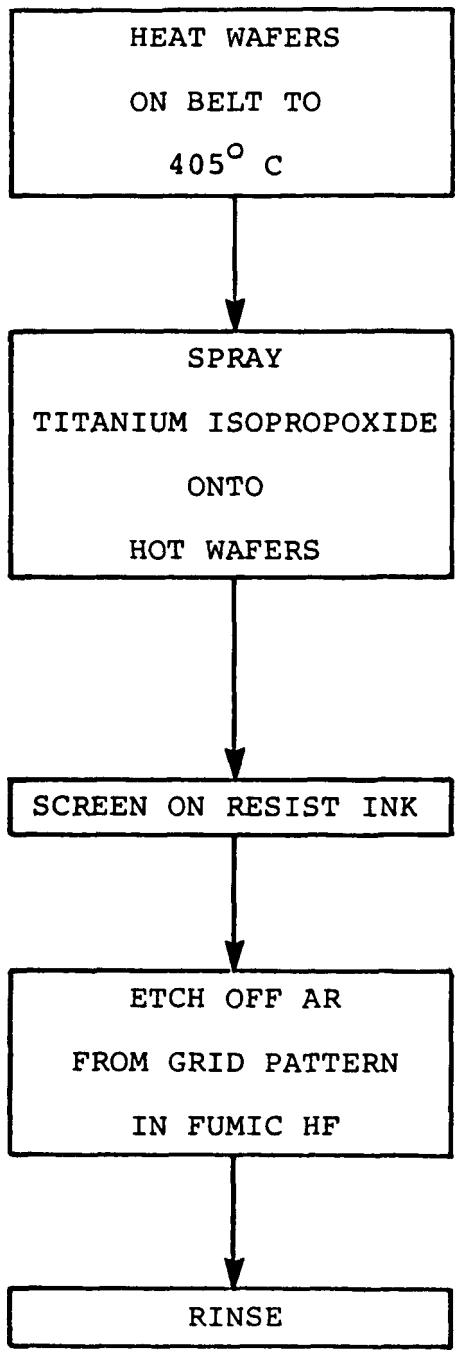
After AR coating the wafers have resist screened on the fronts, leaving the area to be metallized uncovered. The resist is cured per manufacturers specifications. The AR coating is then removed from the pattern by etching in the fumes created by fumic HF. Finally, the wafers are rinsed in deionized water.

Screen printing was chosen because it is compatible with electroless nickel plating and with the available equipment. It is one of the least expensive techniques available for placing a resist on a surface in a defined pattern. It has been utilized in solar cell manufacture for a number of years.

FIGURE 12

FINAL AR COATING

AND GRID PATTERN



2.4.5 Metallization

Metallization is the major cost driver in the cell process sequence. If one excludes the input silicon material cost then metallization accounts for more than 60% of the cell add-on cost in today's technology.

A number of alternate metallization techniques were considered, including:

- Screen-Printed Contacts - These systems suffer from high cost of materials (silver), lower conductivity of the screen-printed material and their limited thickness.

- Copper Plating - There is insufficient evidence that copper can withstand the environmental stresses.

- Aluminum - This system has not been verified and a cost effective deposition technique has not been identified.

- Electroless-Nickel with Solder Dipping - Electroless nickel is a low cost process as long

as complicated (and expensive) pretreatments are not required. Solder is not a particularly inexpensive material in terms of conductivity required, but if the solder is only placed where it is needed it can be a cost effective metallization technique.

Solarex has had extensive experience with electroless nickel-solder contact systems and has verified the process sequence and investigated its environmental stability (16). Based on this background we selected the electroless nickel-solder contact system shown in Figure 13. The cells go directly from the water rinse into the Halma electroless nickel plating bath for seven minutes. The cells are then rinsed and dried. The resist is removed from the cell by an organic solvent. The cells are then fluxed, soldered, rinsed and dried. In this initial process sequence it was clear that the cost goals could not be met if the soldering had to be done by individual dipping of cells and if solder coated the entire back of the cell. Both of these problems were alleviated by switching the back clean-up process to leave the excess Al and then only wave-soldering the fronts. The final metallization process sequence is shown in Figure 14.

FIGURE 13

INITIAL METALLIZATION

PROCESS SEQUENCE

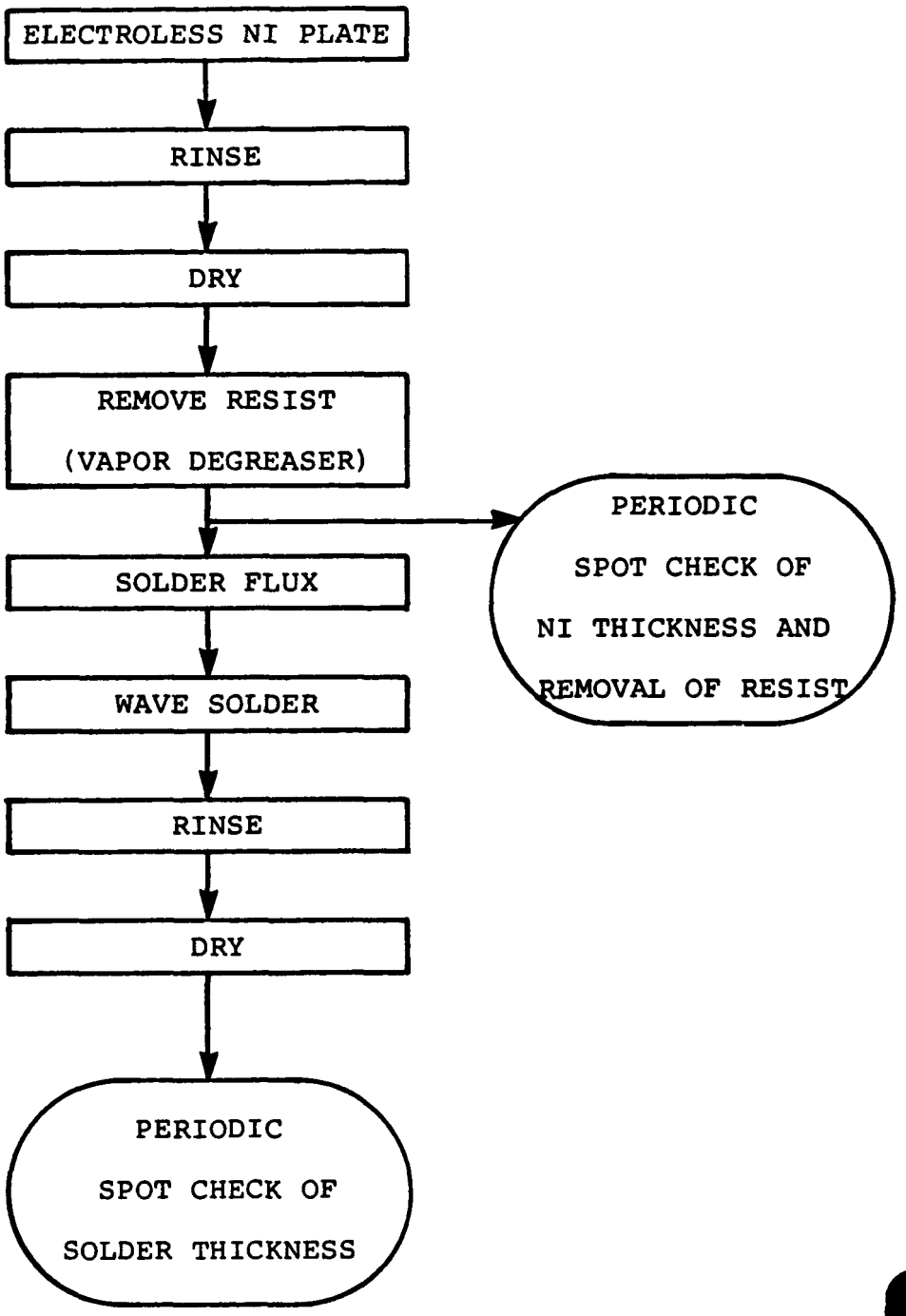
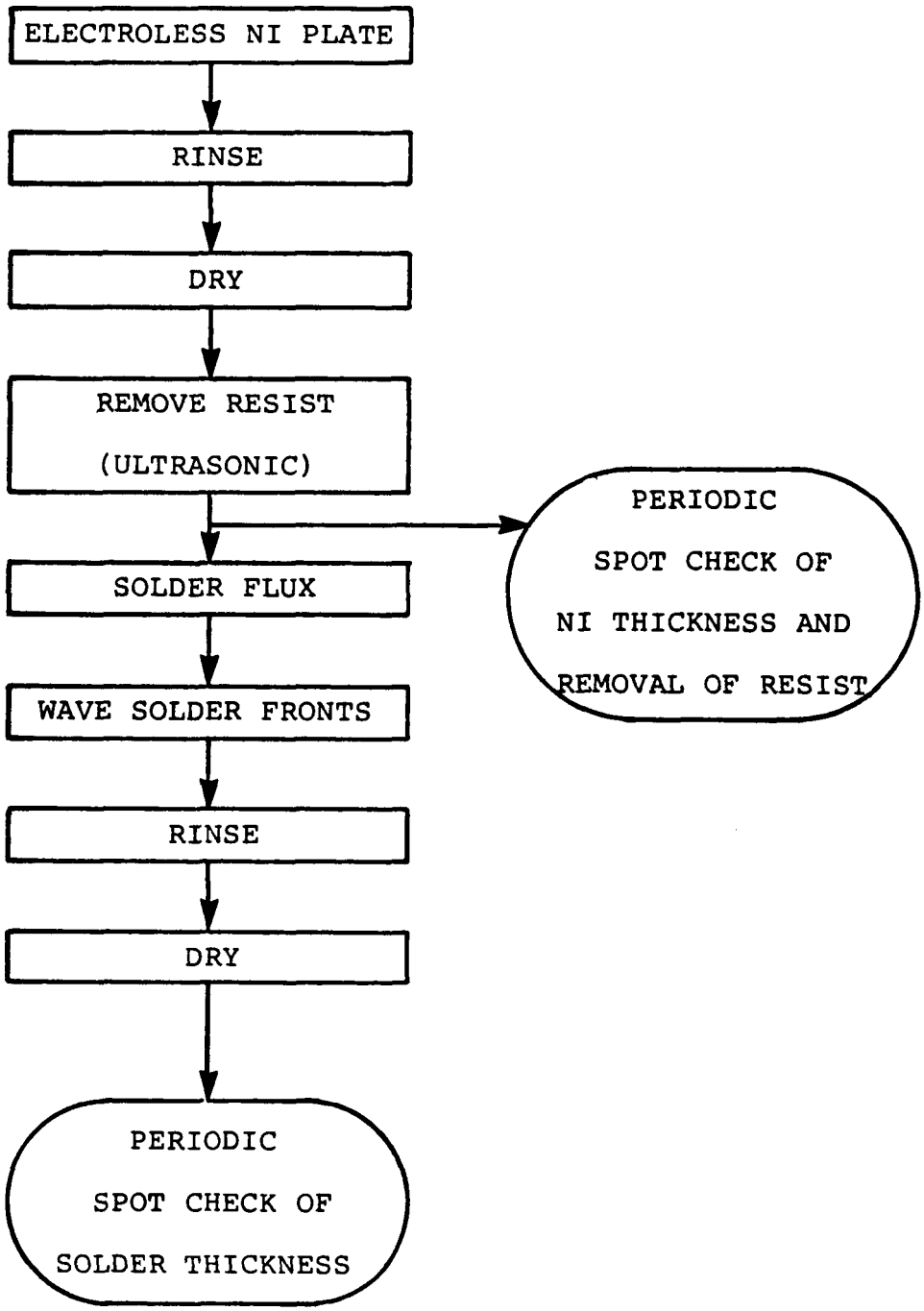


FIGURE 14

FINAL METALLIZATION

PROCESS SEQUENCE



2.4.6 Edging

Solarex originally elected to use a laser scribing system for edging. The cells are unloaded from cassettes, scribed and reloaded into cassettes. The scribed line width is about 0.001 in. with a depth penetration of 0.001 in. The distance between the edge and the laser scribe was to be a minimum of 0.010 in.

The original alternatives considered for edging were:

- Mechanical abrasion, which tends to produce damaged areas that serve as shunting paths or as sources for future breakage.

- Etching, which requires complicated and expensive masking of the junction.

Laser scribing had been verified by Sensor Technology (17) and had been used at Solarex. While the technology does work there were complications associated with our process sequence.

The standard negative screen printing technique we use results in a halo of metal at the edges of the cell. Laser scribing a halo on such a cell requires that the scribe line always be inside of the halo, resulting in significant loss of active cell area. In addition, there is a high likelihood that the front (n^+) interconnect can come in contact with this metallized halo. This would result in shorting of the cell, since this halo is electrically connected to the p^+ back of the cell.

Four alternative edging techniques were evaluated as described in Section 3.0. The results are given below:

1. Oxide Mask Edge - No economic material was identified that could meet all of the requirements.

2. Ion Milling - Preliminary experiments and the cost analysis were very encouraging.

3. Laser Scribe Through the Silicon - Shunting usually occurred.

4. Screen Print Resist Ink All the Way to the Edge - Contamination of the baseplate and screen indicated that this technique would not work.

The results of this work was the selection of ion milling as the preferred edging technique, although more experimental work is required to develop process specifications.

2.4.7 Tabbing and Stringing

Solarex proposed to use a tabbing and stringing machine to assemble the cell strings. The machine would use solder reflow bonding to connect the cells together. The interconnect material was solder plated copper ribbon. Originally the cells were to be fluxed in the areas to be soldered, but by changing the soldering technique we were able to eliminate this requirement.

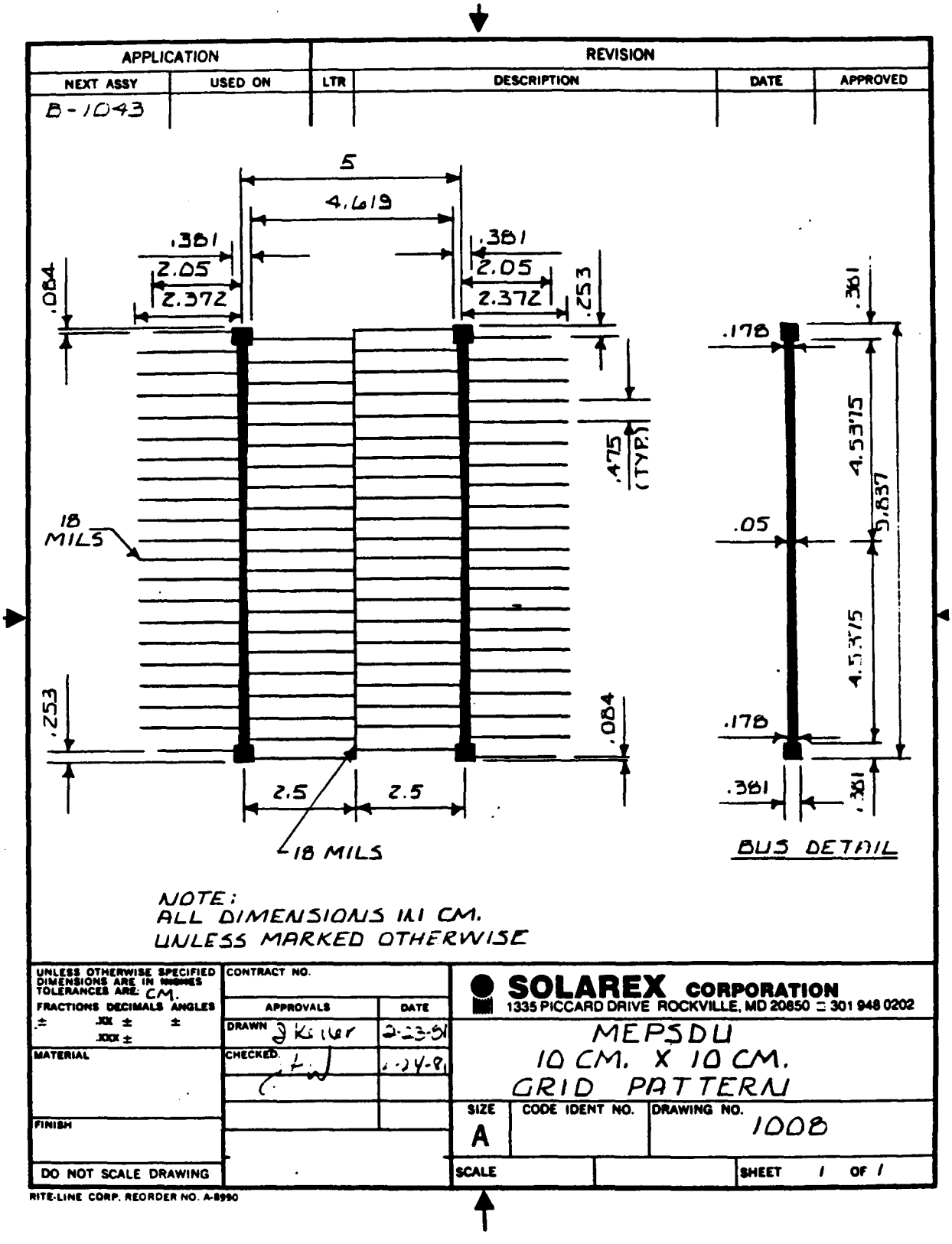
The initial module design called for standard over-under interconnection with only two pads per cell, both on one edge. This design has no crack tolerance, may have insufficient stress relief in the high density package, and results in lower cell efficiency because of the large travel distance required of carriers across the cell face. To improve the design, we elected to use a wraparound type of contact as utilized on our Block IV modules (18). For MEPSDU we elected to use four pads on every cell as

shown in Figure 15. Having four contacts on front and back provides good crack tolerance and means that each 10 cm x 10 cm cell acts like four 5 cm x 5 cm cells, resulting in higher efficiency. Having both wraparound and in plane stress relief improves the stress relief properties of the module. The design of the interconnects are shown in Figure 16. This one piece wraparound interconnect minimizes equipment complexity and cost, with material cost being well within the cost goals.

Of course the use of wraparound contacts requires insulating between the bottom of the cell and the wraparound piece. In Block IV this was accomplished by using insulated interconnects. However our cost analysis indicated that insulated interconnects were not consistent with the MEPSDU cost goals. The most economic technique was to apply an insulating polyester tape with acrylic adhesive in two strips to the back of the cell as shown in Figure 17.

The actual process sequence for tabbing and stringing cells depends on the machine designed to perform the function. Two machines have been fabricated to perform this function, one by Kuliche and Soffa Industries, Inc. (19) and the other by MB

FIGURE 15


APPLICATION
NEXT ASSY
USED ON
B-1043
REVISION
LTR
DESCRIPTION
DATE
APPROVED
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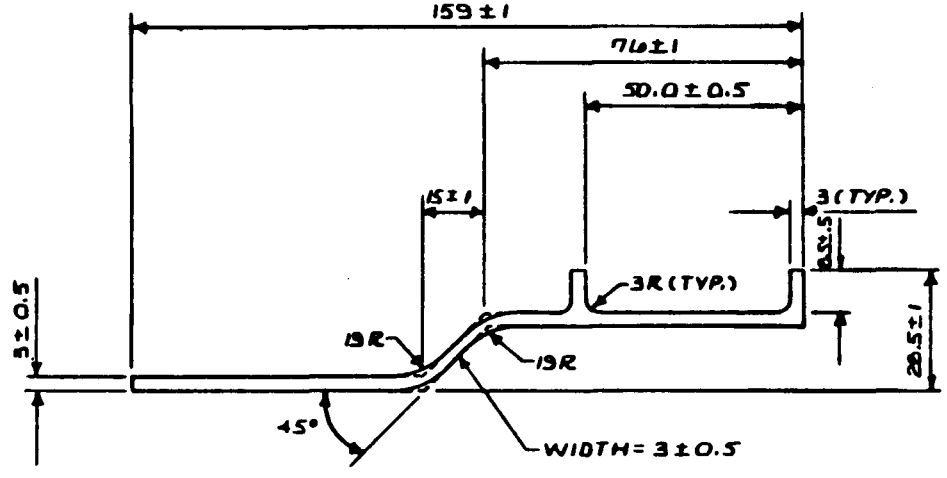
4.619
.381
2.05
2.372
.084
.253
.475 (TYP.)
18 MILS
2.5
2.5
18 MILS
.178
.05
4.5375
5.837
BUS DETAIL
NOTE:
ALL DIMENSIONS IN CM.
UNLESS MARKED OTHERWISE
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: CM.
FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
DO NOT SCALE DRAWING
CONTRACT NO.
APPROVALS
DATE
DRAWN J Keller 2-23-81
CHECKED 2-24-81
SOLAREX CORPORATION
1335 PICCARD DRIVE ROCKVILLE, MD 20850 = 301 948 0202
MEPSDU
10 CM. X 10 CM.
GRID PATTERN
SIZE A
CODE IDENT NO.
DRAWING NO. 1008
SCALE
SHEET 1 OF 1
RITE-LINE CORP. REORDER NO. A-8990

FIGURE 16

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ADDED 3R (TYP.) & NOTE	3/21/91	JFH
	B	GENERAL REVISION	4/29/91	JFH



NOTE:
PART TO BE NESTED ON COIL STOCK TO MAKE MOST EFFICIENT USE OF MATERIAL.

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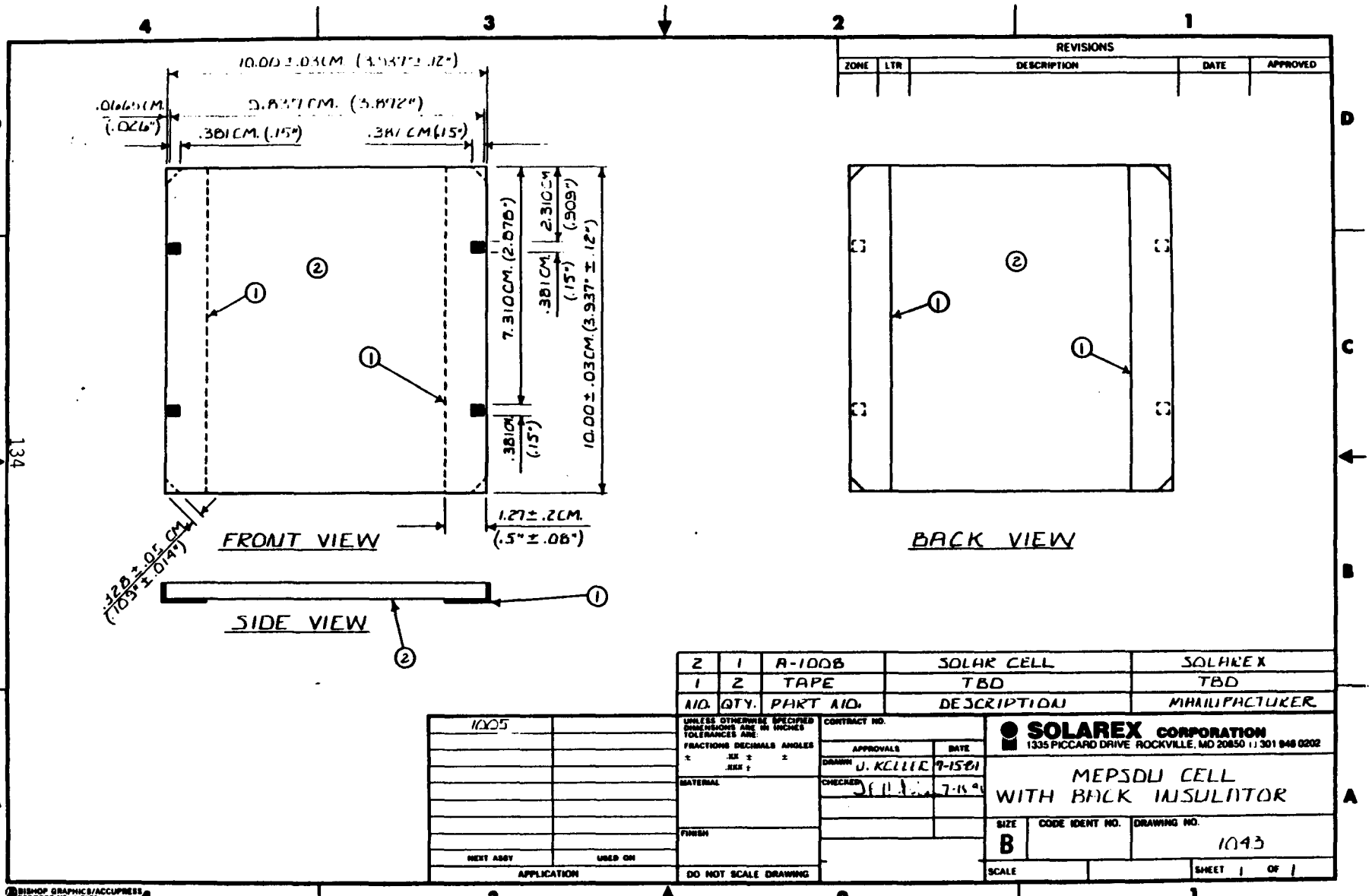
			APPROVALS / DATE	MEPSDU INTERCONNECT
		MATERIAL .003 THK, COPPER W/1.0003 (9X)10 60-40 SOLDER COATING	DRAWN J Keller 2-16-91	
			CHECKED G. Hudson 2-27-91	
D-1005		FINISH		SIZE B / CODE IDENT NO. / DRAWING NO. 10048
NEXT ASSY	USED ON	DO NOT SCALE DRAWING		SCALE FULL / SHEET 1 OF 1
APPLICATION				

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 7771

FIGURE 17


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
.381CM. (.15")
.381CM (.15")
7.310CM. (2.876")
.381CM. (.15")
2.310CM (.909")
10.00 ± .03CM. (3.937" ± .12")
1.27 ± .2CM. (.5" ± .08")
FRONT VIEW
BACK VIEW
SIDE VIEW
2 | 1 | A-1008 | SOLAR CELL | SOLAREX
1 | 2 | TAPE | TBD | TBD
NO. | QTY. | PART NO. | DESCRIPTION | MANUFACTURER
1005
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO.
APPROVALS | DATE
DRAWN J. KELLER 9-15-81
CHECKED 7-15-81
SOLAREX CORPORATION
1335 PICCARD DRIVE ROCKVILLE, MD 20850 (301) 948 0202
MEPSDU CELL
WITH BACK INSULATOR
SIZE B | CODE IDENT NO. | DRAWING NO. 1043
SCALE | SHEET 1 OF 1
BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-7271

Associates (20). During our MEPSDU program both companies provided Solarex with preliminary flow diagrams for tabbing and stringing the designed module. Figure 18 shows the flow diagram prepared by Kuliche and Soffa. Figure 19 shows the flow diagram for the MB Associates machine.

During the MEPSDU program both Kuliche and Soffa Industries and MB Associates were under subcontract to Solarex for design of a tabbing and stringing machine. The details of the preliminary machine designs are given in Section 4.0.

2.4.8 Module Encapsulation Procedure

The process flow sequence for module encapsulation is shown in Figure 20. The glass must be cleaned and primed before it can be used. The cell string should be ready for use since we eliminated the use of flux during soldering of interconnects. The other module materials are rolled out and cut to size.

While a number of lamination/curing cycles were investigated during the program the one selected for use was similar to the one recommended by Springborn (3) except that the modules are not placed in the

FIGURE 18

FLOW DIAGRAM OF KULICKE AND SOFFA INDUSTRIES, INC. TABBING AND STRINGING MACHINE

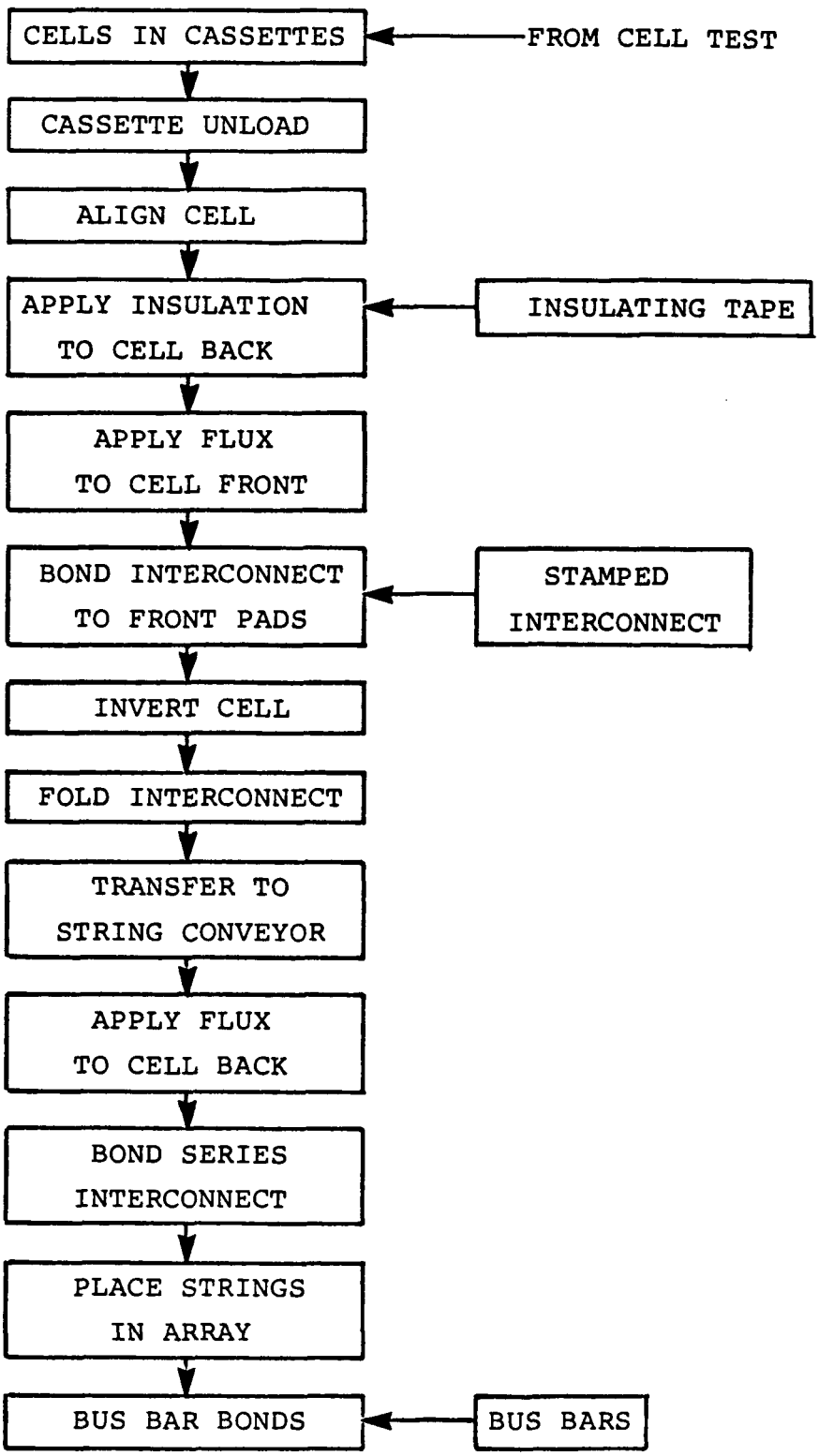


FIGURE 19

FLOW DIAGRAM OF
MB ASSOCIATES
TABBING AND
STRINGING MACHINE

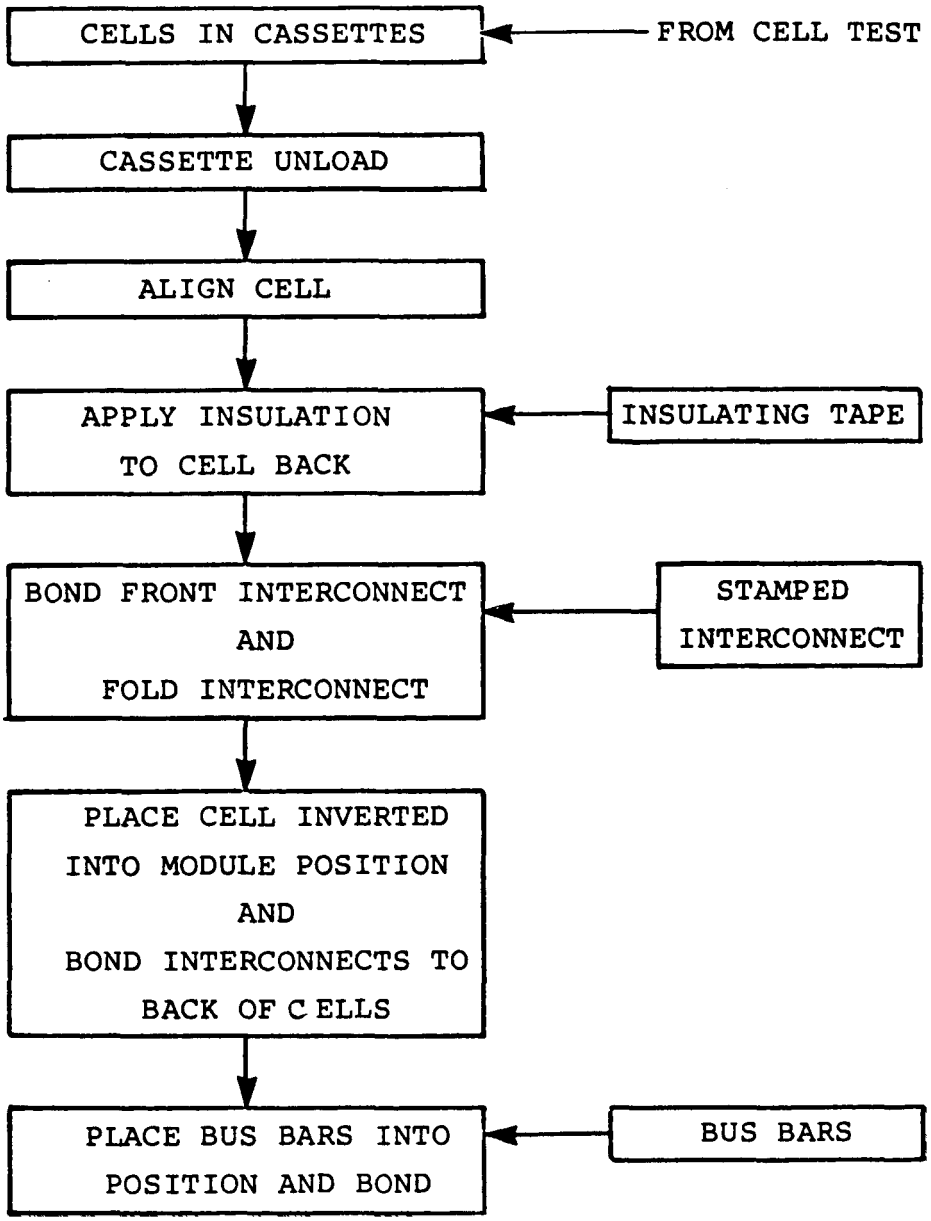
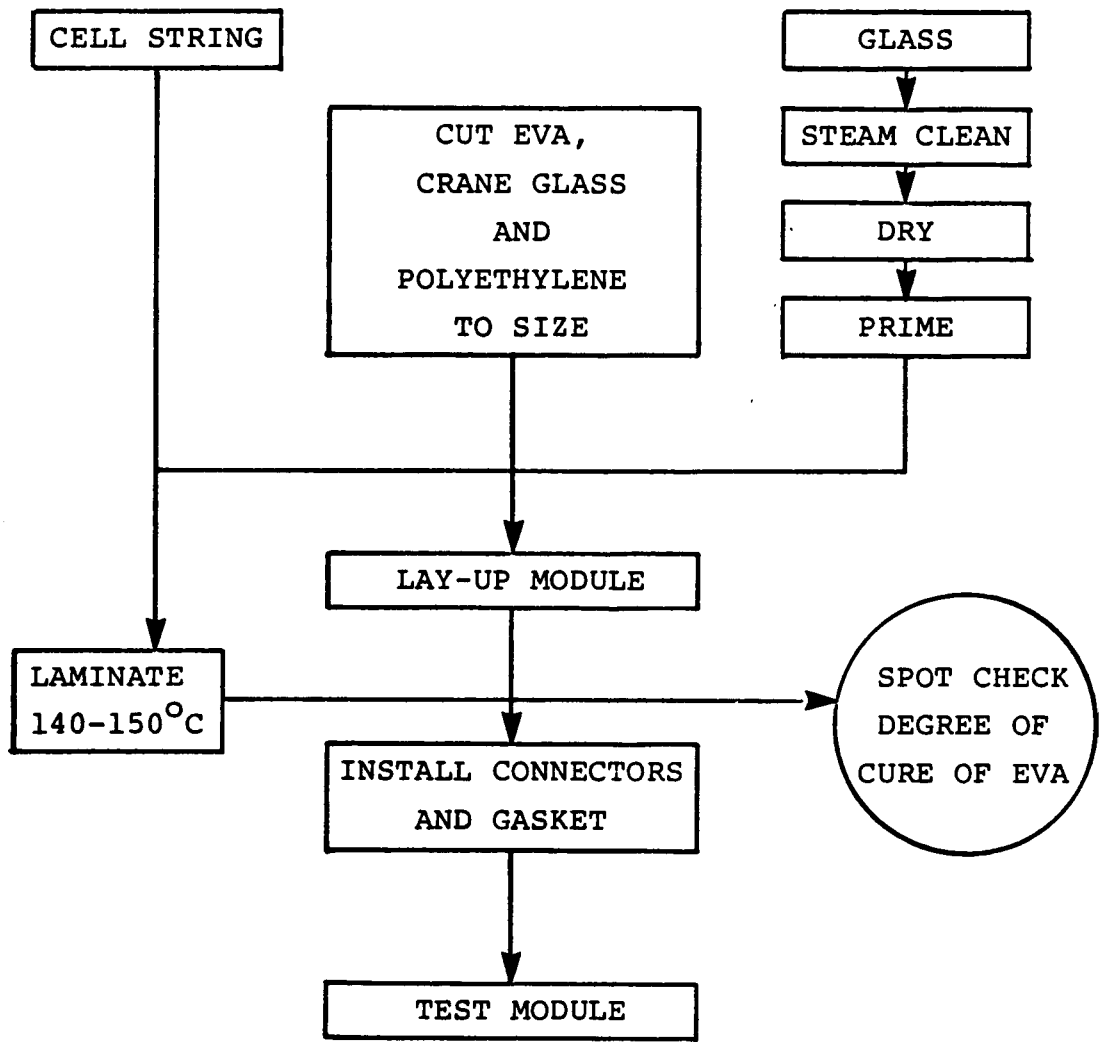


FIGURE 20

MODULE ENCAPSULATION



laminator nor removed at room temperature, but rather at an elevated temperature below the melting point of the EVA. Using a vacuum system with two chambers separated by a diaphragm the process sequence is:

- Evacuate the entire assembly for 5-10 minutes.
- Bleed air into the top chamber until it reaches approximately 3/4 of an atmosphere.
- Heat the module to 150°C as fast as possible.
- Cure for ten minutes at 150°C.
- Turn off heat.
- Release vacuum.
- Remove module.

This procedure was successfully employed to laminate our Block IV modules that passed JPL Block IV environmental tests. It should be noted that larger modules and larger cells are subjected to large forces during lamination. Care must be taken to apply the lamination pressure evenly and slowly to prevent

breakage and/or movement of cells. Larger modules also require more care to assure that all bubbles are removed and that the entire package gets cured sufficiently, especially around the edges.

The final steps in module manufacture is to attached the Amp connectors and the gasket.

2.4.9 Test Systems

Every solar cell and every module should be tested under illuminated conditions to draw an IV curve to provide a measure of power at the design voltage and to provide data for statistical analysis. The individual test systems are described in Section 4.0.

2.5 Final Process Sequence

The final process sequence is diagrammed in Figure 1. The significant changes between this and the preliminary process sequence shown in Figure 2 are:

1. Use of ion milling rather than laser scribing for edging.

2. Glass bead back clean-up rather than HCl etch.

3. Wave solder on the front rather than solder dipping.

4. Hot spray AR coating rather than spraying at room temperature with subsequent firing.

3.0 TECHNICAL DISCUSSION

The following sections describe the experiments performed during the program including a summary of the results and the impact of these results on process and/or equipment design. Detailed performance measurements were presented in the various quarterly reports (see particularly Quarterly Reports 2, 3 and 4 - References 10, 15, 21).

3.1 Front Junction Formation

The initial experiments were designed to verify that sprayed Emulsitone Phosphorofilm for solar cells could serve as a dopant source for solar cell fabrication. Single crystal wafers were sprayed with the phosphorofilm using both an air brush and an Advanced Concepts spray system. Wafers were diffused in a quartz diffusion tube. Those diffused in a helium atmosphere or with no gas flow in the tube developed a diffusion oxide that was impossible to remove. Oxygen or air flow is required for diffusion with the phosphorofilm. Diffusion with oxygen flow at 910°C for ten minutes resulted in sheet resistance between 30 and 50 ohm/square depending on the spray conditions. Processing of 2 cm x 2 cm cells using a standard space cell process (22) - TiPdAg contacts and Ta_2O_5 AR coating - resulted in cells with greater than 15% efficiency at 25°C using the AM1 spectrum. This efficiency is consistent with the

results obtained using gaseous diffusion (23). These initial experiments convinced us that the phosphorofilm can yield results as good as those obtained for gaseous diffusion.

The next set of experiments were designed to evaluate the use of the spray dopant on semicrystalline silicon. Results showed that gaseous and spray doped cells had comparable efficiencies. With a tube diffusion process of 910°C for ten minutes the semicrystalline wafers produced standard space cell 2 x 2 cm cells with AM1 efficiencies varying from 9 to 12.5%.

It was clear that 910°C was too high a diffusion temperature so a set of experiments were run to optimize the diffusion temperature under the sheet resistance constraints imposed by the nickel plating. Diffusion temperatures between 870 and 910°C were examined. Both 2 cm x 2 cm space cells and 10 cm x 10 cm Ni-solder metallized cells were fabricated. Cell efficiency increased significantly for diffusion temperatures below 910°C but the result saturated with little change between 880 and 870°C. Since the nickel plating process appears to require a sheet resistance of 50 Ω/□ or less a diffusion temperature of 890°C was selected with the understanding that this temperature will result in about 5% less current and power than could be obtained by using a somewhat lower diffusion temperature and subsequent higher sheet resistance.

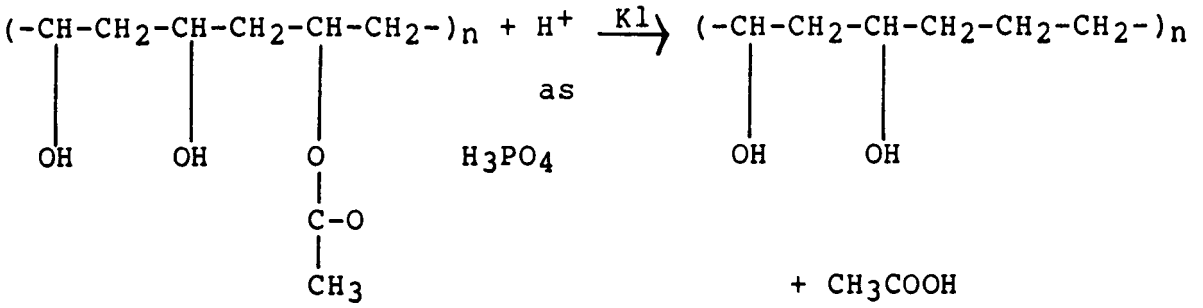
The next step was to evaluate the use of a belt furnace for diffusion rather than the quartz diffusion tube. All experiments were performed using just the air flow obtained by the ventilating system. The initial results showed tube diffusion to produce a full percentage point higher efficiency than belt diffusion for both single crystal and semicrystalline silicon. Subsequent changes in the belt profile led to improvements in the belt diffused samples. Optimizing the belt diffusion for semicrystalline silicon resulted in the semicrystalline 10 x 10 cm cells having higher efficiency than the co-processed 3" round single crystal controls.

The highest average efficiency obtained for 10 cm x 10 cm semicrystalline cells with Ni-solder metallization was about 9% AM1. Further optimization of the belt diffusion process was underway when the effort was terminated.

While the Emulsitone Phosphorofilm spray dopant did prove to yield cells as efficient as those produced by gaseous diffusion, we have had problems with its reliability. Its chief problem is the short shelf life beyond which it does not adequately wet the surface of the wafers.

Analysis of both old and new lots of dopant indicate that the polymer (poly) vinyl alcohol is undergoing decomposition in the acidic solution. The (poly) vinyl alcohol is produced by

hydrolysis of (poly) vinyl acetate. Hydrolysis is typically incomplete, leaving acetate groups in place on the carbon chain, which then react with acid (H^+) to generate acetic acid:



Titration curves on old and new samples show the presence of acetic acid and phosphoric acid in old samples, but only phosphoric acid in new samples. The rate constant of the above reaction (k_1) is unknown, but may be variable since some batches of dopant maintained a useful shelf life for up to six months, while others degraded within a month.

The problem of a short shelf life is a serious one. It indicates that further work is necessary to find a more stable material or possibly to develop the capability to prepare the dopant solution on-site as needed.

3.2 Back Junction Formation

The initial experiments were designed to determine the optimum screening parameters for the Al paste. We used

Englehard Al Ink #A-3484, 3 inch Cz wafers (1-2 Ω-cm), a diffusion process that resulted in a 80-120 Ω/□ diffused sheet resistance, a standard TiPdAg metallization, an 850°C alloy temperature, and a 20 second alloy time. This is a process developed for high efficiency thin cells (12). All other screening parameters except the screen size were held constant, including an 80 mil snap-off point and a medium screen speed. The resultant cells were evaluated indicating little change in current as a function of screen size, but significant improvement in open circuit voltage and fill factor as the screen mesh was decreased from 250 to 100. However using an 80 mesh screen resulted in very poor performance.

This experiment was repeated for 150, 100 and 80 mesh screens, but using both 20 and 30 second alloy times. The best results were obtained for 100 mesh with 20 second fire and 80 mesh with 30 second fire with each giving comparable results. It is clear that the highest voltage and efficiency (the best BSF) is created using the largest screen opening possible within the constraints of cost of the paste and breakage of the wafers due to warping. Thicker pastes must be alloyed for longer times to achieve the same degree of alloying as thinner pastes. These results led us to select a 100 mesh screen as baseline for the MEPSDU process. When we switched to this from our baseline 150 mesh used for thin cells (24) we saw immediate improvements in cell performance mostly associated with increased open circuit voltage.

The second set of back junction experiments was designed to compare tube alloy with infrared belt alloy and with convection belt alloy. The infrared belt yielded the best cell performance, with tube nearly equivalent and convection belt much worse. It should be noted that the profile for the infrared belt and tube have been optimized for semicrystalline silicon while the convection belt was optimized for single crystal silicon. The infrared belt furnace seems ideally suited for firing the Al paste to form a back surface field (BSF).

3.3 Back Clean-Up

3.3.1 HCl Etch

A standard procedure for back clean-up is to etch in HCl. Etching in a bath of HCl with subsequent rinses is not particularly well suited to automated production nor is it easy to provide the controls necessary for high yield production. We therefore decided to utilize an etch-rinse machine to accomplish the etching and rinsing in one system with a well controlled environment.

Experiments were conducted using an FSI 2120 Etch-Strip machine. The machine performed well, was easy to program with sequences of operations, allowing

easy process optimization, and possessed several safety features which prevented operator access to the sample chamber when acid was being sprayed. Based on results obtained on lots of three to six cells, the 2120 could produce 150 visibly clean and dry 10 cm x 10 cm cells in a best time of 13.5 minutes. This time did not include an initial warm up period or the time to load and unload cassettes. Sequential steps of HCl etch, rinse, HF etch, rinse, and dry were carried out for the minimum time that still showed acid neutralization.

Subsequent IR transmission tests however indicated that even a five minute spin clean-up in HCl was not sufficient to remove all of the residues. After recleaning the wafers in hot DI water in an ultrasonic bath, the Reflection plus Transmission curve increased by two to three percent, showing that after etch the samples had a significant residue and therefore were not clean enough to make adequate solar cells.

During these experiments, it was discovered that the HCl degraded rapidly, probably because of the decreased HCl solubility at the 60^{o}C temperature used. This presented two problems: (a) Much fresh HCl must be added for each batch of cells, probably

two liters/150 cells, and most of the used HCl dumped, and (b) Since so much warm fluid is dumped, there is essentially an initial heat up delay of twenty minutes each time a batch of cells is run, drastically lowering throughput.

Lower HCl temperatures were tried, but the reduced reactivity resulted in unacceptably long etch cycles. The success of the glass-bead back clean-up coupled with its advantage of retaining much of the conductive aluminum on the cell back led to abandonment of the HCl back clean-up effort.

3.3.2 Glass Beading

The initial experiments were designed to prove the feasibility of cleaning-up the Al paste residue using glass beading (sand blasting with super fine glass balls) so that the unreacted Al could serve as the principle current carrying component on the back of the cell. Initial experiments removed the residue until the back looked visually like clean aluminum. If the cells were then immediately placed in the nickel plating solution, no nickel would plate to the aluminum. If however the back was subsequently cleaned in fumic HF as would be required in the

process sequence to remove the AR from the front, the Ni did plate to the Al although the pull strengths were unacceptably low.

Subsequent experiments used somewhat longer glass beading times (still under one minute for a 100cm^2 wafer). The results were excellent with good pull strength uniformity. The average was 625 grams with a minimum of 325 grams, all above our standard minimum requirement.

Experiments were performed to compare HCl back clean-up cells with glass bead back clean-up cells, using tape to mask the Ni on the back of the glass beaded cells during soldering. The results on both single and semicrystalline silicon were encouraging. In all cases the glass bead cells had slightly higher average efficiencies than the cells made with HCl back clean-up.

It should be noted that manual glass beading of cell backs is not a high yield process. A great deal of breakage occurred due to movement of the cells during the process. Tooling to hold the cells in place is a very important requirement. Such tooling had only been designed on paper at the time the effort was terminated.

3.4 AR Coating

Preliminary experiments utilized a titanium isopropoxide solution consisting of (13,14):

8.3%	Titanium Isopropoxide
25%	Butyl Acetate
33%	2 Ethyl 1 Hexanol
33%	Isopropyl Alcohol

Spraying onto polished single crystal wafers resulted in uniform blue coatings with a thickness of 850 $\pm$ 100 A with an index of refraction between 2.1 and 2.2 consistent with previous reports and with the requirements of the system. However when sprayed onto NaOH etched semicrystalline silicon the resultant AR coating was a gray color with a residual reflection in excess of 20% compared to the 7% obtained for single layer evaporated AR coatings.

In an effort to improve the uniformity and therefore reduce the reflection from the semicrystalline cells we attempted to find an organic solvent that could be utilized in a pre-spray step. The results are summarized below:

1. N-Butyl Acetate: Dried as the wafer was sprayed.

2.	Sec-Butanol:	Dried as the wafer was sprayed.
3.	Isopropyl Alcohol:	Dried as the wafer was sprayed.
4.	2 Ethyl - 1 Hexanol:	Boiling point too high. It evaporated with the AR on top of it, resulting in the formation of pools with a very uneven AR.
5.	3-Methyle-1-Butanol:	Had no effect on the subsequent AR spray.
6.	1-Hexanol:	Had no effect on the subsequent AR spray.
7.	Pentanol:	Had no effect on the subsequent AR spray.
8.	2-Ethoxethanol:	Resulted in a spotty surface.
9.	3-Methyl-1-Hexanol:	Used both as a prespray and as a replacement for the Butyl Acetate resulting in inconsistent AR coatings.

Rather than continuing to look for a prespray treatment we began to investigate the effect of deposition conditions on the AR coating. It was found that if Titanium Isopropoxide is sprayed directly on a heated wafer (400 to 500°C) a uniform blue color can be obtained. Placing the wafer on a hot plate at 400-500°C and spraying the Titanium Isopropoxide with an air brush resulted in reproducible uniform AR coatings. Figure 21 is a plot of Reflection plus Transmission as a function of wavelength for one sample of semicrystalline Si sprayed in this manner. This compares favorably with evaporated AR coatings.

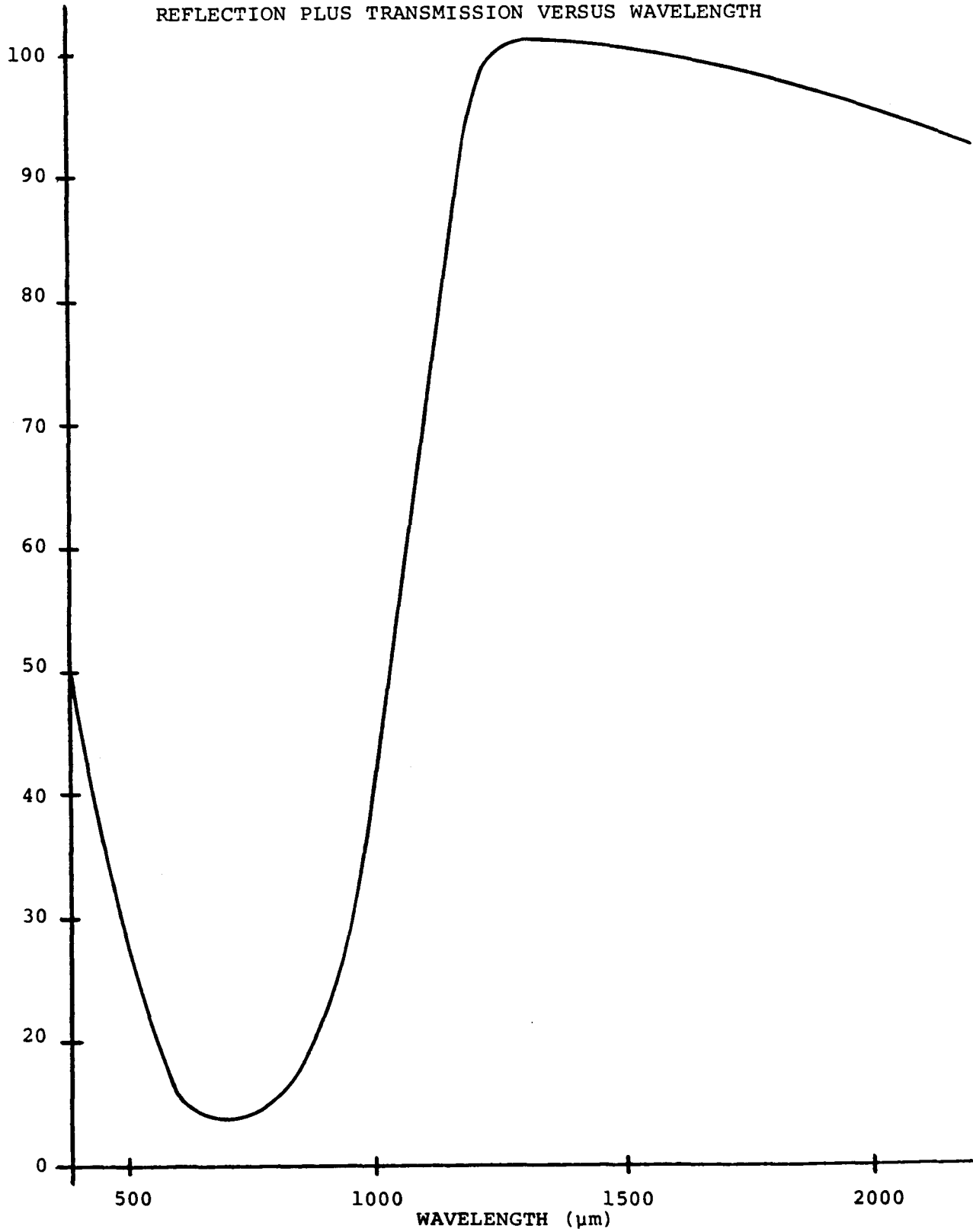
An experiment was conducted in which 2 cm x 2 cm single crystal cells with TiPdAg contacts were tested before AR coating. Half the cells were then given a Ta_2O_5 evaporated AR coating while the other half were AR coated using the new hot spray technique. The sprayed group actually showed a larger increase in peak power than the evaporated group due to a larger increase in open circuit voltage for this group. The current increase for the evaporated group was marginally greater probably due to non-uniformities for the sprayed samples resulting from hand spraying. The use of an automated spray machine for this process should result in uniform AR coatings at least as good as single layer evaporated AR coatings.

The final set of AR coating experiments were to determine the optimum time-temperature sequence for the process. The

FIGURE 21

HOT SPRAY AR COAT Ti ISOPROPOXIDE

REFLECTION PLUS TRANSMISSION VERSUS WAVELENGTH



temperature range investigated was 280 to 425°C for times varying from 5 to 90 seconds. The conditions which produced an acceptable AR coat were achieved within fairly narrow limits: Temperature range - 400-410°C, with 405°C optimum; time - 45 second wafer preheat (with wafer in place on heated substrate) followed by five second (approximate) spray time, with no post-spray heating.

The most typical results of spraying at too low a temperature and/or insufficient preheat time was the presence of uneven and spotty second-order droplets interspersed with variable-sized regions of first-order AR. The most typical result of spraying at too high a temperature and too much preheat time was a smooth, oxide which was partially or totally impervious to removal in fumic HF.

3.5 Resist Inks

One of the key features of the electroless nickel plating process is identification of a resist ink that can meet the technical and economic requirements. The resist ink must:

- Survive the HF etch to remove the AR coating.
- Survive the Ni plating bath.

- Be easily screenable with good resolution.

- Not bleed into the areas to be plated.

- Be easily and quickly cured.

- Be easily and completely removed.

A number of resists were evaluated as described below.

- Warnow Printed Circuit Resist PR1000 - Survives 30 seconds in fuming 70% HF but not two minutes in 48% HF; not completely soluble in either toluene or trichloroethylene so requires a vapor degreaser.

- Hilton-Davis Sup-R-Cryl 5-54-A-300 - Too fluid for good printing; not completely soluble in either toluene or trichloroethylene.

- Chroma-Chem 844 - Too fluid for good printing.

- Inmont RBH - Prints well, dries extremely quickly; all wafers broken in plating bath due to thermal mismatch.

- Universal Color Dispersions UCD 4800A - Excellent printing, no visible breakdown of resist in plating

solution; does not completely dissolve in acetone or trichloroethylene.

- MacDermid Macu-Mask 9251 and 9454 - Good clear print; does not break down in plating solution; is completely removed by trichloroethylene (5 minutes ultrasonic); undercut when AR coating is etched; pattern areas are widened considerably.

- Homemade resists using solid Rhome and Hass Acryloids A-21, B-44, B-48N and B-50 mixed in ethylene glycol monobutyl ether acetate (Butyl Cellosolve) - Prints well; withstands HF etch; is undercut by the Ni plating solution.

- Homemade resist using solid Rhome and Hass Acryloids B66 + B82 and blue dye LCB 2005 mixed in Butyl Cellosolve - Prints well; withstands fumic HF etch; is undercut by the Ni plating solution; at times can be stripped by cold water while at other times is very hard to remove.

- Colonial Printing Resist ER-6028 and ER-6055 R.U. Blue - Prints well and cures in 3 to 6 minutes; survives best the etching and Ni plating of all the inks tested; is removable in cold organic solvents,

although residue can be a problem. Requires ultrasonic agitation.

Colonial Resist Ink #ER6055 was selected for use. A number of experiments were then conducted to develop a satisfactory process sequence. The following observations were made:

- Colonial Resist withstands either 1:1 (24%) HF for five minutes or fumic HF vapors (70% HF) for three minutes without etching or undercutting.

- Colonial Resist withstands seven minutes in Halma electroless nickel solution at 85°C at pH 8.5.

- Resist removal in a trichloroethylene bath for sixty minutes using mild ultrasonic agitation is not sufficient since a number of wafers exhibited low pull strengths.

- Resist removal in consecutive trichloroethylene baths for thirty minutes using mild ultrasonic agitation is not sufficient since a number of wafers exhibited low pull strengths.

- Resist removal in methylenechloride, trichloroethylene and 1,1,2-trichloroethane for seven minutes with

powerful ultrasonic agitation resulted in good cleaning with no trace of residue.

The results showed that Colonial Resist #ER-6055 can meet our requirements as long as adequate ultrasonic agitation is provided.

3.6 Electroless Nickel Metallization

Solarex has reported on the properties of electroless nickel metallization in detail (16). Based on this background the MEPSDU effort was limited to evaluation of pull tests and the influence of heat treatments, especially lamination time - temperature cycles. The following observations were noted (1):

- Low pull strengths corresponded with both stains on the silicon and low electrical performance of the cells.

- Long Ni plating times (greater than eight minutes) resulted in reduced pull strengths.

- Short Ni plating times (less than seven minutes) resulted in good average pull strengths but much greater scatter of the results.

- Lack of complete removal of the resist is a main cause of low pull strengths and poor contact continuity.

- Use of a low temperature soldering iron (600°F) is required for connecting to Ni-solder contacts.

- High pull strengths (greater than 700 grams average) were obtained with few or no very low values when plating, resist clean-up and soldering were well controlled.

- Heat treatments of 150°C for up to one hour had no effect on pull strengths of the high pull strength lots.

It is clear that proper control of sample cleanliness including complete resist removal, nickel plating time and soldering iron temperature are keys to getting good contact adhesion. Once this is achieved the cells will withstand the lamination time/temperature cycle.

3.7 Wave Soldering

Wave soldering is a technique utilized extensively in the printed circuit industry. Its application to photovoltaics was hampered by the use of round wafers and the need to solder to

both sides of the wafer. Our use of square semicrystalline silicon and the development of a process sequence that requires soldering only on the front of the cell made wave soldering a viable option.

The initial experiments run at an 8^{o} tilt angle at 50 inches per minute resulted in good solder coverage, but with some balling along the grid lines. Increasing the tilt angle to 9^{o} eliminated the balling. The use of different geometries both before and after passing through the wave has a significant effect on the amount of solder on the different metallization pattern features, i.e., grid lines, bus bars, pads. For each pattern the best geometry will have to be determined.

Fluxing is an important parameter in determining uniformity of solder coatings. The use of a foam fluxer in line with the wave solder machine resulted in improved solder coating uniformity.

A number of trial runs comparing wave soldering with solder dipping demonstrated at least equivalent yield and average efficiency as obtained with solder dipping. However attempts to wave solder both sides of cells resulted in poor contact adhesion on the side soldered last.

While the results of wave soldering were preliminary they were extremely encouraging. Solarex believes enough in the technology to have purchased a new wave solder machine for manufacturing.

3.8 Edging

A preliminary plan was to utilize a laser to scribe a trench in the front of the cell to isolate the front and back junctions. We had used this technique successfully on a production line using semicrystalline silicon and TiPdAg contacts applied by photolithography. When trying to adapt this technique to Ni-solder contact cells we ran into difficulty with shunting caused by the interconnects. Negative screen printing of resist ink leaves a rim of uncovered silicon around the perimeter of the cell. Attempts to eliminate the perimeter ring were unsuccessful since screening over the edge results in contamination of the chuck plate and excess wear of the screens. Since this perimeter is bare silicon, it Ni plates and becomes coated with solder. This leaves a bead of metal around the perimeter of the cell. When we laser trench, it must be done interior to the metallized perimeter ring. The trench provides adequate isolation, but as shown in Figure 22, the cell interconnects can easily make contact with the metallized perimeter ring. Since this ring is electrically attached to the back side any contact of the interconnect with the ring results in shorting of the cell.

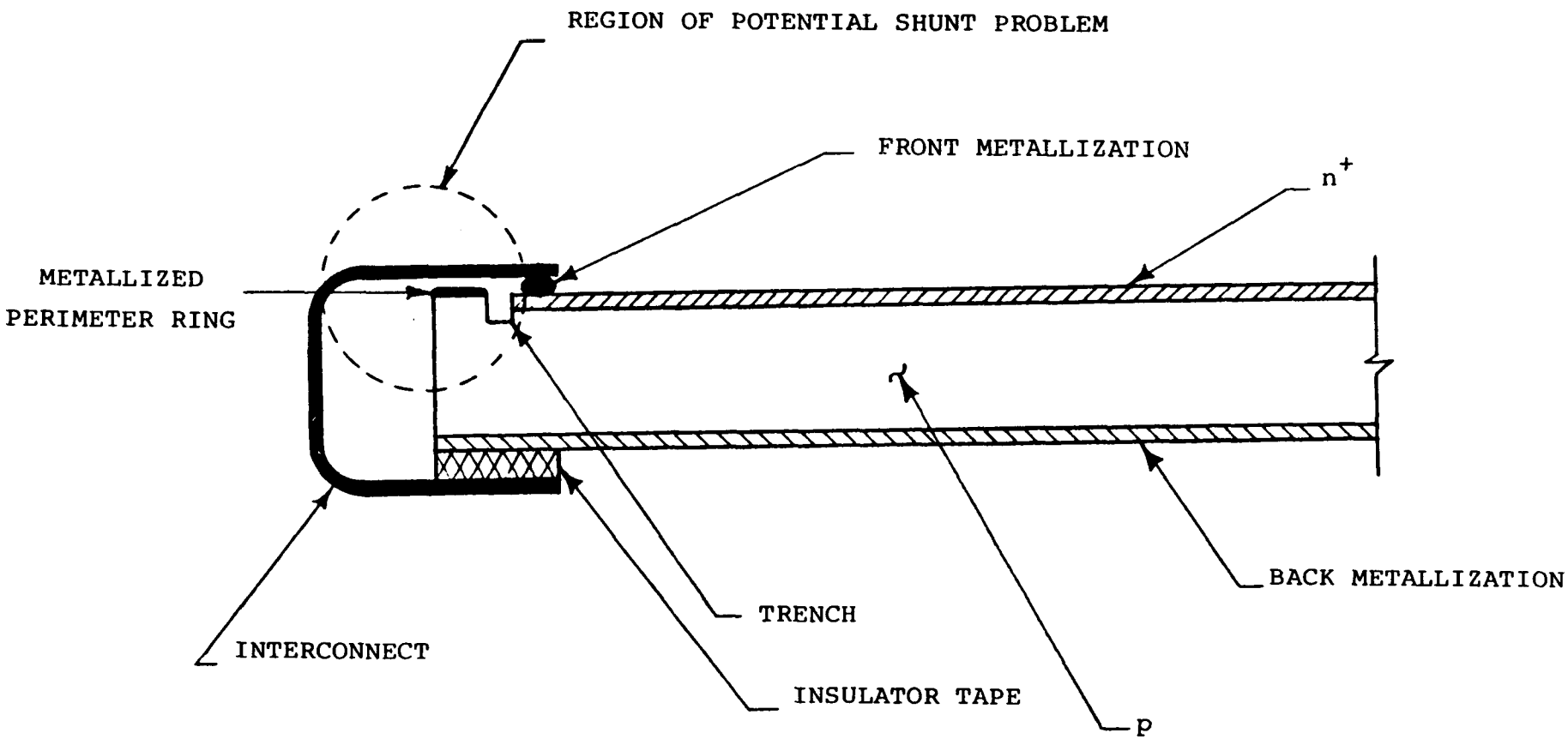


FIGURE 22

POTENTIAL CELL SHUNTING WITH TRENCHING

In a search for a replacement edging technique we have investigated two alternatives, 1) Ion milling, and 2) Edge Masking. Each is described below.

Ion milling entails bombarding the sample with accelerated ions. Because nickel is not readily etched our experiments were done utilizing inert ions of argon. Stacks of wafers were milled in a Technics Ion Microfabrication Systems, Inc. model #MIMTLA20 Ion Milling Machine. The wafers were processed through nickel plating, then ion milled and finally solder coated. Ion milling with too low an acceleration voltage (less than 1,000 volts), or with too low a current density (less than 0.7 mA/cm^2) or for too short a time (less than one hour) resulted in shunted cells. At 1,100 volts and 0.7 mA/cm^2 for sixty minutes the cells exhibited a small amount of shunting. Longer times or higher current densities should alleviate this problem.

Edge masking entails placing a barrier material on the edge of the cell to prevent diffusion and nickel plating from occurring.

A number of experiments were conducted in an attempt to find a material suitable for use as an easily applied diffusion and etchant barrier. Initially we looked at screenable glasses from Englehard including A3025, A3031, A2835 and 4287C. All of

these materials easily etched away in fumic HF. They also tended to be very brittle and easily chip off during normal handling.

We then identified a number of metal oxides in which oxide formation takes place at temperatures below the diffusion temperature used, but whose melting temperature is well in excess of silicon's melting point. Eight candidate materials were selected. These were stannous oxide, titanium isopropoxide, titanium chloride, magnesium acetate, magnesium carbonate, niobium chloride, chromium trioxide and tungsten chloride. A paste was made with each of these powders, using the same formula as we use for aluminum paste. This may not be the best formulation but at least provided a vehicle for testing. After firing these pastes at 500^{o}C, they were all susceptible to HF etch. However after being put through a diffusion time-temperature cycle titanium isopropoxide, titanium chloride, niobium chloride and chromium trioxide withstood the fumic HF treatment. We then attempted to screen print pastes made from these four oxides. The chromium trioxide paste was unstable, it polymerized in a matter of minutes and so it was removed from the list of candidates.

Cells were fabricated using:

- Titanium Isopropoxide
- Titanium Chloride
- Niobium Chloride

Experimental controls were fabricated with no annulus.

The controls and the cells produced using titanium chloride and niobium chloride were shunted. The oxide made with the titanium isopropoxide however showed promise of being a good diffusion, etchant and nickel plating mask. Further work is required to optimize the paste formulation and to provide the uniformity and reliability of this paste as an edge mask.

3.9 Cell Metallization Design

In designing the grid pattern for the cells a number of module design and cell process parameters must be known. The parameters utilized were:

- Four contact pads are located on two opposite edges of the cell.

- N^+ layer sheet resistance = 40 $\Omega/\square$.

- Solder is flat across the top, indicating an almost rectangular cross section.

- Resistivity of the solder = 20 x 10^{-6} $\Omega \cdot$ cm.

- Relationship between initial base width and height of solder was measured as shown below:

INITIAL BUS WIDTH (MIL)	WIDTH OF SOLDER (MIL)	HEIGHT OF SOLDER (MIL)
18	18	3
60	60	6
100	100	9

- Ignore contact resistance since we do not know the value for Ni and because previous calculations that have ignored the term have agreed well with actual cell performance.

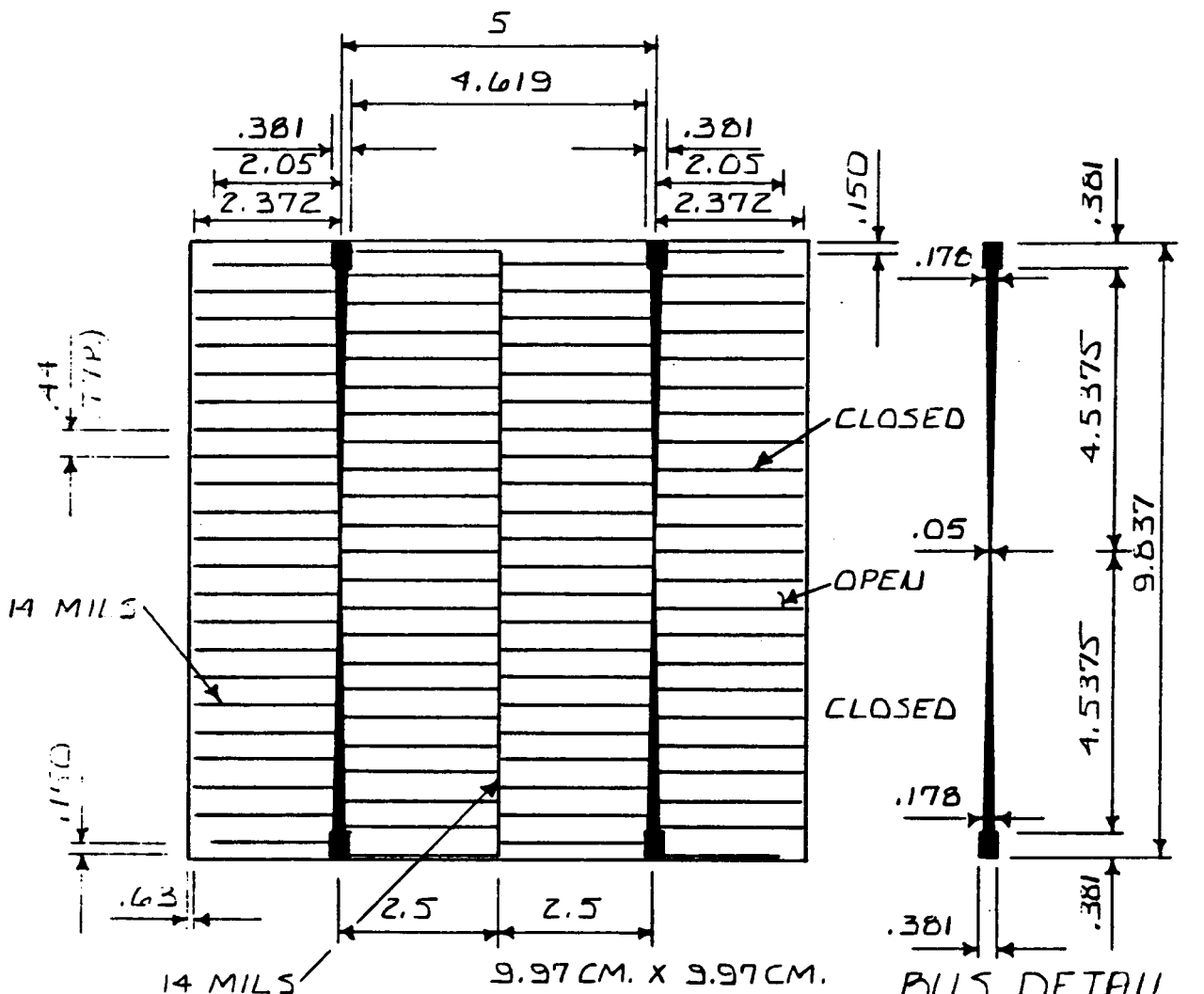
The technique for determining the pattern entails defining all of the power loss terms and then minimizing the total power loss with respect to grid spacing and bus width. The grid width is assumed to be the minimum allowable by technology since using the minimum line width always yields the smallest power loss. Three different patterns were designed using minimum line width of 18, 14 and 10 mils. The results of the calculations are given in Table #1 and the grid patterns are shown in Figures 15, 23 and 24. It is clear from the table that the finer grid lines

TABLE # 1

GRID PATTERN CALCULATIONS

LINE WIDTH (mils)	OPTIMIZED CENTER TO CENTER LINE SPACING (cm)	GRID LINE SHADOW %	BUS BAR & PADS SHADOW %	TOTAL SHADOWING (%)	RESISTIVE LOSS IN GRID %	TOTAL LOSS LINE TO GRID (RES & SHAD) %
18	.475	9.6	2.6	12.2	6.7	18.9
14	.44	8.1	2.6	10.7	6.2	16.9
10	.4	6.4	2.6	9.0	7.7	16.7

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
			FIGURE 23		



NOTE:
ALL DIMENSIONS IN CM.
UNLESS STATED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± ± .XXX ±	CONTRACT NO.	SOLAREX CORPORATION 1335 PICCARD DRIVE ROCKVILLE, MD 20850 □ 301 948 0202	
	APPROVALS / DRAWN J. KELLER / DATE 7-9-81	MEPSDU 10CM. X 10 CM. GRID PATTERN (14 MILS)	
MATERIAL	CHECKED	SIZE A	CODE IDENT NO.
FINISH		DRAWING NO. 10-40	
DO NOT SCALE DRAWING		SCALE	SHEET 1 OF 1

RITE-LINE CORP. REORDER NO. A-8990

APPLICATION		REVISION			
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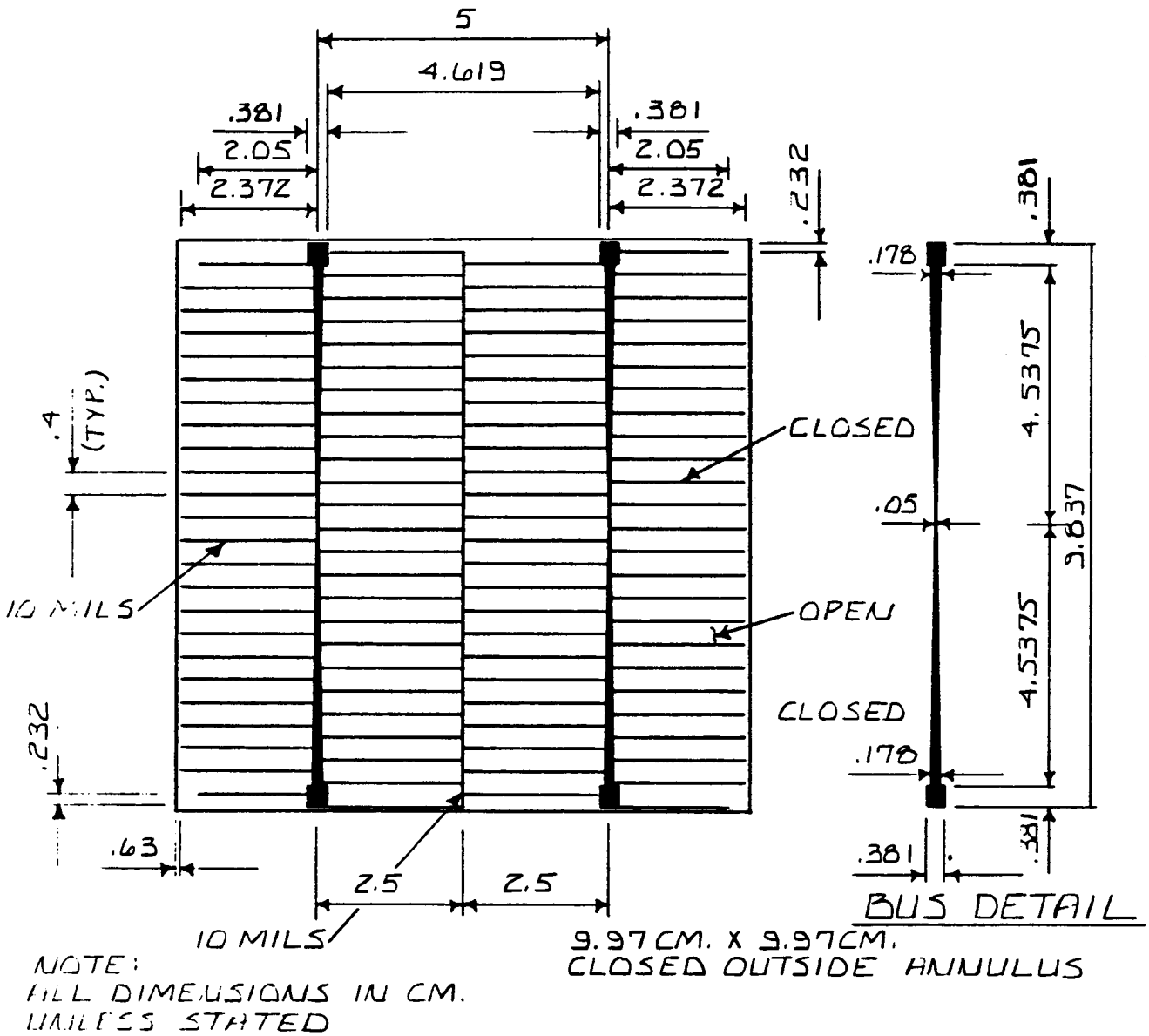
			FIGURE 24		



NOTE:
ALL DIMENSIONS IN CM.
UNLESS STATED

9.97 CM. X 9.97 CM.
CLOSED OUTSIDE ANNULUS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.	SOLAREX CORPORATION 1335 PICCARD DRIVE ROCKVILLE, MD 20850 □ 301 948 0202	
	APPROVALS / DRAWN J. KELLEK	DATE 7-9-81	MEPSDU 10 CM. X 10 CM. GRID PATTERN (10 MILS)
MATERIAL	CHECKED		SIZE A / CODE IDENT NO. / DRAWING NO. 1041
FINISH			SCALE / SHEET 1 OF 1
DO NOT SCALE DRAWING			

RITE-LINE CORP. REORDER NO. A-8990

yield lower grid line loss. However this effect saturates at quite a wide metallization thickness for nickel-solder where the thickness of the solder is a function of the width. It would be hard to measure the 0.2% difference in performance between 14 and 10 mil grid lines, so since the 14 mil pattern offers greater tolerance to process error and more redundancy it would probably result in higher process yields with minimum change in efficiency.

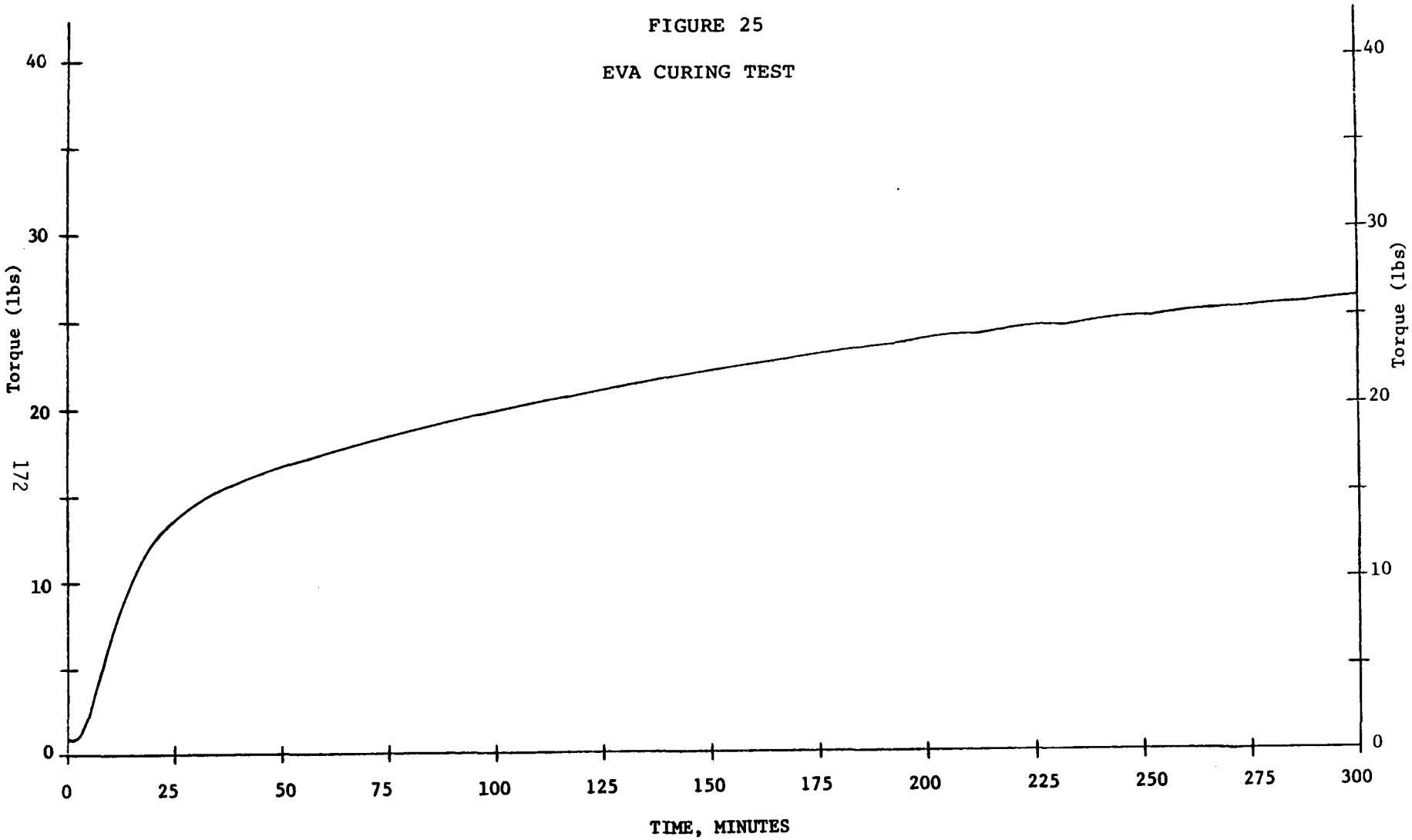
3.10 Encapsulation Materials

3.10.1 EVA Cure Properties

To determine the correct lamination procedure you must know the proper cure cycle for the EVA. EVA samples as received from Springborn were supplied to Monsanto to perform an oscillating disc Rheometer (ODR) test. The results for 140°C and 150°C are shown in Figures 25 and 26 respectively. While a 100% cure is not required a 60-70% cure is desirable. As can be seen from Figure 25, to achieve this kind of cure at 140°C requires about 50 minutes, which is too long for efficient production in a laminator. However curing at 150°C reduces the cure time to a 15 to 20 minute time frame. At this higher temperature however the curing proceeds rapidly with appreciable liberation of

FIGURE 25

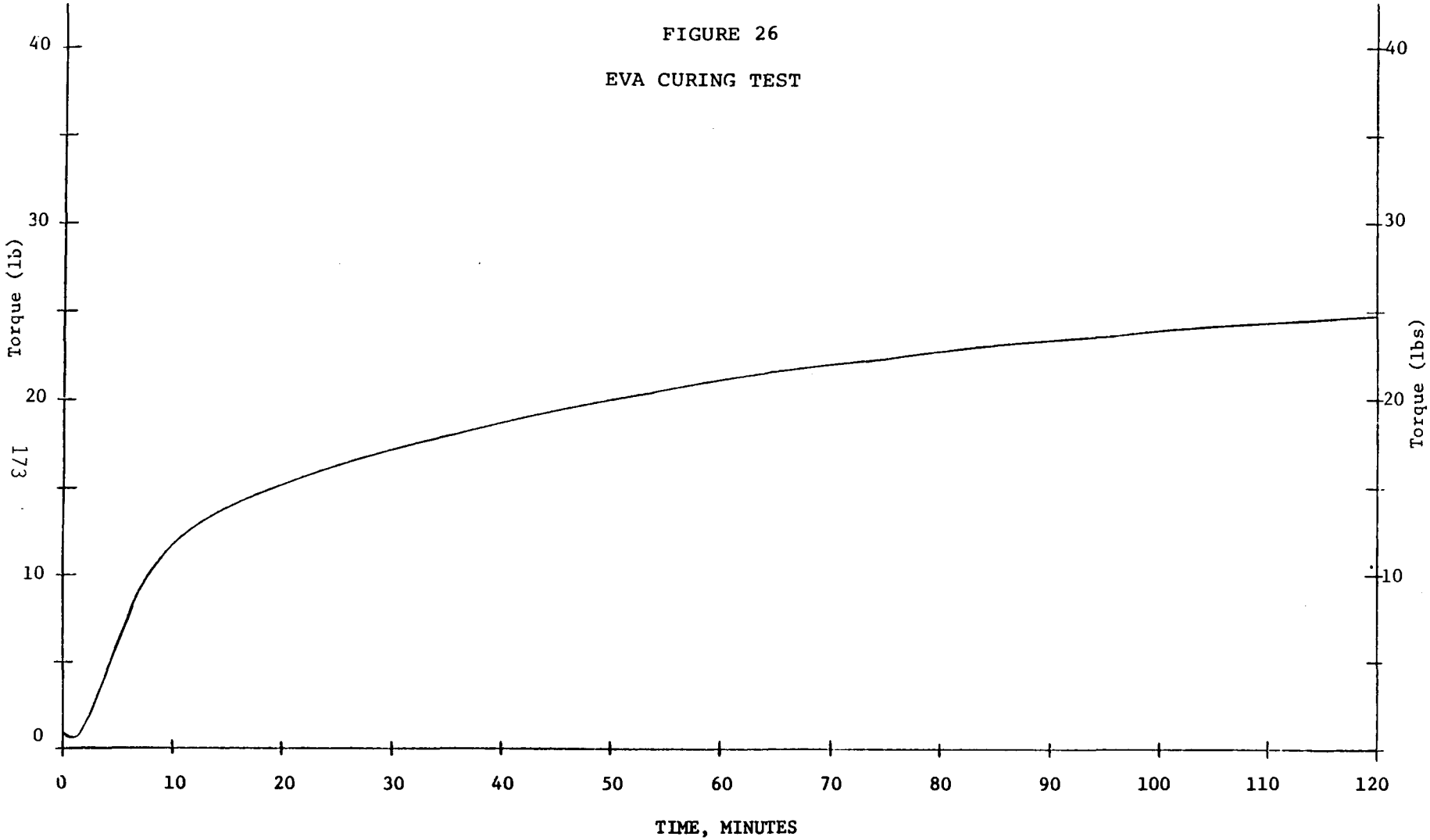
EVA CURING TEST



ODR Test at 140°C

FIGURE 26

EVA CURING TEST



ODR Test at 150°C

gaseous reaction products. Therefore the module must be maintaned under a high pressure (7-20 lb. per square inch) to prevent bubble formation in the curing EVA.

3.10.2 Insulator Tapes

The wraparound cell concept requires the use of an insulator tape on the back of each cell. These tapes must withstand lamination temperatures and pressures, adhere well to the cells and to the EVA and maintain electrical isolation through thermal and humidity cycling. A number of tapes including polyethylene, polypropylene and polyester were tested. All of the tapes passed the thermal cycle and humidity tests. However all of the polyethylene, polypropolene and some of the 1 mil thick polyester tapes failed the lamination pressure test. The tapes selected for use were polyester tapes with acrylic adhesive, either single or double sided depending on the use.

4.0 MEPSDU DESIGN

In the design of the MEPSDU, Solarex chose to develop a unit that would be a forerunner of a production facility. The equiment utilized was to be production equipment, not laboratory-scale equipment. All manual handling of individual cells was eliminated, although cassettes of cells and modules would still be manually handled.

The concept of the MEPSDU was to demonstrate the process sequence and machinery by utilizing a single machine, rather than several parallel machines for each station. This meant that it was not a balanced production line, although we imposed a minimum throughput rate of 1,000 wafers per hour for each process step. Therefore the designed unit would be capable of producing approximately 6.6 MW per year with only minor modifications (e.g., addition of several laminators).

Because of the JPL imposed termination of the module development effort in September, 1981 and termination of all equipment design and development in February, 1982, the design

of the MEPSDU was not completed. The cell process part was nearly completed and adequate equipment was identified for each process step. In the module area preliminary plans had been developed but a design phase was required before specification of the equipment could be made.

4.1 MEPSDU Cell Facility

A list of potential equipment suppliers for each area is presented in Table 2. All of these companies were contacted by Solarex and most provided quotations to our specifications.

The process sequence flow is shown in Figure 27. The following describes how the wafers move through the process. The process flow starts with the wafers loaded into cassettes. The cassettes are then manually loaded into the etch machine described in Section 4.1.2. The cassettes are manually unloaded from the etch machine and stored until needed for diffusion. The cassette is then manually loaded into the cassette unload machine as described in Section 4.1.1. This cassette unloader places them three wide on the spray doping belt and then they are transferred to the diffusion furnace belt as described in Section 4.1.3. At the conclusion of the diffusion process the cells are automatically removed from the belt and placed into cassettes which are automatically placed in a waiting area.

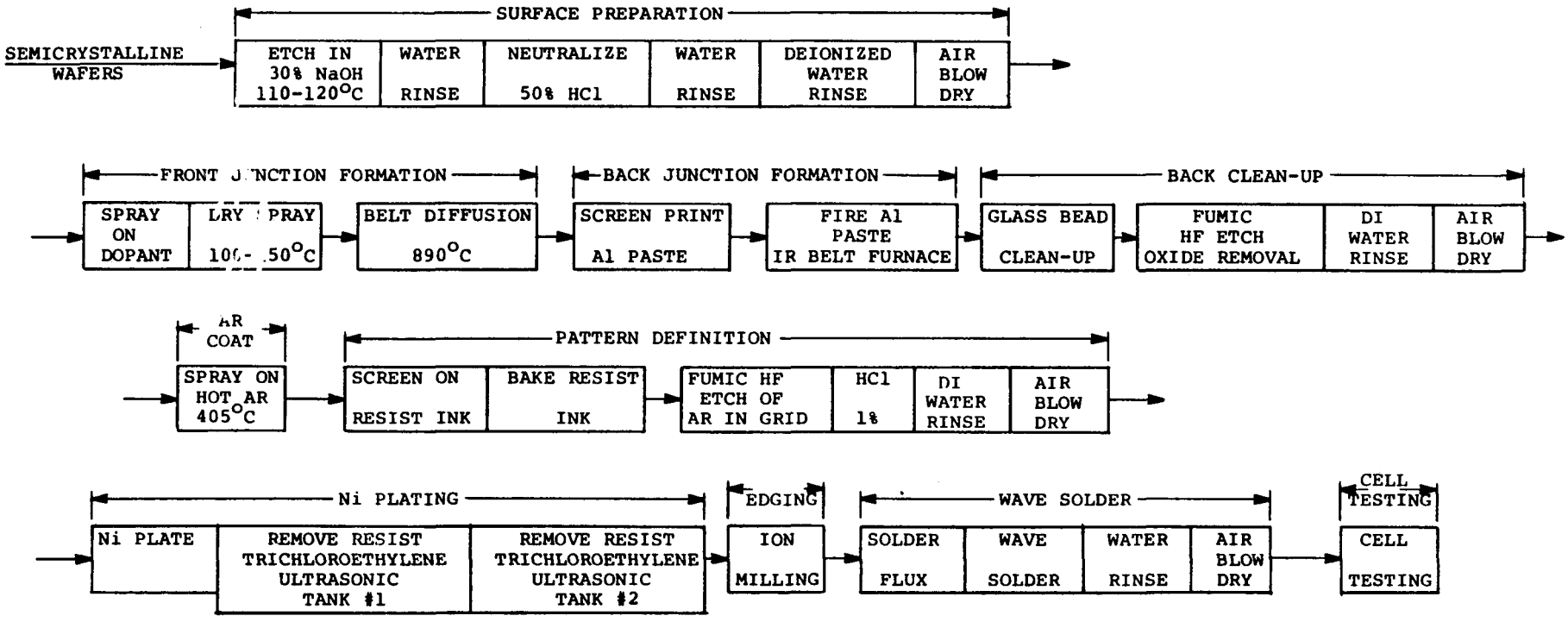


FIGURE 27

SOLAREX MEPSDU BASELINE PROCESS SEQUENCE FLOW CHART

TABLE #2

EQUIPMENT VENDORS

WAFER HANDLING	Kinematics PROA DeHaart AMI
ETCH SYSTEM	Conveyor Engineering Frederick Manufacturing Western Technology Crest Ultrasonics
SPRAY COATERS	ITI Advanced Concepts Corporation
BELT FURNACES	BTU Engineering Thermco Infrared Furnace Systems
SCREEN PRINTERS	AMI DeHaart
SAND BLASTING EQUIPMENT	MTI Empire
PLATING TRANSPORT SYSTEM	Conveyor Engineering Branson Corporation Crest Ultrasonics
WAVE SOLDER EQUIPMENT	Electrovert Hollis
PLASMA ETCH	Technics
XENON LIGHT SOURCE	Oriel Schoeffel Xenon Corporation

The cassettes are manually taken from the waiting area and loaded into the screen printer wafer unloader. The cells are then automatically removed from the cassettes and fed into the screen printer and from there into the paste firing operation as described in Section 4.1.4. At the end of the firing belt furnace the cells are automatically picked up off the belt and placed in cassettes which are then stored until needed.

The cassettes are next manually fed into another cassette unloader. This one automatically feeds a sand blasting system described in Section 4.1.5. The cells are automatically loaded back into cassettes after completion of the sand blasting.

The next step involves manually loading the cassettes into the oxide etch system which is described in Section 4.1.6. After manually unloading the cassettes from this system they are manually loaded onto the AR spray unloader. This unloader automatically places the cells three abreast on the belt of the AR spray system described in Section 4.1.7. At the end of the AR system the cells are automatically placed back into cassettes and the cassettes stored.

The cassettes are manually loaded into the screen printer unloader which feeds them automatically into the resist screen printer and then through a belt furnace to cure the resist ink as described in Section 4.1.8. They are then automatically

unloaded off the belt back into cassettes and stored. The cassettes are then manually loaded into the etch, rinse, Ni plate, and resist remove system through which they are automatically transported as described in Section 4.1.9. The cassettes are then manually removed from the etch system and placed in a stack loader, which removes the cells from the cassettes and puts them into stacks of approximately 1,000 cells. These stacks are then manually loaded into the ion milling machine described in Section 4.1.10.

After completion of ion milling the stacks are manually transferred to the wave solder machine. The wave solder machine is fed automatically by a stack loader. Section 4.1.11 describes the wave solder machine. From the wave solder machine the cells are automatically loaded into cassettes and stored ready for test. For cell test the cells are automatically unloaded from the cassette and fed into the cell test system described in Section 4.1.12. Finally the cell test system automatically loads the cells into cassettes sorted by some predetermined efficiency requirement. The cells are then stored in cassettes until needed for the paneling operation.

4.1.1 Cassette Load - Unload Equipment

The requirements for cassette load-unloader equipment for the Solarex MEPSDU were:

1. Load from stacks into cassettes.

2. Unload from cassette onto belt three abreast.

3. Pick wafer from belt three abreast and reload into cassettes.

4. Unload from cassette into screen printer.

5. Pick wafers from belt three abreast and reload into cassettes.

6. Unload from cassette into sand blast equipment.

7. Pick wafer from sand blast belt and reload into cassettes.

8. Unload from cassette onto belt three abreast.

9. Pick wafers from belt three abreast and reload into cassettes.

10. Unload from cassettes into screen printer.

11. Pick wafers from belt three abreast and reload into stacks.

12. Feed cells from stacks into the wave solder machine.

13. Reload cells into cassettes from wave solder machine.

14. Unload from cassettes into cell test system.

15. Reload cells into cassettes from cell test system.

There are really only two general machines which can be described as:

1. Unload wafer from cassettes (or stack) and place wafer on process machine either singly or three abreast.

2. Pick wafers from unloading area of processing machine either singly or three abreast and place wafers in cassettes (or stacks).

Because of the large throughput (1,000 wafers per hour) and the need to minimize labor, several constraints were placed on the load-unload system.

- Load-unload must be a continuous process with no time lags to reject cassettes.

- Multiple (at least) five cassettes can be loaded at one time.

- Rejected empty cassettes and newly filled cassettes must automatically be removed from the machine into a storage area.

These requirements led us to disqualify most of the load-unload systems built for the semiconductor industry. The four potential suppliers listed in Table 2 have machines designed specifically for automated photovoltaic application. Each machine continuously feeds cassettes with no time lags for cassette rejection. Each unloader takes the cell from the cassette slot and places it at an accurate predetermined position, either a perpendicular belt for obtaining a three abreast configuration or directly into another piece of equipment such as a screen printer, wave solder machine or sand blast system. Each of the suppliers will provide an integrated system for picking up three abreast and placing them on a belt or in reverse picking up three wafers abreast and aligning them to individually feed into the cassette loader.

The throughput rate of each of these machines is about 1,000 per hour. This was consistent with the MEPSDU throughput. In some cases like belt sprayers a faster

throughput can be obtained by using three cassette unloaders rather than one unloader with an attachment to place them three abreast.

4.1.2 Etch Machine

The machine basically consists of a number of tanks for etching, rinsing and neutralizing and a transportation system for moving the cassettes through the system. While a number of commercial etch systems were available none of them met our unique requirements. The problems associated with the required system are:

- A violent reaction occurs when the silicon is placed in the boiling sodium hydroxide. The equipment must be designed to minimize boil over and to protect equipment and personnel from this boil over.

- The high throughput requirements mean the machine must be capable of neutralizing and disposing of the spent sodium hydroxide and replacing it with a new mixture of preheated sodium hydroxide.

These requirements can only be met by engineering a system specifically for this use.

4.1.3 Diffusion Equipment

The diffusion equipment consists of a dopant sprayer, a belt diffusion furnace and a mechanism for transporting the cells from one belt to another. The dopant sprayer is a commercially available product designed specifically for this application. Belt furnaces are also commercially available. The selection of model depends on our desire to diffuse three cells abreast at a transient time of ten to twelve minutes in the hot zone at a temperature of 860 to 890^{o}C.

4.1.4 BSF Formation

The BSF formation equipment consists of a screen printer that automatically removes the wafers and feeds them into a paste curing and firing belt furnace. The screen printer is commercially available from a number of sources. The printer must be able to handle 10cm x 10cm wafers at a throughput of 1,000 hours. It has an automatic alignment and paste dispensing systems. Once the wafer has been screened,

the printer removes it from the chuck and feeds it onto the belt. The paste requires a low temperature bake to cure the paste and then a short 850°C firing. IR furnaces are best suited for providing this type of profile. Such IR furnaces especially designed for this paste firing are commercially available.

4.1.5 Sand Blasting

Deflashing systems are commercially available. For this application the machine must be able to deflash the wafers using glass balls, recollect the balls, filter them and recharge the media for continuous operation. All of these functions are available in commercial machines. What must be engineered is the wafer transport system. Wafers must be carried through the machine after being fed by the cassette unloader. The front of the cell must not be exposed to the deflashing media. In addition the fragile nature of the wafers requires that they be securely held in place during the deflashing operation or they may vibrate and break. This of course must be accomplished without shadowing any of the cell back.

4.1.6 Oxide Etch

The oxide etch system consists of a cassette transport mechanism amd chambers in which the cassettes pass. One chamber has fumic HF which is automatically filled to a specified level. A second chamber is for spray rinsing and a third for blow drying with warm air. A number of transport systems are commercially available for this requirement and the chambers can be adapted to this use.

4.1.7 AR Spray

The AR spray system is similar to the dopant spray system but requires preheating of the wafers to about 405^{o}C. Such a preheat option can be supplied in some of the commercially available units. Various belt widths are available. We have chosen one wide enough to hold three cells across.

4.1.8 Resist Print

The resist can be printed by a screen printer identical to the one required to print the Al paste BSF. The printer then must automatically remove the wafer from the chuck and feed it to a small commercial

belt furnace on which the resist ink is cured. Once again a belt three wafers wide is recommended to provide the necessary throughput without using a very long furnace.

4.1.9 AR Etch, Nickel Plating and Resist Removal

The AR etch process is virtually identical to the oxide etch and can be performed in a machine built to the same specifications. The nickel plating and resist removal system is similar in concept to the etch machine, namely a number of tanks and a transport mechanism to move the cassettes through the system. The complexity of this system is in the number of different steps with varying times and the operating parameters of the various baths. The nickel plating solution must be automatically maintained at a particular temperature and level. The resist removal is done in two consecutive ultrasonic tanks. The solvent must be automaticaly filtered and replaced to maintain a continuous throughput. Such a system must be engineered to meet these requirements.

4.1.10 Ion Milling

Ion milling machines are standard commercial products. One must specify the required mill area, in this case approximately 10.5cm x 10.5cm, the milling ions in this case inert argon and the operational parameters, i.e., voltage and beam current. Our efforts were halted before determination of these parameters.

4.1.11 Wave Soldering

A wave solder machine is a standard commercial product. The unit should contain a foam fluxer module, a solder module with air knife, a wave cleaner (water rinse) and a drier. The only unique requirement is the transport mechanism. Of the two options, pallet and direct conveyor, pallet is probably easier to engineer but less likely to meet the throughput goals. A conveyor system may be a modified version of those used for circuit boards. The entire system can be designed at widths to allow for soldering a number of wafers at the same time.

4.1.12 Cell Test System

The cells are unloaded from a cassette, transported on a belt, optically scanned to assure that the contact pads are in place, placed on a temperature controlled test block, illuminated by a Xenon source, a light I-V curve taken, and the good cells loaded back into cassettes. A block diagram of the test system is presented in Figure 28. The Cell Test Subsystem Components and the Data Flow are shown in Figure 29. The components are recommended based upon their use in similar test systems now in operation. The computer controlled testing will follow the flowchart overview shown in Figure 30.

4.2 MEPSDU Module Facility

The module part of the facility consists of three parts, a tabbing and stringing machine, a module lay-up machine and module test equipment. Each is described in the subsections below. It should be noted that the module equipment design was not as complete as cell equipment design because the module effort was terminated six months earlier than termination of the cell equipment design. One area in which no equipment was adequately identified was the processs of applying the insulator tape to the back of the cell.

FIGURE 28

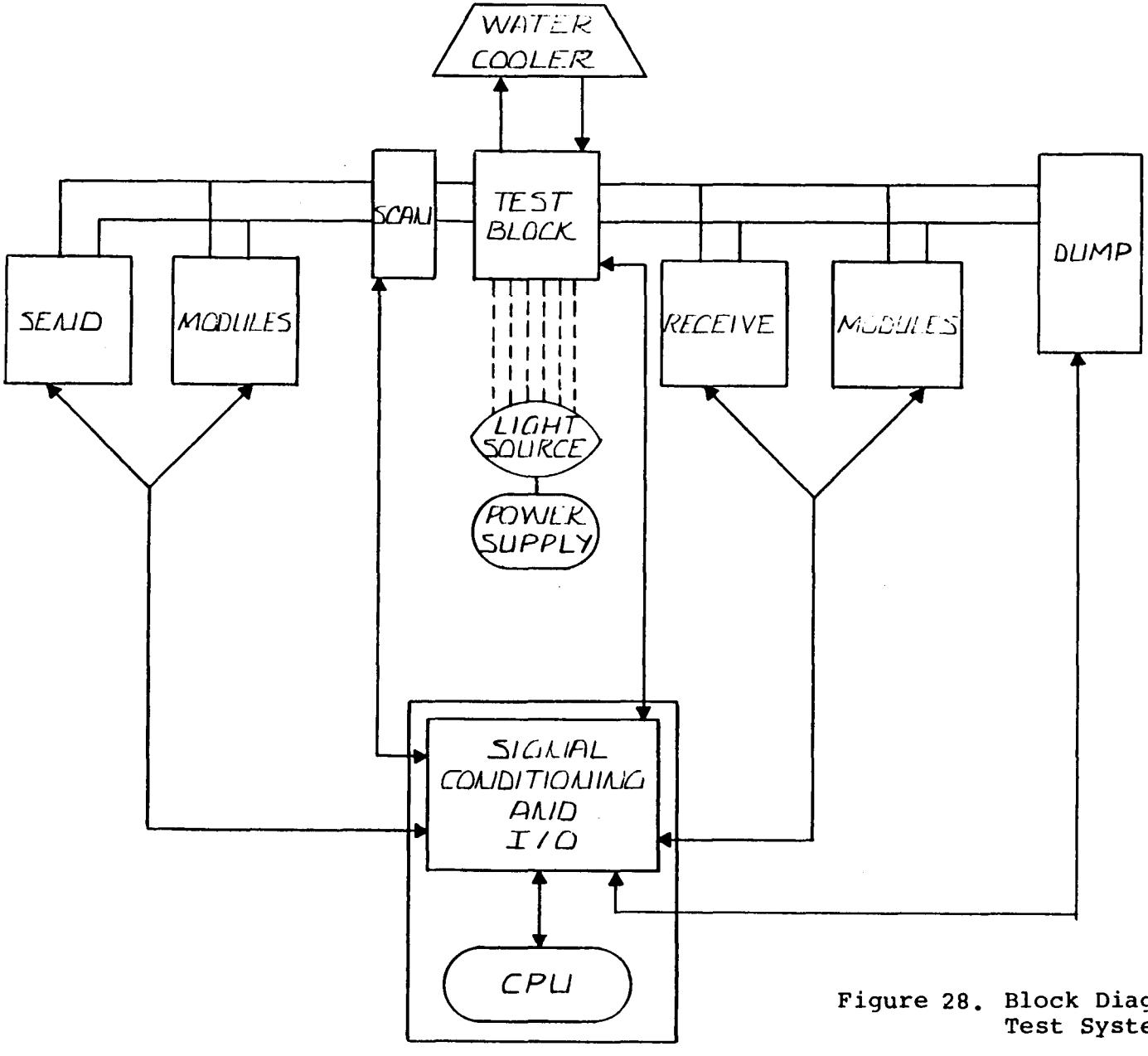


Figure 28. Block Diagram of Test System

FIGURE 29

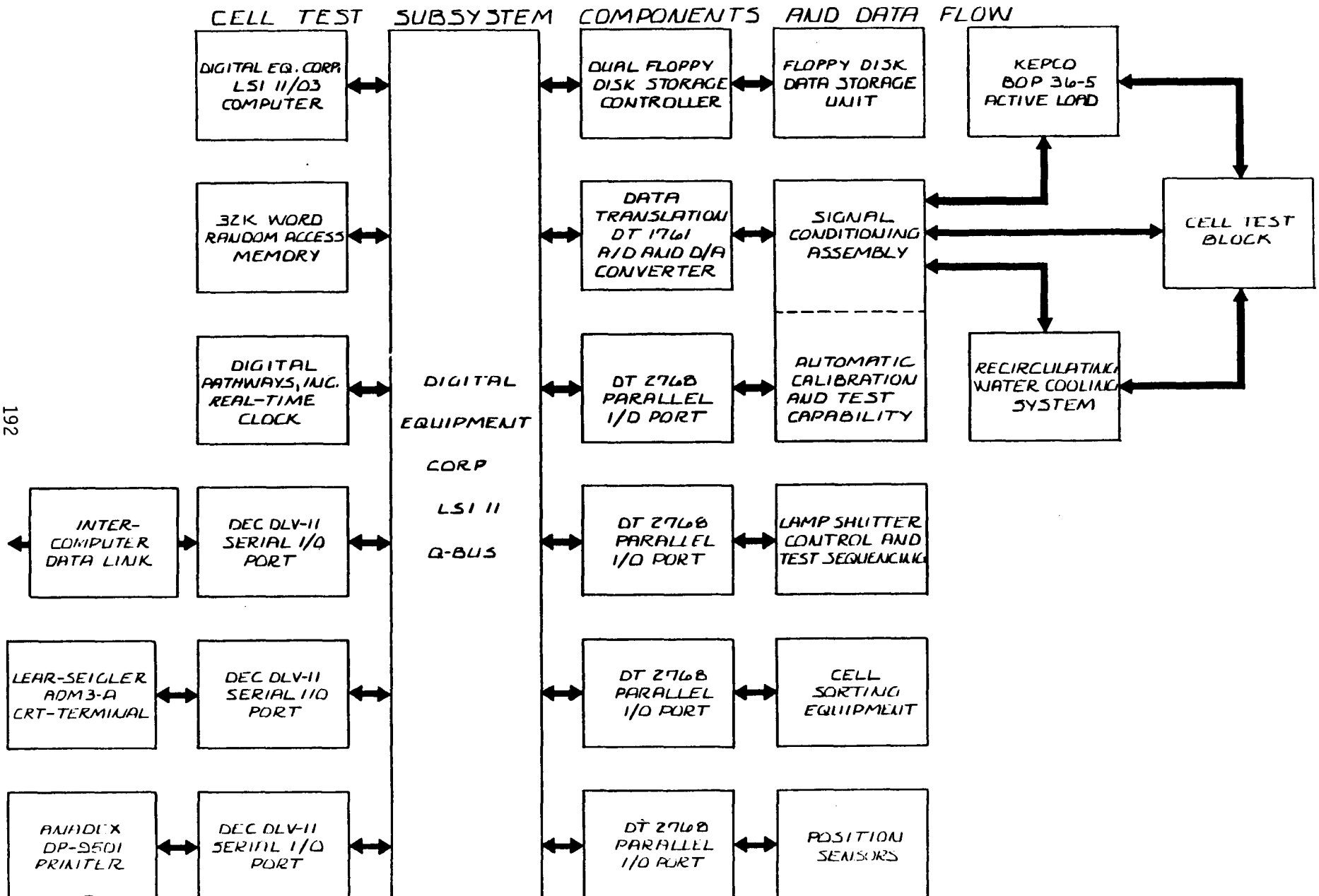
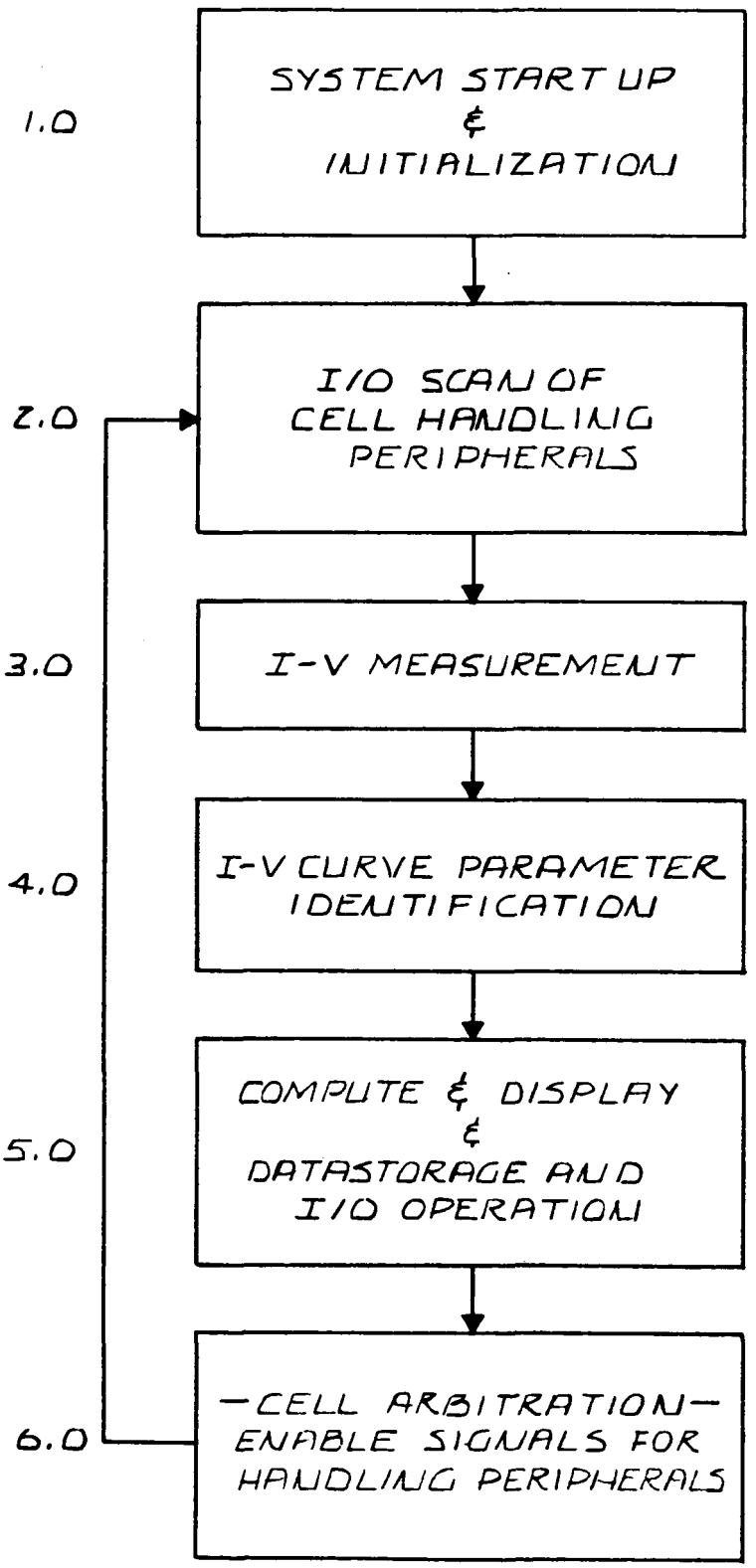

CELL TEST SUBSYSTEM COMPONENTS AND DATA FLOW
DIGITAL EQ. CORP. LSI 11/03 COMPUTER
32K WORD RANDOM ACCESS MEMORY
DIGITAL PATHWAYS, INC. REAL-TIME CLOCK
INTER-COMPUTER DATA LINK
LEAR-SEIGLER ADM3-A CRT-TERMINAL
ANADEX DP-9501 PRINTER
DEC DLV-11 SERIAL I/O PORT
DEC DLV-11 SERIAL I/O PORT
DEC DLV-11 SERIAL I/O PORT
DEC DLV-11 SERIAL I/O PORT
DIGITAL EQUIPMENT CORP LSI 11 Q-BUS
DUAL FLOPPY DISK STORAGE CONTROLLER
DATA TRANSLATION DT 1761 A/D AND D/A CONVERTER
DT 2768 PARALLEL I/O PORT
DT 2768 PARALLEL I/O PORT
DT 2768 PARALLEL I/O PORT
DT 2768 PARALLEL I/O PORT
FLOPPY DISK DATA STORAGE UNIT
SIGNAL CONDITIONING ASSEMBLY
AUTOMATIC CALIBRATION AND TEST CAPABILITY
LAMP SHUTTER CONTROL AND TEST SEQUENCING
CELL SORTING EQUIPMENT
POSITION SENSORS
KEPCO BOP 36-5 ACTIVE LOAD
CELL TEST BLOCK
RECIRCULATING WATER COOLING SYSTEM

FIGURE 30

CELL MEASUREMENT OVERVIEW FLOWCHART



4.2.1 Tabbing and Stringing Machine

Solarex funded two designs for the tabbing and stringing machine, one by Kulicke and Soffa Industries and a second by MB Associates. Each will be described briefly.

Kulicke and Soffa Industries design was based upon their early effort for JPL (19) in which they built a linear machine for tabbing 4" round cells and series interconnected them. The machine they designed for Solarex would assemble the 10cm square solar cells into series connected strings, and place the strings in a module array format. The machine should accomodate the module layout described in Section 2.3 including the use of wraparound contact. The target machine cycle time was five seconds per cell with a yield of 95% or better. The bonding technique to be used was pulsed heat solder reflow.

Figure 18 showed a flow diagram for the proposed machine. In the proposed machine, cells would be automatically dispensed from cassettes and aligned prior to entering the machine. A walking beam conveyor system, which maintains cell registration,

transports the cells through the various initial process stations.

The cells could first enter an insulating station that applies strips of adhesive backed tape to the back of each cell.

Next, a fluxing station applies flux to bond sites on the top side of each cell using a stamp pad technique or metered dispensing system. The cells would then enter the interconnect stations, where the one-piece stamping interconnects are fed, sheared, and transferred into position over the cells, then solder bonded to each cell using a pulsed heat bonding technique.

After interconnects are bonded to the cell face, the conveyor moves each cell to an inverter station, which turns the cells over (upside down) prior to the stringing operations. An interconnect foldover station then positions each cell and folds the interconnect over to the cell back for series bonding operations. The cells are then transferred onto a string conveyor, which maintains inter-cell registration while indexing the cells through the stringing operation to the discharge area of the machine.

The cells would then enter a second fluxing station, which applies flux to the cell back, and proceed to the second interconnect stations, where the cells are joined together into strings. A string pickup and transfer station would automatically pick up completed strings and place them in the module array area where strings are manually connected. One option for this design is to have the machine make double strings bonded in parallel with buss bars attached. These double strings would have to be manually aligned and soldered together.

The MB Associates machine design was based on the one they developed for JPL (20).

The solar module assembly system proposed by Tracor MBA consists of an indexing conveyor flanked on both sides by a Unimate 500 Series PUMA robot (Figure 30). Each robot assembles half the module and, in addition to placing and soldering each cell, also terminates each string to the parallel bus and installs the Solarlok output buss bars. The system, as shown in Figure 31, represents the position just after the conveyor has indexed and both robots are reached for their first cell.

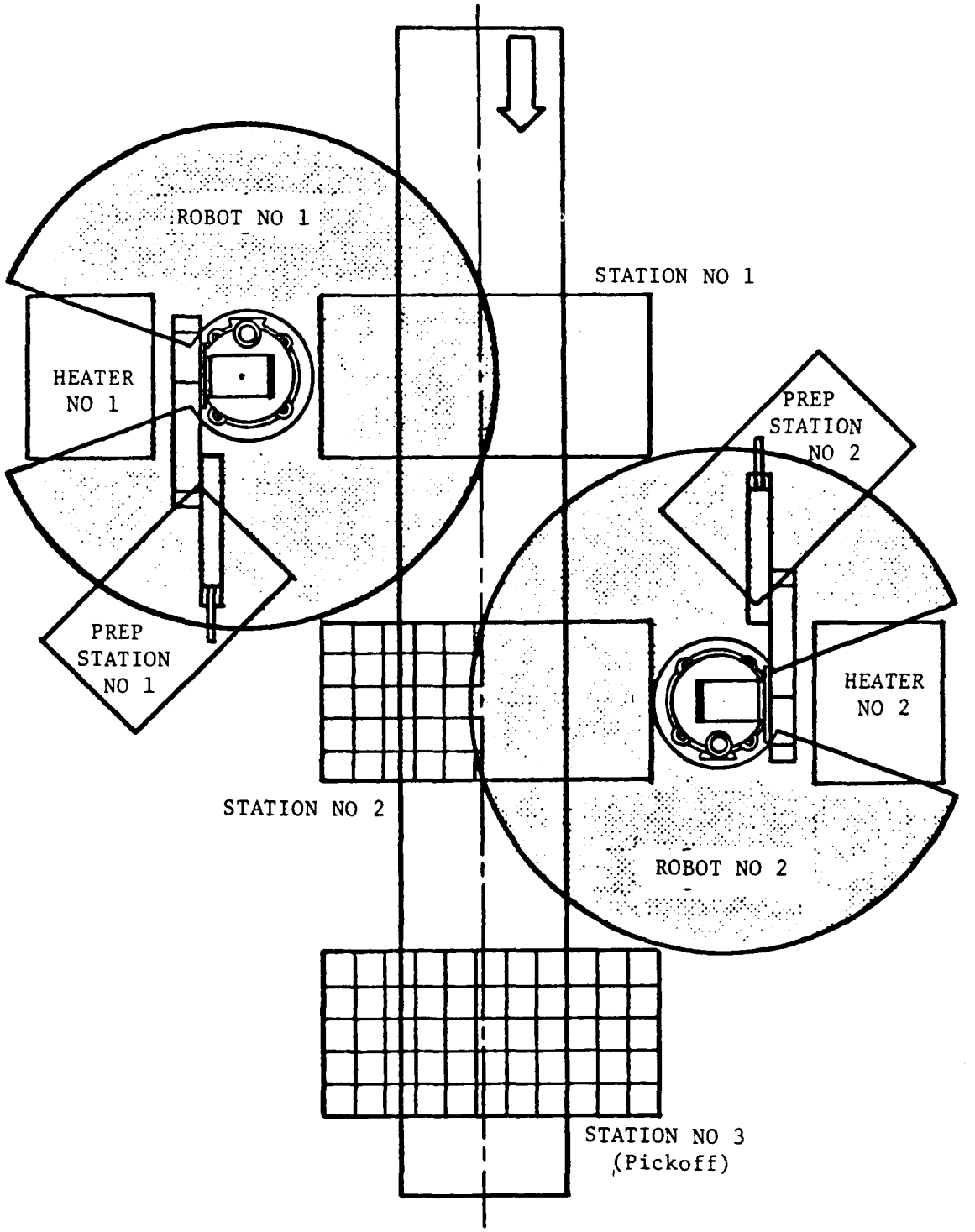


FIGURE 31

MB ASSOCIATES MODULE ASSEMBLY SYSTEM

The cell interconnections are made using a short pulse resistance heating technique with four electrodes mounted in the cell preparation pad and five electrodes mounted in the end effector of the robot arm.

The heart of this system is the Tracor MBA designed cell preparation station which, as its name implies, prepares the cell for assembly into the module by unloading it from the cassette, aligning it and dispenses, cuts, fluxes, positions and folds the interconnect leads. The robot then picks up this fully prepared cell using a Tracor MBA designed end-effector (the robot's "hand") and places it in the module. As it places the cell in the module it bonds the interconnects. The result is a fully laid up module ready for lamination.

4.2.2 Module Lay-Up and Encapuslation Machine

The process sequence for module encapsulation was shown in Figure 20. The glass cleaning, drying and priming was to be performed on a conveyor belt with chambers built to steam clean, dry and a spray on the primer. The various sheets of EVA, Craneglass and

polyethylene can be cut on a commercially available sheeter or a machine especially designed for that purpose (27).

The key piece of encapsulation machinery is the laminator. The process sequence required for lamination is well known (see Section 2.4.8 and Reference 3). Laminators for this process are commercially available. The key to their utility is the cycle time. The standard procedure requires a thirty minute cycle in the laminator so the capital equipment cost is quite high. Lamination of multiple modules at the same time or an extremely fast lamination cycle (say five minutes) with a low cost oven for post care are two possible solutions to this problem.

4.2.3 Module Test

The modules are manually loaded onto a light table and connected electrically to the system. The operator then initiates the computer, which draws the I-V curve, stores the data, and prints out a label for the module, including the model number, serial number and power measured at the design voltage. The operator then disconnects the module, applies the

label and places the module on a storage rack. The light source will be twelve 1,000 watt quartz lamps with individual variac controls for each lamp. The light intensity will be set using 18 calibrated solar cells. Module measurements will be periodically checked with sunlight and Xenon flash simulator measurements to assure the correct calibration.

A block diagram of the Module Test System is given in Figure 32. The module test subsystem components and the data flow are shown in Figure 33. The components are recommended based upon their use in similar test subsystems now in operation.

MODULE TEST SYSTEM

PROCESS SEQUENCE

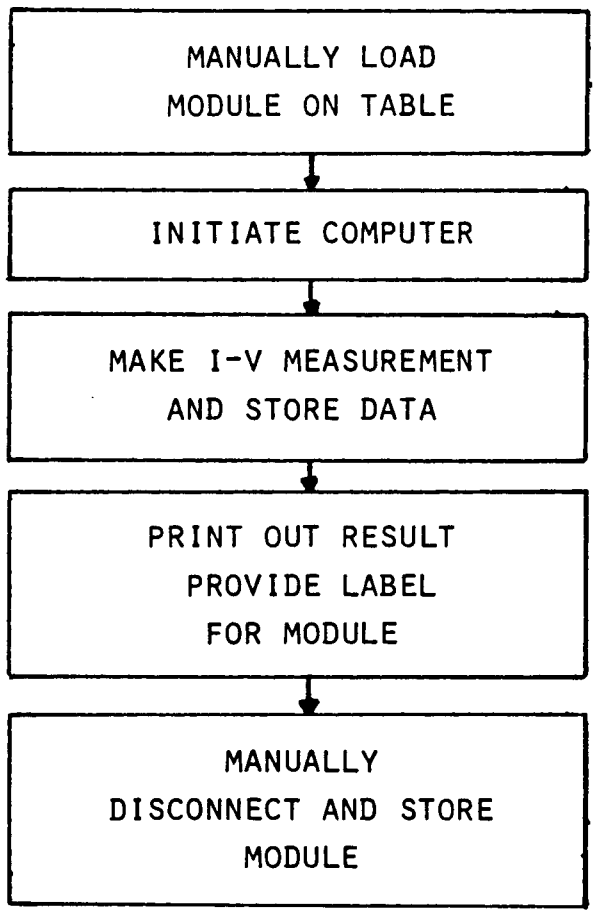
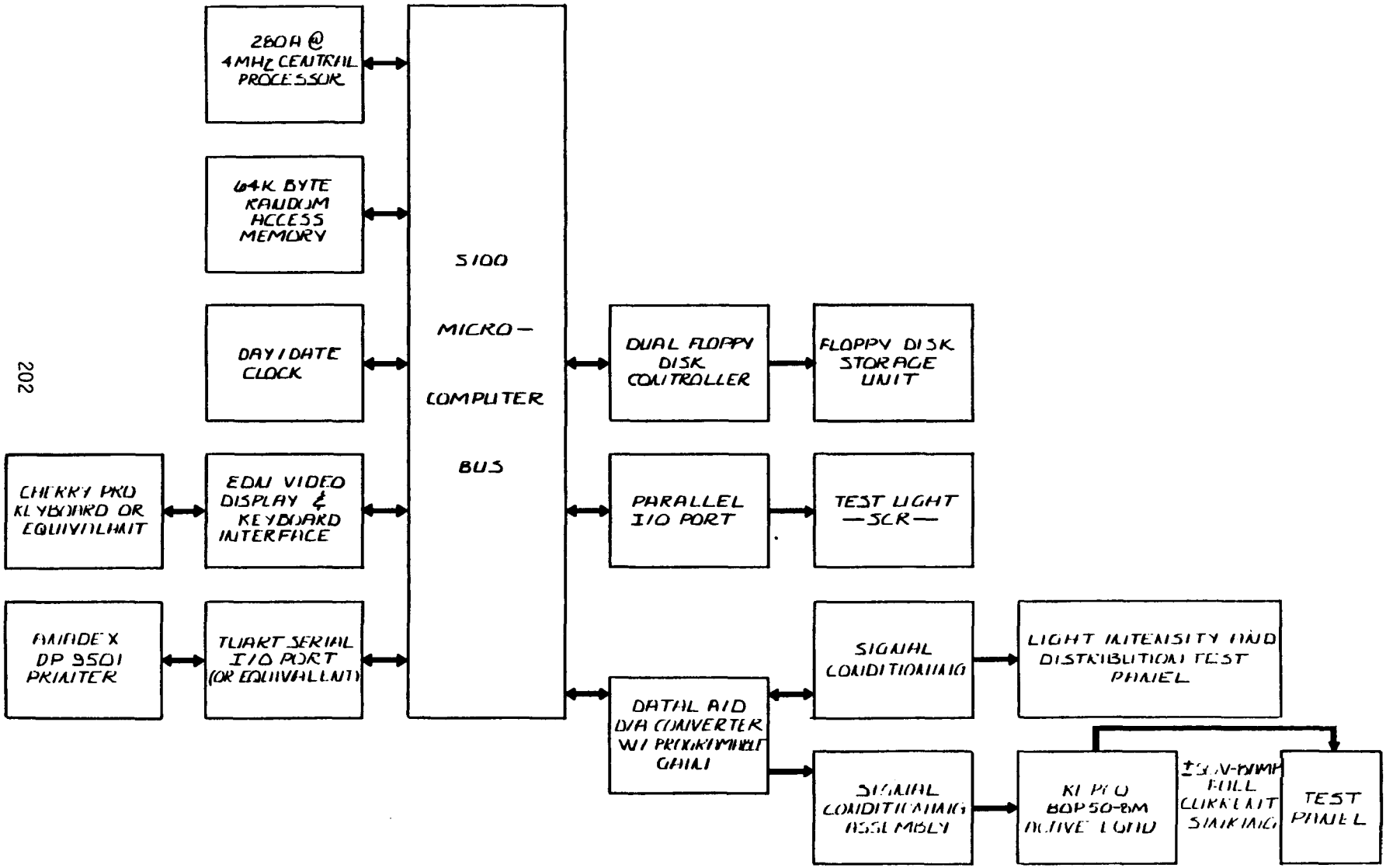


FIGURE 32

FIGURE 33

PANEL TEST SUBSYSTEM COMPONENT AND DATA FLOW



5.0 SAMICS COST ANALYSIS

A cost analysis has been performed for the 6.6 MW/yr output MEPSDU pilot line. An IPEG 2 (26) methodology was utilized to obtain the estimated cost. Since the module fabrication efforts were terminated before the cost analysis was performed, the analysis was performed only for cell fabrication. Since this process sequence is not limited to Semix semicrystalline silicon, the silicon cost was taken out of the total. The calculation then will be for the add-on cost to manufacture solar cells. Because an 80% cell process yield was utilized, the add-on cost should include an additional 25% of the initial wafer cost.

The calculations are based upon:

- 10% efficient cells
- 80% yield - wafer to finished cell
- 3 shifts/day
- 345 days/yr operation
- Production of 1,000 good cells/hr

Table 3 lists the required materials for cell fabrication, the amounts needed per wafer, the cost of the materials, the calculated cost per wafer, the number of wafers processed per year and the total item cost per year.

TABLE #3

		AMT/WAFER	COST/AMT $	COST/WAFER $	# WFRS/YR	COST/YR $
ETCH	NaOH	.01 Kg	.18 Kg	1.8 E-3	8.25 E-6	14850
	HCl	.0011 liter	1.13/l	1.2 E-3	8.25 E-6	10255
DIFFUSION	Dopant	.64 cm^3	.0092/cm^3	6 E-3	8.15 E-6	48900
BSF	Al Paste	.65 m^3	.002/gm	3.5 E-3	8.05 E-6	28175
	Screens	5 E-5	55/ea	2.75 E-3	8.05 E-6	22138
	Squeegee Blades	3.75 E-4	2.4/ea	8.3 E-4	8.05 E-6	6704
BACK CLEANUP	Glass Beads	2 E-4 lbs	1/lb	2 E-4	7.95 E-6	1590
	HF 70%	1. ml	.67/lb	2 E-3	7.95 E-6	15900
AR COAT	Titanium Isopropoxide	.65 cm^3	.0143/cm^3	9.3 E-3	7.86 E-6	73098
PATTERN PRINT	Colonial Ink	2 cm^3	.0131/cm^3	2.6 E-2	7.76 E-6	203310
	Screens	1.7 E-4	55/ea	9.4 E-3	7.76 E-6	72556
	Squeegee Blades	3.75 E-4	2.4/ea	8.3 E-4	7.76 E-6	6441
Ni PLATE	HF 70%	1.0 ml	.67/lb	2 E-3	7.67 E-6	15340
	Electroless Ni	.005 gal	5./gal	2.5 E-2	7.67 E-6	191750
	Trichloroethylene	4.5 E-4 gal	21.73/gal	9.8 E-3	7.67 E-6	75000
ION MILLING	Filaments	1.25 E-4	5./ea	6.2 E-4	7.5 E-6	4650
	Oil	1.4 E-6 gal	100/gal	1.4 E-4	7.5 E-6	1050
	Argon	4E-7 tank	60/tank	2.4 E-5	7.5 E-6	180
WAVE SOLDERING	Solder	.1 cm^3_3	5.18/lb_3	8.6 E-3	7.33 E-6	63038
	Flux	.5 cm^3	.002/cm^3	1 E-3	7.33 E-6	7330
						862255

MATERIALS REQUIREMENTS FOR MEPSDU

Table 4 lists the required utilities, their usage rate, the amount needed per wafer, the cost of the utilities, the cost per wafer, the number of wafers processed per year and the total item cost per year.

Table 5 presents equipment costs and lifetimes, square footage used, the number of workers needed, the direct labor costs, the total materials cost (from Table 3) and the total utilities cost (from Table 4).

Table 6 presents the cost data in a format which reflects the IPEG2 equation (26).

$$\text{cost} = \frac{(C_i^* \times \text{EQPT})+(109 \times \text{SQFT})+(2\ 1\ \text{DLAB})+(1.2\ \text{MATS})+(1.2\ \text{UTIL})}{\text{QUAN}}$$

(*Coefficients C_i are presented in Table 7 as taken from Reference 27) and tabulates the costs by category and process step.

The result is a cell process add-on price of $0.5570 per peak watt in 1980 dollars. This is well below the add-on price being paid today, but is not consistent with the $0.70 per watt price goal for the entire module. It is clear that scaling this line up will lead to appreciable cost savings. The following costs savings should be realized in scaling to a 25 to 50 MW per year factory.

TABLE #4

UTILITIES USAGE AND COST FOR MEPSDU

		USEAGE RATE	AMT/ WAFER	COST/AMT $	COST/WAFER $	# WAFERS/ YR	COST/YR $	ELEC COST/ YR $	VENT COST/ YR $	AIR COST/ YR $	COOLING H_2O COST/YR $	TAP H_2O COST/YR $	DI H_2O COST YR $
ETCH	Elect	20 KW	.016 KW hr	.047/KW hr	7.5 E-4	8.25 E6	6204.	6204.					
	Vent	2000 cf/m	96 ft^3	.0000047/ft^3	4.5 E-4	8.25 E6	3741.		3741.				
	Tap H_2O	8 cf/h	.0064 ft^3	.0098/ft^3	6.3 E-5	8.25 E6	517.					517.	
	DI H_2O	9.9 cf/h	.0079 ft^3	.263/ft^3	2.1 E-3	8.25 E6	17424.						17424.
DIFFUSION	Elect	43 KW	.034 KW hr	.047/KW hr	1.6 E-3	8.15 E6	13024.	13024.					
	Vent	1600 cf/m	77.7 ft^3	.0000047/ft^3	3.6 E-4	8.15 E6	2993.		2993.				
	Air	15 cf/m	.729 ft^3	.00039/ft^3	2.8 E-4	8.15 E6	2290.			2290.			
BSF	Elect	19.5 KW	.0157 KW hr	.047/KW hr	7.4 E-4	8.05 E6	5940.	5940.					
	Vent	600 cf/m	29.2 ft^3	.0000047/ft^3	1.4 E-4	8.05 E6	1105.		1105.				
	Air	10 cf/m	.486 ft^3	.00039/ft^3	1.9 E-4	8.05 E6	1526.			1526.			
BACK CLEANUP	Elec	2 KW	.00166 KW hr	.047/KW hr	7.8 E-5	7.95 E6	620.	620.					
	Vent	3000 cf/m	149 ft^3	.0000047/ft^3	7.0 E-4	7.95 E6	5567.		5567.				
	Air	272 cf/m	13.5 ft^3	.00039/ft^3	5.2 E-3	7.95 E6	41856.			41856.			
	DI H_2O	9.6 cf/h	.008 ft^3	.263/ft^3	2.1 E-3	7.95 E6	16695.						16695.
ARC	Elect	31 KW	.125 KW hr	.047/KW hr	1.2 E-3	7.86 E6	9235.	9235.					
	Vent	1200 cf/m	59.8 ft^3	.0000047/ft^3	2.8 E-4	7.86 E6	2209.		2209.				
	Air	15 cf/m	.75 ft^3	.00039/ft^3	2.9 E-4	7.86 E6	2299.			2299.			
RES PRINT	Elect	11.25 KW	.00956 KW hr	.047/KW hr	4.5 E-4	7.76 E6	3486.	3486.					
	Vent	600 cf/m	36.6 ft^3	.0000047/ft^3	1.4 E-4	7.76 E6	1116.		1116.				
	Air	10 cf/m	.51 ft^3	.0039/ft^3	2.0 E-4	7.76 E6	1543.			1543.			
Ni	Elect	14 KW	.012 KW hr	.047/KW hr	5.6 E-4	7.67 E6	4325.	4325.					
	Vent	7200 cf/m	372 ft^3	.0000047/ft^3	1.8 E-3	7.67 E6	13410.		13410.				
	Di H_2O	.26 cf/m	.0134 ft^3	.263/ft^3	3.5 E-3	7.67 E6	26979.						26979.
	Cooling H_2O	.5 cf/m	.0258 ft^3	.0027/ft^3	7.0 E-5	7.67 E6	534.				534.		
ION MILLING	Elect	7.5 KW	.0066 KW hr	.047/KW hr	3.1 E-4	7.5 E6	2326.	2326.					
	Air	.01 cf/m	.005 ft^3	.00039/ft^3	1.9 E-7	7.5 E6	1.			1.			
	Cooling H_2O	.134 cf/m	.0070 ft^3	.0027/ft^3	1.9 E-5	7.5 E6	141.				141.		
WAVE	Elect	14.25 KW	.0128 KW hr	.047/KW hr	6.0 E-4	7.33 E6	4409.	4409.					
	Vent	600 cf/m	32.4 ft^3	.0000047/ft^3	1.5 E-4	7.33 E6	1116.		1116.				
	Air	2 cf/m	.108 ft^3	.00039/ft^3	4.2 E-5	7.33 E6	308.			308.			
	Tap H_2O	7 cf/m	.0063 ft^3	.0098/ft^3	6.1 E-5	7.33 E6	452.					452.	
TEST	Elect	3 KW	.0028 KW hr	.047/KW hr	1.3 E-4	7.17 E6	943.	943.					
	Vent	100 cf/m	5.52 ft^3	.0000047/ft^3	2.6 E-5	7.17 E6	187.		187.				
TOTAL						6.6 E6	194521.	50512.	31444.	49823.	675.	969.	61098.

TABLE #5

EQUIPMENT, SQUARE FOOTAGE, LABOR AND MATERIALS COSTS FOR MEPSDU

	EQUIP	EQUIP LIFETIME YRS	FT^2	WORKERS/ SHIFT	DLAB	MATS/YR	UTIL/YR
ETCH	65,000	5	200	1	70400.	$ 25105	$ 27886
DIFFUSION	173,000	10	504	1	70400.	48900	18307
BSF FORM	83,000	10	328	1/2	33000.	57017	8571
BACK CLEANUP	138,000	3	288	1	70400.	17490	64738
AR COAT	104,000	10	224	1/2	33000.	73098	13743
RESIST PRINT	126,000	10	392	1	70400.	282307	6145
Ni PLATE	50,000	5	378	1	70400.	282090	45248
ION MILL	135,000	10	200	1	65686.	5880	2468
WAVE SOLDER	100,000	5	400	1	65686.	70368	6285
TEST	55,000	10	150	2	150543.	0	1130
	$1,029,000		3064 ft^2	10	$699,915./yr	$862,255/yr	$194,521/yr

TABLE #6

	Ci x EQUIP / 6.6 E-6	FT^2 x 109 / 6.6 E-6	2.1 x DLAB / 6.6 E-6	1.2 x MATS / 6.6 E-6	1.2 x UTIL / 6.6 E-6	TOTALS
ETCH	.0064	.0033	.0224	.0046	.0050	.0417
DIFFUSION	.0136	.0083	.0224	.0089	.0033	.0565
BSF FORM	.0065	.0054	.0105	.0104	.0016	.0344
BACK CLEANUP	.0174	.0048	.0224	.0029	.0118	.0593
AR COAT	.0082	.0037	.0105	.0133	.0025	.0382
RESIST PRINT	.0099	.0065	.0224	.0513	.0011	.0912
Ni PLATE	.0049	.0062	.0224	.0513	.0082	.0930
ION MILL	.0106	.0033	.0209	.0011	.0004	.0363
WAVE SOLDER	.0098	.0066	.0209	.0128	.0011	.0512
TEST	.0043	.0025	.0479	.0000	.0002	.0549
	.0916	.0506	.2227	.1566	.0352	.5567

ALL COSTS ARE EXPRESSED IN DOLLARS

IPEG2 COST DATA FOR MEPSDU

TABLE #7

IPEG2 CAPITAL EQUIPMENT COEFFICIENTS

EQUIPMENT LIFETIME	3	5	7	10	15	20
COEFFICIENT, C_i	.83	.65	.57	.52	.48	.46

- The MEPSDU pilot line was not designed as a balanced line, but rather was to use one piece of equipment per process to demonstrate the concept. Going to a balanced line and utilizing multiple machines will lead to a lower cost. The MEPSDU costs were based on quotations for one piece of equipment which included any engineering costs. Subsequent purchases of multiple machines should be made at a considerable cost savings. A preliminary estimate concluded that equipment costs could be cut by 50%.

- Factory design with multiple machines would result in reduced floor space requirements per wafer. This saving was estimated at 25%.

- Labor costs were based in most cases on one operator per process step. Using either larger production machines or identical multiple machines should lead to a 50% saving in labor cost.

- Minor savings in material would result from procuring an order of magnitude more material in a production setting. A 10% savings in material cost was estimated.

- Utility costs will reduce somewhat due to more efficient use of machines in a balanced line. A 10% cost reduction was estimated.

- A 10% cell efficiency was assured in the calculations. Developments in polycrystalline silicon production and in cell process should improve the cell efficiency. A 12% average cell efficiency seems within reach in the time frame of a 50 MW factory.

- An 80% yield was selected as a conservative estimate based on manual experience. A well automated line should increase this appreciably with 90% an obtainable goal.

Using these estimated effects on cost a cell add-on price of $0.274 per peak has been calculated as shown in Table 5-6. Using a estimated price of $0.30 per peak watt for the Semix silicon (2) and an estimated module add-on cost of $0.25 per peak watt (1) would yield a module selling price of $0.85 per peak watt. Based on the broad assumptions used in this calculation, it is encouraging to see that the result is reasonably close to the $0.70 per peak watt goal. The two major cost components in cell process are materials and labor. The use of more stringent process controls, recycling of some materials and even selling of waste products could result in significant reductions in the materials cost. Further developments in automation, i.e., automatic movement of cassettes from station to station could also lead to significant reductions in the direct labor costs. Finally further

TABLE #8

50 MW CELL PRICE ESTIMATE IN 1980 DOLLARS PER PEAK WATT

COST COMPONENT	FACTOR	PRICE PER PEAK WATT $	12% CELL VS 10% CELL	YIELD IMPROVEMENT 80% TO 90%
EQUIPMENT	0.5	0.046	0.038	0.034
FACILITY SPACE	0.75	0.038	0.032	0.028
DIRECT LABOR	0.5	0.111	0.093	0.083
MATERIALS	0.9	0.141	0.118	0.105
UTILITIES	0.9	0.032	0.027	0.024
TOTAL		0.368	0.308	0.274

MODULE PRICE:	CELL ADD-ON	=	0.27
	WAFER COST	=	0.30
	WAFER YIELD LOSS	=	0.03
	MODULE COST ADD-ON	=	0.25
	TOTAL		0.85

improvements in polycrystalline material could lead to a material that is capable of producing as efficient a cell as single crystal silicon, meaning average cell efficiencies as high as 14 or 15% may be obtainable. These development would almost assuredly mean that the 25 to 50 MW line would meet the $0.70 price goal.

6.0 CONCLUSIONS AND RECOMMENDATIONS

The main result of this effort was the identification of a process sequence that:

1. Has the potential for meeting the DOE cost goals when utilized in an automated mode for large volume production, and

2. Can be utilized today with mostly commercially available equipment to significantly reduce PV module costs.

To obtain this integrated process sequence it was necessary during the program to develop four new process steps, namely:

- Hot Spray AR Coating
- Glass Bead Back Clean-Up
- Wave-Soldering
- Ion Milling

Laboratory verification has been completed on the first three but is still to be finalized for ion milling.

These process steps can now be evaluated for their use in solar cell production. Solarex has purchased a wave solder machine and is still pursuing the hot sprayed AR process. The other two will fit into other process sequences to help reduce cost.

Of course the ultimate recommendation remains the original plan, that is to build a MEPSDU line and operate it to evaluate yields, material usage, performance parameters, etc. Much of the engineering and design has been done, but in certain areas like ion milling laboratory work still remains to be done before the equipment can be engineered. A MEPSDU pilot line could be operational within eighteen months with a yearly throughput of 6.6 MW. This line would be able to produce cells with a cell add-on cost of $0.50 per peak Watt, a significant improvement over the lines presently in operation.

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