ORNL/TM-5639
(Vol. 2 of ORNL/TM-5638)

ORELA Data Acquisition System Hardware

Vol. 2: Four-Channel Priority Multiplexers (Q-5036-1, -3, -12 through -25, and -29)

J. W. Reynolds

OAK RIDGE NATIONAL LABORATORY
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INSTRUMENTATION AND CONTROLS DIVISION

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ABSTRACT

This report describes programming, word formats, control signals, voltage levels, connector layouts, ground isolation, input level-matching, and a theory of operation with a simplified logic diagram for the Four-Channel Priority Multiplexer on the SEL 810B data acquisition computers at ORELA.

1. INTRODUCTION

The Four-Channel Priority Multiplexer[1,2] has a maximum data rate of 25,000 events/sec per channel (100,000 events/sec if only one channel is operating). Each channel transfers two 16-bit words into the computer memory via a direct memory access connection from the multiplexer. The Oak Ridge Electron Linear Accelerator (ORELA) Data Acquisition Routines (ODAR), a subset of the ORELA Data Acquisition Monitor System,[3] and the semirandom access fixed head disk[2,4] (maximum access rate is 11,140 channels/sec on DAC 1 and 2 and 14,790 channels/sec on DAC 3) reduce the system event rate to either 5000 or 8000 disk storage increments per second on DAC 1 and 2 or DAC 3 respectively.

A ground isolation module[5] (Dwg. No. Q-5036-25)* provides isolation of 10^{10} Ω for each of the signals into (32) and out of (3) a channel of the Four-Channel Priority Multiplexer. The four ground isolation modules and the multiplexer chassis are located in the Data Collection Equipment (DCE) Cabinet. See ORNL Instrumentation and Controls Division Dwg. No. Q-2928-2 for the DCE location on the computer equipment floor plan. Note that all cables from the experimenters are connected at a panel in the DCE on DAC 3.

The information contained herein is sufficient for the user to design an interface for his experimental equipment. It is assumed that he has a knowledge of electronics, digital control logic, and machine language programming[6] for SEL 810B computers. Further logic details can be obtained from Drawing Series Q-5036 as listed in Table 1 and Systems Engineering Laboratories, Inc. (SEL) *Technical Manual, Data Acquisition System*, vol. 1, Publication No. 315-219100-000, pp. 3-1 through 3-7. Note that the SEL TM does not contain the revisions for dual-word input on all four channels of the multiplexer and that it references SEL's obsolete drawing series 53320; however, the sequence of operation is valid. The sheet numbers correspond to the Drawing Series Q-5036 dash numbers.

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*See Sect. 9, Engineering Drawings, for a list of Q-drawings pertinent to the topics discussed in this volume. These drawings are available from the author.

Table 1. Four-Channel Priority Multiplexer drawing list

ORNL Drawing Series Q-5036
SEL Drawing Series 53320 with revisions, digital MUX

Number	Subtitle
-2	I/O Sync Logic
-3	Decode Unit 23
-12	Strobe Register
-13	Priority Part 1 (word A, B, C, & D — Channels 0 & 1)
-14	Priority Part 2 (word E, F, G, & H — Channels 2 & 3)
-15	Input Gates = A&B
-16	Input Gates - C&D
-17	Input Gates - E&F
-18	Input Gates - G&H
-19	Strobe Generator
-20	DTC Interface
	Logic Diagram, Unit 1R2
-21	I/O Bus Bits 0-3
22	I/O Bus Bits 4-7
-23	I/O Bus Bits 8-11
-24	I/O Bus Bits 12-15
	SEL 810B Multiplexer Isolation
-25	Ground Isolators, Drivers and Receivers
-26	Ground Isolators, Front and Rear Panels
-27	Multiplexer Input Ground Isolators, Drivers and Receivers
-28	Multiplexer Input Ground Isolators, Front and Rear Panels
	SEL 810B Multiplexer-Scaler Isolation
-29	Assembly, Four-Wide Nuclear Instrument Module for DEC A,K, R&M Series Logic Cards

2. PROGRAMMING

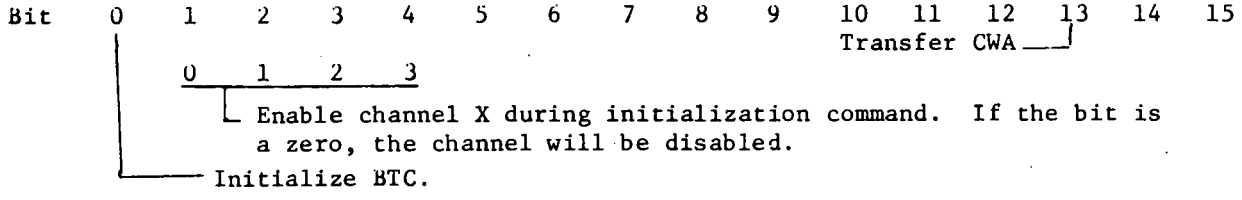
The multiplexer, unit '23, is an input device operating with Block Transfer Control (BTC). The hardware does not contain logic for test instructions (TEU) or word transfer input instructions (AIP or MIP). Three operating requirements should be followed:

1. The BTC complete interrupt level should be enabled before the BTC is initialized.
2. The word count for the BTC must be an even number; otherwise, the BTC complete gating will always generate a Multiplexer Error priority interrupt. The Multiplexer Error circuit detects that an odd number of words have been transferred to the computer either during the middle or at the end of a block transfer.
3. A second CEU '23 should not be executed until the BTC complete interrupt is received. The second CEU '23 will steal the multiplexer from the first CEU '23 before the first CEU terminates.

CAUTION: Pulse height data will not have a normal distribution if it is sent to the multiplexer with the same clock channel (e.g., a clock channel selected by a pulser).

2.1 CEU Second Word Format

The CEU second-word format[6] for the multiplexer is



All other bits are unassigned and should be set to zero so that any future modifications will not require a revision of all existing programs.

2.2 Multiplexer Error Interrupt

The occurrence of a Multiplexer Error interrupt is used by ODAR[3] to increment a double precision counter and to reset the multiplexer by issuing a CEU to initialize the multiplexer in the 7MUL routine of ODAR. The error rate is about 2×10^6 events/error with three independent experiments running, or 50×10^6 events/error with two experiments. The actual rate is dependent upon the relative data rates and their channel assignments.

2.3 Test Program

A test program, 8MPT, to display the input data in the A and B registers is given in Fig. 1. The program can be used when no one is taking data on the system. If possible, the data rate or the data should be adjusted to allow inspection of the registers. See Sect. 8, Maintenance, for a test program that can be run during data acquisition.

3. DATA WORD FORMATS

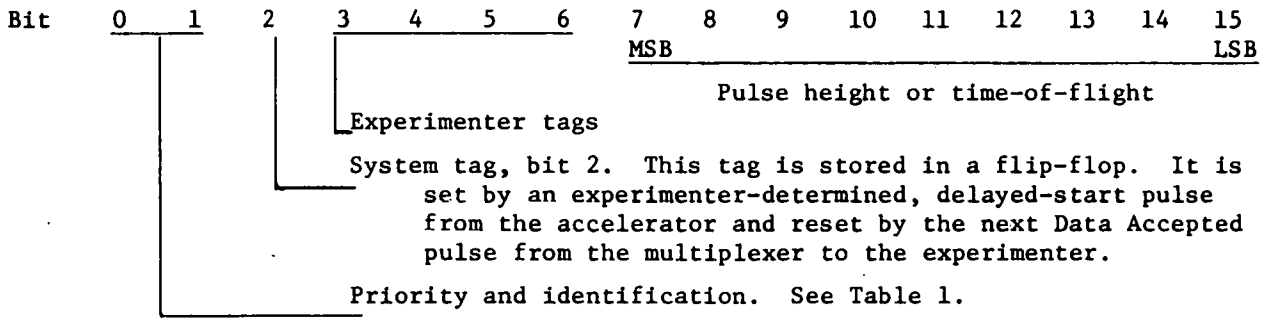
A Four-Channel Priority Multiplexer is the primary device for the input of experimental data to each SEL 810B data acquisition computer. Each channel, when activated, controls the input of two 16-bit computer words to the 810B memory. Although most of the bits are dedicated to data information, three are dedicated to specific tasks — two identification bits and a System Tag bit.

ORNL-DWG 76-15906

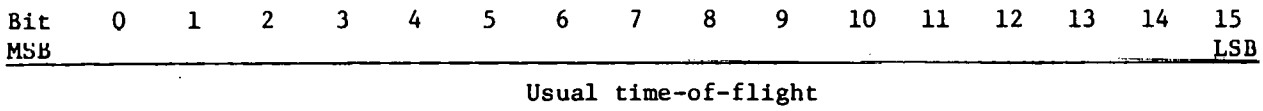
```
0001 00000                    *8MPT[106,1000]    3-27-73    MULTIPLEXER DISPLAY J.W.REYNOLDS  BLDG 6010
0002 00000                    *
0003 00000                    *     DISPLAYS THE 1ST WORD IN "A" & THE 2ND WORD IN "B"
0004 00000                    *     SET SENSE SWITCH 15 TO RETURN TO THE SYSTEM.
0005 00000                    *
0006 00000                          REL
0007 00000                          ORG   0
0008 00000  00000033          SYST  NOP
0009 00001  00000033          ME    NOP
0010 00002  12100003                SPB   MAP         GET CORE LOCATION OF PROGRAM.
0011 00003  13000000          MAP   ZZZ   **
0012 00004  00136021                PID               DISABLE BTC COMPLETE INTERRUPT
0013 00005  00000200                DATA  '200              GROUP 0 LEVEL 8
0014 00006  01100033                LAA   MPXL        SET THE LOCATION FOR BTC COMPLETE INTERRUPT.
0015 00007  05100003                AMA   MAP
0016 00010  03300030                STA*  MPIL
0017 00011  01100034                LAA   FWAL        GET FIRST WORD ADDRESS LOCATION
0018 00012  05100003                AMA   MAP
0019 00013  03300031                STA*  FWAJ
0020 00014  01100027                LAA   TWO         SET WORD COUNT , TERMINATING
0021 00015  03300032                STA*  WC3
0022 00016  00136023                CEU   '23         INITIALIZE THE MULTIPLEXER
0023 00017  00100000                DATA  '100000
0024 00020  11100016                BRU   *-2
0025 00021  00136020                PIE               ENABLE BTC COMPLETE INTERRUPT
0026 00022  00000200                DATA  '200        GROUP 0 LEVEL 8
0027 00023  00000033                NOP               WAIT LOOP
0028 00024  00130417                SNS   15
0029 00025  11100035                BRU   END
0030 00026  11100023                BRU   *-3
0031 00027  00100002          TWO   DATA  '100002
0032 00030  00001011          MPIL  DATA  '1011       GROUP 0, LEVEL 8
0033 00031  00001064          FWAJ  DATA  '1064
0034 00032  00001065          WC3   DATA  '1065
0035 00033  00000042          MPXL  DATA  NTDM-MAP
0036 00034  00000061          FWAL  DATA  FW-MAP
0037 00035  00000000          *
0038 00035  00130601          END   PID               DISABLE BTC COMPLETE INTERRUPT
0039 00036  00000200                DATA  '200        GROUP 0 LEVEL 8
0040 00037  01100041                LAA   A1
0041 00040  12300000          A     SPB*  SYST
0042 00041  00000001          A1    DATA  A1-A,10,''8MPT''
0042 00042  00000012
0042 00043  00134315
0042 00044  00150324
0043 00045  00000000          *     BTC COMPLETE INTERRUPT DISPLAY IN "A" & "B"
0044 00045  13000000          NTDM  ZZZ   **
0045 00046  01100064                LAA   FW
0046 00047  02100065                LBA   SW
0047 00050  14100063                IMS   DLY
0048 00051  11100050                BRU   *-1
0049 00052  14100063                IMS   DLY         NO OP THESE INSTRUCTIONS FOR FASTER CYCLING
0050 00053  11100052                BRU   *-1        NO OP THESE INSTRUCTIONS FOR FASTER CYCLING
0051 00054  00130417                SNS   15
0052 00055  11100061                BRU   *+4
0053 00056  00136023                CEU   '23         INITIALIZE THE MULTIPLEXER
0054 00057  00100000                DATA  '100000
0055 00060  11100056                BRU   *-2
0056 00061  00000033                TOI
0057 00062  11300045                BRU*  NTDM
0058 00063  00000030          DLY   DATA  30          2 SECONDS
0059 00064  13000000          FW    ZZZ   **          FIRST WORD OF DATA
0060 00065  13000000          SW    ZZZ   **          SECOND WORD OF DATA
0061 00066  01100000                END
```

Fig. 1. 8MPT multiplexer test program.

The format of the first word is



The format of the second word is



In these formats, the bits labeled MSB and LSB are the most and least significant bits respectively. Typically, the second word contains time-of-flight data bits, whereas the first word contains either pulse-height or time-of-flight bits in locations 7 through 15. The data portion of the first word may extend to bit 3 if no tagging is used. The actual word formats are defined for each experiment with the least significant bit of the time-of-flight data always occurring in bit 15 of the second word.

4. CHANNEL IDENTIFICATION

The channel number, priority, identification, and designation of the words within the multiplexer are given in Table 2. The channel number (priority) to be used by an experimenter is determined by the connection to the multiplexer. If a level-matching (Sect. 7) or a cable drive module is to be used, the channel number can be indicated on the front panel by using the wiring of Fig. 2.

Table 2. Priority, identification, and word names

Channel Number	0	1	2	3
Priority	0	1	2	3
Identification				
Bit 0	0	0	1	1
Bit 1	0	1	0	1
First Word	A	C	E	G
Second Word	B	D	F	H
Connector	J13	J14	J15	J16

5. SIGNALS

The signal levels to and from the multiplexer via the ground isolation module are +3 V for the true condition and 0 V for the false condition. The input and output circuits to and from the multiplexer are shown in Figs. 3a and 3b respectively. The levels representing the data bits into the multiplexer must remain at either level from the moment Data Ready becomes true (+3 V) until the Data Accepted pulse is returned by the multiplexer, with the exception of the System Tag bit. It is stored in a flip-flop as a result of the negative-to-positive transition on the leading edge of the signal.

5.1 Ground Isolation

The circuits for inputs to and outputs from the ground isolation system are shown in Figs. 4a and 4b respectively. The ground isolating receiver and driver circuit cards[5] (Dwg. Nos. Q-5072-9B and 13B), which connect to the circuits of Figs. 3a and 3b, use an Iso-switch[7] rated at 10^{10} Ω resistive isolation. Other parameters for the Iso-switch are contained in Iso-switch Data Sheets 869 and 870. The input drive signal to the isolation circuit is not restricted to the signal from a TTL integrated circuit. A no-current condition on the isolation input will produce a positive output voltage. The Iso-switch requires a 4.2-V positive input

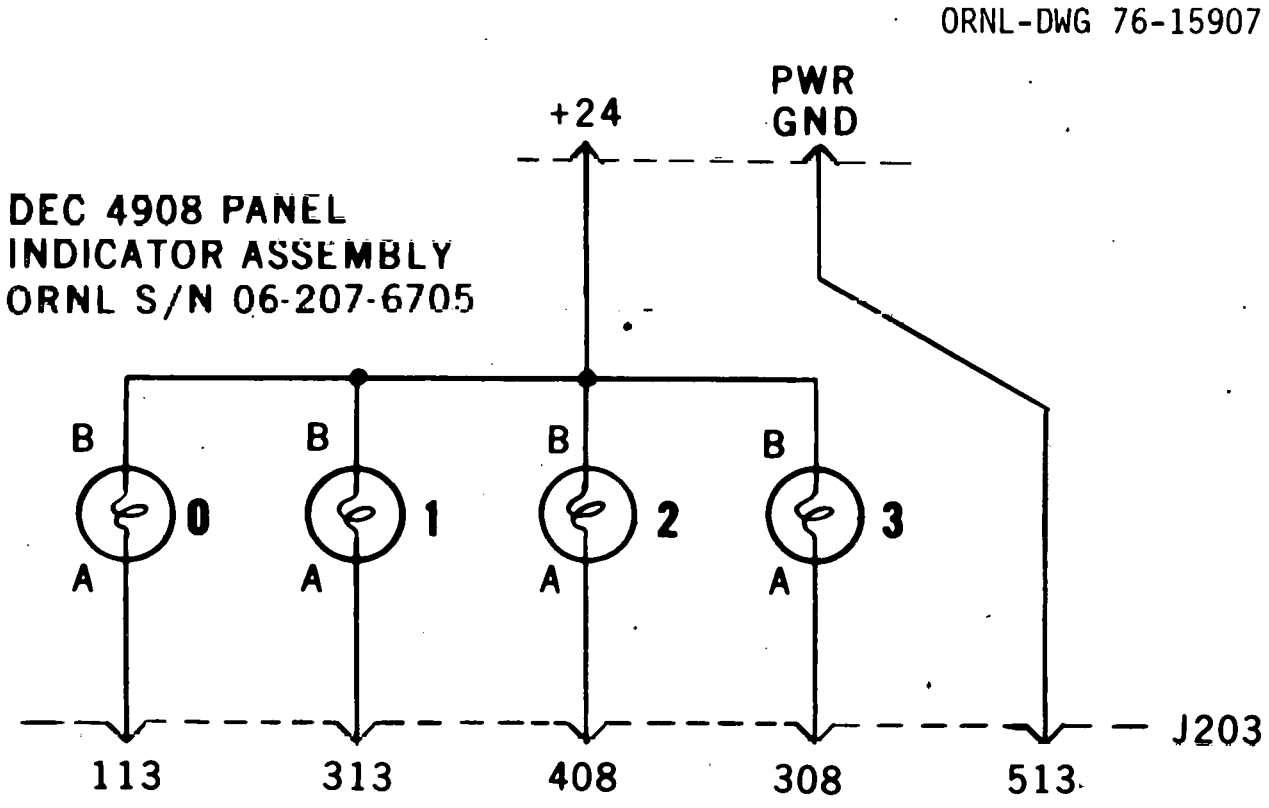


Fig. 2. Channel identification wiring.

ORNL-DWG 76-15920

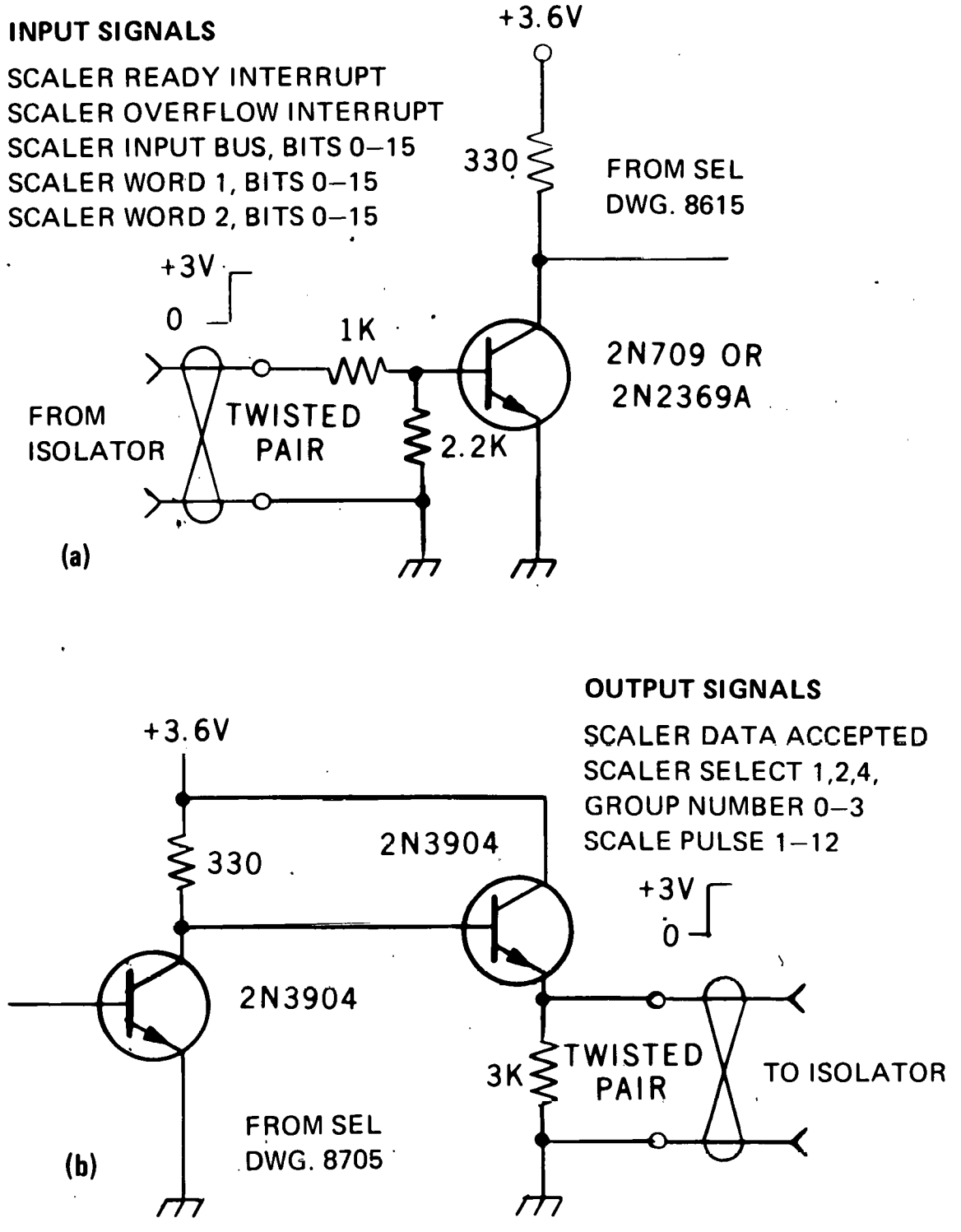


Fig. 3. Multiplexer input/output: (a) cable terminator, (b) cable driver.

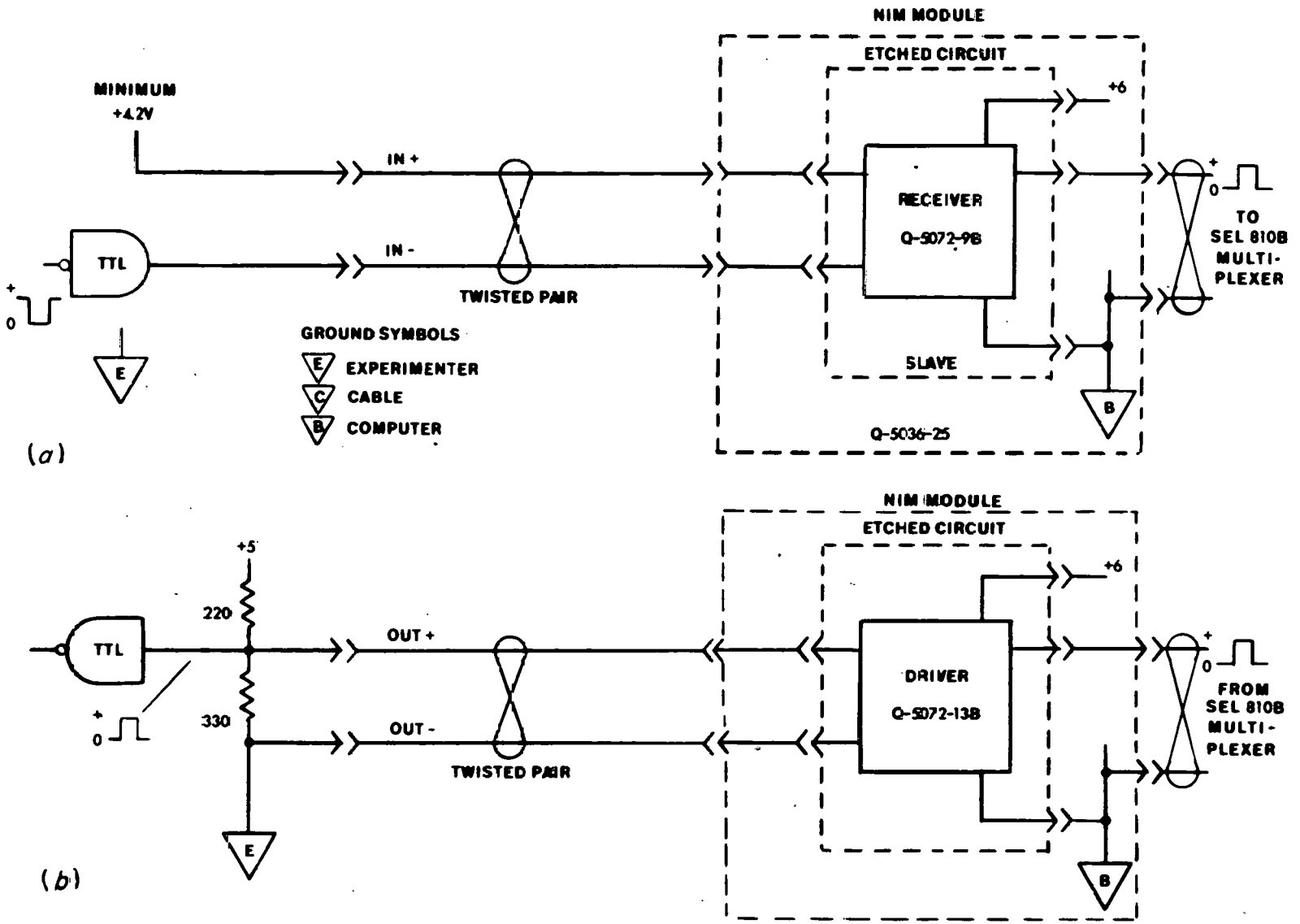


Fig. 4. Single isolation for signals (a) to and (b) from the SEL 810B Multiplexer.

signal at 5 mA for the ON (ground output) condition. The ground isolators are assembled in a four-wide Nuclear Instrument Module (NIM) (Dwg. No. Q-5036-29) per Dwg. No. Q-5036-25.

5.2 Connectors

The connections to each channel (Table 3) are identical. All of the PIN- terminals on the 37-pair cable between the multiplexer and the ground isolation module are tied to ground at both ends of the cable except for pin 408, which is used to control a light. Pin 513 is tied to the cable shield at both ends of the cable. See SEL 810B Multiplexer, Ground Isolators Schematic (Dwg. No. Q-5036-25) for the wiring in the ground isolator module. At the computer end, pin 513 is jumpered to pin 113, 313, 408, or 308 in the connectors J13, 14, 15, and 16 (channels 0, 1, 2, and 3 respectively) to provide a return path for the channel indicator in both the experimenters level-matching module or equivalent and the ground isolator module.

At the experimenters end of the cable to the multiplexer, pins 201, 406, 407 (OUT- of Fig. 4b), and 513 are tied to the experimenters ground while pins 101, 306, and 307 are terminated per Fig. 4b, OUT+. All PIN+ pins except for outputs and channel indicators are connected to a +5-V TTL power supply per Fig. 4a, IN+. The data bits and control signals are on the PIN- pins in the connector labeled IN- on Fig. 4a.

The cable and connector assemblies between the multiplexer (P13, 14, 15, or 16) and the ground isolator (P201) and the ground isolator (P202) and the experimenter level-matching module (P203) are specified on Dwg. No. Q-2928-11.

5.3 Signal Function

The functions of the signals in the multiplexer are described below.

MPXR Control, when positive, indicates that the multiplexer is ready to receive data on channel X. Four conditions must be satisfied to allow data acquisition:

Table 3. Multiplexer cable connections

PIN+	PIN-	Function	PIN+	PIN-	Function
101[a]	201	MPXR Control	308		Channel 3 Indicator
102	202	MPXR Interrupt		408	Channel 2 Indicator
103[b]	203	System Tag, Bit 2	309	409	Second Word, Bit 0
104[b]	204	First Word, Bit 3	310	410	Second Word, Bit 1
105[b]	205	First Word, Bit 4	311	411	Second Word, Bit 2
106[b]	206	First Word, Bit 5	312	412	Second Word, Bit 3
107[b]	207	First Word, Bit 6	313		Channel 1 Indicator
108	208	First Word, Bit 7	501	601	Second Word, Bit 4
109	209	First Word, Bit 8	502	602	Second Word, Bit 5
110	210	First Word, Bit 9	503	603	Second Word, Bit 6
111	211	First Word, Bit 10	504	604	Second Word, Bit 7
112	212	First Word, Bit 11	505	605	Second Word, Bit 8
113		Channel 0 Indicator	506	606	Second Word, Bit 9
301	401	First Word, Bit 12	507	607	Second Word, Bit 10
302	402	First Word, Bit 13	508	608	Second Word, Bit 11
303	403	First Word, Bit 14	509	609	Second Word, Bit 12
304	404	First Word, Bit 15	510	610	Second Word, Bit 13
305	405	Data Ready	511	611	Second Word, Bit 14
306[a]	406	Data Accepted	512	612	Second Word, Bit 15
307[a]	407	Channel Busy	513	(Shield)	Channel Indicator GND

[a]Output from the multiplexer.

[b]These inputs are used for experimenter tags.

1. The computer mainframe must be executing instructions; this is indicated by a RUN signal.
2. The Block Transfer Control (BTC) must have the UNIT CONNECTED signal present as a result of initialization for input data transfers.
3. The Enable Channel X flip-flop must be set during initialization of the multiplexer.
4. The Data Ready switch on the ground isolation module must be in the ON (down) position.

An AND gate in the BTC control combines the first three signals. The Data Ready switch shorts the isolated output in the OFF (up) position.

MPXR Interrupt is a future priority interrupt to the SEL 810B mainframe. It has not been implemented or used to date.

System tag, bit 2 is a signal generated by the experimenter's equipment at the beginning of each accelerator start pulse (see Word Format).

It is used by ODAR[3] to keep track of bursts of data in a Burst Used (BU) counter for each experimenter. If data cannot be used due to a high data rate or some other cause, a Burst Not Used (BNU) counter is incremented and all data from one System Tag to the next is included in the data that is thrown away.

Experimenter tags, if used, define a maximum of 16 sets of data to be accumulated by providing routing information to the program under the control of external status signals. They are used as required by the experimenter.

First word, bits 3 to 15, consists of either the tag bits and pulse-height data or tag bits and the high-order time-of-flight bits from an experiment.

Second word, bits 0 to 15, contains the time-of-flight data from the experiment.

Data Ready is a signal to the multiplexer, preferably a positive 1-μsec-wide pulse, that starts the transfer of 30 bits of data through the multiplexer to the SEL 810B memory. A positive level that is terminated by the return of Data Accepted is also allowed. It sets a Channel Busy flip-flop in the multiplexer chassis.

Data Accepted is a positive 0.75-μsec pulse from the multiplexer to the experimenter that occurs when the 30-bit double-word data transfer started by Data Ready has been completed. It occurs at the same time that Channel Busy returns to the not-true condition.

Channel Busy is a status signal from the multiplexer that is true from Data Ready until Data Accepted. The input data should not change during the time Channel Busy is present.

Channel indicator is a set of four signals that indicate to which channel an experimenter is connected and which channels are active at the SEL 810B Four-Channel Priority Multiplexer (Fig. 2).

6. THEORY OF OPERATION

The channels are asynchronously controlled by two signals: Data Ready, which indicates that the data is at the input to the multiplexer,

and Data Accepted, which is generated by the multiplexer control when the second data word has been transferred to the computer memory. A hardware priority within the multiplexer controls the entry of data words so that the first word will always be entered before the second word. However, if an odd number of words is transferred between the multiplexer and the computer memory, the Multiplexer Odd-Word Error logic detects the transmission. This error can occur when two Data Ready signals occur with a relative timing of 100 to 150 nsec. A Channel Busy signal is brought out of the multiplexer for use in external equipment. A typical Channel Busy time, when using an operating program, is 10 to 14 μsec for ∿90% of the input, with the remaining 10% less than 18 μsec. A few events are beyond 18 μsec.

The operation of one channel of the multiplexer is explained with the use of a simplified logic diagram (Fig. 5) and a timing diagram (Fig. 6). The typical control for each channel is within the dotted lines at the top center (the ground isolation is not shown), and the channel word control (two words per channel) is enclosed by a dashed line in the center of Fig. 5. The control signals common to all channels are heavy lines, and the data path is a heavy dashed line. Experimenter-generated or -used signals begin with the word "data," and the signals to and from the computer are underlined. All other signals are internal to the multiplexer. It is assumed that a Master Clear signal from the computer has occurred to set the control flip-flops to an initial state: Strobe 1 (STBE1) will be true, Strobe 2 (STBE2) will be false, and Read Word Reset (RWRST) to the read latches will be false. It is assumed that the BTC connected to the multiplexer has been initialized and that the data enter into channel 1.

When the Data Ready signal becomes positive at the input to the cable terminator (CT), the negative signal at its output is strobed into the Data Channel 1 Busy (DCH1B) flip-flop by a clock signal from the computer if the Channel Enable flip-flop was set during BTC initialization by the 7MUL package of ODAR.[3] (The experimenter's dispatch routine controls the enabling and disabling of his channel via 7MUL.) The output of the Channel Busy flip-flop is gated by STBE1 in gate 1 to set the Priority flip-flops for words C and D. The outputs of the C and D Priority flip-flops hold the

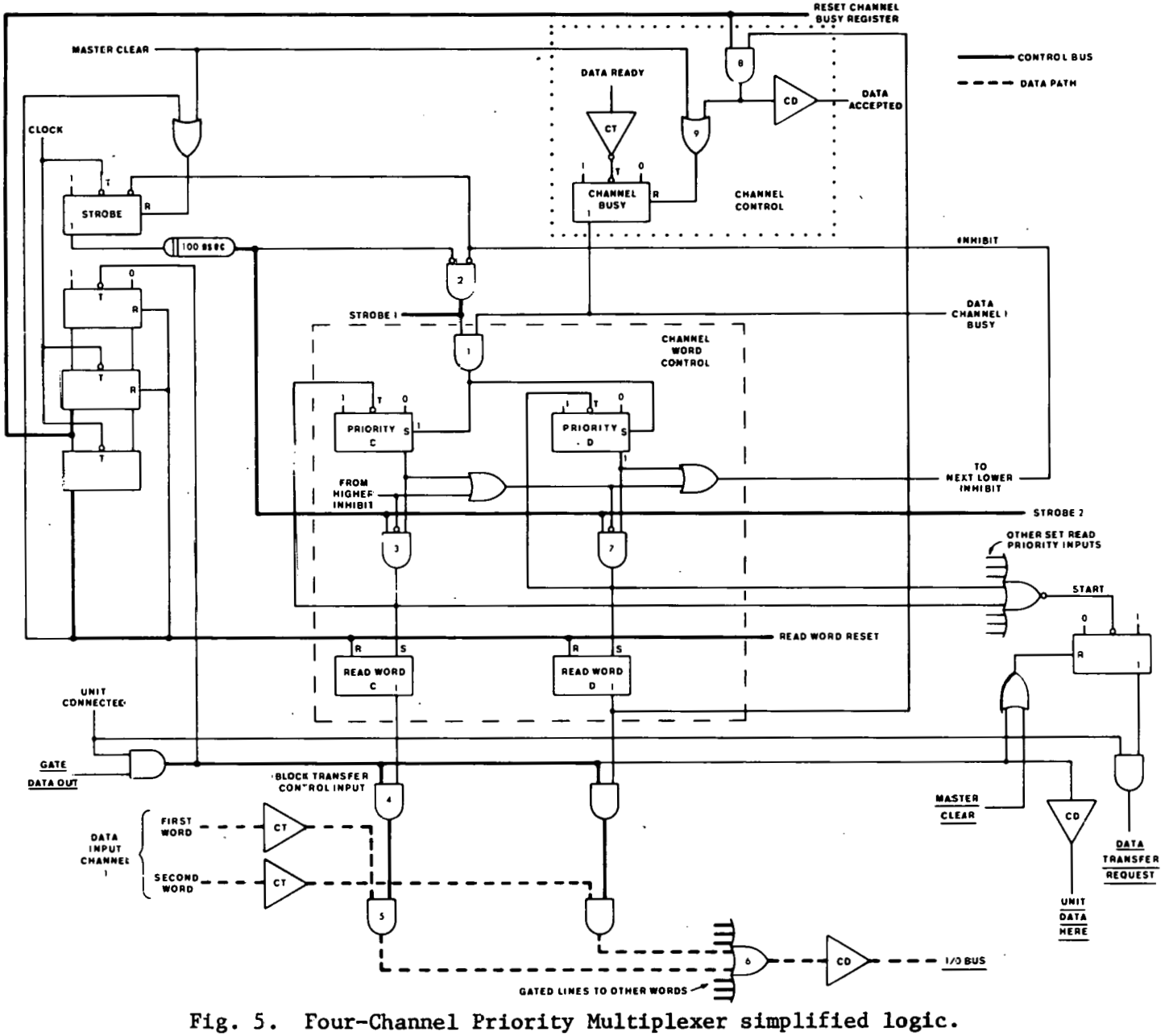


Fig. 5. Four-Channel Priority Multiplexer simplified logic.

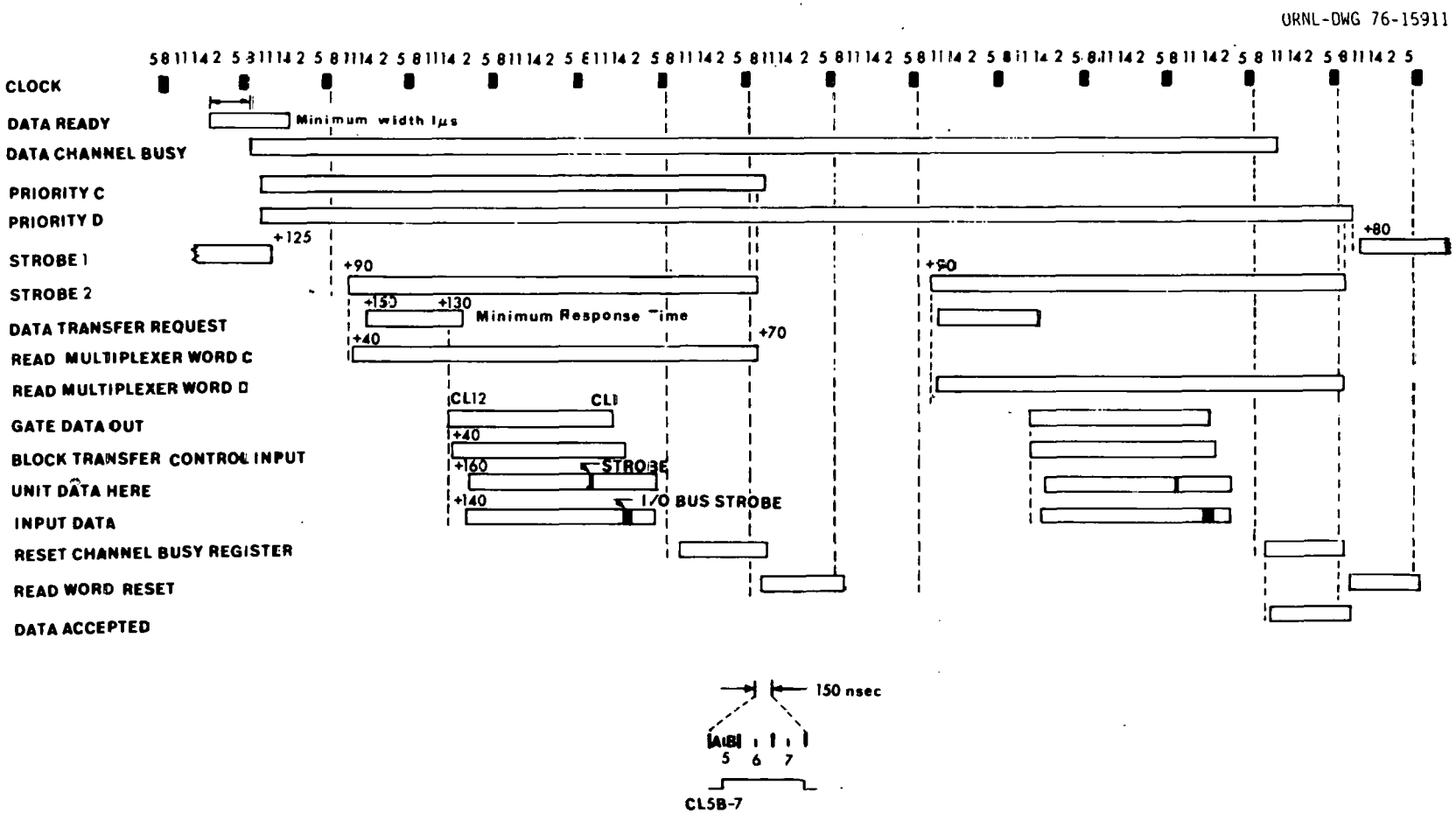


Fig. 6. Four-Channel Priority Multiplexer timing.

Inhibit line (INH2) true, which removes the STBE1 signal from gate 1 via gate 2 after a typical propagation time of 125 nsec from a true condition of Channel Busy. The Inhibit signal steers the Strobe flip-flop. It is set by Clock pulses (CL5B-7) from the mainframe via the I/O Bus and reset by Read Word Reset.

The Clock pulse is derived in the SEL 810B from a crystal oscillator operating at 2.6667 MHz, a flip-flop, a 400-nsec tapped delay line, and numerous gates. The 750-nsec period out of the flop-flop is divided into 25-nsec time increments by combining the delay line outputs in AND gates. The clock periods are numbered CL1A, CL1B, CL2A, etc., to CL15A and CL15B (see SEL Dwg. No. 130-810017-000, sheets 16 and 29). CL5B-7 is a timing signal on the computer I/O Bus which is used to synchronize the peripheral devices to the mainframe clock during data transfer.

The STBE2 line becomes true 200 nsec after the trailing edge of the first Clock pulse following Inhibit. Note that gates 3 and 7 are controlled by inhibits from the higher-priority word inputs (A and B in our example). If there is no inhibit present, the true signal from gate 3 to the Read Multiplexer Word C (RMWC) latch sets the latch and generates a Start signal at STBE2 time. Start causes a Data Transfer Request to be sent to the Block Priority Control (BPC) via the Block Transfer Control (BTC) connected to the multiplexer. (See *SEL 810B Technical Manual*, pp. 3-22 through 3-24, or *SEL 810B I/O Interface Manual*, pp. 4-1 through 4-18, for BTC operation.) When priority is granted for use of the memory and the I/O Bus, the BPC will send a Gate Data Out (GDO) signal to the multiplexer via the attached BTC. The response time will depend on which instruction is being executed at the time of the Data Transfer Request (DTR). A typical response time variation from the true condition of Channel Busy to GDO is 2.4 to 3.1 μsec. GDO is gated with the Unit Connect signal from the BTC interface to form the signal Block Transfer Control Input (BTCIN). (The Unit Connect flip-flop has been set by the control program upon execution of a command external unit '23 (CEU '23), with the initialization bit set in the second word.)

The signal BTCIN is combined with the output of the RMWC latch in gate 4 to gate the first word of input data on channel 1 through the

multiplexer onto the I/O Bus via AND gates 5 and OR gates 6. The BTCIN signal is also routed to the BTC as Unit Data Here (UDH). The presence of UDH in the BTC-BPC will result in GDO and BTCIN becoming false 450 nsec after Clock (CL1 time in the computer). The trailing edge of BTCIN will set the first flip-flop in a three-stage walking-1 register.

The trailing edge of Clock, 250 nsec after the end of BTCIN ($\overline{\text{BTCIN}}$), gates the 1 of the first stage to the second stage of the walking-1 register. The output signal Reset Channel Busy Register (RSTCBR) is not used during the first word transfer. The second Clock signal after BTCIN gates a 1 to the third stage, Read Word Reset (RWRST), of the walking-1 register, the RMWC latch, and the Strobe flip-flop. Removing STBE2 from gate 3 allows its output to go false. Priority C flip-flop resets, which removes the inhibit to gate 7 on the RMWD flip-flop. The third Clock pulse after $\overline{\text{BTCIN}}$ resets the RWRST flip-flop. The fourth Clock pulse after $\overline{\text{BTCIN}}$ sets the Strobe flip-flop.

STBE2 then sets the RMWD latch via gate 7 and generates a Start signal which causes a Date Transfer Request, etc. This time the first Clock pulse after $\overline{\text{BTCIN}}$ will reset the DCH1B flip-flop via gates 8 and 9 and generate the Data Accepted signal. The second Clock pulse will remove RMWD and STBE2 via RWRST. STBE2, becoming false, will reset the Priority D flip-flop, resulting in Inhibit becoming false. STBE1 will become true unless channel 2 or 3 is busy and will gate any channel Strobe signal DCH0B, DCH1B, DCH2B, and/or DCH3B into the respective Priority flip-flops: A, B, C, D, E, F, G, or H. The input transfer sequence from the multiplexer will then repeat, starting with the highest priority, word A, and proceeding to the lowest, word H.

The Multiplexer Odd-Word Transfer Error logic shown in Fig. 7 was added to detect possible transfer errors caused by the relative timing of Data Ready. The signal BTCIN from the initialization of the BTC through the 7MUL program sets the MPXR Error flip-flop to the no-error state. A signal from each word transferred (RMWX) toggles this flip-flop; for example, RMWC would set it to the error condition and RMWD would set it to no error. Each time STBE1 is present or at the End of a Block (EOB) transfer, the MPXR Error status is gated to the Multiplexer Error interrupt

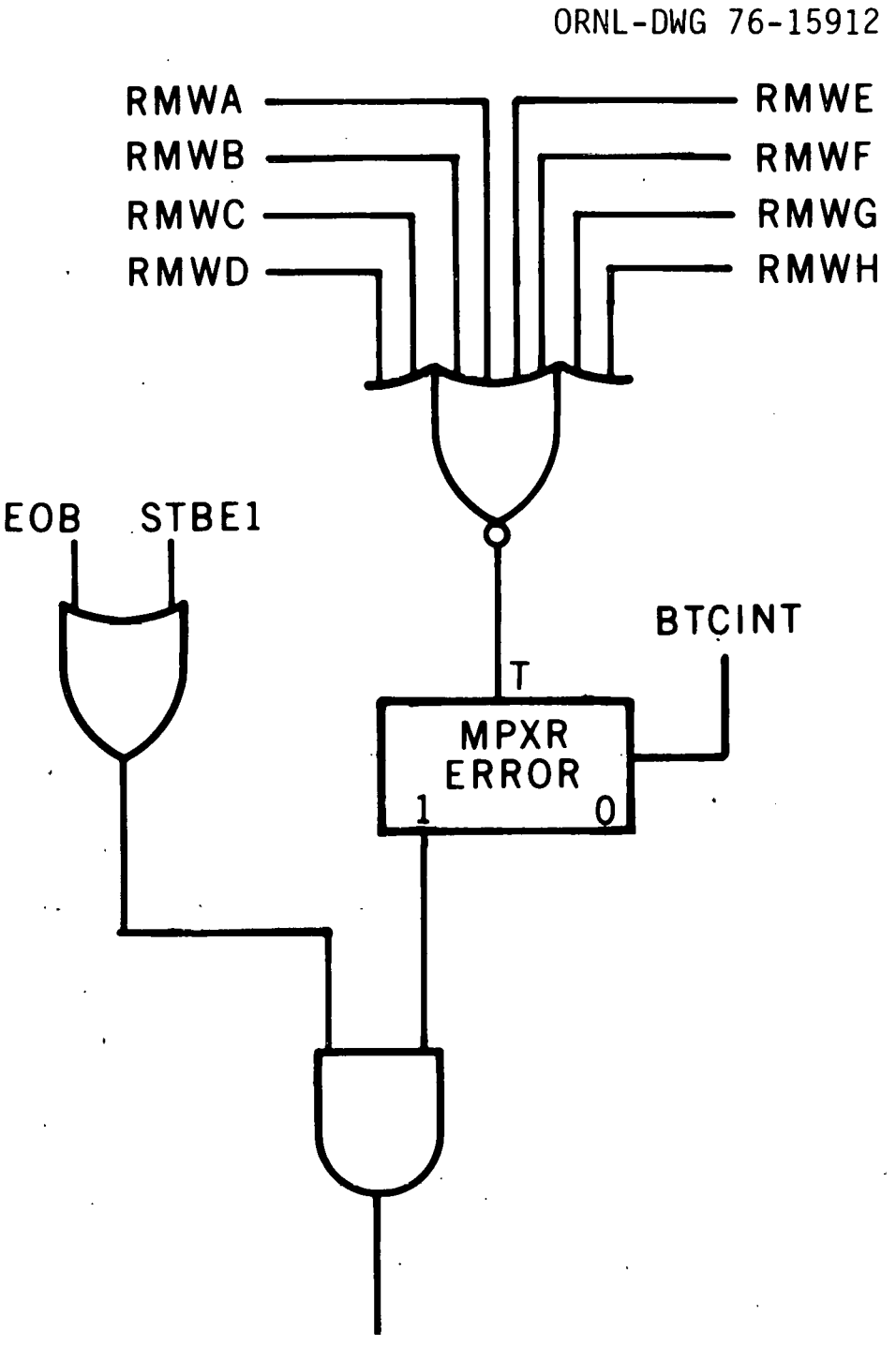


Fig. 7. Multiplexer Odd-Word Transfer Error logic.

signal line to inform ODAR when an error condition exists. The usual result is a reinitialization of the BTC logic and an error indicator to each experimenter program. (See Sect. 2.2.)

No single channel can block out all other channels, even if the highest data-rate experiment operates on the highest-priority channel, because of the triple gating from Data Channel Busy to Priority to Read Multiplexer Word to Data Channel Not Busy under the control of the signals Data Ready, STBE1, STBE2, and RSTCBR. A possible random sequence of events for four experimenters is shown in Fig. 8. Note that the actual transfers to memory are always A, B, C, etc., for all the active channels (Data Ready present) between two STBE1 positive levels.

7. INPUT LEVEL MATCHING

Three level-matching modules have been constructed for interfacing several time-of-flight units and analog-to-digital converters into the multiplexer. They are for an Eldorado 5-nsec Clock (-3 V = "1," Dwg. No. Q-5110-1), a TMC TF 440-10 Clock with a series ND 2200 8192 ADC (-3 and +3 V = "1," Dwg. No. Q-5110-2) and an EGG TDC-100 Time Digitizer with two Series ND 2200 4096 ADCs (+3 V = "1," Dwg. No. Q-5110-3).

The assembly drawing for the level-matching modules is Dwg. No. Q-3079-5, with the front panels numbered Q-5110-11, -12, and -13. The above units were constructed in a two-wide NIM. There is space for eight DEC modules using DEC M Series, Logic Modules;[8] in particular, M100-Bus Data Interface (-3/0 to +3/0 for 15 signals), M101 Bus Data Interface (+3/0 to 0/+3, 15 signals), M502 High-Speed Negative Input Converter (0/-3 to +3/0, dual), and M652 Negative Output Converter (+3/0 to 0/-3, dual). In addition, the M506 Medium Speed Negative Input Converter (0/-3 to +3/0, triple) and M650 Negative Output Converter (+3/0 to 0/-3, triple) may be useful for some applications.

The Level-Matching, Input Cable Connections are given in Table 4. (Space has been allowed for the experimenter to write in his bit assignments.)

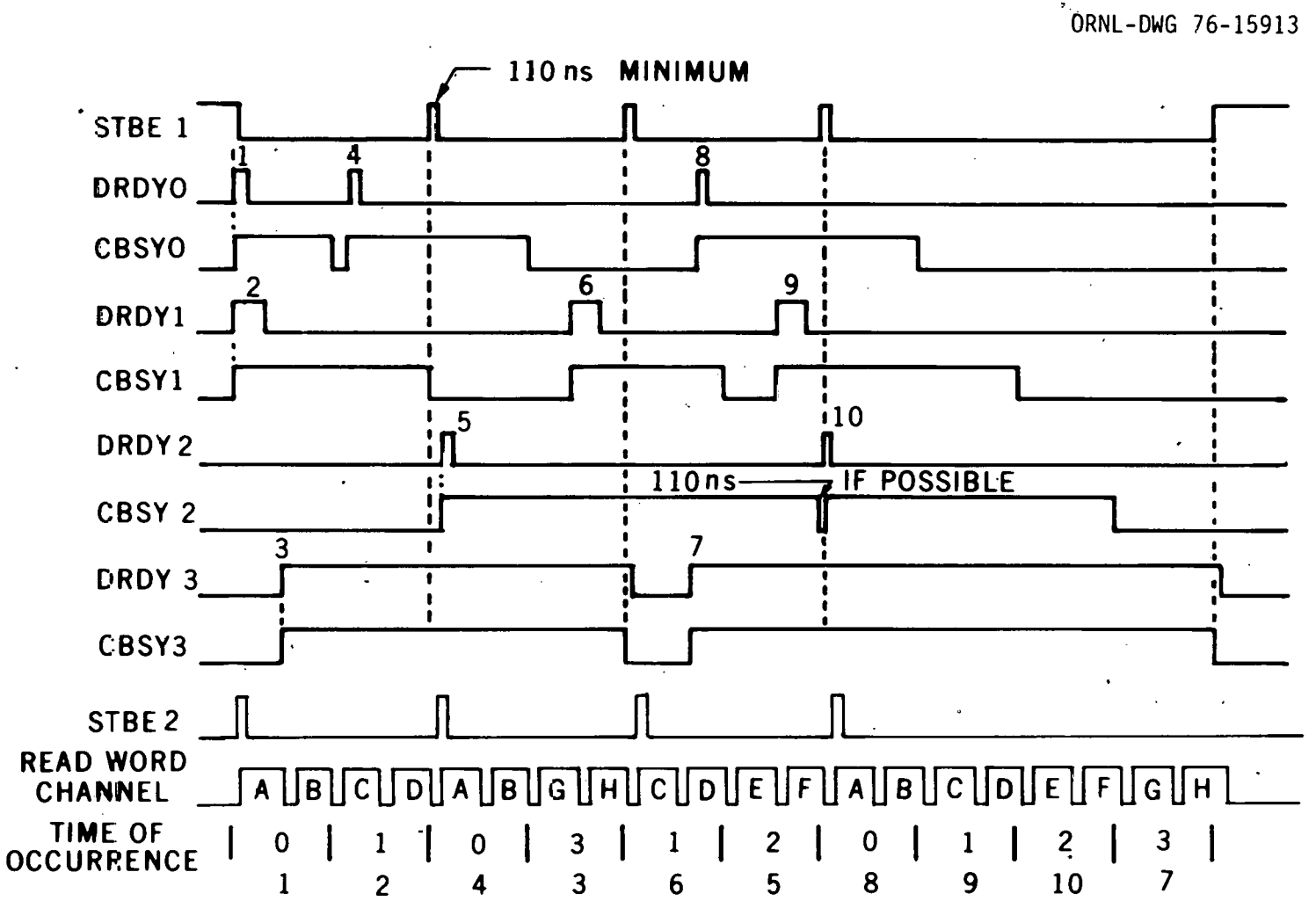


Fig. 8. Word transfer timing for a random order of multiplexer input. The Data Ready (DRDYX) signals are numbered in order of time of occurrence and are indicated as pulses for channels 0, 1, and 2 and as a level for channel 3.

Table 4. Multiplexer level-matching; input cable connections (P204-J204)

Pin	Function[a]	Pin	Function[a]
101	MPXR Control	301	SWB0
102	MPXR Interrupt	302	SWB1
103	System Tag, Bit 2	303	SWB2
104[b]	FWB3	304	SWB3
105[b]	FWB4	305	SWB4
106[b]	FWB5	306	SWB5
107[b]	FWB6	307	SWB6
108	FWB7	308	SWB7
109	FWB8	309	SWB8
110	FWB9	310	SWB9
111	FWB10	311	SWB10
112	FWB11	312	SWB11
113	FWB12	313	SWB12
201	FWB13	401	SWB13
202	FWB14	402	SWB14
203	FWB15	403	SWB15
204		404	
205		405	
206		406	
207		407	
208		408	
209		409	Data Ready
210		410	Data Accepted
211		411	Channel Busy
212	Ground	412	Ground

[a] FWBX — First Word bit X; SWBX — Second Word bit X.

[b] Experimenter tags (typical).

The Eight-Stage Stacking Buffer Memory (Dwg. No. Q-5066)[9] can be connected directly to the multiplexer ground isolators. The level-matching module, if required, would then drive the inputs to the Stacking Buffer Memory.

8. MAINTENANCE

A multiplexer test program, 7MPX*, has been written to operate with ODAR[3] and a Multiplexer-Scaler Tester (Dwg. No. Q-5130).[10] It checks the data provided by the tester for pickups and dropouts in each of the 30 data bits and types the correct and incorrect data as the errors occur. By repeating test runs after moving the tester logically and physically closer to the multiplexer, an intermittent error in a stacking buffer memory, in the ground isolation or in a channel of the multiplexer, may be isolated and then repaired.

A test program, 8MUP, uses the Multiplexer-Scaler Tester. It does not share the Four-Channel Priority Multiplexer with other inputs. All the incoming multiplexer data is checked by 8MUP; therefore, any extraneous inputs from another channel will appear as an error. Data can be displayed in the A and B registers without checking, the correct word can be displayed in the B accumulator with the error word in the A accumulator, and one error per block can be printed. The teletype bell rings for each error. Operating instructions for 8MUP are included on a listing of the program.

A second test routine, 8MPX, is used for checking multiplexer input from the PDP-4 or PDP-9 Intercomputer Link.[11] See a listing of 8MPX for the operating instructions.

These programs are available from the author.

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*Available from J. G. Craven, Computer Sciences Division.

9. ENGINEERING DRAWINGS

The following Q-drawings are related to the topics discussed in this volume. They are not included here due to space limitations, but are available from the author.

Q-2928-2 — ORELA Data Acquisition, Bldg. 6010, Central Data Area, Computer Equipment Layout

Q-2928-11 — ORELA Data Acquisition, BTC, Multiplexer, and I/O Bus or Scaler Cable Connectors

Q-3079-2 ORELA Digital Multiplexer, Level Matching, DEC Connector Block NIM Mounting Bar

Q-3079-5 — ORELA Digital Multiplexer, Level Matching, Moldule Assembly and Details

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