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Evaluation of the Guardband Implant Diffusion Processes

Kansas City Division

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Topical Report
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MASTER

EVALUATION OF THE GUARDBAND IMPLANT DIFFUSION PROCESSES

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Prepared by M. F. Williams

Breakdown voltage is a measure of damage inflicted upon a wafer during ion implantation. If the voltage is low, it is desirable to increase the voltage, which should increase the wafer yield. Two methods can be implemented to increase this voltage. One is to increase the pre-implant oxide thickness, and the other is to increase the annealing process to reduce the damage. This study encompassed both methods. Results indicated that an increase of 150 Å in the pre-implant oxide and an increase of 50°C in annealing temperature improved yield by approximately 9% due to increased breakdown voltage.

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SUMMARY

Ion implantation is a method of introducing dopants into a silicon wafer. The process requires ion bombardment of the wafer and, therefore, damages the wafer structure. Two methods are used to decrease the impact damage of implantation. One is to place a sufficiently thick oxide layer on the wafer prior to implantation, and the other is to anneal the damage out with a high-temperature step after the implant procedure. Both processes are performed in atmospheric diffusion furnaces.

The guardband implant is important in the manufacture of integrated circuits to help eliminate current leakage and parasitic transistors. The implanting procedure was causing detrimental damage to devices, resulting in voltage breakdown. To decrease damage, several implant oxides were evaluated prior to the implantation process. Several annealing processes were also evaluated. Key parameters of oxide thickness, sheet resistivity, and junction depth of the dopant were analyzed for each of the implant oxides and the implant annealing processes. Breakdown voltage data, an indication of implant damage, revealed that increasing the implant oxide thickness and the annealing temperature greatly reduced guardband implant damage without incurring detrimental damage to the device.

DISCUSSION

SCOPE AND PURPOSE

Low breakdown voltage and resulting gate ruptures cause premature failure of device circuits. Because this is a processing problem, it is advantageous to increase the voltage breakdown to the maximum allowable level without shifting other device parameters. An increase in pre-implant oxide is beneficial to decrease damage without greatly changing the device characteristics. Increasing the implant annealing temperature is more difficult because the higher the process temperature, the greater the change in device characteristics. However, it is beneficial to increase breakdown voltage and to push the other processes to their limits to achieve the largest overall improvements.

The study was performed in two parts. Initially the effect of increasing pre-implant oxide on several parameters was determined. Thickness of oxide, post-implant junction depth (Xj), and post-implant sheet resistivity (Rs) were evaluated. To increase implant oxide, times and temperatures were varied to achieve desired thickness. Wafers were then implanted. Following implantation, the wafers underwent standard annealing; and Xj and Rs were measured. During the second section of study, an ideal pre-implant oxide was selected. Several wafers were implanted and taken through different annealing processes with varied times and temperatures. Again the ideal process was selected from an evaluation of Xj, Rs, and breakdown voltage. The two ideal processes were combined and tested on a split production lot. All evaluated data were favorable, and the changes were implemented on all production guardband processes.

PRIOR WORK

No prior work has been done by Allied-Signal Inc., Kansas City Division's Albuquerque Microelectronics Operation regarding this subject, but Sandia National Laboratories suggested that two process changes could reduce the guardband breakdown problem. The first change was to increase the implant annealing temperature to 1100°C, based on computer modeling; and second was to change the implant species from boron (B) to difluoroborine (BF_2). Tests were completed with the BF_2. However, its use was not feasible because of processing problems related to the change and because the larger implant species caused voids in the silicon that could be detrimental to some electrical tests. The former option to increase breakdown voltage was a starting point for the second half of this study.

ACTIVITY

Experiment Preparation

This experiment was conducted in two steps. Initially, the pre-implant oxide was examined; secondly, the post-implant annealing process was evaluated. Standard bare 3-4 ohm, phosphorous-doped wafers were used for the initial study. Phosphorous-doped wafers were used so that boron guardband implant species would better replicate standard processing and yield a sharper junction depth. These wafers were cleaned with a standard sulfuric acid and hydrogen peroxide solution. The wafers were then split through several time- and temperature-varied furnace processes, and thickness measurements were recorded using an optical measuring system. The wafers then received a standard boron implant at 60 keV with a dose of 4×10^{15} atoms/cm^2. The wafers underwent the standard guardband implant annealing process of 1000°C in oxygen ambient for

15 min. Data for the sheet resistivity and implant junction depth were then measured. The Rs was recorded by a fourpoint probe, and Xj was measured by the groove and stain method.

The second half of the experiment varied the guardband implant annealing process by time and temperature. The experiment was conducted using standard pre-implant oxide and the best pre-implant oxide from the earlier test on the same wafers that were previously described. The wafers received the standard implant and were split during annealing. Again the Rs and Xj were measured. The wafers received a gate oxide of 450 Å and evaporated aluminum/silicon dots. They were then tested for breakdown voltage.

Results

Pre-Implant Oxide

The parameter goal was to increase thickness of the pre-implant oxide to the upper range of the existing specification limit of 50-300 Å. Standard lots averaged 90-120 Å, but an oxide this thin provided little protection from implant damage. To increase thickness and to remain within specifications, the target oxide thickness was set at 250-300 Å. Temperature was not elevated greatly, nor was a time increase to be excessive. An oxide grown from a dry oxygen process, rather than one from a steam or wet process, was required.

The standard process is exposure to 900°C in oxygen for 15 min. Two splits were exposed to 900°C for 60 min and 80 min, respectively; and one was exposed to 950°C for 40 min. Six wafers were processed in each of the splits, one in the front, center, and back of each of two main processing boats in the center of a four-boat paddle. Oxide thickness was measured for each wafer in five positions on the wafer: top, center, bottom, left, and

right. Table 1 lists the average thickness measurement for the total load and for each boat. Notably, the lot processed at 950°C produced the desired thickness, but the increased time exposure at 900°C did not achieve the desired thickness. Increasing processing time further to obtain a thicker oxide would have violated the stated limitations.

After the guardband implanting and standard annealing processes were complete, resistivity was measured in the same pattern as oxide thickness. Averages are listed in Table 1. Neither an increase in time nor temperature affected the resistivity.

Wafers were grooved and stained to reveal junction depth, the depth to which doped species traveled during the implanting and annealing cycles. Each wafer was measured once, and the average is listed in Table 1. The standard process resulted in the highest measurement, although the increased time and temperature processes were within tolerance of the measurement technique. The groove and stain method is an inexact technique, but it can approximate the depth that the dopant reached. All increased time and temperature groups exhibited approximately the same Xj.

Oxide thickness was the determining factor in process selection. The 950°C temperature was selected as the best process for increasing oxide thickness because its results were within the chosen thickness range, it had no detrimental effects on Rs or Xj, and it did not breach any of the limitation criteria.

Guardband Annealing

Based on the previous data, a 950°C process for 40 min was selected to yield the optimum pre-implant oxide. To evaluate the guardband annealing effectively, wafers were divided between the standard and optimum pre-implant oxides. They were given the standard boron implant and divided for different times and

Table 1. Average Data for Pre-Implant Oxide Trial Runs

Run Parameter	Thickness (Å)	Rs (Ω/cm^2)	Xj (μm)
900°C/O_2/15 min (Standard)	102	38.91	0.782
Boat 1	100	38.78	0.842
Boat 2	104	39.03	0.720
900°C/O_2/60 min	185	39.54	0.657
Boat 1	191	39.56	0.623
Boat 2	179	39.52	0.690
900°C/O_2/80 min	230	37.83	0.557
Boat 1	229	37.87	0.630
Boat 2	231	37.78	0.483
950°C/O_2/40 min	264	39.13	0.627
Boat 1	264	40.11	0.560
Boat 2	263	38.15	0.693

temperatures for the annealing process. The standard annealing process is 1000°C for 15 min in an oxygen ambient. Time splits varied from 15 min to one hour in increments of 15 min. Temperature splits varied in increments of 50°C from 950°C to 1100°C. Because oxide produced by this process is not used in an ensuing step, the oxide thickness is not a critical parameter. Two wafers from each split underwent each process. Thickness, resistivity, and junction depth data were recorded using the previous format. Tables 2 and 3 show averages of the parameters for both pre-implant oxide thicknesses.

Data for all splits indicated minimum variation; however, results were inconclusive regarding which annealing temperature would improve breakdown voltage. Therefore, a standard annealing split and three experimental splits were processed again and tested for voltage breakdown. Results are listed in Table 4. The data suggests that although 1100°C provides acceptable results, the 1050°C annealing temperature yields the highest breakdown voltage.

Table 2. Average Data for Annealing Splits Using Standard Pre-Implant Oxide

Run Parameter	Thickness (Å)	Rs (Ω/cm^2)	Xj (μm)
1000°C/O_2/15 min (Standard)	401	38.10	0.770
1000°C/O_2/30 min	474	39.04	0.840
1000°C/O_2/45 min	530	40.96	0.800
1000°C/O_2/60 min	606	43.06	0.770
950°C/O_2/15 min	273	42.56	0.840
1050°C/O_2/15 min	605	33.61	0.850
1100°C/O_2/15 min	955	44.48	1.01

Table 3. Average Data for Annealing Splits Using Improved Pre-Implant Oxide

Run Parameter	Thickness (Å)	Rs (Ω/cm^2)	Xj (μm)
1000°C/O_2/15 min (Standard)	411	40.66	0.870
1000°C/O_2/30 min	478	41.88	0.850
1000°C/O_2/45 min	562	44.36	0.850
1000°C/O_2/60 min	658	46.48	0.850
950°C/O_2/15 min	276	44.52	0.970
1050°C/O_2/15 min	638	45.06	0.900
1100°C/O_2/15 min	1004	48.56	0.830

To complete the test, the two improved processes (pre-implant oxide at 950°C/O_2/40 min and implant annealing at 1050°C/O_2/15 min) were processed as a split production lot. Parametric electrical test data and probe test data were compared following standard processing. The data showed no difference between the split wafers and the standard wafers in voltage threshold shifts and sheet resistance. The number of parts

Table 4. Average Data, Including Breakdown Voltage, for Annealing Splits Using Standard and Improved Pre-Implant Oxides

Run Parameter	Thickness (Å)	Rs (Ω/cm^2)	Breakdown (MV/cm)
Standard Oxide			
1000°C/O_2/15 min (Standard)	397	38.46	4.59
1000°C/O_2/60 min	608	44.64	7.18
1050°C/O_2/15 min	607	43.48	8.40
1100°C/O_2/15 min	964	45.98	8.20
Improved Oxide			
1000°C/O_2/15 min (Standard)	410	41.14	7.64
1000°C/O_2/60 min	635	46.86	6.18
1050°C/O_2/15 min	640	45.68	8.45
1100°C/O_2/15 min	995	48.02	8.18

passing voltage breakdown increased, paralleling an increase from the probe data on the split difference. The probe yield was increased by an average of 9%.

ACCOMPLISHMENTS

A combination of thicker pre-implant oxide and increased annealing temperature produced the desired results of increasing the breakdown voltage. This increased breakdown voltage also resulted in increased overall wafer yield. Process changes have been implemented. Additional data from production lots using the improved process are not yet available, although a general improvement in product has been observed.