ERDA/JPL-954405-76/5
Distribution Category UC-63

AUTOMATED ARRAY ASSEMBLY TASK
PHASE I

Texas Instruments Report No. 03-77-22

Quarterly Report

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April 1977

JPL Contract No. 954405

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, under NASA Contract NAS7-100 for the U.S. Energy Research and Development Administration, Division of Solar Energy.

The JPL Low-Cost Silicon Solar Array Project is funded by ERDA and forms part of the ERDA Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays.

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SECTION I
INTRODUCTION

The overall goal of the Array Automated Assembly Task, Phase I, of the Low-Cost Silicon Solar Array Project is a comprehensive assessment of the processes, conceptual designs, and new technologies required to achieve, by 1985, annual solar cell array production capability greater than 500 megawatts per year at a cost less than $500 per kilowatt. This goal is being approached from two directions. The first is to build a model or models of the costs involved in the various steps used to fabricate solar cell modules. These costs are being analyzed in terms of present-day capabilities and projected capabilities. Also, new technologies will be fitted to these models to determine the cost ranges for solar cell processing using new or emerging technologies. The second approach is to determine the cost goals for each of the processing steps. The program will then undertake a series of studies that are intended to point the way from existing and projected costs to the cost goals. The design-to-cost concept will establish allowable costs for each cell manufacture/array assembly step consistent with the 1985 cost goals.

During this quarter, effort was concentrated on evaluating the technical feasibility of two key solar cell process steps, surface texture etching and patterned electroless nickel plating. Design improvements have been made on the long life LSSA module design that improve packing density (efficiency) and lower cost. A follow-on program featuring sensitivity analysis of solar cell performance versus physical parameters has been initiated.

SECTION II
TECHNICAL DISCUSSION

The approach this quarter has been to complete the items on the technical assessment, in particular to evaluate texture etching as a technically feasible operation and to evaluate electroless metal plating on Si and to initiate the sensitivity analysis on solar cell processing steps. The technical evaluation of texture etching was based on success using this technique as reported by others[1,2] and on the favorable cost projections made earlier in this study. The technical evaluation of electroless Ni plating was based on the cost impact of contact metallization in the solar cell processing sequence. Technical problems still exist in the application of electroless metal plating to the shallow front-side junction on solar cells.

A. TEXTURE ETCHING

The concept of using preferential etchants to produce a more absorptive (less reflective) solar cell surface was introduced in 1974.[1] The most popular method at present is to convert ⟨100⟩ surfaces to arrays of tetrahedral protrusions (texture) having ⟨111⟩ facets by the use of either hydrazine hydrate[2] or sodium hydroxide solutions.[3,4] New developments are still occurring in the process technology and a potentially significant finding, proximity texturing, is disclosed in this report.

The optimization of surface texturing as a process element in solar cell fabrication is based on the following criteria:

1) Low Reflection

   Total illuminated surface should be covered with a uniform array of pyramids. Pyramid size should be greater than maximum usable light wavelength.

2) Low Cost

   Process should be automatable for high throughput with low capital equipment cost and low materials cost.

3) Process Control

   Process should be repeatable with low sensitivity to concentration, ambient effects and handling.

4) Metallization

Good uniformity of pyramid perfection and height for compatibility with metallization process.

5) Safety

Etchants and by-products should not impose undue safety hazards. Sodium hydroxide solutions are better candidates than hydrazine solutions.

Based on these criteria, sodium hydroxide solutions are to be preferred over hydrazine hydrate solutions as texture etches. Metallization of the textured surfaces appears to present no problem when the pyramids are of uniform size. Schwartz[3] reported "the lower the NaOH concentration, the smaller, deeper, and better defined are the crystallographic pits, and this effect is independent of etch temperature." A concentration of 1% and later 2% with added isopropyl alcohol was chosen for this process. Other workers[4] are using similar procedures and are achieving very consistent results.

This study has observed that surface texturing on ⟨100⟩ Si surfaces is enhanced by proximity to another surface, proximity texturing, when using dilute aqueous NaOH etchants. (In fact, it is possible to texture one area or surface of a wafer while other unmasked areas remain in a polished state.) Optimum spacing for proximity texturing is between 500 and 1000 micrometers. For example, if two wafers are held face-to-face at a spacing of 750 μm, the facing surfaces can be textured while the back surfaces remain polished. The theoretical basis for this effect is not completely understood but the effect is well behaved and consistent. In this fashion, wafers can be front-side textured, back-side polished by carrying out the texture etch process in a suitably designed holding fixture. Since back-side texturing offers no advantage in solar cell fabrication, proximity texturing promises to be an important addition to the list of usable process elements in solar cell fabrication.

The reduced reflection from the textured surface reduces the need for a "good" AR coating. Typical reflection data as a function of incident wavelength on polished and textured surfaces is shown in Figure 1.

B. ELECTROLESS NICKEL DEPOSITION

Metallization for front-side and back-side contacts on a solar cell represents a significant cost element in the fabrication of silicon solar cells. Patterned electroless metal plating appears to be one approach to lower cost for contact metallization. A brief investigation of electroless nickel plating was undertaken to establish technical feasibility. In order to maintain minimum material cost, electroless plating of patterned contacts was chosen.

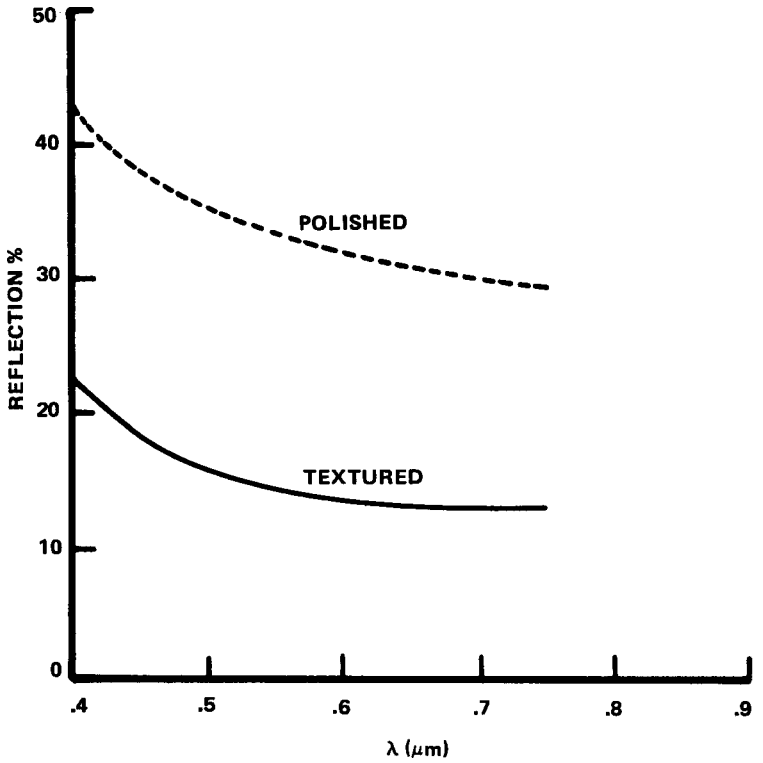

Figure 1. Total Reflection for Polished and Textured Surfaces

Three approaches to patterned electroless Ni plating were investigated: (1) plating through an oxide mask, (2) plating through a photoresist mask, and (3) photo-impeded metal deposition (PIMDEP). Approaches (1) and (2) gave essentially identical results and are reported together.

Electroless Ni plating solution, either acidic or alkaline, readily plate onto Si surfaces after a catalytic or sensitizing operation. Plating rates are a function of temperature and plating bath composition. All surfaces investigated, as sawed, chemically polished or texture etched, would readily plate. Either silicon oxide or standard photoresist will act as a plating mask. Photoresist has also been used to pattern the sensitizer, the resist can then be removed and the plating will proceed only in the sensitized regions. Several commercial or published sensitizers were tried and all were effective. This approach is not as cost-effective as desired due to the patterning operation. One possible compensating factor is the use of an AR coating as the masking medium. This has not been demonstrated.

The PIMDEP approach uses UV light to desensitize part of the surface and thereby achieve patterned plating. The process sequence that has been successfully used on other materials is as follows.

Apply $SnCl_2$

Expose to UV light

Apply $PdCl_2$

Electroless Plate

The chemistry of the process is straightforward, the Sn^{+2} is oxidized to Sn^{+4} under the influence of UV light to deactivate the exposed areas. $PdCl_2$ reacts with the remaining Sn^{+2} to produce a very thin layer of Pd^0 and Sn^{+4} (monatomic layer?). The thin layer of Pd provides the plating surface for the electroless plating operation. Very dilute solutions of $SnCl_2$ and $PdCl_2$ are used, so the material cost is very low. Several attempts were made using variations of this basic process. Only partial success was achieved. The patterned surfaces would exhibit selective plating for a period of time, then the "deactivated" area also begins to plate. Selective plating was only achieved for plating thicknesses of a few thousand angstroms.

Post plating sintering of the plated Ni to improve adhesion and ohmic contact to the thin, 0.3 μm, diffused layer on the front surface has been only partially successful. Significant degradation of the N^+P junction under the Ni plated contact occurs after sintering at 420°C for 30 minutes. Contact resistance measurements have not been made due to the junction degradation.

Although patterned electroless Ni plating appears promising as a low-cost metallization, significant process development will be necessary before this technology could be implemented into a solar cell process.

C. LSSA MODULE DESIGN

Further evolutionary improvements have been made in the LSSA module proposed in earlier reports. The current modification is called LSSA Module Design III. Design III eliminates the outside flanges, thereby improving the overall external dimensions, and eliminates the spacer ring. (See Figure 35 of the 1976 Annual Report.)

The design is a more regid structure because the stiffening ribs are now part of the substrate. The substrate is made by deep drawing followed by bending the flanges inward (Figure 2). The lock frame is external and made of four parts, eliminating cumbersome corner welding operations. The spacer ring has been eliminated by recessing the cell array area. At the same time, the sealable circumference is cut in half, improving the probability of obtaining a hermetic enclosure.

The changes incorporated into Design III have reduced the estimated cost by $\approx$14%. An estimated add-on cost for this module design is given in Table 1.

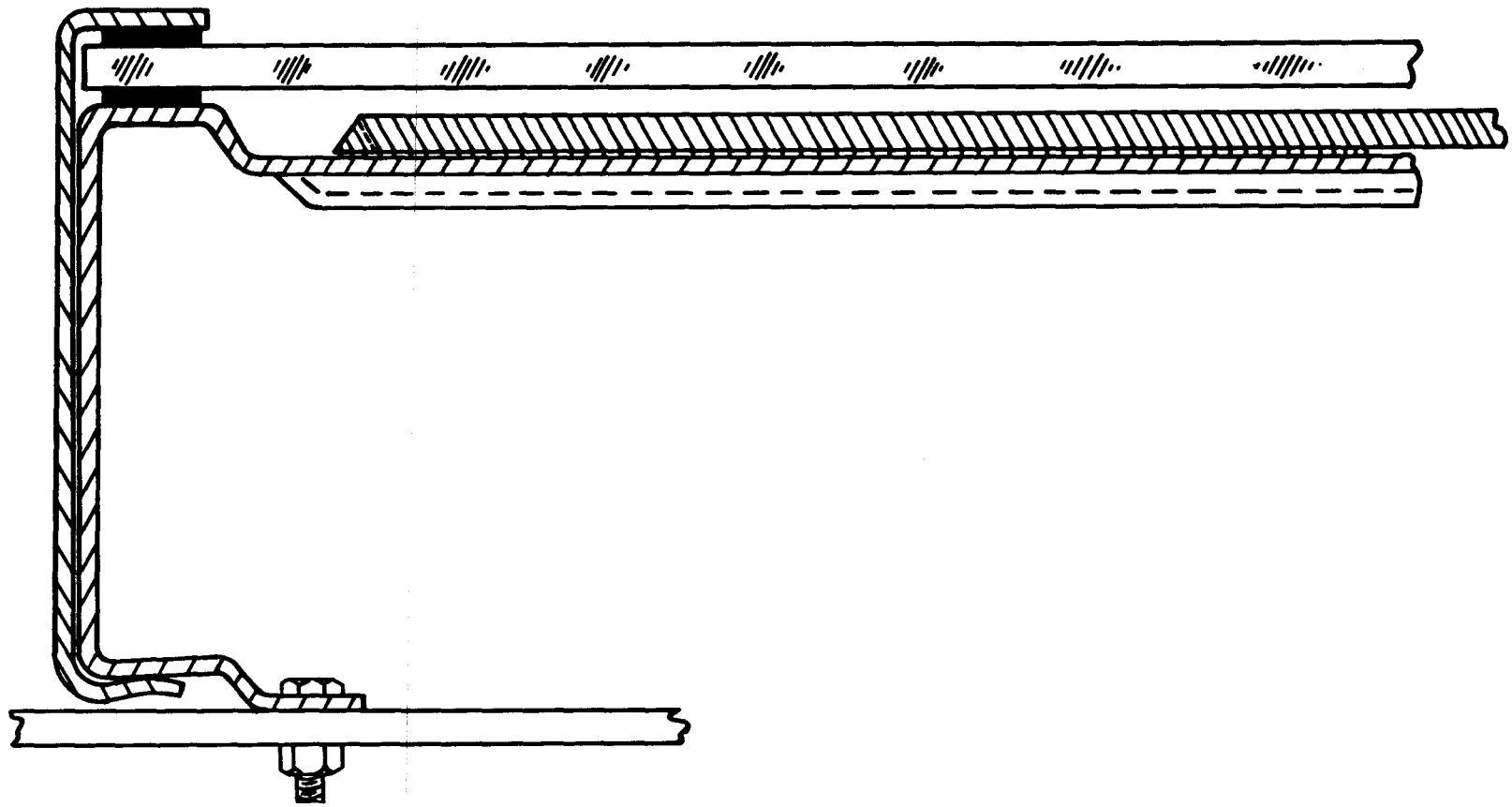

Figure 2. Cross Section of Proposed LSSA Module Frame – Design III

Table 1. Estimated Material and Component Cost of Proposed LSSA Module – Design III

Item	Low		Probable		High	
	$/mod	$/W	$/mod	$/W	$/mod	$/W
1. Glass Cover						
Ann. window	2.66	0.040				
Temp. window			3.84	0.057		
Temp. low iron					9.28	0.130
2. Sealant two places	0.20	0.003	0.24	0.004	0.28	0.004
3. Substrate						
Enameled steel	4.64	0.069	6.04	0.090	9.60	0.134
4. Front conductor	0.60	0.009	0.75	0.011	1.00	0.014
5. Back conductor	2.01	0.030	2.41	0.036	2.82	0.039
6. Adhesive	0.81	0.012	1.22	0.018	1.62	0.023
7. Connectors	0.75	0.011	1.00	0.015	1.50	0.021
8. Lock frame						
Enameled steel	1.60	0.024	2.06	0.031	2.94	0.041
9. Lock frame fasteners	0.15	0.002	0.25	0.004	0.35	0.005
Subtotal	13.42	0.200	17.81	0.266	29.39	0.411
Assembly L+OH	3.64	0.054	4.85	0.073	7.28	0.102
TOTAL M+L+OH	**17.06**	**0.254**	**22.66**	**0.339**	**36.67**	**0.513**

D. SENSITIVITY ANALYSIS

The objective of this activity is to quantify the sensitivity of solar cell performance to manufacturing process variables. For this study, cell performance is characterized by the efficiency components which comprise conversion efficiency. These efficiency components are related to different physical parameters of the cell as shown in the matrix of Figure 3. Models are available for relating physical device parameters to process variables.

The approach of this program will be to develop theoretical and/or empirical models for the dependence of efficiency components on physical parameters. Test structures for measurement of physical parameters will be designed such that they can be fabricated on each cell. Models will be validated and refined by correlating cell performance to physical parameters. Based on cell and process models, tests will be designed and implemented to evaluate process control requirements.

PHYSICAL PARAMETER	EFFICIENCY COMPONENT						
	REFLECTION	METAL COVERAGE	COLLECTION-DIFFUSED REGION	COLLECTION-BASE REGION	VOLTAGE FACTOR	FILL FACTOR	SERIES RESISTANCE
INSULATOR THICKNESS	X						
REFRACTIVE INDEX	X						
FINGER WIDTH		X					X
METAL SHEET RESISTANCE							X
METAL CONTACT RESISTANCE							X
DIFFUSED REGION SHEET RESISTANCE							X
JUNCTION DEPTH			X				
BASE RESISTIVITY					X		
BASE LIFETIME				X		X	

Figure 3. Dependence of Efficiency (Loss) Components on Physical Parameters

Quantitative relationships between efficiency components and physical parameters will be established as described below:

1) A computer program has been written which calculates reflection, as a function of wave length, and percent of the total spectrum reflected. The sensitivity of reflection efficiency to insulator thickness and refractive index is obtained directly.

2) A computer program was developed earlier in this contract to determine the spacing of metal fingers which minimizes the sum of metal-coverage and series-resistance losses and calculates these losses for the cell. A modification of this program will be used to calculate the sensitivity of coverage efficiency and series-resistance efficiency to variations in finger width, metal sheet-resistance, and diffused sheet-resistance.

3) Computer programs are available to calculate dark current and light-generated current for solar cells in terms of the physical structure. A program of this type will be used to compute voltage factor and collection efficiency as a function of physical cell parameters.

4) For fixed values of open circuit voltage and series resistance, fill factor depends upon the value and slope of the excess (exp [qV/NKT]) current. Excess current is related to the concentration of recombination centers, which can be monitored by minority carrier lifetime. Relationships between excess current and lifetime will be developed empirically.

Desirable features of the test patterns for measuring physical parameters are as follows:

1) Test patterns should be compatible with in-line probing on 100% of cells.

2) Test patterns should add no additional complexity to processing of cells.

3) Test patterns should not deteriorate cell performance or reduce useful area of cell.

4) Test patterns should be compatible with various process options; e.g., screen printing versus photolithographic metallization; etched versus planar junctions; N on P versus P on N cells.

Test patterns under consideration are described. Metal sheet resistance will use a standard 4-point pattern shown in Figure 4. Current is supplied through the outer pads and voltage measured at the inner pads to eliminate contact resistance effects.

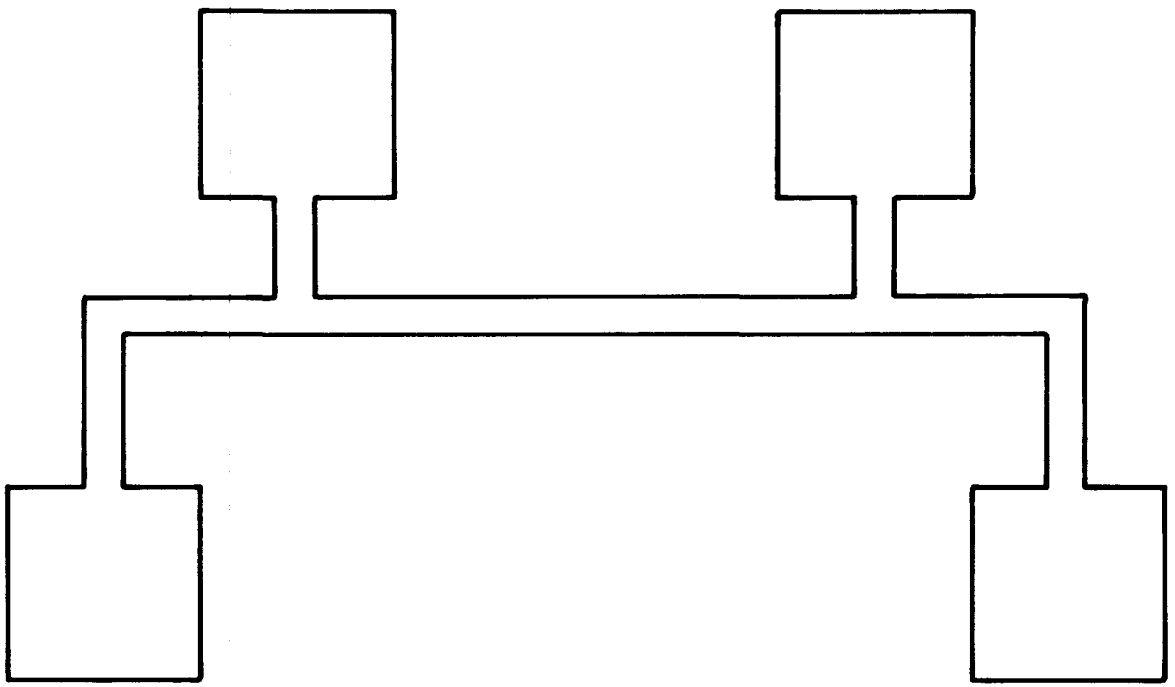

Figure 4. Test Pattern for Metallization Sheet Resistance

A pattern of this type can be used for measuring diffused sheet resistance only if the diffused region is patterned. For mesa-type cells, this requires an extra etch step. For nonplanar cells, a guard ring around the patterned region is required to prevent inversion of the surface. It would be desirable to have a closed test pattern which would not require definition of the diffused area. One proposed configuration, shown in Figure 5, consists of concentric metal rings, alloyed to the diffused layer.

The pattern is designed such that the diffused region resistance between each set of contacts is equal. If contact resistance is significant, the resistance readings will differ. Relationships must be developed to separate diffused sheet resistance and contact resistance from combinations of resistance readings.

A diode will also be included as a test pattern. The diameter (or length of side) for the diode should be somewhat larger than the cell thickness so that current spreading is not significant. Reverse recovery time measurements will give a direct indication of lifetime. Additionally, dark VI characteristics can be related to open circuit voltage for an ideal cell.

It is expected that these masks will be located near the center of the cell. The conceptual design for the cell array configuration includes a triangular bar, 0.30 cm on each side, across the major diagonal of each hexagon. Since the area under this bar will not contribute to light collection, the test patterns can be placed there with no penalty on efficiency. The metal sheet resistance test pattern and the diffused region sheet resistance test patterns are compatible with cell fabrication. For mesa cells, an additional mask and etch operation will be needed to define the test diode.

Cells will be fabricated with variations of process parameters to correlate device performance with measured device parameters. Device and process models will provide a basis for relating the sensitivity of cell performance directly to processing parameters, e.g., times and temperatures.

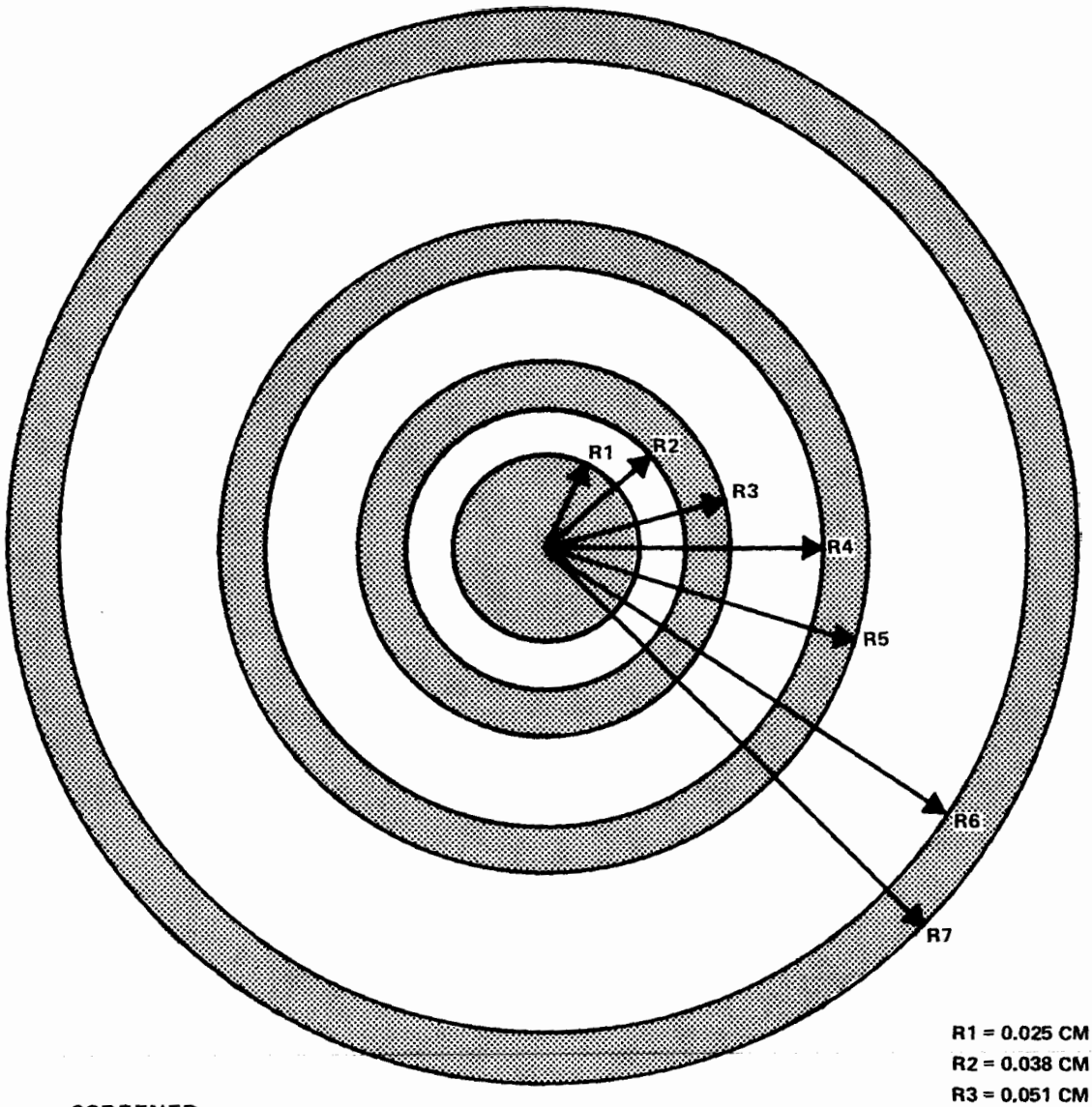

Figure 5. Test Pattern for Diffused Region Sheet Resistance and Contact Resistance

SECTION III
CONCLUSIONS AND RECOMMENDATIONS

Texture etching of ⟨100⟩ Si solar cell front surfaces is a very attractive, and cost-effective process element for solar cell fabrication. Proximity texturing is a very useful addition to the low-cost silicon solar cell process library.

Patterned electroless plating is an attractive low-cost contact metallization process. Technical feasibility has not been conclusively demonstrated. Process development work is required in this area.

Design improvements have been made in the proposed long-life LSSA module that improve module efficiency and reduce material cost. Further improvements are required to meet low-cost goals.

Solar cell efficiency components can be related to physical device parameters. Specific sensitivity analysis is required to identify parameters that require close process control.

SECTION IV
NEW TECHNOLOGY

An innovation in texture etching called proximity texturing was discovered this quarter. Proximity texturing is a maskless technique for texturing one side of a ⟨100⟩ Si wafer in dilute aqueous NaOH etchant while retaining a polish on the other side. The process is carried out by bringing a surface parallel to and in proximity to the ⟨100⟩ Si surface being textured. Spacings of the order of 1 mm are appropriate. When the aqueous NaOH etchant concentration is adjusted to a concentration range slightly greater than the normal range used for texture etching, the proximate surface texture etches while the reverse surface polish etches. No masking is required.

SECTION V
PROGRESS SUMMARY

The progress on each of the activities in this task is shown in Figure 6. The initial phase of this program is complete. Progress on the follow-on program is shown in Figure 7.

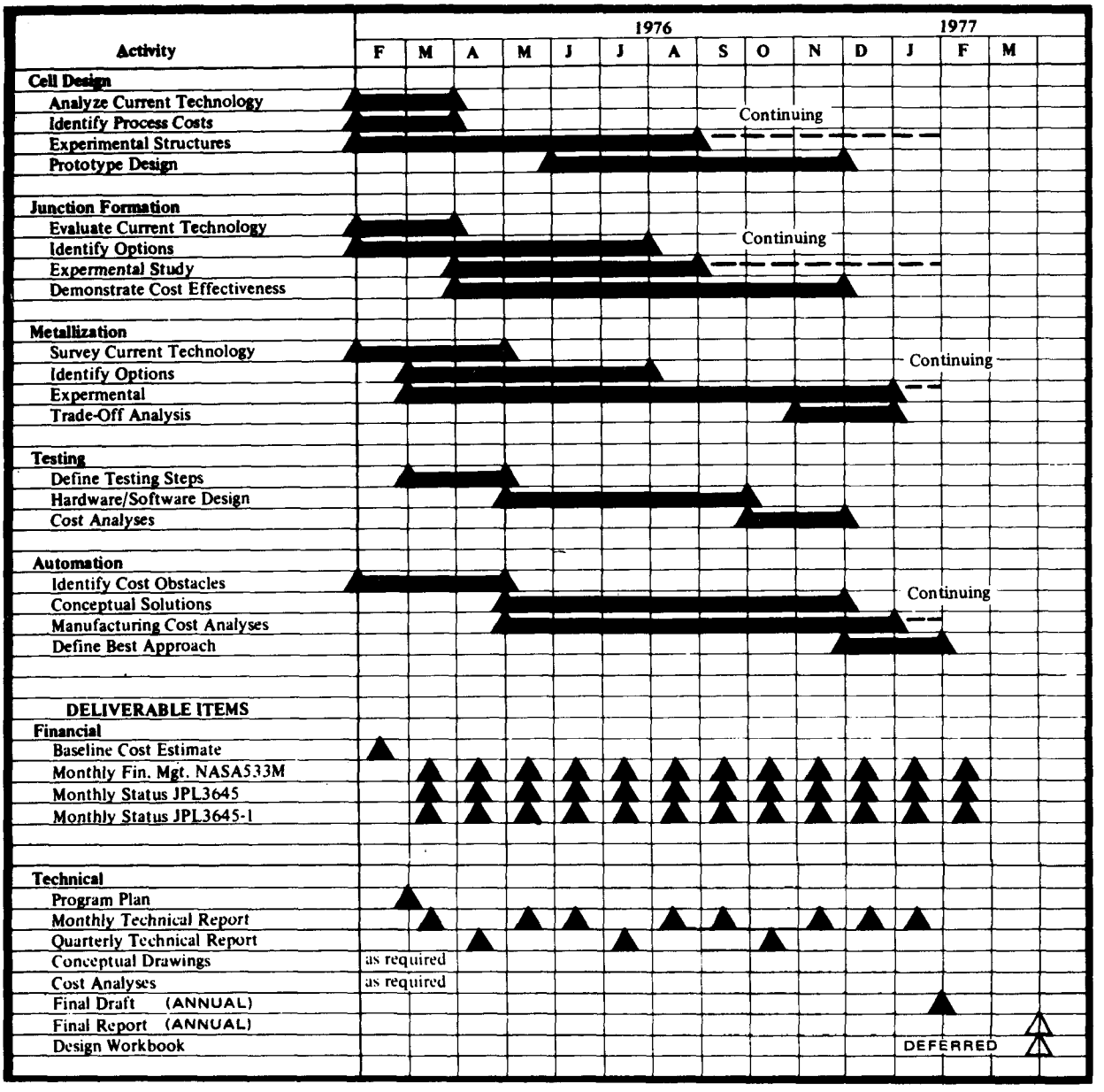

Figure 6. Work Plan Status

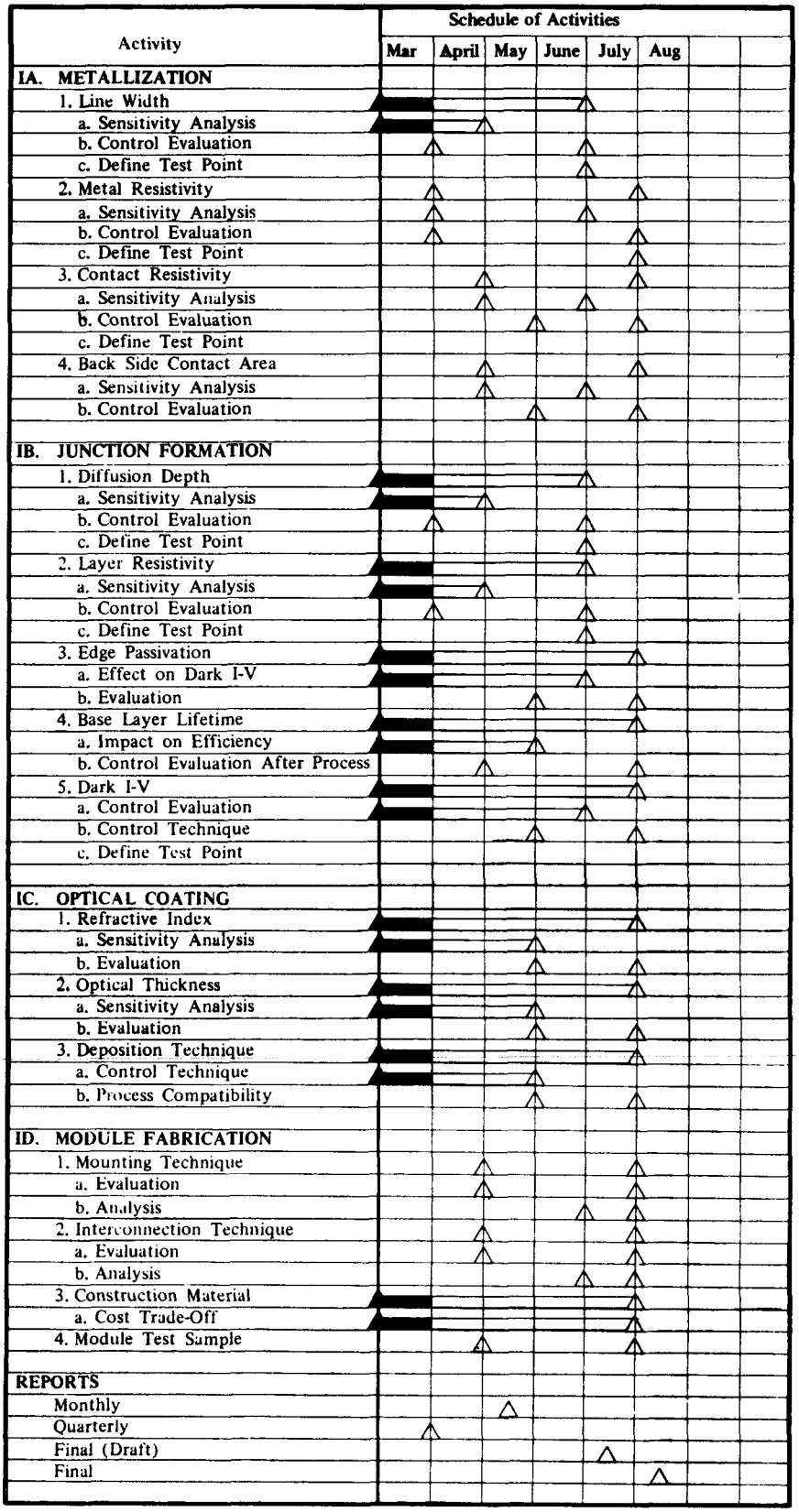

Figure 7. Program Plan

SECTION VI
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