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Using Embedded Microcontrollers in Radar Test Equipment

Kansas City Division

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Loren E. Riblett

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USING EMBEDDED MICROCONTROLLERS IN RADAR TEST EQUIPMENT

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Loren E. Riblett

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Technical Communications
Kansas City Division

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USING EMBEDDED MICROCONTROLLERS IN RADAR TEST EQUIPMENT

by

Richard S. Binney
Loren E. Riblett
Allied-Signal, Inc.,
Kansas City Division*

Abstract

With the recent advancements in microcontroller technology, radar test equipment can be designed to improve the accuracy of measurements being made and simplify designs. An embedded integrator monitor design application (hardware and software) is presented and comparisons are made between the embedded design and the more traditional discrete design approach.

Introduction

As radar becomes more sophisticated, radar test equipment must become more accurate, functional, and flexible.

Before microcontrollers were developed, many of the desired capabilities in custom test equipment were not practically implemented due to the complexity of discrete digital designs. Even microprocessor designs of the early 80's were quite combursome and required lots of tedious code writing even for the most simple minded applications (not to mention a good background in microprocessor hardware design).

Late 80's technology now provides us with a simpler solution for these involved digital control problems. Several microcontrollers are available from the 4-bit to 32-bit varieties which are much more self-contained than a standard microprocessor and are easily programmed in high level languages (BASIC, C, PL\M to name a few).

Intel's 80C196 microcontroller was selected as the heart of the embedded designs because of its data handling throughput (16-bit widths at speeds to 20 MHZ) and adequate development tools and support. C was selected as the embedded language because of its versatility and current popularity as an embedded language.

* OPERATED FOR THE UNITED STATES DEPARTMENT OF ENERGY UNDER CONTRACT NUMBER DE-AC04-76-DP00613

Measurement Problem

Monitoring capabilities were required for a 16-bit, 1 KHZ word rate emitted from a radar fuze. It was desired to monitor and display the current integrator value as well as the mean and sigma values for a sample size n in real time. Historically, this information would have been acquired and displayed on the host CRT or printer. This design required dedicated, real-time monitoring without the need for external controller intervention (however communication between the embedded design and the host was necessary). Buffering of the integrator data was also required for playback of previous integrator values.

Hardware Solution

Four basic hardware functions can be identified as a solution to the embedded design requirements. Those functions are processor inputs and memory, memory-mapped outputs, controller-to-GPIO interconnections, and integrator FIFO data.

Figure 1 represents the schematic diagram for the processor inputs and EPROM memory. Essentially the 16-bit parallel data (D0 thru D15) is presented to the microcontroller input ports 0 and 1. Three handshake lines are provided to ensure solid data-to-controller flow control. Controller software is stored in the two latched EPROMs (U22 and U23). These two 8-bit memories are connected in a parallel fashion to provide 16-bit wide program data. Oscillator, reset, and microcontroller operation indicators circuits are also shown.

The memory-mapped output circuits (Figure 2) provide three 16-bit memory locations to which three panel displays can be connected (for displaying integrator data, mean, and sigma values). Line drivers (U7 thru U9 and U16 thru U18) allow the host computer to selectively read any one of the three displayed values. A minimum of address decoding hardware is also necessary to decode the three displays as well as the FIFO hardware (Figure 4).

Figure 3 details the GPIO interface circuitry allowing for communication between the embedded design and the host computer (HP 200 or 300 series). Controls available on the host computer include which of the three panel displays to read, controller reset, mean and sigma calculation restart, sample size selection, and FIFO read control.

The FIFO circuitry (Figure 4) provides a circular storage location for the last 2K words of integrator data. This data is available for playback to the host computer on demand. Once 2K of integrator data has been captured, the oldest integrator value is discarded leaving room for the next integrator word (thus giving the buffer its circular nature).

Software Generation

One of the biggest advantages of embedded designs is the design flexibility one has as a result of the embedded software. Applications that were once complicated hardware designs have become simple, standardize hardware projects with flexible, intelligent code. As mentioned earlier, the C programming language was chosen as the development language because of it popularity and easy adaptation to the embedded controller world.

Intel makes available their IC-96 C compiler for the 8096 family of microcontrollers. It provides the user with full floating point math capabilities in addition to near ANSI C standardization. Software has been generated and tested in Microsoft C first and then submitted to the IC-96 compiler with little or no change necessary.

The software flow-chart (Figure 5) shows the embedded software organization. There are two main entry points in the bulk of the process, a reset embedded control entry which is accessed following an embedded controller reset, and a restart entry which can start a FIFO read or sample size change.

The 80C196 initialization includes program variable and integrator data flow initialization and processor interrupts set-ups.

Provided the controller requests a FIFO read, the processor reads the buffered integrator words and writes them to the BCD data display (address 8001H, J2 in Figure 2). The sample size (n) on which the running mean and sigma calculations are made is then read and saved internal to the program.

Reading integrator data requires both the NEW DATA and DATA VALID inputs to be logic highs (+5V). Once these conditions are met, the data is acquired, running mean and sigma is computed, and the current integrator value is displayed. The running mean and sigma values are only displayed once the n samples have been satisfied. Again, full floating math computations are made in this control loop, in real-time without any program optimization for speed required. This is a solid indicator of the embedded controller's speed capability.

Benchmarking and Hardware Emulation

Long before any custom hardware is built, most of the embedded software can already be written, tested, and benchmarked to ensure timely operation on the target hardware. This is easily accomplished by combining two development products available for the target processor.

The first of these products is a microcontroller evaluation board. These evaluation boards provide the user with a board containing memory, I/O, and support configurations to at least partially test out any embedded software. Such a board can serially communicate to a host PC and allow a host of debugging commands.

Because some of the embedded controller's capabilities are used by the monitor program residing on the evaluation board (for serial communications, etc) this author prefers the combination of the evaluation board and an In-Circuit Emulator (ICE). The ICE is essentially a window into the target hardware and is invaluable for viewing user ROM contents and memory locations. Little or no performance degradation has been seen when operating the embedded integrator monitor board on the ICE (compared to operation of the board with its own processor).

The mentioned development hardware is an excellent hardware platform on which to test, debug, and benchmark embedded software. By toggling the processors high speed outputs (HSI.0 thru HSI.3) within critical timing loops and viewing those outputs on an oscilloscope accurate benchmarking can be achieved.

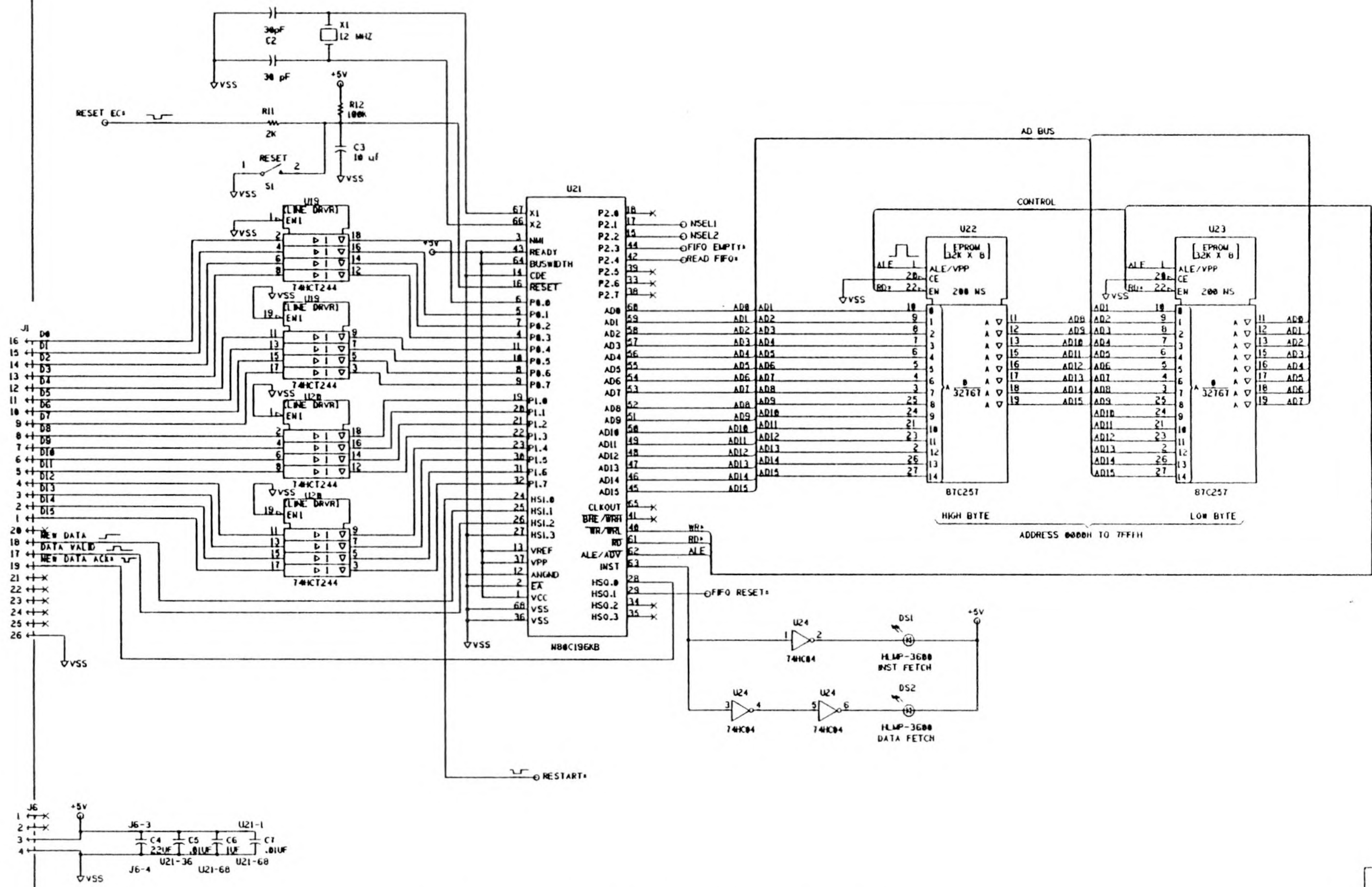
Summary

This paper describes a single embedded microcontroller application for radar test equipment. An embedded microcontroller is being used to calculate digital integrator statistics in real-time.

All indications are that embedded controllers are the design of choice for involved digital control schemes. All software has been debugged and benchmarked using development hardware. Design complexity has been decreased as a result of these designs from multi-sheet designs to ones of minimal hardware and software.

SKETCH CLASSIFICATION
UNCLASSIFIED

EMBEDDED CONTROLLER



DECOUPLING CAPS SHOULD BE PLACED AS CLOSE ABOSSIBLE TO DEVICE PINS INDICATED HERE

FIGURE 1. PROCESSOR INPUTS AND MEMORY

TEST EQUIPMENT
ENGINEERING
SKETCH

SKETCH NUMBER
EMBEDINT

SKETCH CLASSIFICATION
UNCLASSIFIED

SIZE	ISSUE	SCALE None
E	3	SHEET 1 OF 4

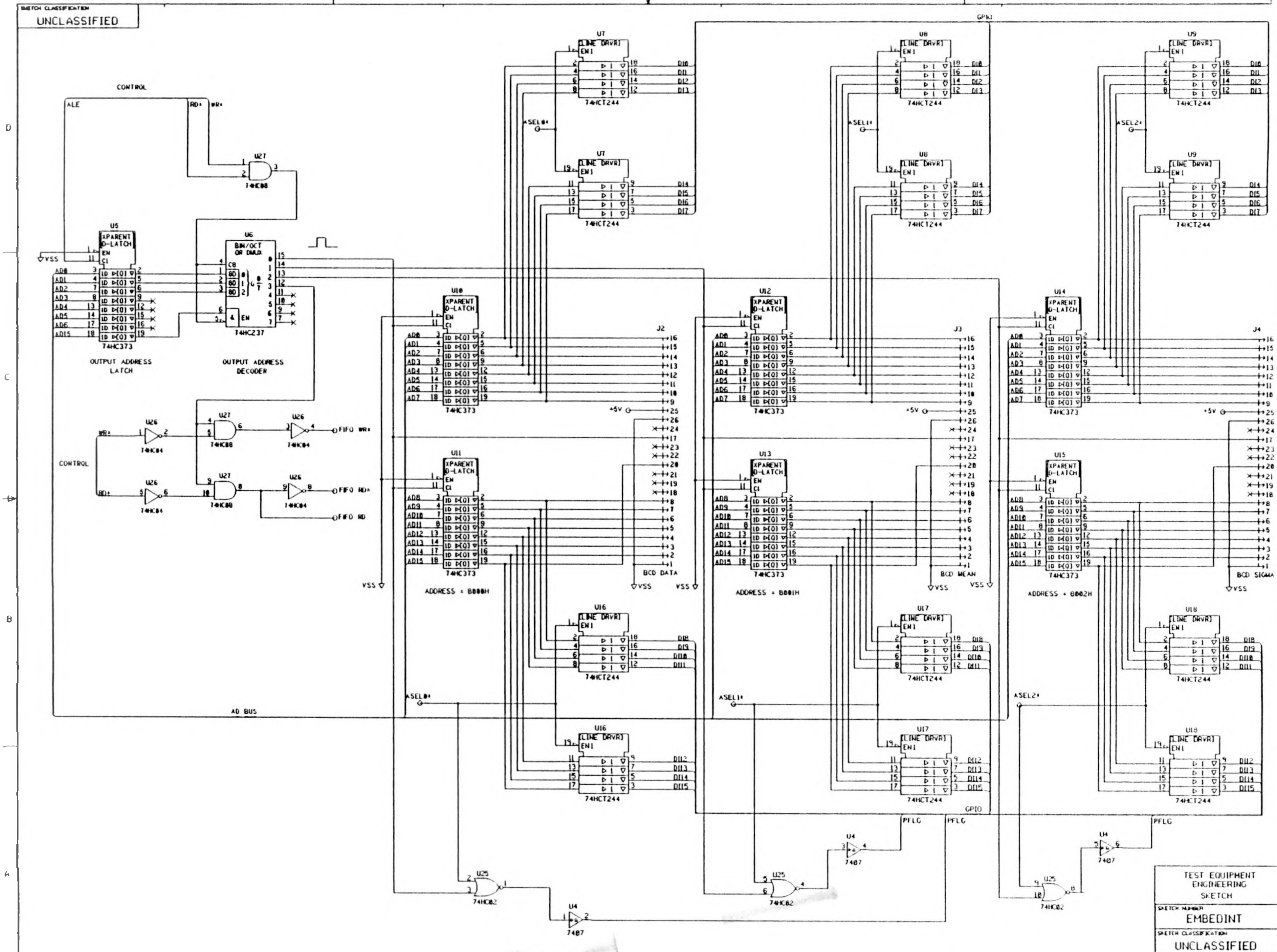


FIGURE 2. MEMORY MAPPED OUTPUTS

SKETCH CLASSIFICATION
UNCLASSIFIED

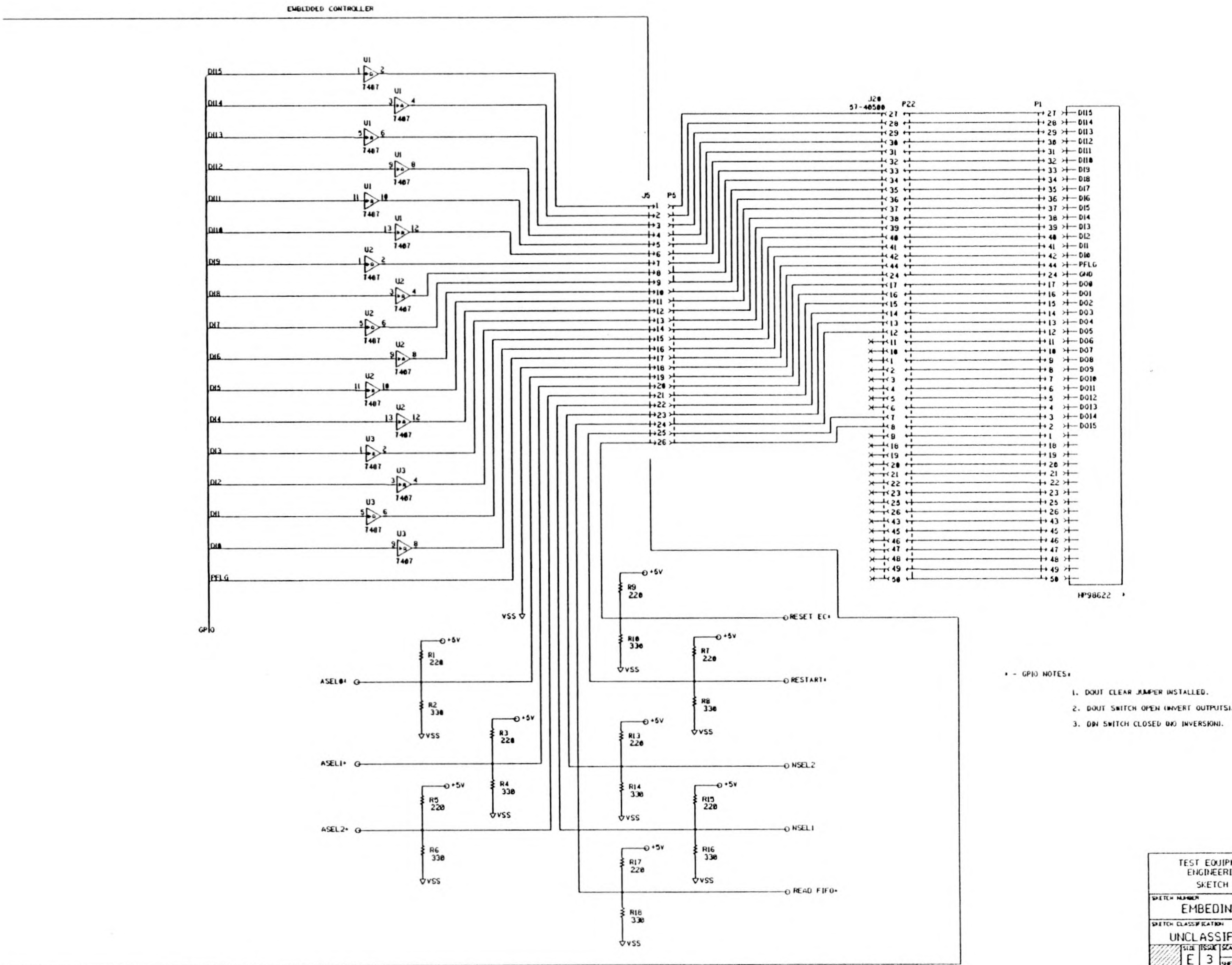


FIGURE 3. GPIO INTERFACE CIRCUITRY

TEST EQUIPMENT ENGINEERING SKETCH

SKETCH NUMBER: EMBEDINT

SKETCH CLASSIFICATION: UNCLASSIFIED

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SHEET 3 OF 4

SKETCH NUMBER EMBEDINT

SKETCH CLASSIFICATION
UNCLASSIFIED

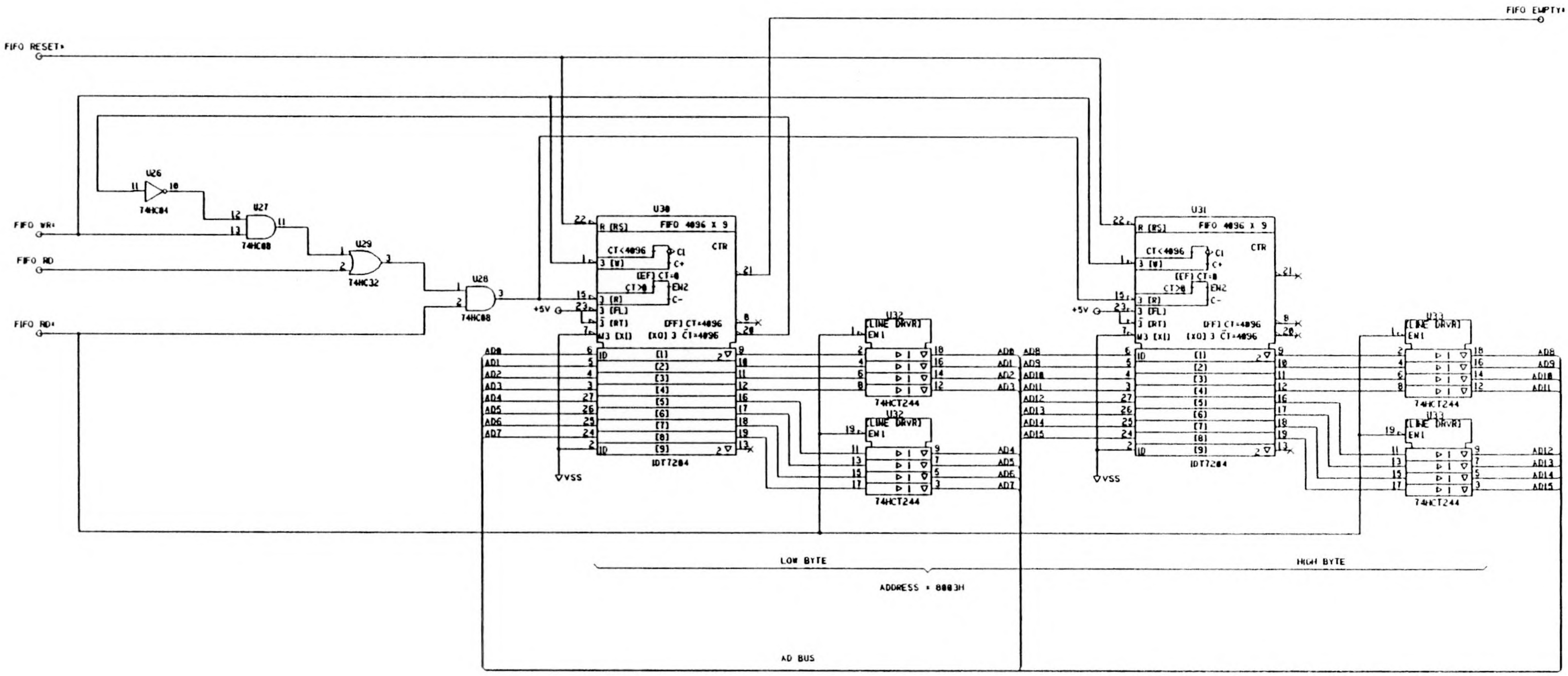


FIGURE 4. FIFO CIRCUITRY

TEST EQUIPMENT
ENGINEERING
SKETCH

SKETCH NUMBER
EMBEDINT

SKETCH CLASSIFICATION
UNCLASSIFIED

SIZE E | ISSUE 3 | SCALE None | SHEET 4 OF 4

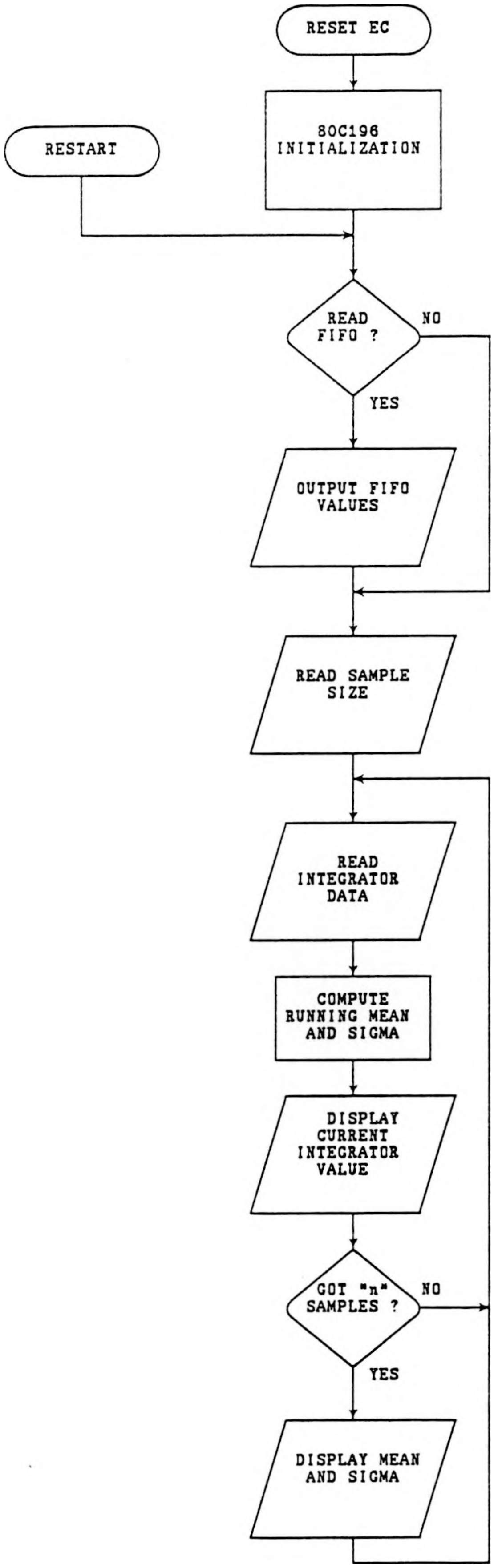
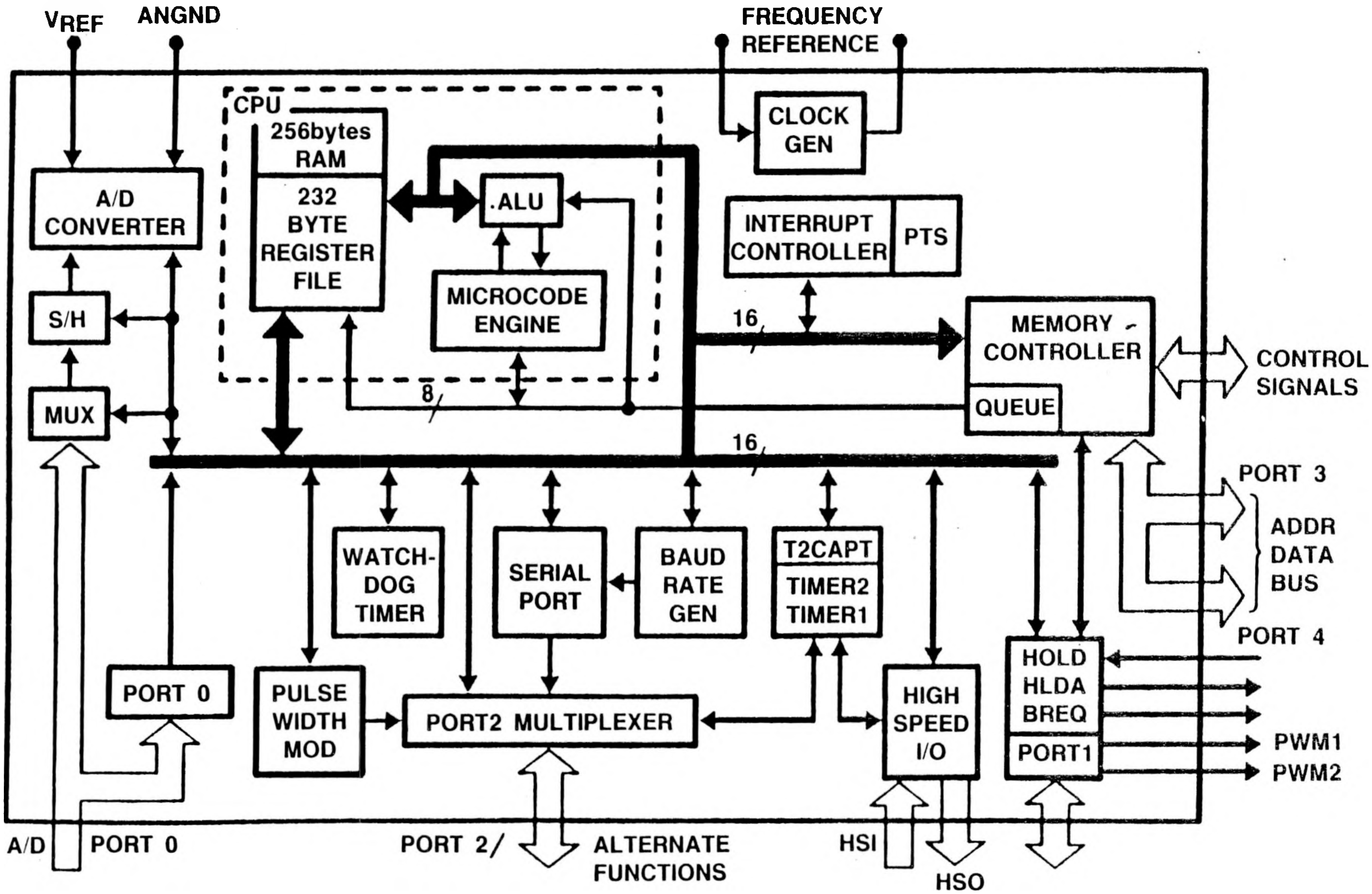


FIGURE 5. SOFTWARE FLOW CHART

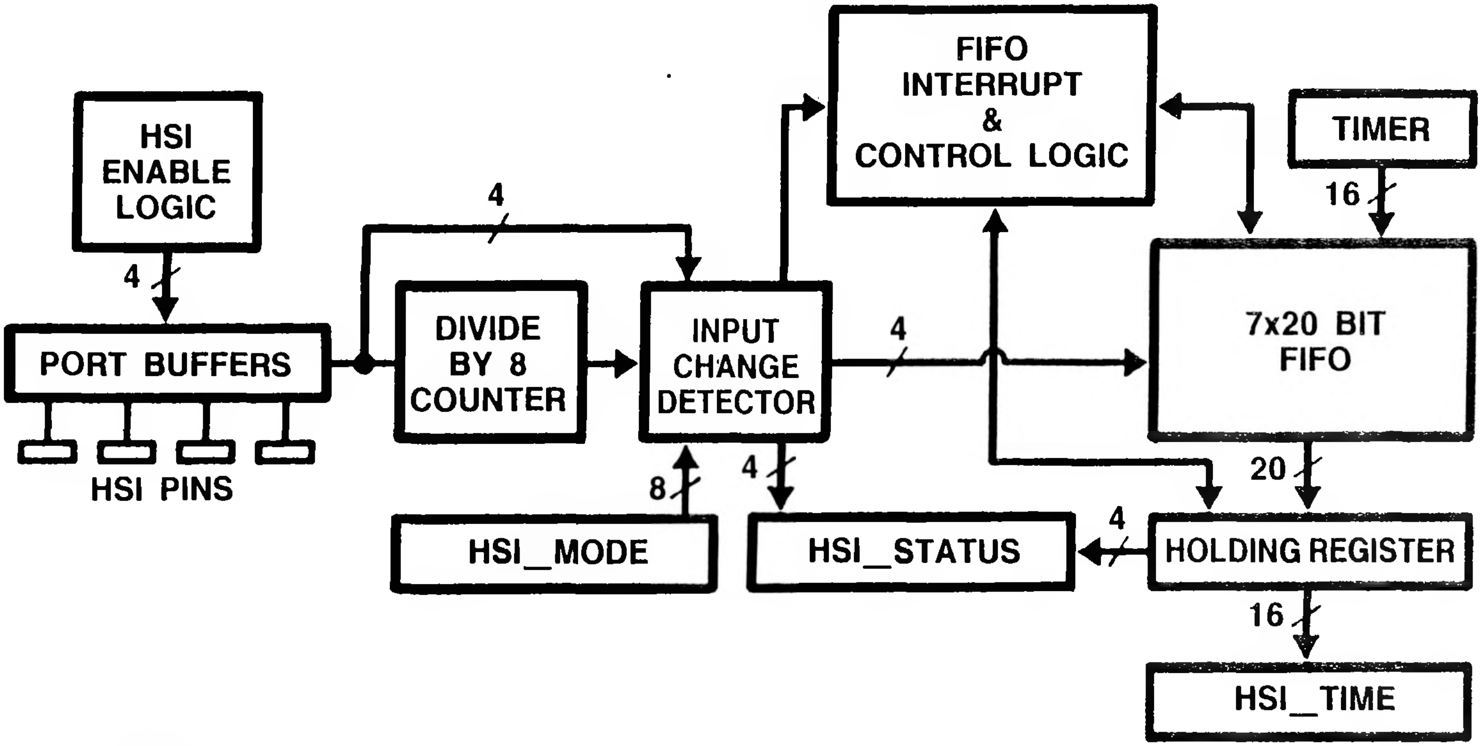
80C196KC BLOCK DIAGRAM



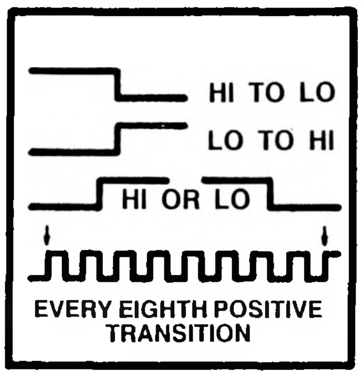
	FFFFH
EXTERNAL MEMORY OR I/O	6000H
INTERNAL ROM/EPROM OR EXTERNAL MEMORY	2080H
RESERVED	205EH
PTS VECTORS	2040H
UPPER INTERRUPT VECTORS	2030H
ROM/EPROM SECURITY KEY	2020H
RESERVED	2019H
CHIP CONFIGURATION BYTE	2018H
RESERVED	2014H
LOWER INTERRUPT VECTORS	2000H
PORT 3 AND PORT 4	1FFEH
EXTERNAL MEMORY	200H
ADDITIONAL RAM	100H
RESISTER FILE AND EXTERNAL PROGRAM MEMORY	0

80C196KC MEMORY MAP

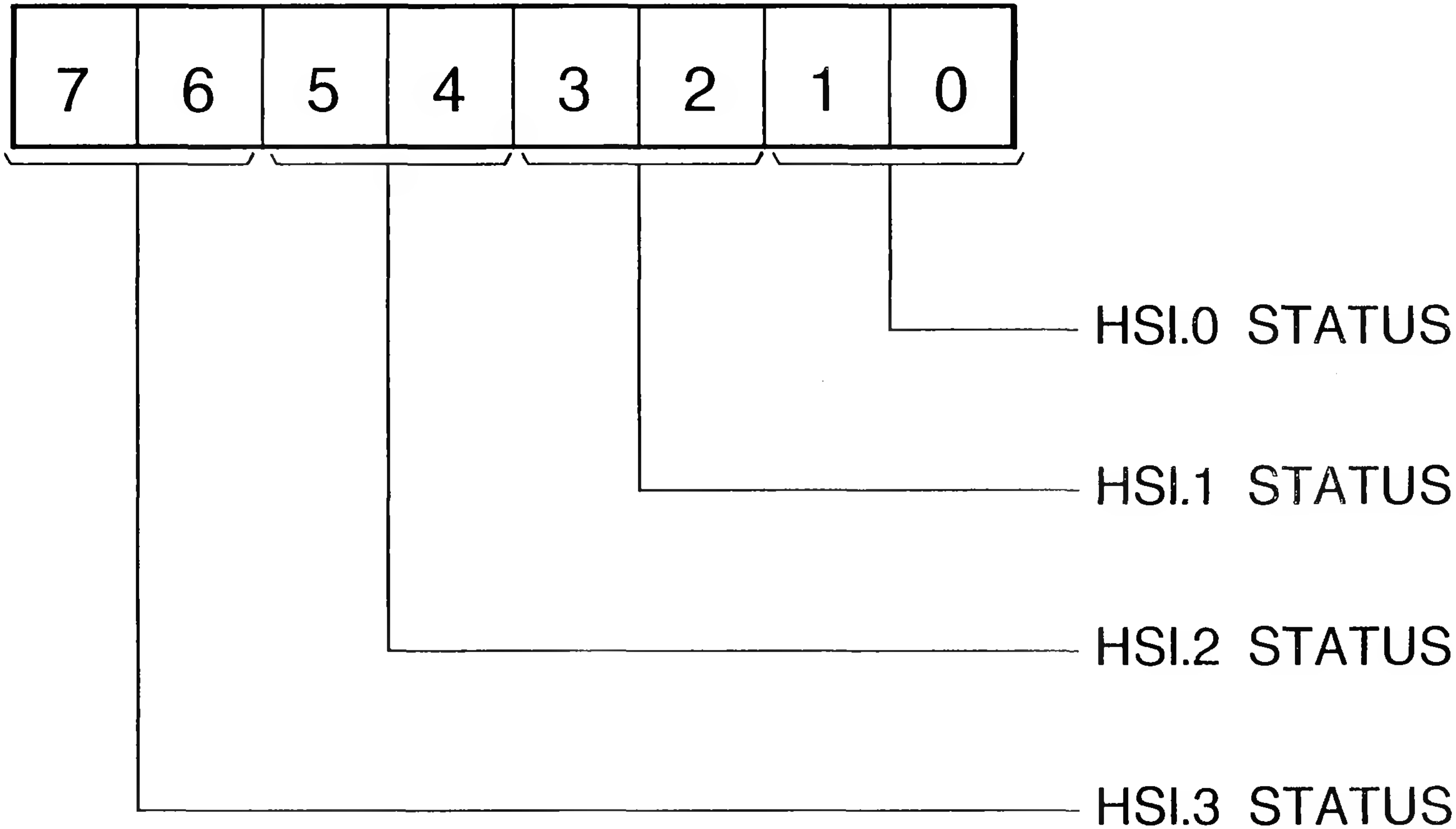
HIGH SPEED INPUT UNIT



HSI TRIGGER OPTION

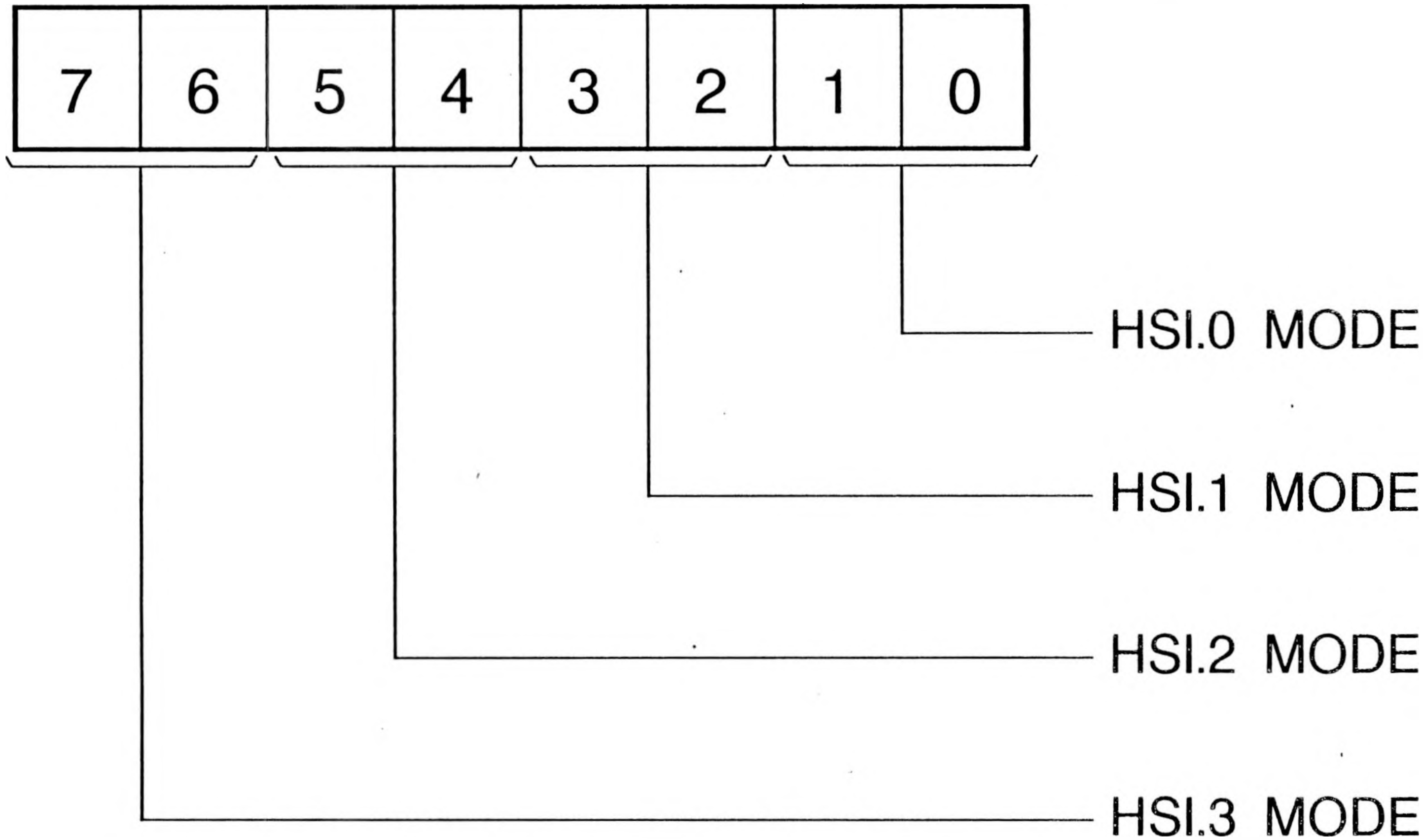


HSI STATUS REGISTER (hsi_status)

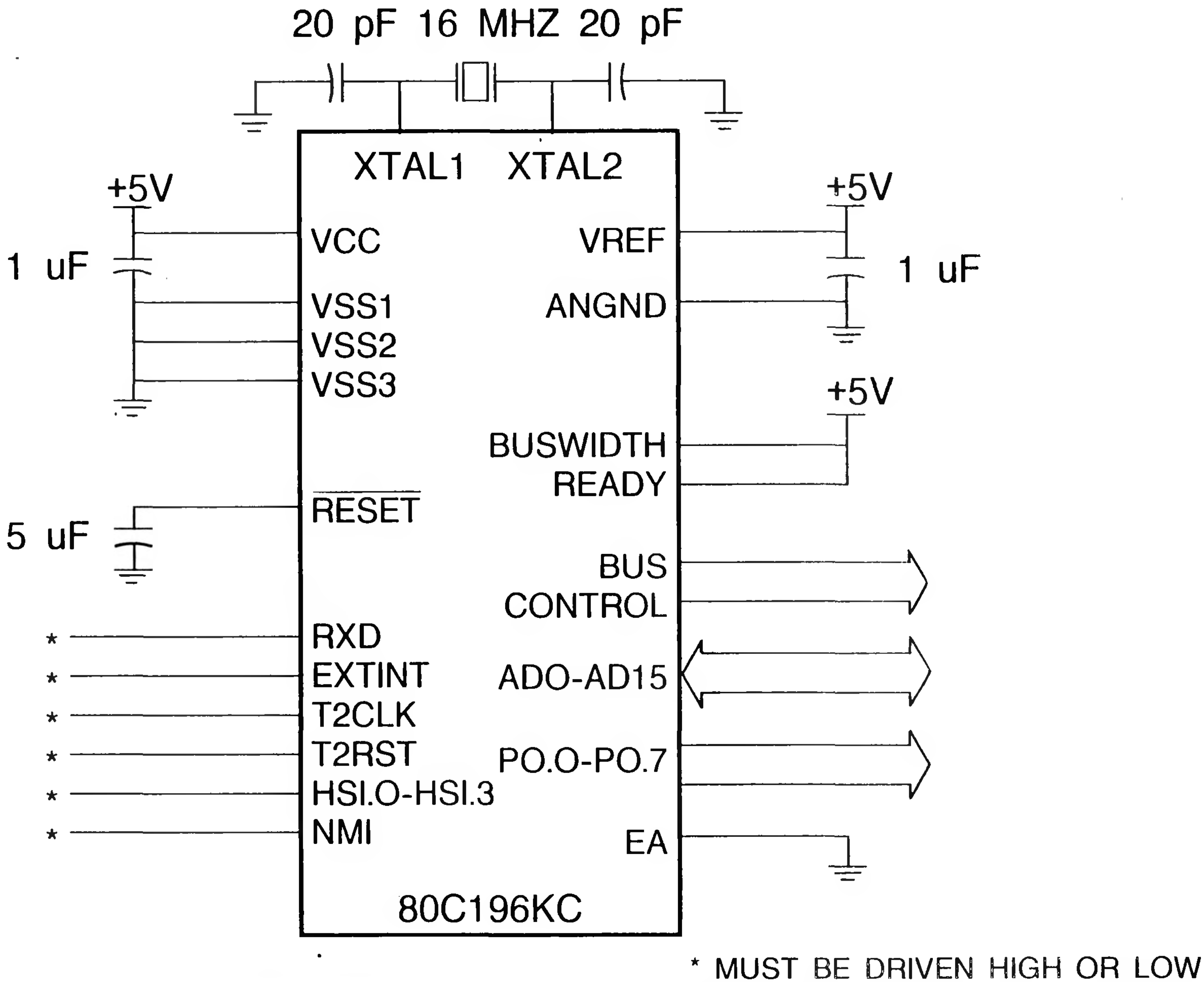


- **LOWER BIT INDICATES OCCURRENCE OF AN EVENT**
- **UPPER BIT INDICATES CURRENT STATUS OF INPUT**

HSI MODE REGISTER 1 (hsi_mode)

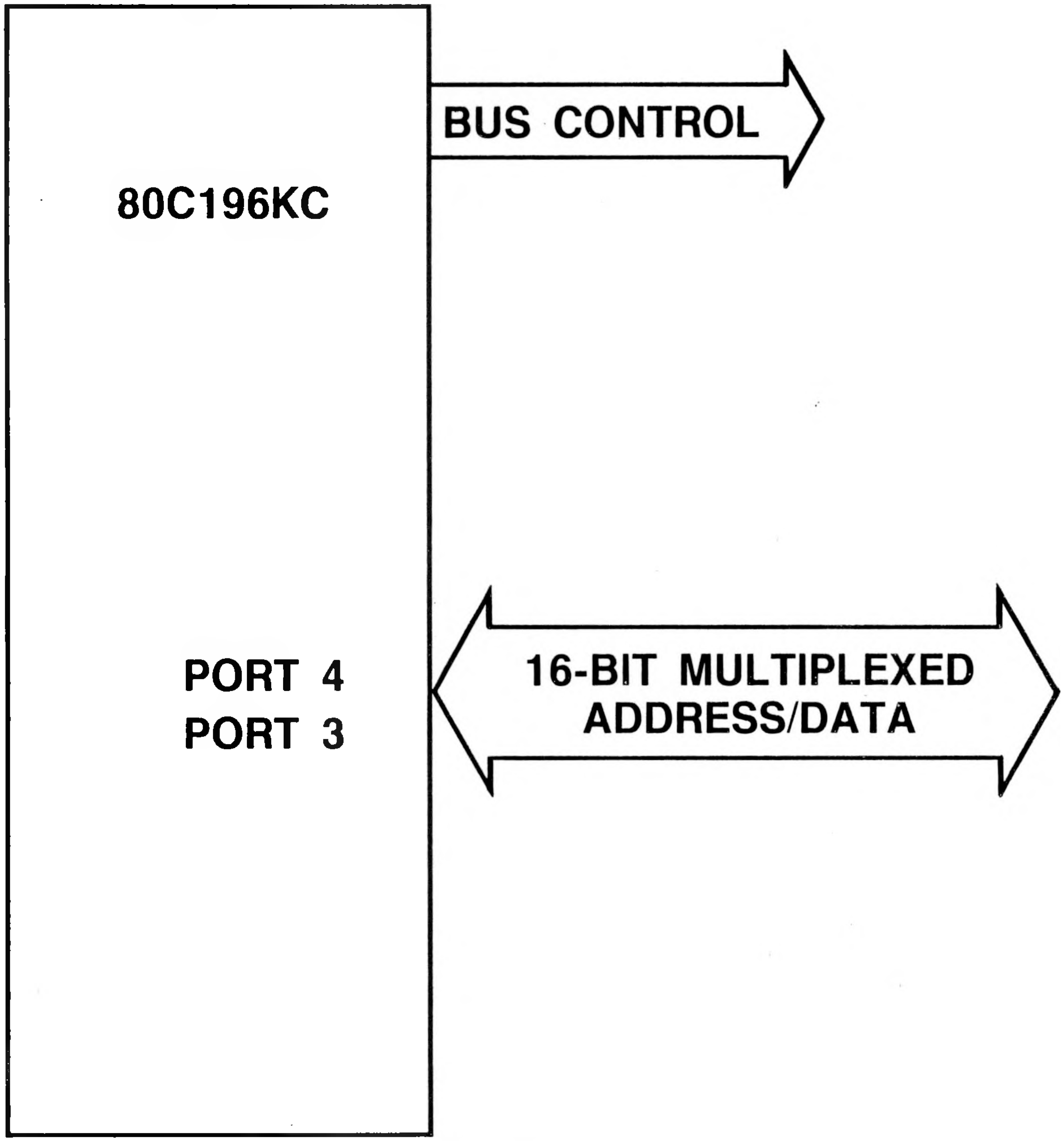


- **00 8 POSITIVE TRANSITIONS**
- **01 EACH POSITIVE TRANSITION**
- **10 EACH NEGATIVE TRANSITION**
- **11 EVERY TRANSITION (POSITIVE AND NEGATIVE)**

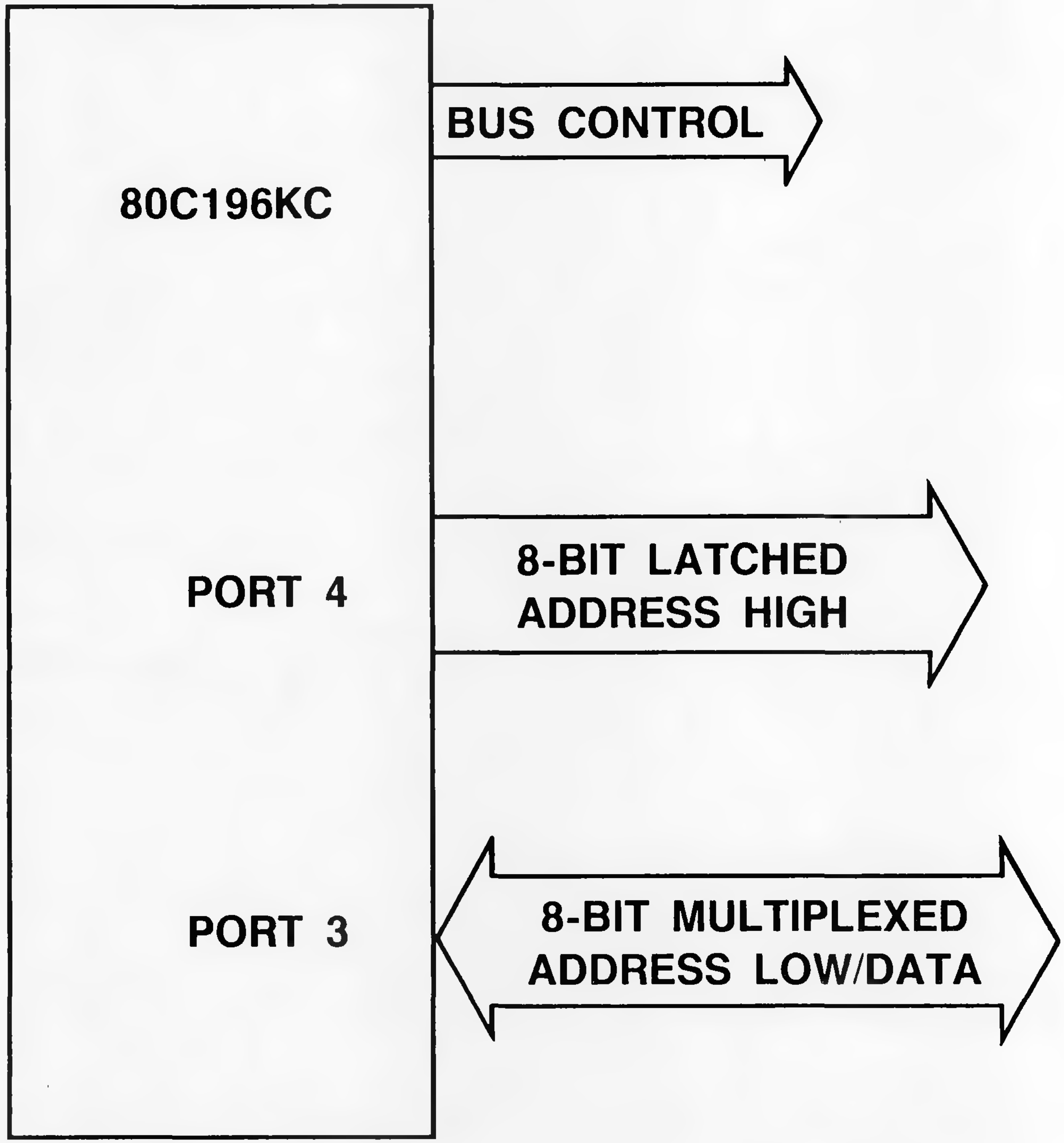


80C196 MINIMUM HARDWARE CONNECTIONS

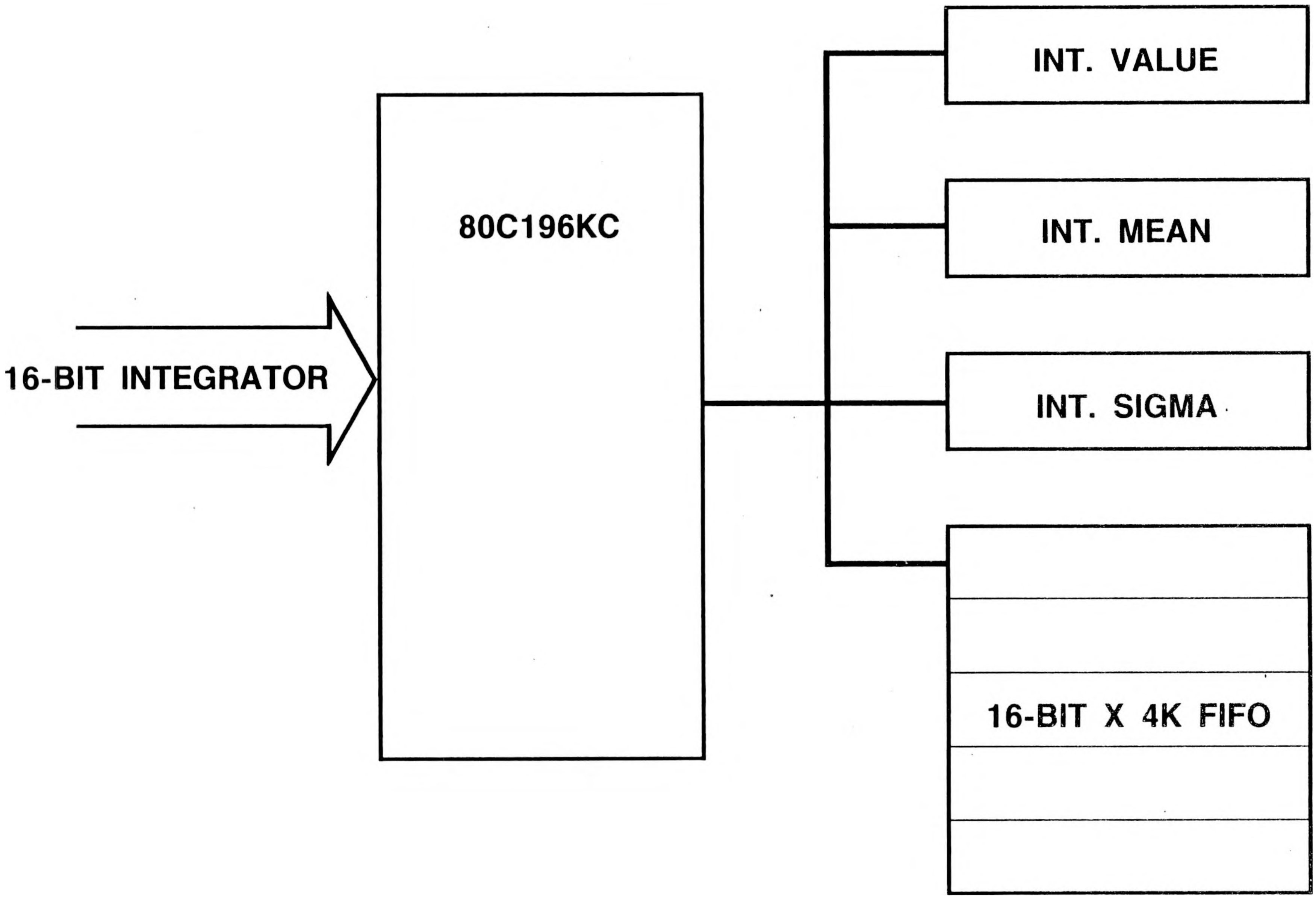
16-BIT BUS


BUS CONTROL
80C196KC
PORT 4
PORT 3
16-BIT MULTIPLEXED
ADDRESS/DATA

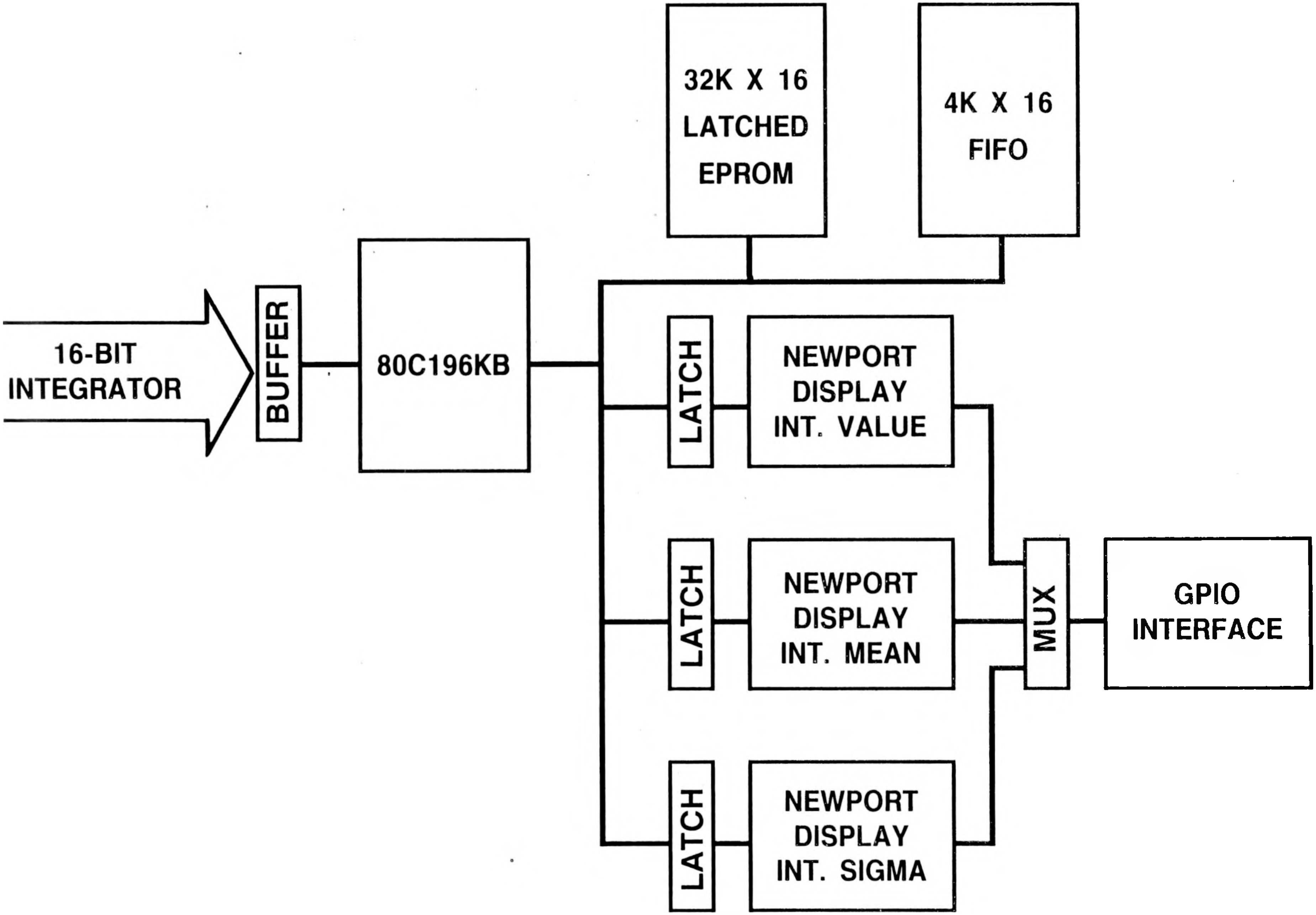
8-BIT BUS


80C196KC
BUS CONTROL
PORT 4
8-BIT LATCHED ADDRESS HIGH
PORT 3
8-BIT MULTIPLEXED ADDRESS LOW/DATA

EMBEDDED INTEGRATOR MONITOR

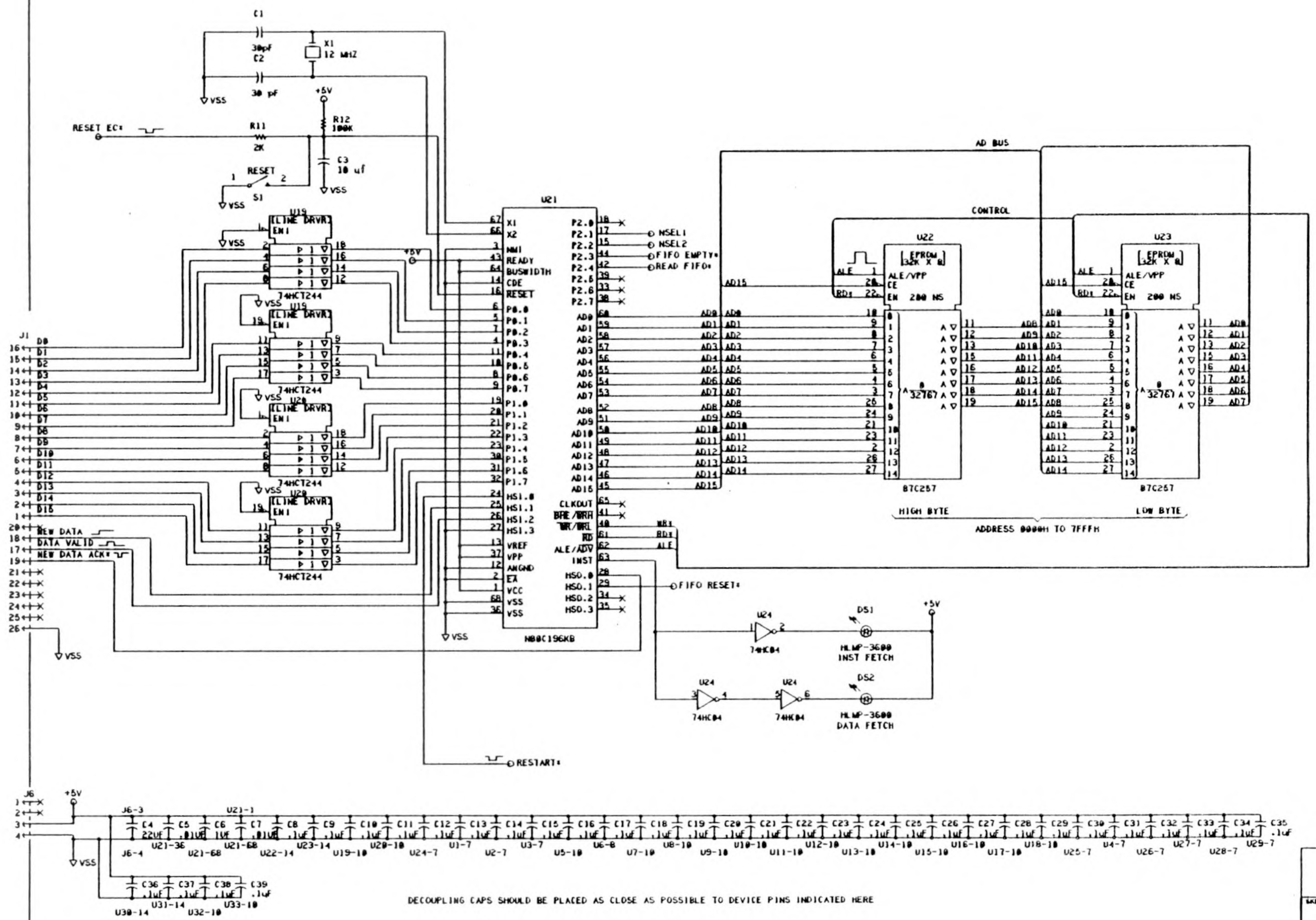


EMBEDDED INTEGRATOR MONITOR



UNCLASSIFIED

EMBEDDED CONTROLLER



PROCESSOR INPUTS AND MEMORY

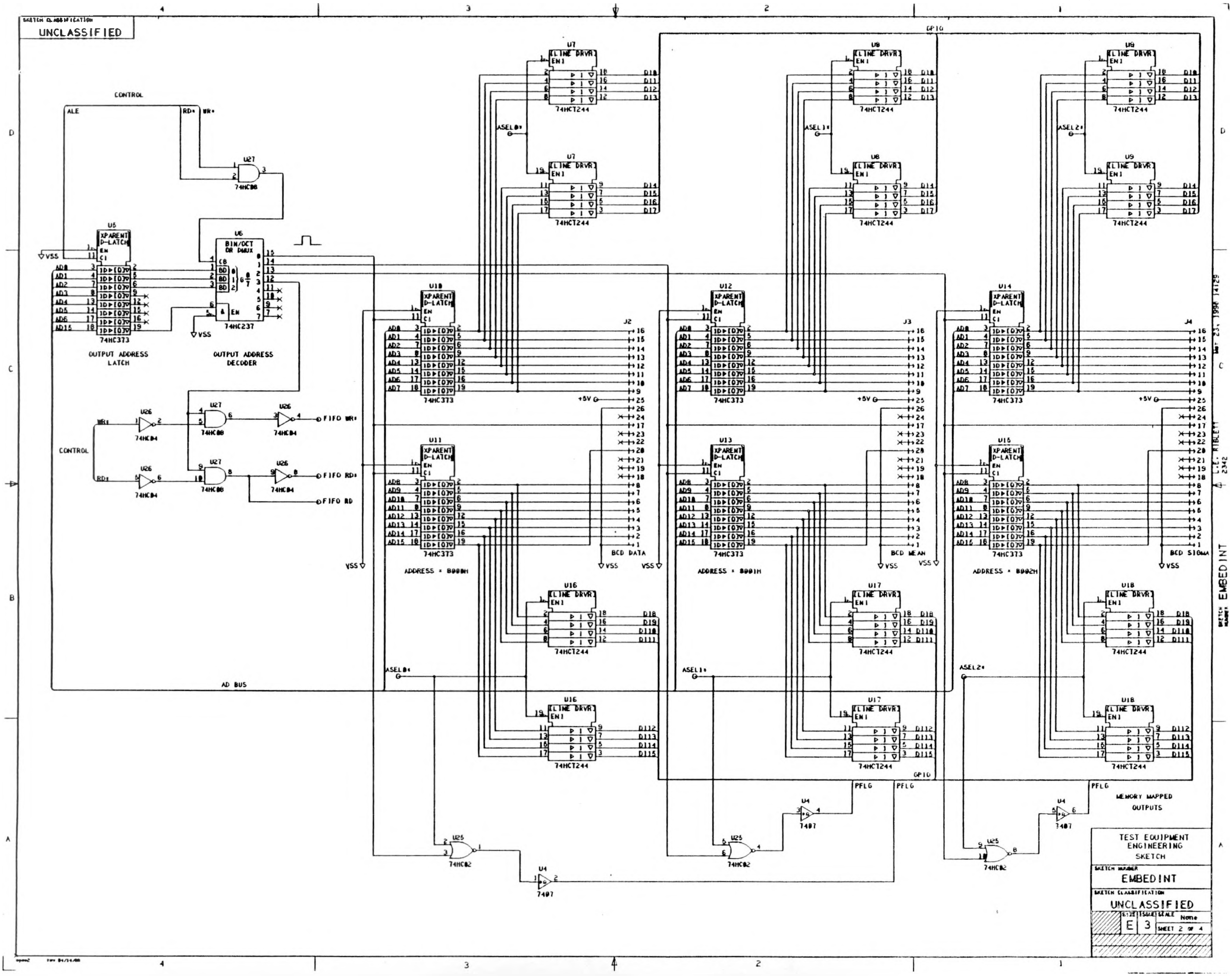
TEST EQUIPMENT ENGINEERING SKETCH

SKETCH NUMBER: EMBEDINT

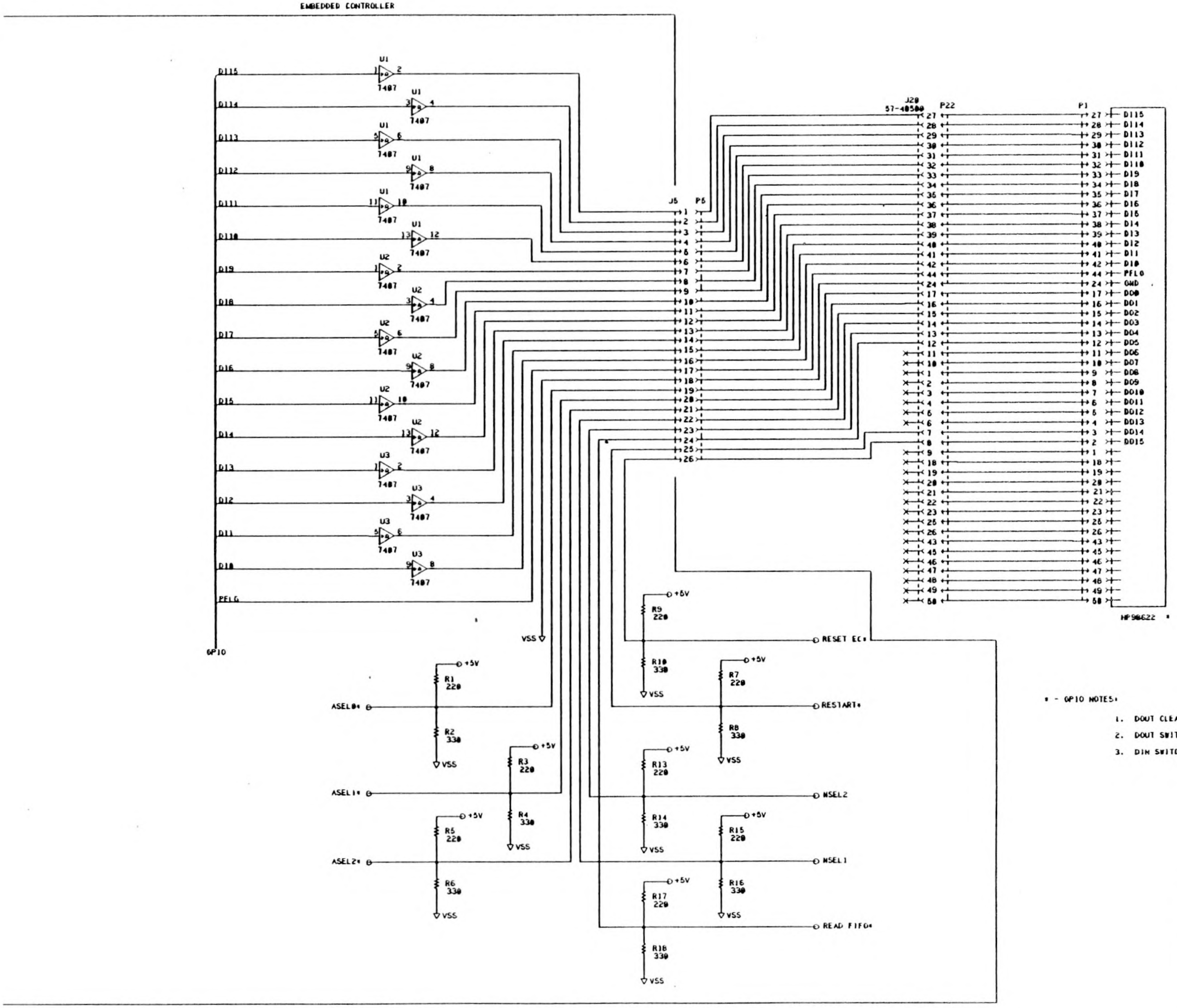
SKETCH CLASSIFICATION: UNCLASSIFIED

SIZE	ISSUE	SCALE
E	3	None

SHEET 1 OF 4


UNCLASSIFIED
CONTROL
ALE
RD*
WR*
U27
74HC08
U5
XPARENT D-LATCH
74HC373
OUTPUT ADDRESS LATCH
U6
BIN/OCT DMUX
74HC237
OUTPUT ADDRESS DECODER
U26
74HC04
FIFO WR*
FIFO RD*
FIFO RD
U7
LINE DRVR
74HCT244
U8
U9
U10
U11
U12
U13
U14
U15
ASEL0*
ASEL1*
ASEL2*
GPIO
J2
J3
J4
+5V
VSS
BCD DATA
BCD MEAN
BCD SIGMA
ADDRESS = 8000H
ADDRESS = 8001H
ADDRESS = 8002H
U16
U17
U18
AD BUS
PFLG
U4
7407
U25
74HC02
MEMORY MAPPED OUTPUTS
L.E. RIBLETT 2342
MAY 23, 1990 14129
SKETCH NUMBER EMBEDINT
TEST EQUIPMENT ENGINEERING SKETCH
SKETCH NUMBER
EMBEDINT
SKETCH CLASSIFICATION
UNCLASSIFIED
SIZE E
ISSUE 3
SCALE None
SHEET 2 OF 4

SKETCH CLASSIFICATION
UNCLASSIFIED



* - GPIO NOTES:

1. DOUT CLEAR JUMPER INSTALLED.
2. DOUT SWITCH OPEN (INVERT OUTPUTS).
3. DIN SWITCH CLOSED (NO INVERSION).

CONTROLLER-TO-GPIO INTERCONNECTIONS

TEST EQUIPMENT ENGINEERING SKETCH

SKETCH NUMBER
EMBEDINT

SKETCH CLASSIFICATION
UNCLASSIFIED

SIZE	ISSUE	SCALE None
E	3	SHEET 3 OF 4

SKETCH NUMBER EMBEDINT

L.E. RIBLETT 2342 MAY 23, 1990 14:53

SKETCH CLASSIFICATION
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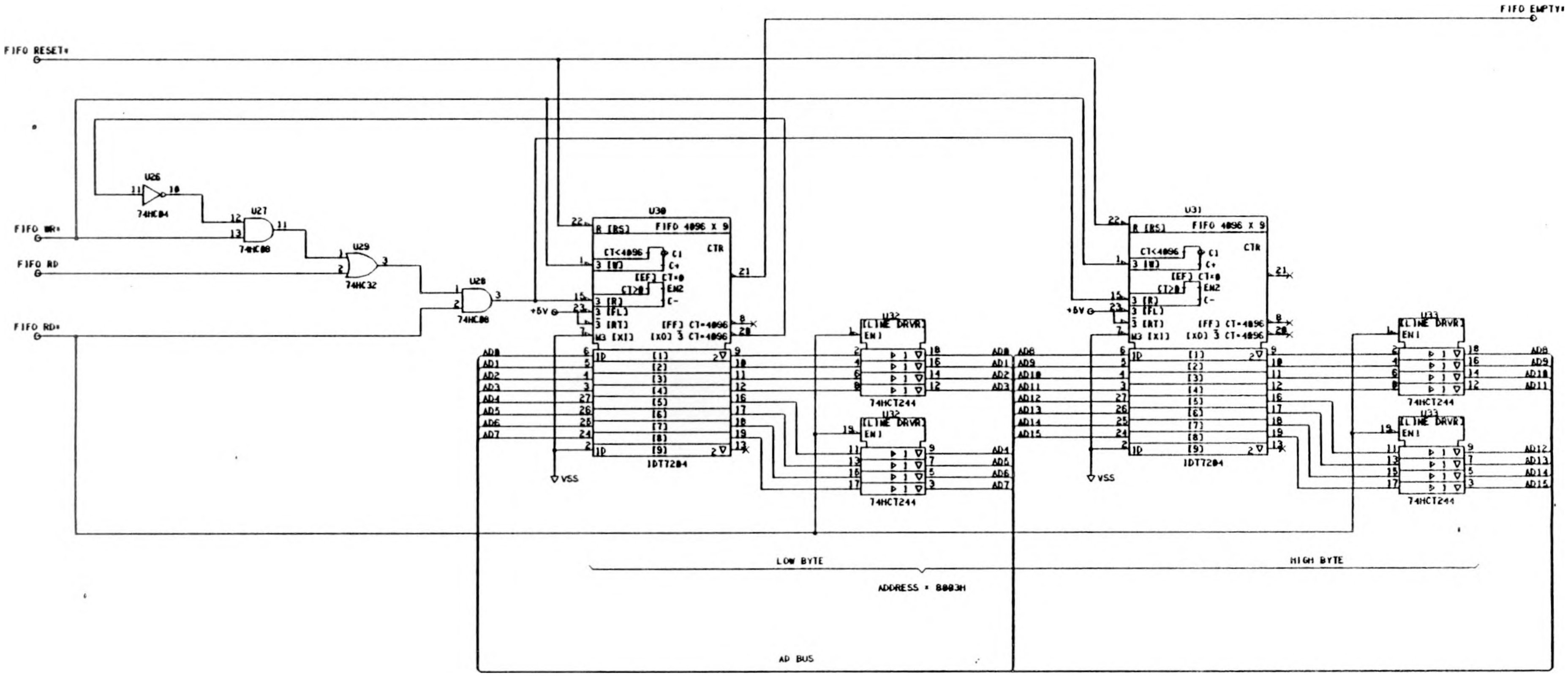


INTEGRATOR DATA
FIFO

TEST EQUIPMENT
ENGINEERING
SKETCH

SKETCH NUMBER
EMBEDINT

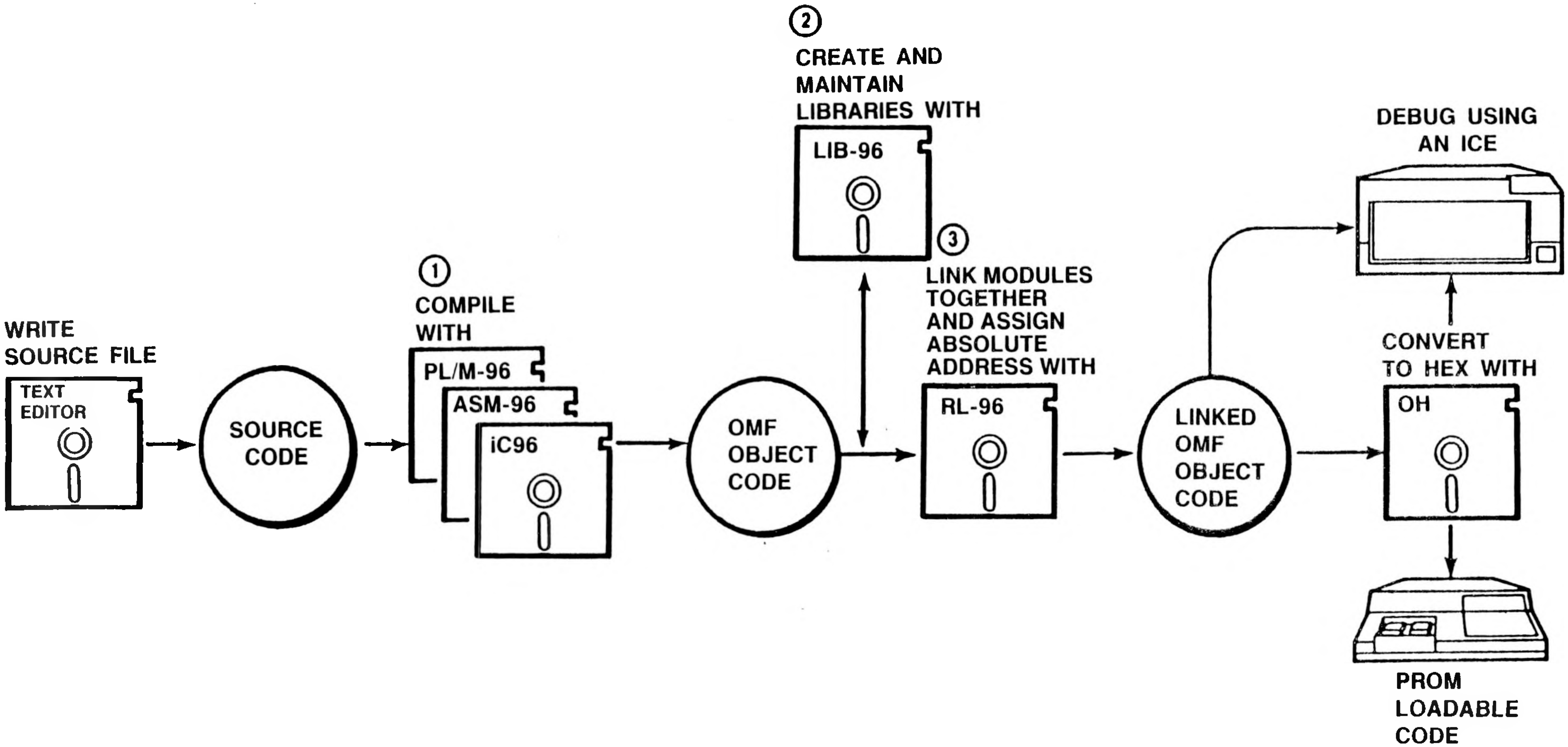
SKETCH CLASSIFICATION
UNCLASSIFIED

SIZE E | ISSUE 3 | SCALE None | SHEET 4 OF 4

SKETCH NUMBER EMBEDINT

L.E. RIBLETT 2342

THE APPLICATION DEVELOPMENT PROCESS



SOFTWARE EXAMPLES

READING I/O PORTS:

```
# define ioport3 (*((char *)0x1ffe))

residual_loop=ioport3;
```

A/D CONVERTER:

```
float sample_voltage(channel)
int channel;
{
float result;
ioc2=0;
ad_command=0x08 + channel;          /* Slow conversion mode */
do{ }while (ad_result_lo & 0x08);        /* Wait till A/D idle */
result=((ad_result_lo & 0xc0)>>6) + (ad_result_hi<<2);
result=result * VREF /1023;
return result;
}
```

SOFTWARE EXAMPLES

WRITING TO HSO's:

```
hso__command=(0x20) | hso;
hso__time=timer1+2;
hso__command=(0x00) | hso;
hso__time=timer1+2;
hso__command=(0x20) | hso;
hso__time=timer1+PULSE__WIDTH;
```

READING HSI's:

```
temp__hsi_status=hsi_status;
temp__hsi_time=hsi_time;
```

SUMMARY

- RECENT ADVANCES IN MICROCONTROLLERS HAVE SIMPLIFIED DESIGN
- INTEL'S 80C196 CONTROLLER AND DEVELOPMENT SYSTEM ARE INEXPENSIVE
- MINIMUM HARDWARE CONFIGURATIONS ARE POSSIBLE WITH THE 80C196
- DETAILED HARDWARE DESIGNS ARE REPLACED WITH SMART, EMBEDDED SOFTWARE
- ACCURACY AND RELIABILITY OF MEASURED PARAMETERS ARE ENHANCED

June 6, 1990

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Rome Air Development Center
RADC/OC TP
Griffis AFB, New York 13441-4381

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Sincerely,

Keithley F. T. Lake
Counsel

KFTL:vp/lla

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cc: ✓Loren E. Riblett
Richard S. Binney, (w/att.)
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