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ABSTRACT

During the course of this quarter, peak cell performance has been improved from 0.455V to 0.510V, from 11.8 to 20.2 mA/cm^2 and from 3.3% to 6.5% as regards open circuit voltage, short circuit current density and conversion efficiency, respectively. Information exchanges and critical reviews of process details have been made with the cooperation of the group at the Institute of Energy Conversion, University of Delaware. As a result of these, two areas were identified which lead to higher cell performance. Substrate temperature control and monitoring during deposition were improved by the use of a thermocouple welded to the foil substrate. Fast, thorough rinsing of the CdS films in the interval between the etch for surface texturing and the immersion in cuprous chloride for barrier formation resulted in a less reflective surfaces, and simultaneously high short circuit current and open circuit voltage performance.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (Cont'd.)

1. SUMMARY

During this quarter, the emphasis has been on identifying and duplicating those details of processing for Cu_2S/CdS solar cells, which appear to be critical for high cell performance. The basic features of that processing, e.g. production of CdS films by evaporation from single sources, specifics of the solutions, times and temperatures of the wet etching and barrier formation steps, and post-fabrication annealing, were being followed at the beginning of the quarter.[1] The best performance, using these procedures, obtained prior to the third quarter was a cell of 3.3% conversion efficiency having V_{oc}, J_{sc} and fill factor values of 0.455V, 11.8 mA/cm^2 and 0.62, respectively. At the end of the present quarter, four cells from two different film depositions had been obtained with conversion efficiency values above 6%. The best had V_{oc}, J_{sc} and fill factor values of 0.510V, 20.2 mA/cm^2 and 0.65, respectively.

The improvement in cell performance was due to several factors. Changes in several details of the evaporation process resulted in better electrical contact to the substrate foil and a more uniform distribution in size of the CdS grams. Cell results controlled by the wet processing steps (etching of the CdS film and Cu_2S formation by the wet dip method) appear to be critically dependent on rapid, thorough rinsing of the cell surface. Identification of the details which are important in the process steps was accomplished by meetings between Westinghouse and IEC workers, at which the processing practices were reviewed and critiqued. Two such meetings were held, one at the beginning and the other near the end of the quarter.

During the course of the reported work, 40 CdS film depositions were made, 13 being under standard conditions incorporating the critical features and using substrate and source temperature schedules which were

identified at the first Westinghouse/IEC meeting. Most of the remaining runs involved deliberate departures from standard conditions to test for influences on film structure or quality and on cell performance. From 18 of the CdS films, about 50 cells were fabricated, under standard conditions, and evaluated during extensive annealing. A somewhat smaller number of cells was prepared and evaluated using non-standard conditions for the purpose of elucidating sensitivity to variables in post-deposition processes.

As a result of intensive scrutiny given to the processing details, careful implementation of key procedures, and detailed tracking of performance results obtained on many cells, significant improvement in cell performance has been obtained over this quarter. In particular, because certain sensitive aspects of film deposition and of wet processing have been identified, there is good reason to expect continued performance gains in the fourth quarter as tighter controls are imposed in these matters.

2. PROGRAM DESCRIPTION

2.1 Objective

The objective of this program is to produce copper sulfide/cadmium sulfide solar cells with conversion efficiency of 9% or greater. Specifically, effort is to be applied to duplicate the basic elements of the cell fabrication sequence used at the Institute of Energy Conversion (IEC) of the University of Delaware.[1] This will demonstrate the transferability of process steps which have resulted in 1 cm^2 cells of 9.15% efficiency at IEC.

2.2 Approach and Program Tasks

An analysis was made of the differences between IEC and Westinghouse cell fabrication details prior to the start of this program. On the basis of that review, the known differences were judged to have first and second order influences on cell performance. Matters considered of most importance were (1) the CdS film deposition methods and its effect on grain size and the barrier interface topology, (2) barrier formation and heat treatment details, and (3) electrode grid contact preparation. These considerations, along with assessment of the role played by optical reflection of the back contact and consequences of spectral content of illumination, constitute Task 1 of the present program.

In the improvement of cell performance beyond 9%, a major unknown is the role played by the free surface and the grain boundary regions of the polycrystalline material. This includes matters such as the formation of the Cu_2S absorbing layer, the minority carrier transport properties within the layer, surface or grain boundary recombination mechanisms, and the electronic nature of the space charge region in the CdS adjoining the heterojunction. Empirical and modelling efforts addressing these matters constitute Task 2.

2.3 Review of First Half Program Progress

During the first quarter, the preparation of CdS films by evaporation from a single graphite source was implemented.[2] Previously at Westinghouse, four evaporation sources were used to permit uniform coverage of large area substrates. The graphite source used in the first half was somewhat smaller than the IEC design to permit accommodation to the source heater which was available. Initial efforts with the single source evaporation focussed on characterizing the thickness profiles of the deposited films, in order to permit selection of tions for obtaining films suitable for cell fabrication.

During the second quarter of the program the CdS films produced by the single graphite source were shown to be different in structural detail from four-source films, consistent with having greater structural perfection.[3] The best cells produced on single source films by the barrier processing methods used by IEC[1] gave cells of 3.0 to 3.3% conversion efficiency. These cells were lower in open circuit voltage, fill factor and short circuit current than cells usually produced by IEC. The films prepared near the end of the second quarter often exhibited a bi-modal distribution of grain sizes, that is, about half the surface area was covered by grains of 1 to 2 μm size, with the remaining area composed of sub-micron grains.

3. PROGRESS TO DATE

At the beginning of the third quarter of the program an assessment was made of the degree to which CdS film preparation, barrier processing, gridding, and heat treatment at Westinghouse duplicated the essential features used by IEC. Most of the emphasis involved aspects of deposition of the CdS films. Implementation of several key changes resulted in suppression of the bimodal grain size distribution observed in earlier single source films. The best cells fabricated on that material had somewhat lower values of short circuit current than did control cells fabricated on material provided by IEC. About three quarters of the films produced cells with short circuit current density values below 10 mA/cm^2.

A number of variations in the etch and barrier dip steps were tried to improve short circuit current performance, but the results were not dramatic. Early in April a visit was made to the laboratories at IEC to compare details of etching, barrier processing, annealing and cell testing. Several subtle features of wet processing at IEC were identified. When these were incorporated with barrier annealing in pure hydrogen, significant improvements in cell performance were obtained, leading to cells with conversion efficiency values of 7% or higher.

3.1 Identification of Critical Cell Processing Steps

A meeting was held in January 1980 involving representatives from Westinghouse, the Solar Energy Research Institute and the Institute of Energy Conversion. Its purpose was to compare the details of Westinghouse and IEC practice for producing cells from which 9% conversion efficiency could be expected. Westinghouse procedures for post-deposition processing were derived from Ref. 1 and from earlier private communications with workers at IEC.

In the steps following CdS film deposition only one major change from the procedures of Ref. 1 was identified as being desirable. That was to use a more dilute HCℓ etch (1:3 HCℓ in water [vol/vol]) for a longer time (10 to 40 sec) prior to barrier formation. Previously a stronger solution (55:45) had been used for a very short ($\sim$ 2 sec) etch at 60°C. The milder etch for a longer time was proposed as permitting better control during this step.

Also proposed as a convenience was the use of a silk-screenable thermoplastic adhesive resin TPA-85* to provide an insulator under the grid electrode contact bars instead of the Fortin adhesive film used previously. The TPA-85 material is applied prior to etching and barrier dipping and acts as a chemical resist mask to define the active area of the cell.

A number of differences were noted between IEC and Westinghouse practice regarding copper foil substrate preparation and details of the CdS deposition. In order to duplicate the IEC procedures which earlier resulted in 9% cells, the following changes were undertaken at Westinghouse:

a. Eliminate HNO_3 etching of the copper foil substrate to prevent spurious texturing. Use H_2SO_4 for etching and storing of the substrates prior to deposition.

b. Permit no heating of the CdS source or of the substrate until the deposition chamber pressure is less than 10^{-5} T.

c. Deposit the CdS at a pressure of 10^{-5} T or better. Do no glow discharge cleaning of the substrate prior to CdS deposition, to eliminate the possibility of oxidation. Use a thermocouple welded to the back of the foil substrate for substrate temperature monitoring and control.

In most other respects, other details of substrate preparation and CdS

*Available from American Liquid Crystal Chemical Corp., 501 Gougler Avenue Kent, OH 44240.

deposition procedures in use at both laboratories were judged to be sufficiently similar or of minor consequence in affecting CdS film properties relevant to cell performance.

Changes were made in CdS deposition and cell processing to address the major points just discussed. The impacts of these changes on film characteristics and cell performance are discussed in Sections 3.2 and 3.3. Although cell performance improved as a result of these efforts, cells produced on samples of CdS films supplied by IEC were significantly poorer in performance than expected on the basis of earlier IEC results on the same films.

The parameters of the etch and barrier formation steps were varied to determine if new optimum conditions prevailed. Such was not the case. This led to the hypothesis that some subtle, but critical, aspects of the IEC procedures were being overlooked. In early April, 1980 a visit was made to the IEC facilities to observe cell processing on substrates produced at IEC and at Westinghouse.

An important part of the interaction with IEC in April involved co-processing of CdS films from Westinghouse and IEC by IEC personnel. This afforded the opportunity to observe minute details, including operator movements which are not generally treated as a part of process step specification. Eight of the cells fabricated in this exercise were split into two groups: one for annealing and testing by Westinghouse; the other, by IEC. Each group contained two cells on IEC material and two on Westinghouse material. Data on peak efficiency and short-circuit current density (for 100 mW/cm^2 illumination) are given in Table 1. These results established that the CdS material prepared at Westinghouse was capable of making 7% cells with short circuit current density values (for 100 mW/cm^2 illumination) comparable to those obtained at IEC. Furthermore, the annealing results established that the annealing capabilities at Westinghouse were equivalent to those at IEC.

Table 1. Comparison of Westinghouse and IEC CdS Films and Annealing Procedures on Cells Produced Simultaneously at IEC

CdS Film	Annealed and Tested at Westinghouse	Annealed and Tested at IEC
Westinghouse #681	7.25%, 20.41 mA/cm^2	7.40%, 21.51 mA/cm^2
	7.10%, 20.10 mA/cm^2	6.59%, 21.67 mA/cm^2
IEC #2-1115	8.39%, 20.41 mA/cm^2	5.78%, 18.14 mA/cm^2
	8.42%, 20.03 mA/cm^2	6.74%, 18.14 mA/cm^2

Of all the process details which were scrutinized during that visit, two were considered by the Westinghouse group to be significantly different from Westinghouse practice: (1) the use of apparatus more effective at excluding air by maintaining an argon cover gas over the cuprous chloride bath; (2) more rapid withdrawal of the workpieces from the etch and the dip solutions, with a flicking motion used to remove the liquids retained on the surface. Both factors could influence the formation and properties of the Cu_2S absorbing layer and of the heterojunction with the CdS substrate. After these changes were instituted at Westinghouse, considerable improvement in cell performance was noted, as discussed in Section 3.3.1.

Two additional changes were made to conform to current IEC practice: (1) the use of a commercial laboratory detergent to clean CdS pieces before application of the TPA-85 epoxy masking material and before etching in HCℓ; (2) the use of pure hydrogen for the annealing heat treatments, rather than H_2/Ar mixtures. These were not considered crucial to cell performance, since good quality cells had been made earlier without such cleaning and using dilute H_2 mixtures. Definitive experiments to assess the quantitative effects of the wet processing step changes have not yet been done. These will require a careful statistical treatment or the use of CdS film material known to be capable of producing cells with very tight distributions of performance parameter values.

3.2 Improvements in Substrate Preparation and Cds Deposition

3.2.1 Substrate Cleaning

During this period changes were made in the substrate cleaning process to bring Westinghouse practice into closer conformity with that of the University of Delaware. Previously, the copper foil was cut to size, suspended in a copper wire frame using tungsten wire spring hooks and cathodically degreased. After rinsing in flowing deionized water, the copper foil was etched in 1:3 HNO_3 solution at 45°C for about 6 seconds and then thoroughly rinsed in flowing deionized water, and then immediately zinc plated. This cleaning procedure usually yielded very uniform zinc platings with little or no indications of streaks or splotchy areas.

In trying to switch over to the University of Delaware process, some difficulties were encountered with visual inhomogeneities in the zinc plating of the substrates characterized as stained, streaky or splotchy areas that would affect the CdS film deposition. Since the University of Delaware workers did not encounter such difficulties, it was reasoned that there must be significant differences either in the substrate material being used, or in the equipment facilities at Westinghouse.

Initially, it was thought that these differences might be chiefly in the copper foil, since the substrates used by Delaware had no stain-proofing and were heavily oxidized, whereas those used at Westinghouse were lightly stain-proofed (i.e. had a proprietary chromate-type coating to inhibit corrosion) and were free from oxidation. It was presumed that the stain-proofing coating was not being completely removed by anodic degreasing and H_2SO_4 acid soaking, hence the substrates were given a dilute HCℓ acid solution soak prior to anodic degreasing. This helped, but did not completely cure the difficulty.

The difficulties were effectively alleviated when the substrates were processed without using the wire frame mounting holders for the anodic degreasing steps and when the anodic degreasing was

carried out at a reduced current. Such operation requires more handling of the substrate and increases the risk of contamination of the substrate. However, the absence of the wire frame holder in the anodic degreasing step appears to eliminate most of the streaking and splotchiness of the substrate during subsequent zinc plating. The use of decreased current in anodic degreasing has eliminated the tendency for "burning" of the substrate in this step.

3.2.2 CdS Film Deposition

At the beginning of this quarter a new graphite evaporation source, purchased from IEC, was put into use. No substantial difference in the grain size or structure of deposited CdS films could be attributed to this source, in comparison to the graphite source of Westinghouse design, which was used previously. Additionally, no direct effect on cell performance was noted when in-situ glow discharge cleaning of the foil substrates was eliminated prior to CdS deposition.

The use of a thermocouple welded to the copper foil substrate for monitoring and controlling its temperature had a significant impact on results of the deposition. Previously, a mechanically contacted thermocouple applied to the back of the substrate, was used for controlling power to a radiant heater positioned above the substrate. Several experiments were made using two thermocouples, one welded to and the other mechanically contacting the back of the foil substrate. Data, taken simultaneously from both sensors, showed that the mechanically contacted unit read higher than the welded one by 60° to 100°C. This difference is attributed to a high thermal contact resistance between the mechanically mounted couple and the substrate which makes that couple more responsive to radiant heating. Such an effect would result in control of the substrate heater power to produce a lower temperature in the substrate foil than indicated by the thermocouple.

The conclusion drawn from comparing results of the two methods of thermocouple attachment was substantiated when a welded

thermocouple was used for substrate temperature control during actual CdS film depositions. In the first such use of the welded thermocouple, an indicated substrate temperature of 182°C was maintained at approximately the same substrate heater power previously used for 220°C depositions with the mechanically contacted couples. The smallest grains in the resulting film were larger (Fig. 1a) than in the case with a mechanically contacted couple reading 220°C (Fig. 1b).

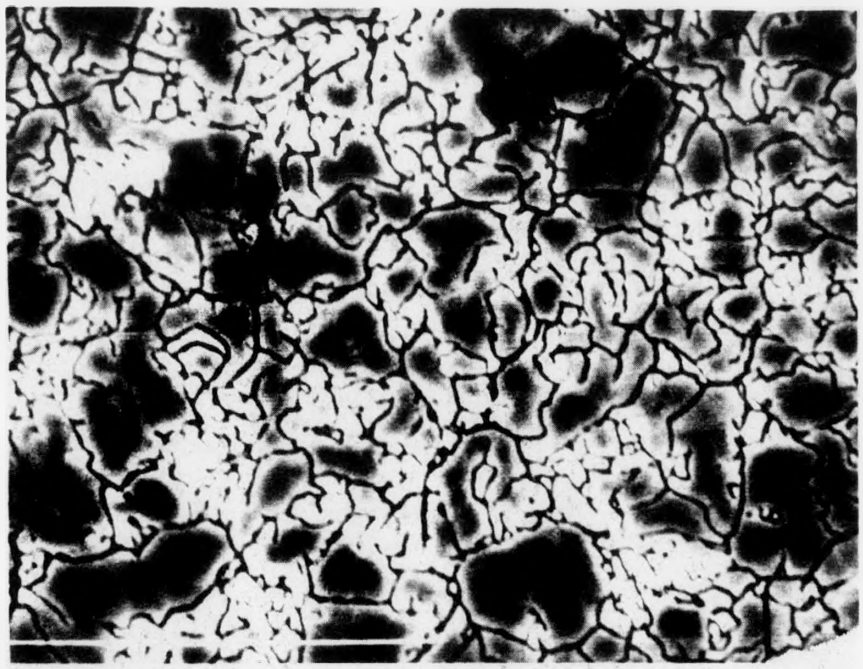
Typically depositions made with a welded thermocouple reading 220°C, resulted in the larger grains and more uniform size distribution of Figs. 2a and b. In depositions for which deliberately higher substrate temperatures (240°C) were called for by the welded couple, the CdS grains were slightly larger, as shown in Figs. 3a and b.

During this quarter, 29 depositions of CdS films were made. Of these, 13 were made under standard conditions. A number of non-standard depositions were made at higher substrate temperatures or with modified evaporation tooling. Results on the performance of cells from 18 of these films are presented in the following section. The remaining films were not completely characterized to the point of permitting selection for cell fabrication.

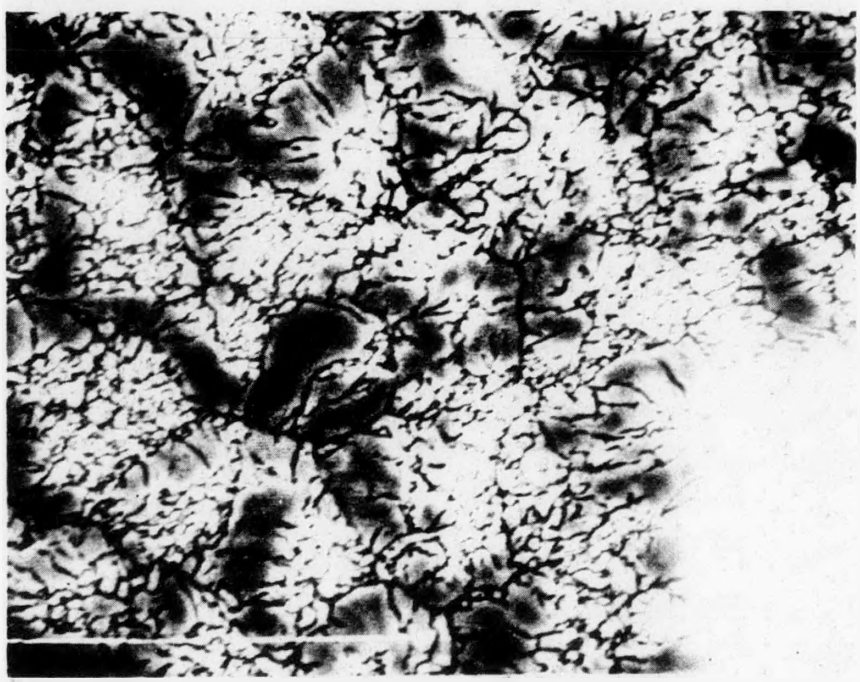
3.3 Cell Fabrication Results

3.3.1 Overview

Approximately 35 to 40 cells per month were fabricated, using modifications (described in Section 3.1) of the processing (Type D) described in Ref. 2, page 11, and evaluated during the third quarter of the contract. During this period emphasis was put on assessing the influences on cell behavior of the changes introduced in the CdS deposition step (Section 3.2). Of particular interest were effects on cell performance of changes in grain size and distribution related to monitoring and controlling substrate temperature with welded thermocouples. As discussed in Section 3.2.2, use of the welded couples to control at a fixed temperature (e.g. 220°C used for

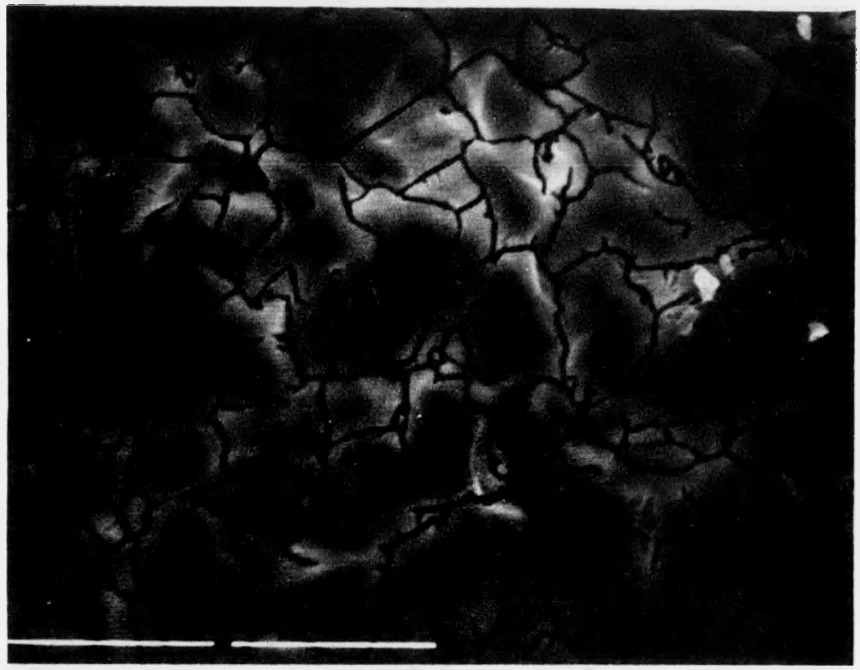


(a)

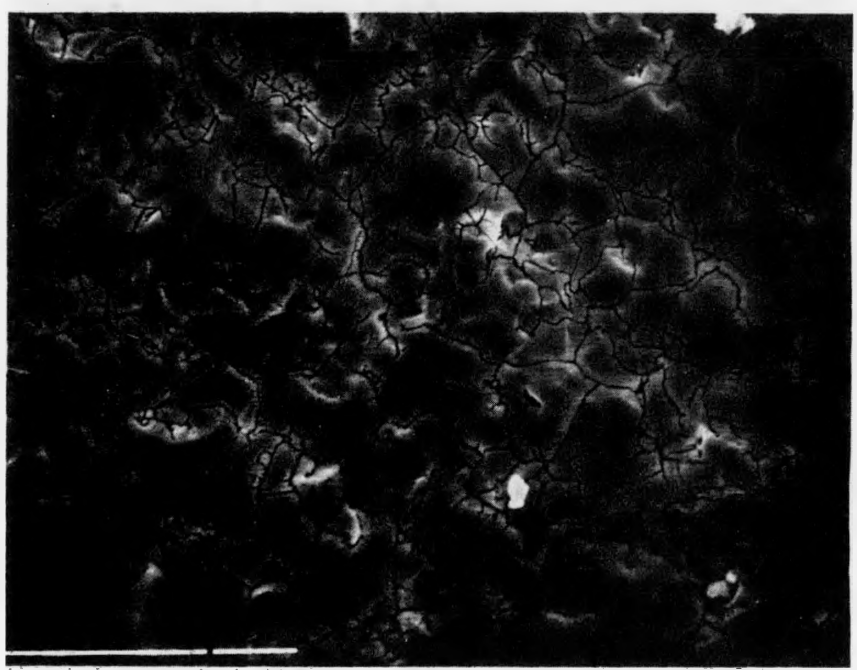


(b)

Fig. 1. Examples of grain size differences (revealed by Cu_2S decoration and removal) in CdS films deposited at (a) 182°C as indicated by a welded thermocouple (Film #664) and at (b) 220°C as indicated by a mechanically contacted thermocouple (Film # 663).

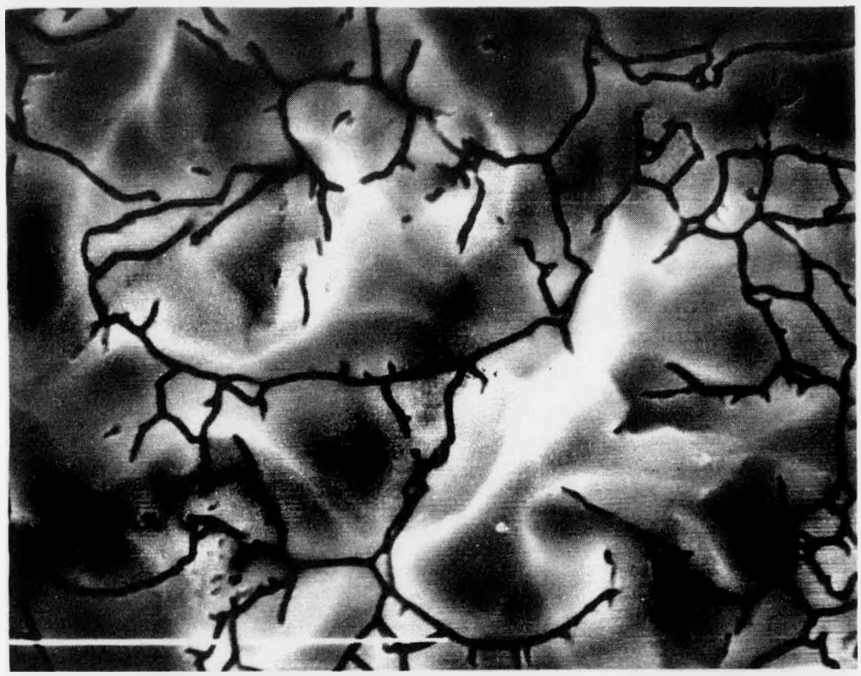


(a)

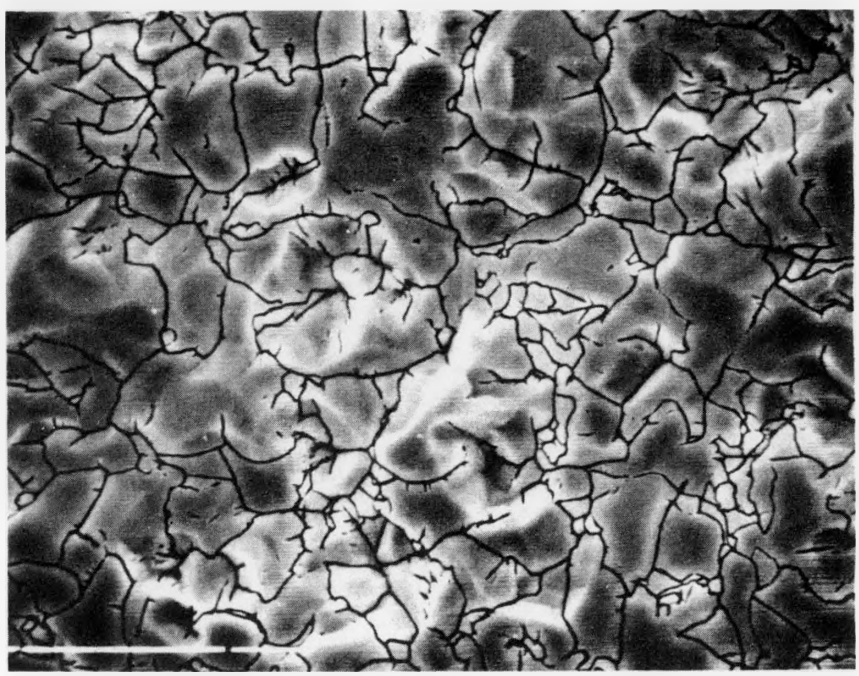


(b)

Fig. 2. Large grains (a) and uniform grain size distribution (b) in a typical CdS film (#667) prepared at 220°C substrate temperature indicated by a thermocouple welded to the back (heated) foil surface.



(a)



(b)

Fig. 3. Example of increased grain size in a CdS film (#676) deposited at 240°C, as read on a thermocouple welded to the back surface of the substrate. (a) High magnification view of typical area. (b) Lower magnification view to illustrate grain size distribution.

standard depositions) resulted in higher actual substrate temperatures than when mechanically contacted couples were used, indicating the same temperature. In addition, during this quarter two-thirds of the CdS films used for cell fabrication had been prepared by evaporation using unsintered charges of CdS, based on the desire to follow IEC practice. The remaining films used for cells had been prepared using pre-sintered CdS powder, according to earlier Westinghouse practice (see Ref. 3, page 9). In all cases, the gridded cells were annealed under a flowing atmosphere of hydrogen and argon (both 6 and 10% mixtures were used) at temperatures of 130 to 170°C.

Figures 4, 5 and 6 give short circuit current density,* open circuit voltage+, and fill factor data for cells from 19 different CdS film depositions. Consideration of the possible effects of CdS deposition conditions variables on cell performance leads to the following observations:

(1) The best cells with highest J_{sc} and V_{oc} values were made on films (671 and 681) prepared a month apart in time using pre-sintered CdS source material under similar conditions of substrate temperature (Table 2 gives typical cell results).

(2) Cells produced on films from intervening deposition runs had much lower values of J_{sc} with only moderate values of V_{oc} (ranging from 400 to 450 mV). The factor common to these cells was their fabrication from films produced from unsintered CdS source material.

(3) The use of higher substrate temperatures (240°C vs. 220°C in standard runs) in Runs 676 through 680, although it produced larger CdS grains in the deposited films, did not improve open circuit voltage.

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* Projected for 100 mW/cm^2 ELH illumination

+ As measured for 90 mW/cm^2 ELH illumination.

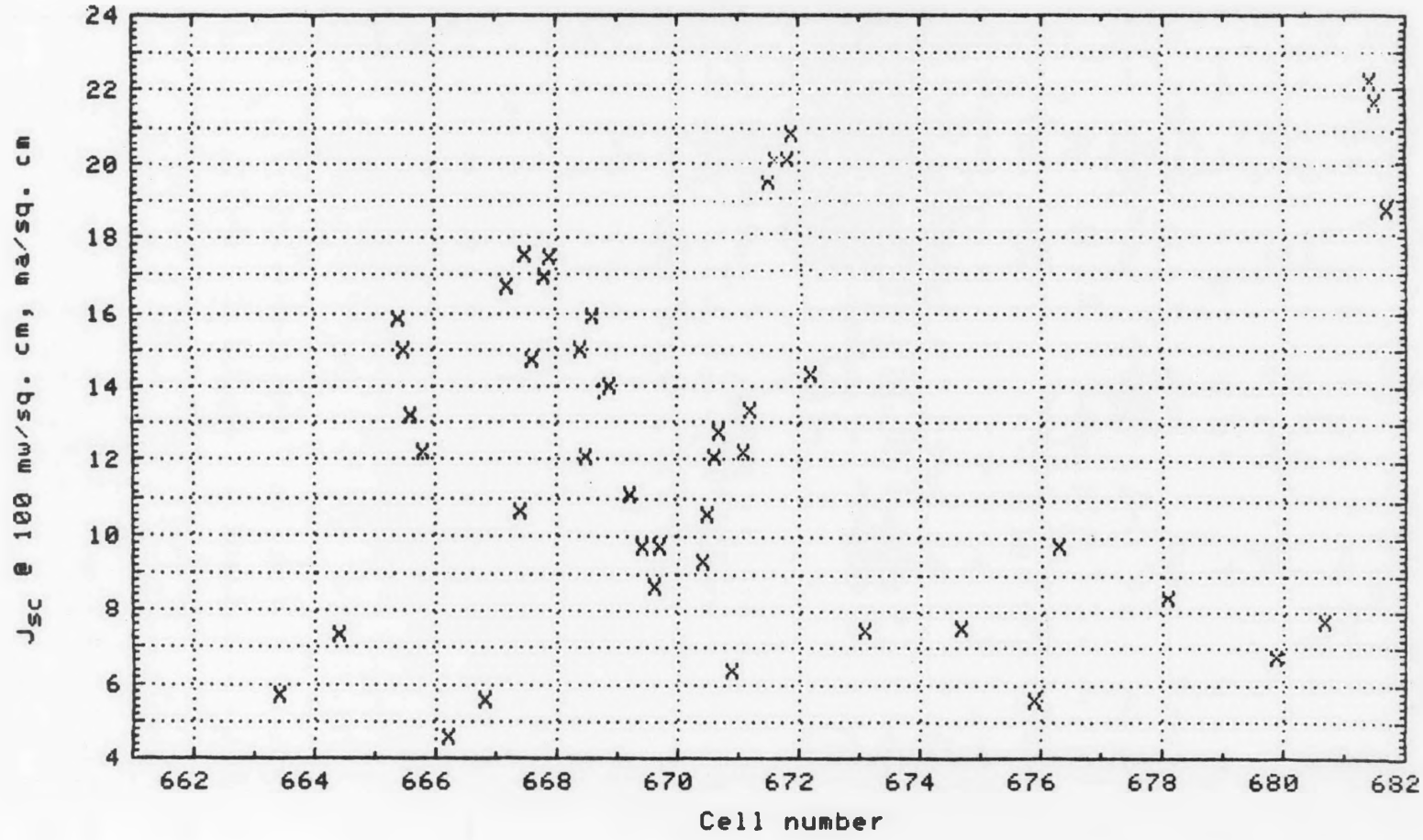

Fig. 4. Short circuit current density (projected for 100 mW/cm^2, ELH illumination) performance of solar cells produced by standard processing during the third quarter of this program.

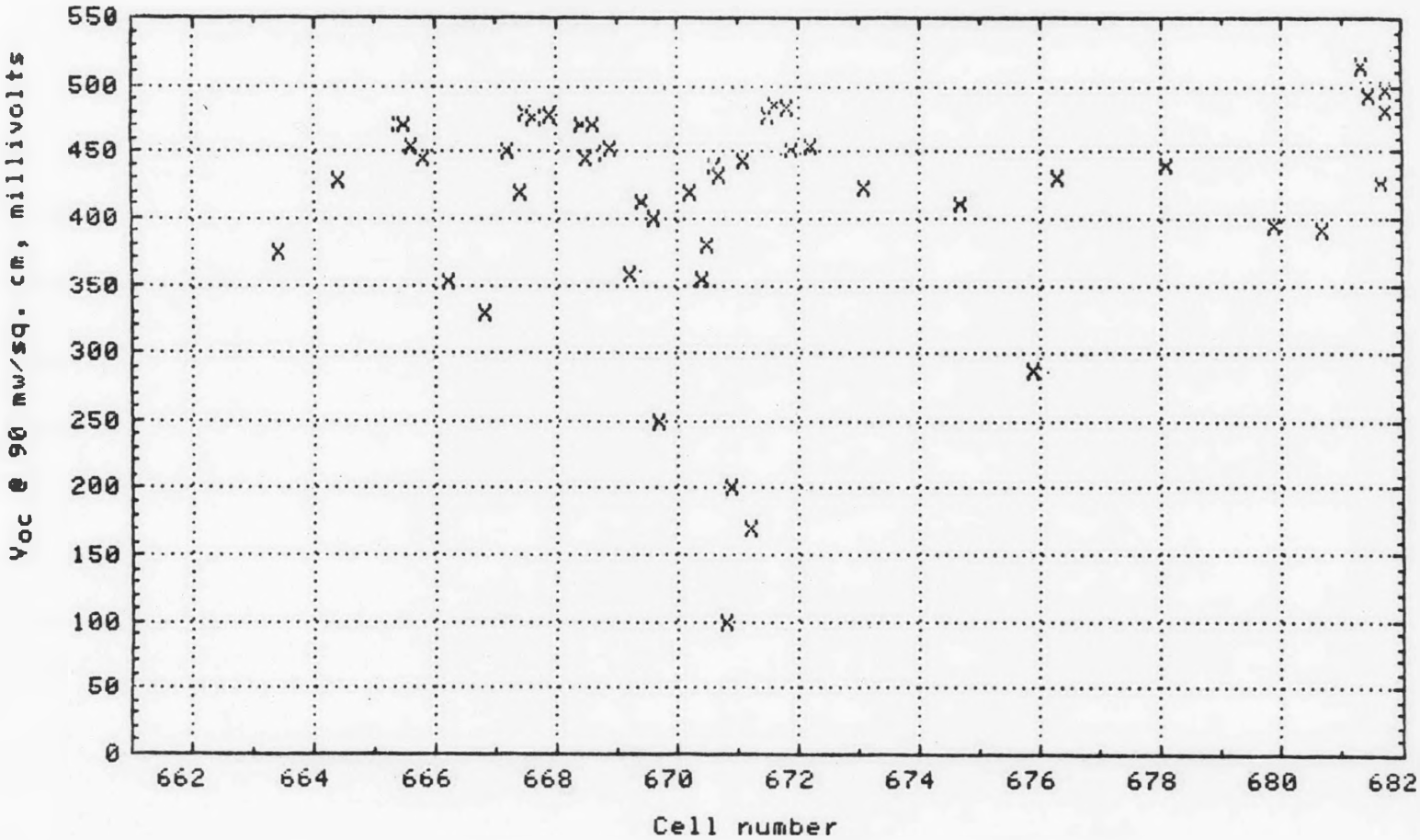

Fig. 5. Open circuit voltage (for 90 mW/cm^2, ELH illumination) performance of standard process solar cells during the third quarter of the program.

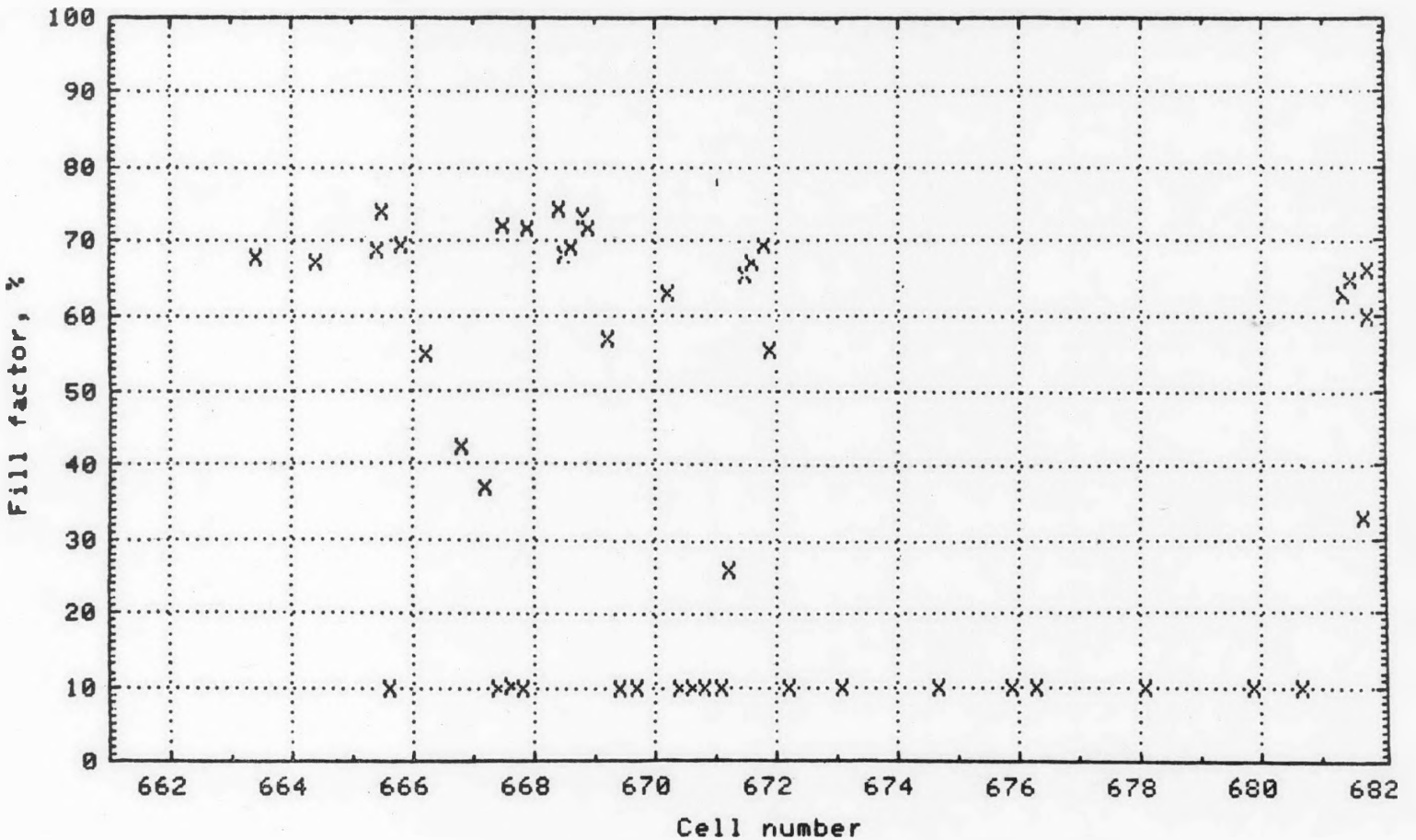

Fig. 6. Fill factor results for standard process cells during the third quarter of the program. Points at 10% signify cells for which fill factor values were not calculated.

Table 2. Typical Parameters for 90 mW/cm^2 ELH Illumination of 1 cm^2 Cells from the Two Highest Performing Cell Lots

Cell No.	V_{oc} (v)	J_{sc} (mA/cm^2)	ff	η (%)
671-5	0.480	17.50	0.66	5.61
-6	0.486	18.13	0.67	6.00
-8	0.485	18.13	0.69	6.16
-9	0.455	18.75	0.55	4.90
681-5	0.510	20.20	0.63	6.53
-6	0.490	19.50	0.65	6.39
-8	0.426	16.83	0.33	2.60

3.3.2 Effects of Wet Processing Steps

During the quarter, except for the cases of films #671 and 681 which gave cells of good performance as noted in Section 3.3.1, the other films yielded cells with short circuit current density and open circuit voltage values consistently lower than expected. At the time, attention was not given to the possible influence of sintering the CdS charge. The emphasis of the deposition effort was to use unsintered material, duplicating the practice at IEC. A number of studies were taken to determine the degree to which etching and barrier processing conditions were controlling photovoltaic performance.

An initial effort established that the Westinghouse CdS films and barriers were topologically similar to the IEC ones when standard wet processing was used. The details of grain structure for the CdS films produced during the period were similar to those for typical specimens supplied by IEC. This is illustrated in Fig. 7 in a comparison of top surface replicas made after the removal of standard Cu_2S films formed on unetched CdS films typical of IEC and Westinghouse at the time. These views show that the grains delineated by the chemically active CdS grain boundaries are comparable in size* and general

*Since a 45° angle of beam incidence was used for these views, only the horizontal dimensions are accurately given by the 0.5 μm space and the 5.0 μm white bar (at the right) scales in the figure.

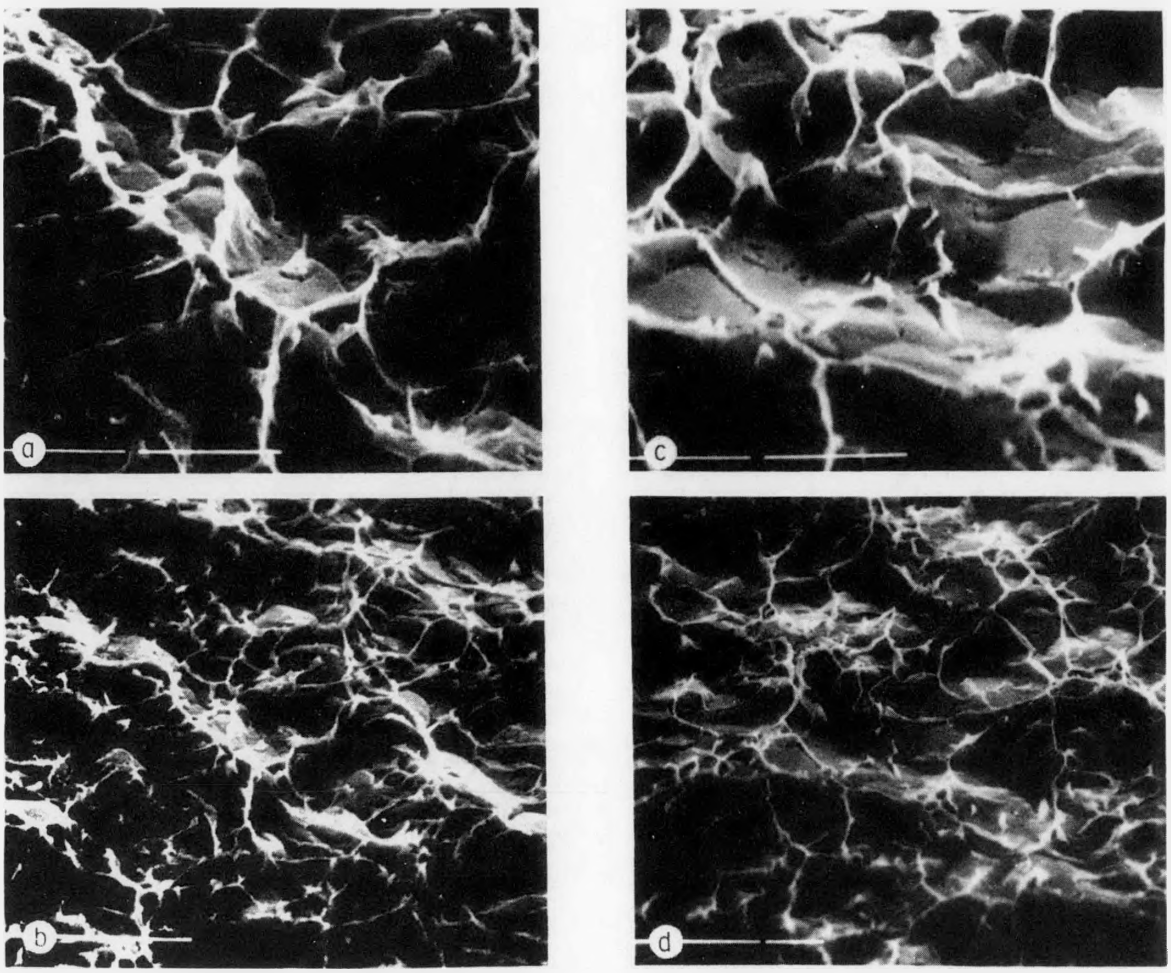

Fig. 7. SEM views at high and low magnifications of replicas formed on typical CdS films produced by IEC (a and b) and Westinghouse (c and d). The replicas were made after removal of standard Cu_2S films produced on unetched CdS layers (Beam angle: 45° to normal.

distribution for the two types of films. Furthermore, the depth of Cu_2S penetration down the grain boundaries is nearly the same for both films.

After standard etching ($\sim$ 30 sec in 1:3 HCℓ in water [vol/vol] at 60°C) and barrier formation, the surfaces of cells produced on IEC material generally appeared to be blacker than those on Westinghouse material. SEM views did not show significant differences in surface texture. Nonetheless, studies were continued with Westinghouse material to determine if any of the wet chemical processing associated with etching and barrier formation influenced cell performance.

Three different strength HCℓ etch solutions (1:3, 55:45 and 2:1) were used to etch specimens of the same CdS film (#665) for various lengths of time. The etched samples were then subjected to standard barrier processing. SEM characterizations were done to compare the degree of surface texturing on the various specimens.

In the case of the most concentrated etch, clear texturing was obtained, even for the shortest time (Fig. 8a). Longer etch times, produced etch pits which grew in diameter and depth (Figs. 8b, c, d). The extraction of more detailed information regarding the fine texturing as a function of time is not possible since the specimen orientations for the SEM work were not respectively coordinated with orientation in the original film.

For the somewhat milder 55:45 etch, Fig. 9d shows that the longest etch time (8 sec) gave fine texture results similar to the 2:1 etch. For shorter etch times, even as long as 4 sec, the surface texture was less well defined in terms of a regular geometry.

Finally in the case of the dilute etch (1:3 HCℓ in water) used for the standard cell processing in this quarter, the CdS texturing effects are very subtle for the scale of the SEM views in Fig. 10. For 10 sec and 20 sec etches, the surface exhibits very slight texturing. Some facets of the grain surface exhibit a "pebbled" texture after 30 sec. This type of texture is quite prominent after a 40 sec etch.

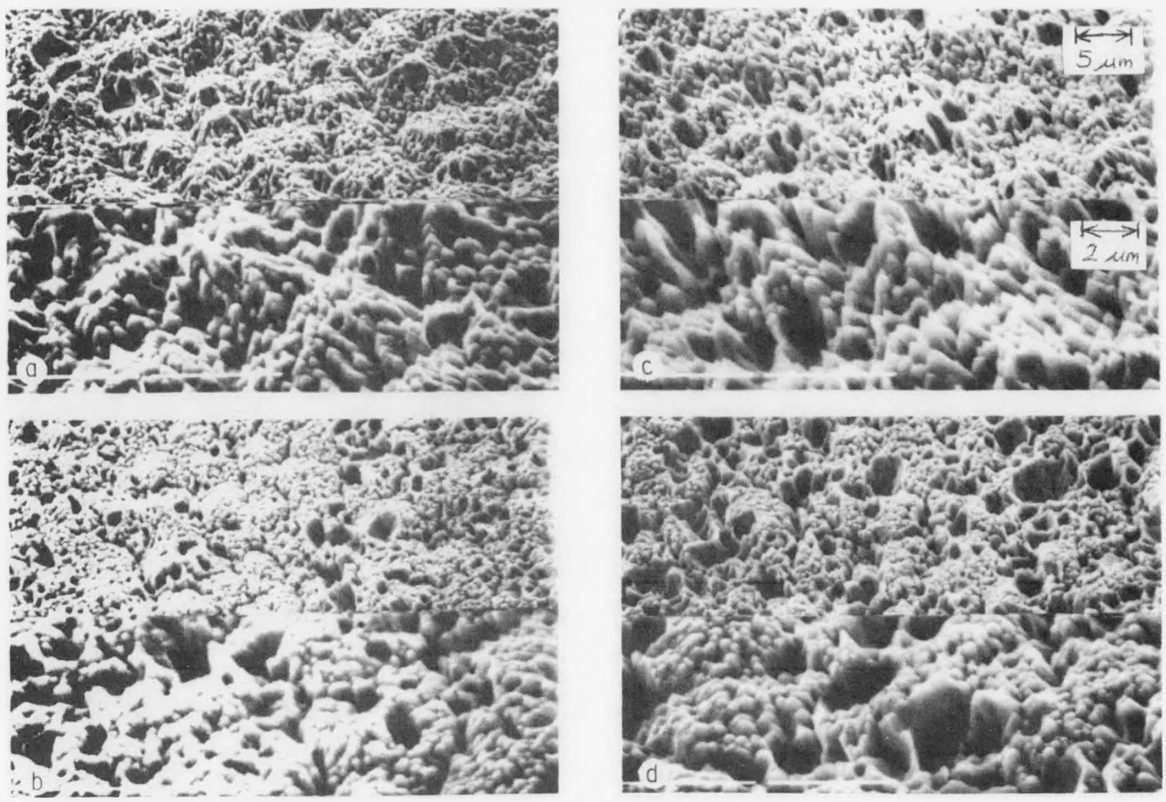

Fig. 8. SEM views of the top surface of a Cu S layer on film #665 which was etched prior to barrier formation for a) 3, b) 6, c) 8, and d) 10 seconds, in 2:1 HCℓ at 45°C. N.b. that half of each view is presented at low and at high magnification for which the scales indicated in (c) apply.

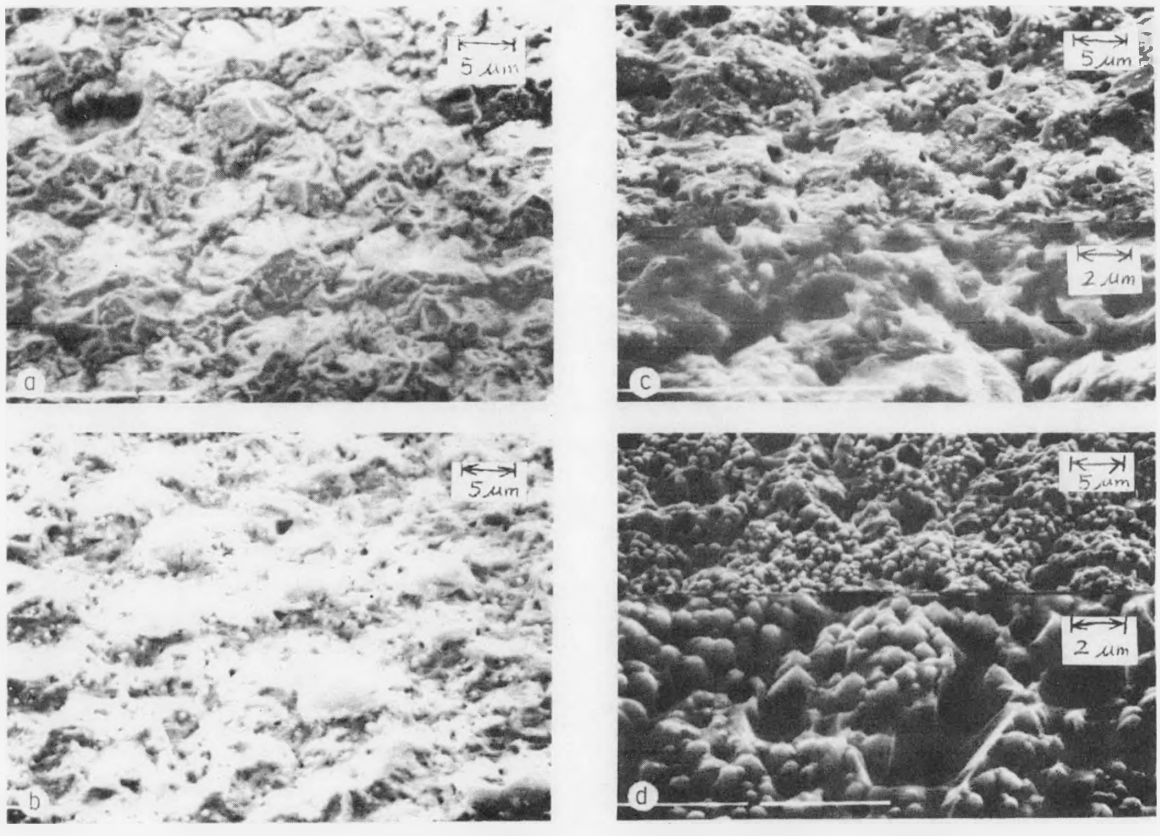

Fig. 9. SEM views of the top surface of film #665 on which standard Cu_2S barriers were formed after etching for a) 1, b) 2, c) 4, and d) 8 seconds, in 55:45 HCℓ at 60°C.

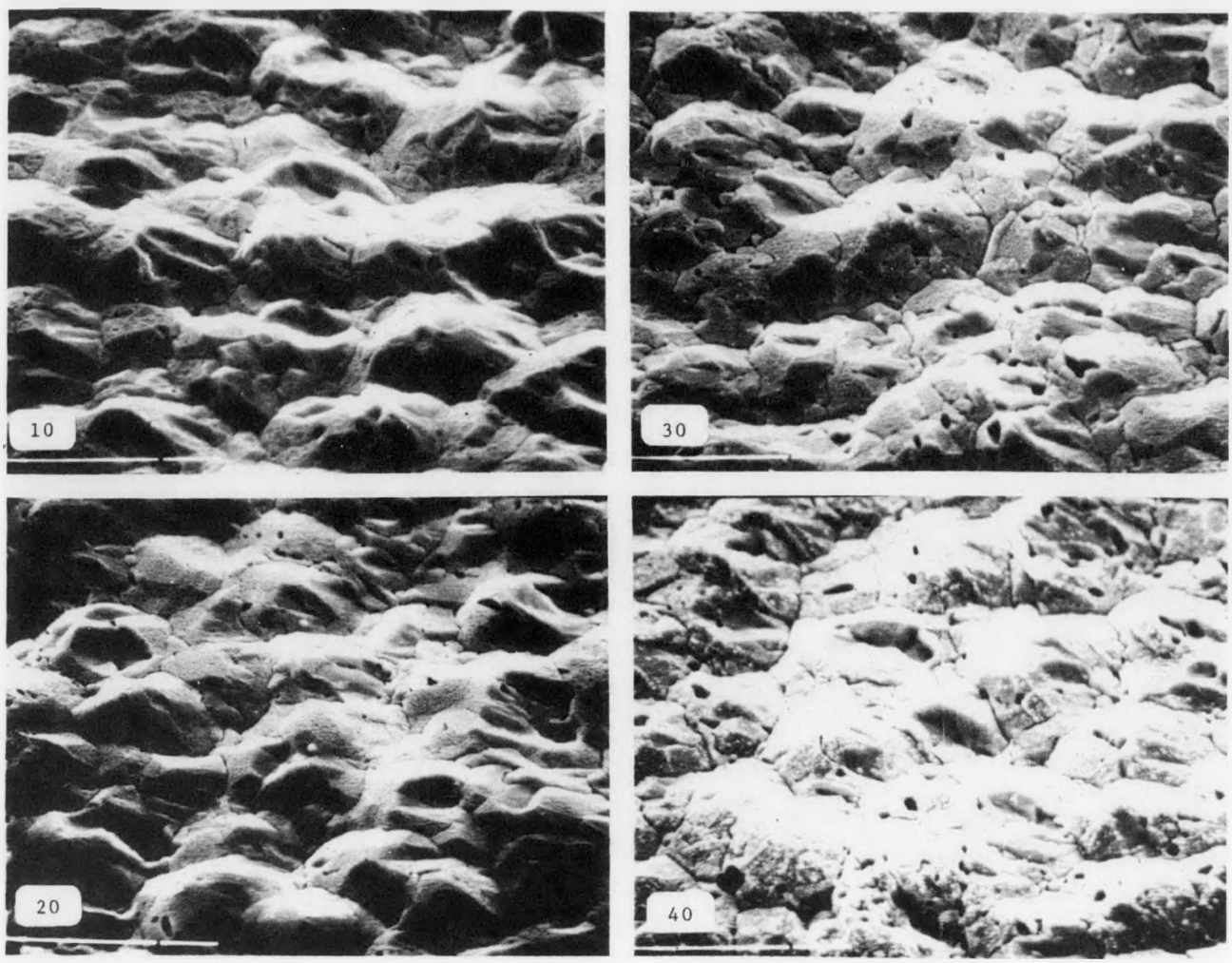

Fig. 10. Views of specimens after Cu S formation on a CdS film etched in 1:3 HCℓ at 60°C for 10, 20, 30 and 40 seconds, as indicated.

Cells were fabricated on material using two etch conditions, viz. 2:1 HCℓ at 45°C for 3 sec and 1:3 HCℓ at 60°C for 40 sec. The former was chosen to produce a high degree of coarse texturing without a high incidence of deep etch pits; the latter, to produce as high a degree of fine texturing as possible with the mild etch. The mild etch gave a higher V_{oc} value (0.478V vs. 0.405V). Short circuit current density values were comparable for the two cells, even though the one produced using the strong etch was blacker in color than the other. Although a statistical comparison using more cells would have been desirable it was not deemed worthwhile. Other studies of etch parameter changes, not involving detailed SEM characterizations, had yielded similarly insensitive results regarding attempts to improve J_{sc} significantly.

Although the comparison experiment just described did indicate higher V_{oc} values for cells processed using the mild etch, other reasons were sought for the wide range of results (cf. Fig. 5) and the failure to achieve 500 mV open circuit voltage values when standard processing was used. Two experiments were devised to compare normal procedures with some extreme cases as regards the etching procedure.

In the first experiment (whose results are shown in terms of the I-V curves of Fig. 11) effects of normal rinsing after a standard 1:3 HCℓ etch were compared with variations involving short and long rinses. In each case, the rinse consists of transferring the cell after etching into a series of four beakers of deionized water. Normally, the cell (on its backing plate) is hand agitated for 5 sec in each of the beakers. Increasing the time in each beaker to 30 sec was associated with a slightly lower value of V_{oc}. For a very short (2 sec) single beaker rinse, the open circuit voltage was much lower.

In the second experiment the duration of the transfer between withdrawal from the hot etch solution and insertion into the first rinse beaker (which is normally about 1 sec) was increased to 30 sec. In this interval the sample dried leaving a white residue on the surface. After processing, the cell with the delayed rinse was again significantly poorer in its V_{oc} performance, as shown in Fig. 12.

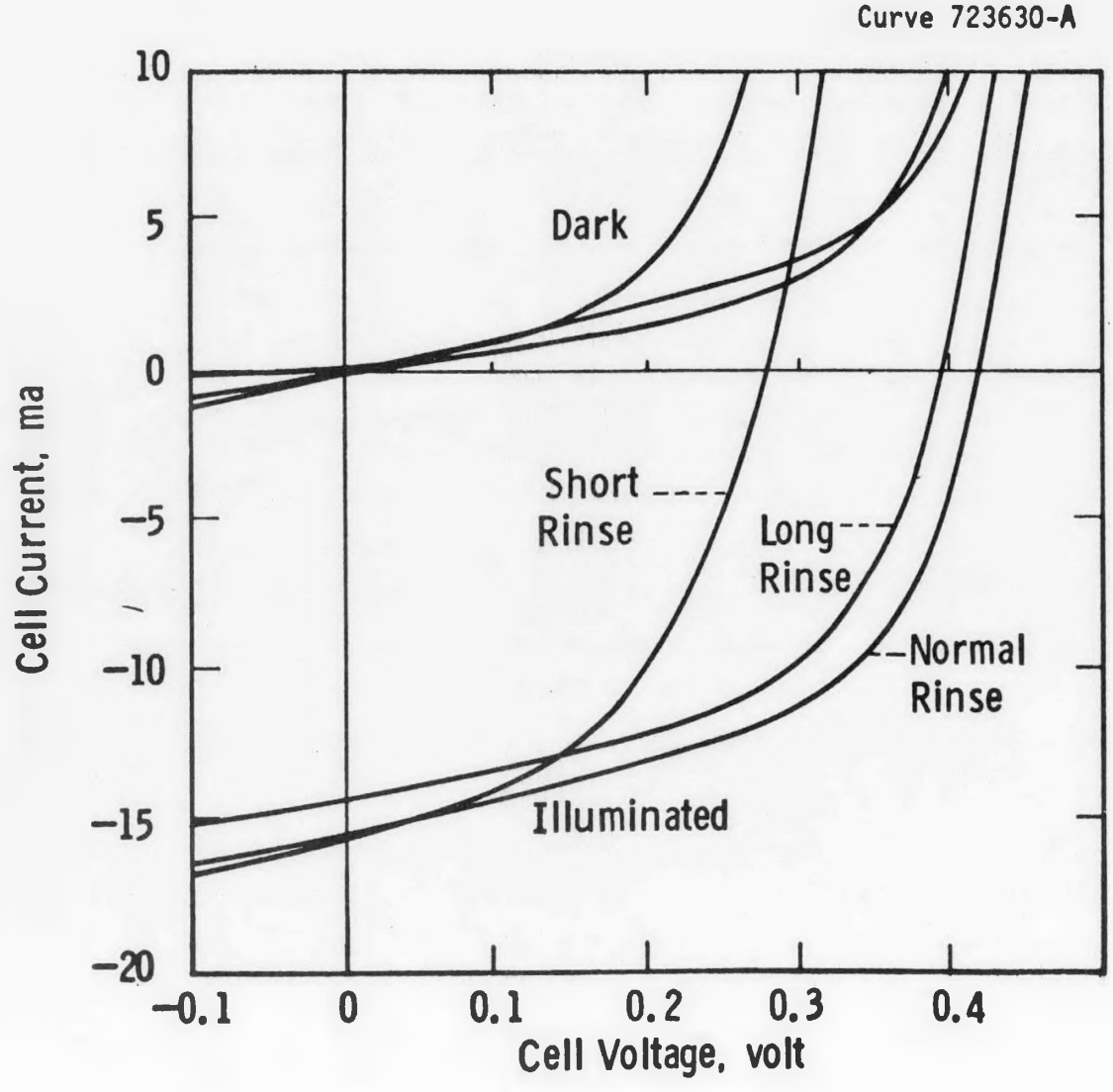

Fig. 11. Effect on cell performance of modifying the duration of the rinse step following etching in HCℓ. Normal rinse: 5 seconds in each of four beakers. Long rinse: 30 seconds in each of four beakers. Short rinse: 2 seconds in one beaker.

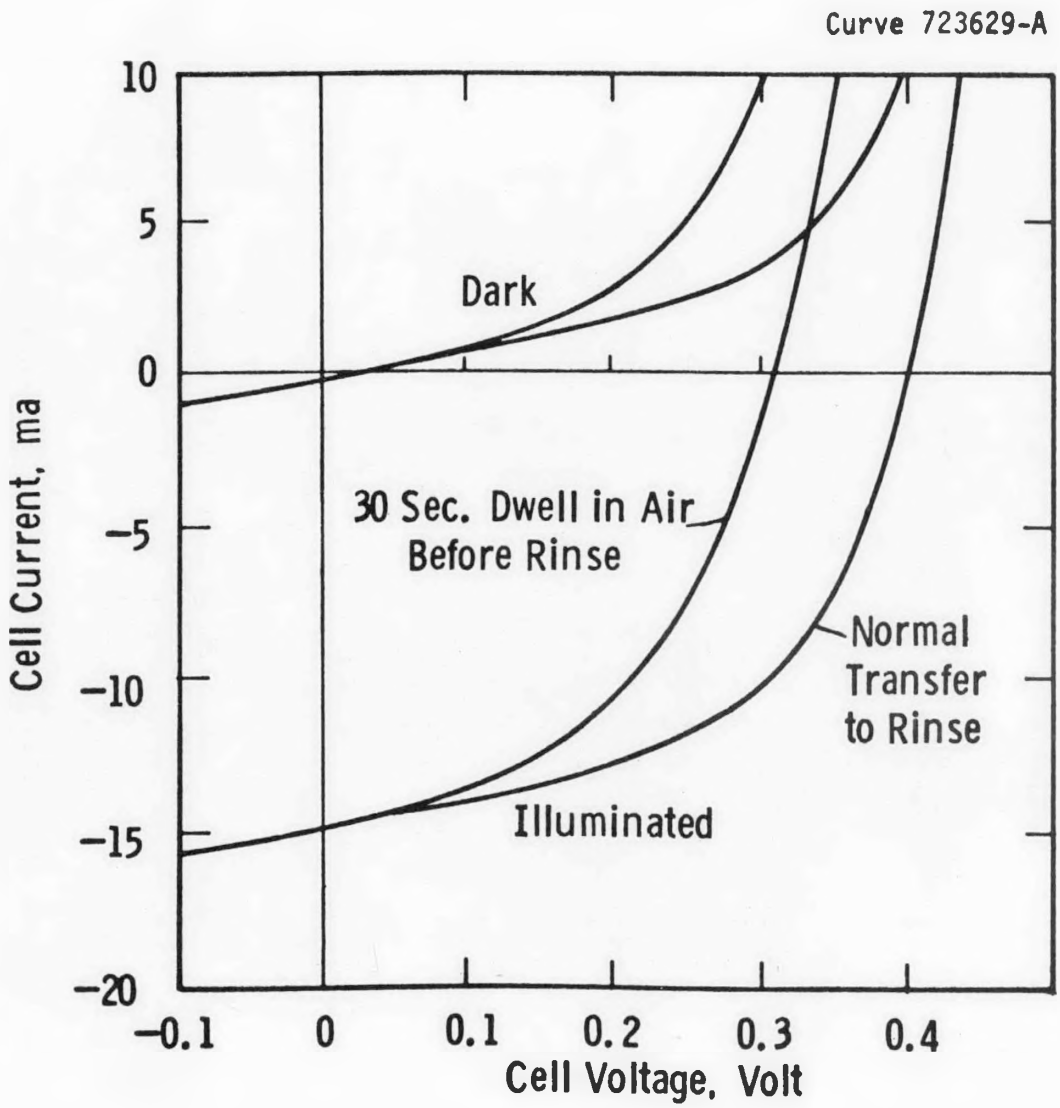

Fig. 12. Reduction of open circuit voltage produced by a 30 second dwell in air during cell transfer from the CuCℓ solution to the rinse.

The experiments just described involved the deliberate use of extremes in the duration of the rinse and transfer parts of the HCℓ etching operation. Their results indicate the need for closer attention to and control of these parts of the cell fabrication steps if better uniformity and reproducibility of cell performance is to be achieved.

4. PLANS FOR THE NEXT QUARTER

The CdS preparation and cell fabrication procedures in use at the end of the third quarter will be exercised to develop base-line information on cell performance. The capacity for generating and analyzing this information, which will include annealing history, will be expanded through the use of computer-controlled equipment. Progress on the program will be reviewed for preparation of a comprehensive report and for guidance of future efforts.

5. REFERENCES

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6. ACKNOWLEDGMENTS

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