Presented at the IEEE 1992 Nuclear Science Symposium
October 25-31, 1992, Orlando, Florida

CONF-9210055--22

BNL--48315

DE93 006649

Dipole Power Supply for National Synchrotron Light Source Booster Upgrade*

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SUMMARY

The booster at the NSLS is being upgraded from .75 to 2 pulses per second. To accomplish this, new power supplies for the dipole, quadrupole, and sextupole magnets have been designed and are being constructed. This paper will outline the design of the dipole power supply and control system, and will present results obtained thus far.

INTRODUCTION

The design of the power supply systems are based, to a considerable degree, upon work previously done at the Light Source. (1,2,3) A substantial departure from the previous approach, however, is that all feedback, feedforward and control functions are performed in a general purpose digital signal processor. This allows the use of control elements of substantially greater complexity and performance than can be obtained from an analog system. The following is an outline of some of the key elements of the system.

POWER SUPPLY

Excitation of the dipole magnets requires a voltage range of 14:1. In order to avoid operating at large phase back angles, two power supplies are provided, connected in series. A 0-100 volt supply provides IR excitation, while a +/- 0-1000 volt power supply provides reactive excitation. Both power supplies are 24-pulse and use the bridge configuration described in (4) and shown in Fig. 1. This is the same configuration previously used (1) but differs in that thyristors 7,8 are controlled. To allow inversion this bridge structure has the property of being able to provide a true zero voltage, rather than a zero integral voltage. Thyristors 7 and 8 are, in effect line commutated free-wheeling diodes. The transfer function of this bridge is shown in Fig. 2. It may be seen that the function is somewhat more linear than the cosine function of a conventional bridge.

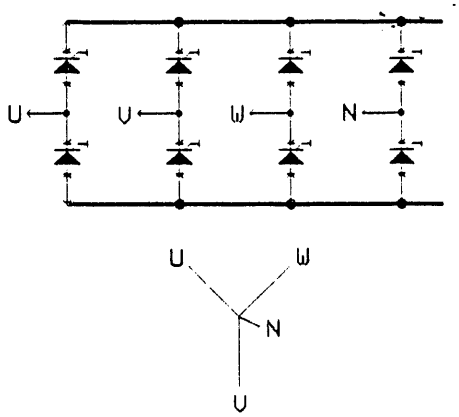

Fig. 1

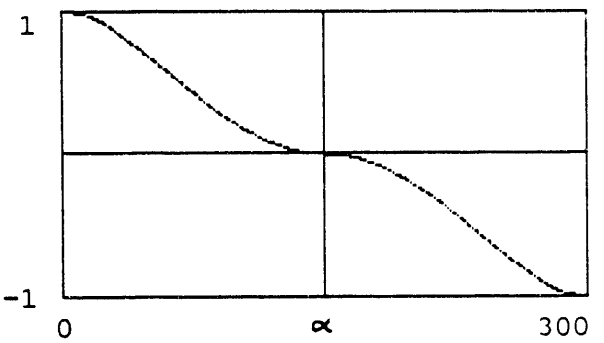

Fig. 2

CONTROL SYSTEM

The control system is packaged in a single 6U VME crate. Slot 1 holds an interface to the NSLS control system, slots 2 and 3 are spare, and slot 4 holds the ramp generator. These four slots are provided with their own VME J1 backplane. A separate backplane for J105-J121 is provided for the servo control system A16 D16 communication. A backplane for J204-J221 provides address and data extension for the servo VME bus and the VSB bus. System initialization, interprocessor non-real-time communication, and fault monitoring takes place over the VME bus while real time

*Work performed under the auspices of the U.S. Department of Energy, under contract DE-AC02-76CH00016.

interprocessor data is transferred on the VSB bus. Real time data between a DSP and an application board such as the I/O channel take place over a private bus (P3). A DSP may operate as stand alone unit or it may be mated with up to two application boards to form an application package.

The system host is a VME format PC AT using a 80386. For development purposes, it is equipped with hard and floppy disks. The final version will use battery backed up RAM. In addition to the host, the control system is composed of the following seven boards.

SERVO I/O CHANNEL

The function of the SIOC is to provide the interface between the digital portion of the control system and power supply outputs such as voltage feedback. It is provided with two A/D channels, one D/A channel, one 16-bit digital input and one 16-bit digital output. The digital inputs are used to convert power supply derived voltages to 16-bit values for processing. The D/A converter is not normally used in the feedback loop, but is used to monitor internal data points in the process stream by linking them to the D/A channel by means of software, and observing the output on an oscilloscope. The digital I/O provides a general purpose mechanism for the connection of diagnostic tools, such as a spectrum or network analyzer.

DVM INTERFACE

Load current is measured by means of a DCCT. The output voltage of the DCCT is converted with 20-bit precision using an HP3458A digital multimeter. The DMM communicates with the interface board in IEEE 488. An embedded TMS320C31 receives the data, converts it to 32-bit floating point, and transfers it to the VSB port for transmission to the DSP performing the current feedback loop functions.

RAMP GENERATOR

The power supply ramp is formatted as a file of sampled data points. These are generated on a work station in the NSLS control system, and downloaded to the ramp generator. The ramp generator, under control of the system clock, outputs this data file cyclically. This ramp data is transferred over the VSB bus to the DSP performing the current feedback loop functions. Two memory pages are provided. One page is always idle, and may be loaded with a new ramp while the other page is in use.

PHASE LOCKED LOOP

The PLL assembly consists of a DSP, an SIOC, and the PLL board. The function of the PLL is to provide the 5.898240 MHz master clock and other timing signals required by the system. The PLL board provides the oscillator, phase comparator, and scaler hardware functions. The filter functions required to close the loop are implemented on the DSP. The phase reference is derived from a 5 volt ac input which is converted in the SIOC. This is filtered in a constant phase filter, and the sign bit is used as the reference to the phase comparator.

TRIGGER GENERATOR

The trigger generator provides the timing signals necessary to drive the 32 thyristors in each power supply. The trigger generator consists of two interconnected state machines, one controlling the 24 main thyristors, and one controlling the 8 free-wheeling thyristors. The control input to the trigger generator is over the P3 private bus. Each state machine is controlled separately, allowing for optimal control of power factor (4).

GATE DRIVER CONTROL

The gate driver control converts the TTL level output signals from the trigger generator to optically isolated signals which are fed to the gate driver crates located in the power supply. A secondary function of this board is to monitor the gate drive current and voltage of each channel for diagnostic purposes.

DIGITAL SIGNAL PROCESSOR

The DSP consists of a mother board and a daughter board. I/O capability includes master/slave A32 D32 VMEbus and VSBbus, and P3 private bus. The VME and VSB I/O is handled by an MC68030. The main processor is a TMS320C30, and this communicates with the private bus directly. One slave TMS320C31 is provided. Communication between processors is accomplished by means of multi-port memory. The master and slave processors are each provided with 128K x 32 SRAM which is equipped with error detection and correction.

The daughter board holds up to an additional six slave processors. Downloading and initialization is accomplished using the TMS320CX emulation port and a 74ACT8990 test bus controller connected to a stand-alone A16 D16 VME slave. This also allows for the facile debugging of programs using the emulator porting kit. A block diagram of the DSP is shown in Fig. 3.

SYSTEM SOFTWARE

All feedback and control functions are performed by software in the four DSP's included in the system. High level functions are performed by the SPOX(5) operating system and are written in C. Filter functions which must run at high speed are written in ASM30. The balance of the time constants used in the voltage and current feedback loops are RCR single pole single zero networks. The feedback loops were designed in the s domain, and then transformed to the z domain using the Bilinear Transform. Each network is executed as a single biquadratic section employing eleven machine cycles. The more complex filter and inverse filter functions, such as those required to implement the feed-forward and PLL were designed in the Z domain using the Maple (7) and Gnuplot packages.

The feed-forward scheme outlined in (3) has been substantially improved and has been described in (6). Additional applications currently under development include ripple reduction using Fourier analysis of the supply output voltage with error feedback, and dynamic control of the output LC filter transient response.

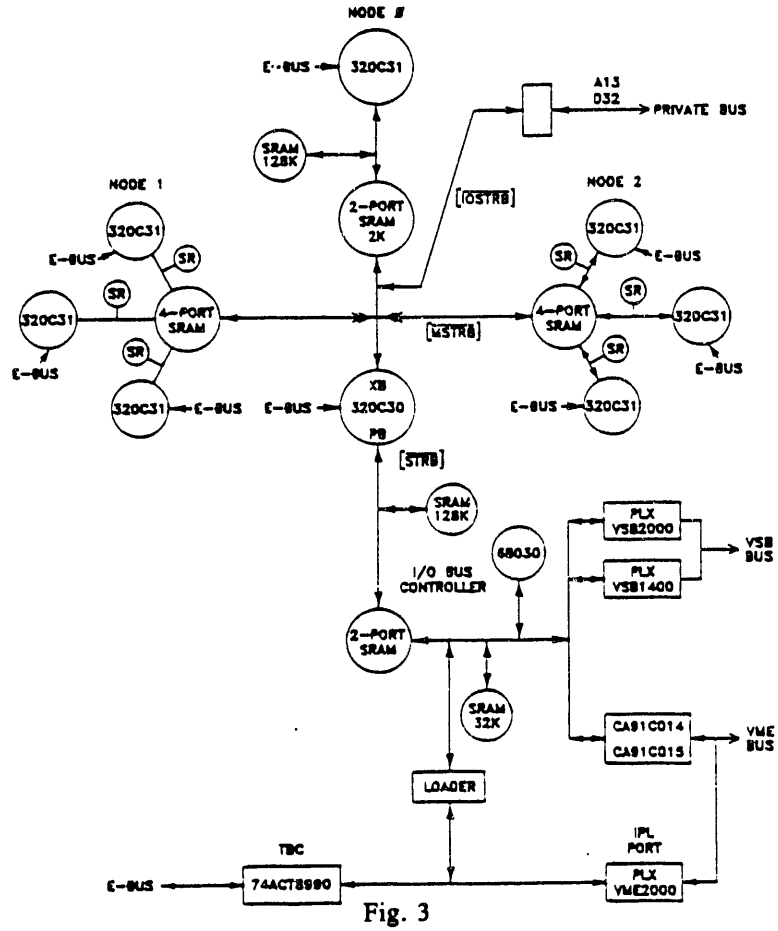

Fig. 3

REFERENCES

1. Olsen, R., Langenbach, H., High Precision Power Supplies for the National Synchrotron Light Source, Proceedings of the 1987 IEEE Particle Accelerator Conference Vol. 1-3 Washington DC, March 16-19, 1987.

2. Olsen, R., A High Performance Digital Triggering System for Phase-controlled Rectifiers, IEEE Transactions on Nuclear Science, August 1983. Vol. NS-30. #4 p. 2867.

3. Culwick, B., Olsen, R., Application of a Digital Trigger Generator to NSLS Booster and Storage Ring Dipole Power Supplies IEEE Transactions on Nuclear Science, August 1983 Vol. NS-30 #4 p. 2865.

4. Stfanovic, V. R., Power Factor Improvement with a Modified Phase-Controlled Converter, IEEE Applications on Industry Applications, Vol. 1A-15, No. 2, March-April 1979.

5. Trade Mark of Spectron Microsystems.

6. Murray, J., Olsen, R., A Differential-Delay Control for Ramped Magnet Current, Proceedings 1992 IEEE Regional Controls Conference, July 24-25 1992, Polytechnic University, Brooklyn NY Page 85-88.

7. Trademark of Waterloo Maple Software.

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