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Thermal Analysis of a SHIELD Electromigration Test Structure

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Abstract

The steady state and transient thermal behavior of an electromigration test structure was analyzed. The test structure was a Sandia SHIELD© (Self-stressing HIgh frequency rELiability Device) electromigration test device manufactured by an outside vendor. This device has a high frequency oscillator circuit, a buffer circuit to isolate and drive the metal line to be tested (DUT), the DUT to be electromigrated itself, a metal resistance thermometry monitor, and a heater element to temperature accelerate the electromigration effect.

The original Sandia device was analyzed for the thermal effects of the heater. Significant changes to the thermal characteristics of the device were made when converting the design from the original Sandia fabrication technology to the vendor's fabrication technology. These changes made it necessary to thermally characterize the new device. The thermal effects of DUT self heating and the transient thermal behavior of the DUT due to the high frequency current pulses used to power it were also investigated.

The behavior of the device with only the heater powered was first measured using metal thermometry monitors on a test die and infrared microscopy. These data along with device cross sections were then used to create a 3D computer thermal model. The model was modified to include the effects of DUT self

heating and then further modified to observe the transient thermal behavior of the DUT.

This analysis characterized the temperatures that electronic circuits in the device are exposed to during test, the increase in DUT temperature due to self heating by the electromigration driving signal, and the amplitude of temperature variations along the DUT due to the frequency and amplitude of the electromigration driving signal.

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CHAPTER 1: INTRODUCTION

1.1 Background

Sandia National Laboratories has developed a high-frequency self-stressing electromigration test structure on a silicon chip. This device is one in a series of SHIELD© (Self-stressing HIgh frequency rELiability Device) test structures[1] developed to aid in the study of high frequency reliability problems. The structure was originally manufactured using Sandia's 0.5 μm CMOS 6 fabrication process. The Sandia device was characterized to determine the thermal effects of operating the heater on nearby CMOS circuitry.[2]

This device was later licensed by an outside vendor and manufactured in a 0.25 μm CMOS process. This process supports five planarized metal interconnect layers as opposed to the original two metal layer Sandia process. As a result of the process change, the new device has different interlevel dielectric thicknesses and a substantially thicker oxide layer over the entire device. A heater structure within the device is used to accelerate the electromigration effect. The heater was narrowed in the new device to keep its resistance in the same range as the Sandia device. Since the new device is significantly different in fabrication from the old one, the new device will be thermally characterized as part of a performance evaluation.

1.2 Purpose of the Electromigration Test Structure

The Sandia electromigration test structure was designed to characterize high frequency electromigration phenomena in metal interconnects on integrated circuits at signal frequencies up to 500 MHz.[3] Most electromigration studies have concentrated on DC or low frequency pulsed DC electromigration. Until now, costly special packaging and test setups have made high frequency electromigration tests difficult to perform. This device allows higher frequency electromigration testing to be performed by combining an oscillator, a heater, a thermometry line and an electromigration test line (DUT) into a single test structure. Conductor lengths are minimized in this structure allowing higher frequency pulsed DC and bipolar signals to be used in characterizing the electromigration performance of metal interconnects. An advantage of this device is that electromigration testing can be performed at the wafer level. These test structures can be placed on production wafers. This allows electromigration characteristics of the metal in that product die to be accurately monitored for wafer to wafer process fluctuations using an in-line wafer probing station.

1.3 Importance of Work

This thermal characterization work is important for the following reasons:

- The rate of electromigration is extremely sensitive to temperature. A 10°C difference in test temperature can cause a factor of two difference in calculated device lifetime.

- The device electronics must be sufficiently cool to function and may require modification either in die design or packaging to meet this requirement.
- Temperature gradients along the DUT and the temperature monitor must be known. The temperature monitor will measure the average temperature along its full length. Gradients along the DUT length will cause uncertainty in the effective electromigration temperature.
- Self heating due to the high average DUT current during a test may cause the DUT temperature to be significantly different from that measured by the temperature monitor. This temperature difference must be characterized to properly analyze the electromigration data.
- The transient thermal effects of a high frequency pulsed DUT signal will cause deviations in the DUT temperature during a test, depending on the test current frequency and amplitude. This input-related temperature change needs to be characterized so the proper temperature conditions in the high frequency electromigration current model may be used.

1.4 The Electromigration Test Structure

A block diagram of the electromigration test structure is shown in Figure 1. The structure has a current controlled oscillator coupled through a current controlled buffer to a metal line used as an electromigration test strip (DUT). This metal line, and a parallel metal line used as a temperature monitor, are heated by a polysilicon/platinum silicide heater.

The current controlled ring oscillator has two control current inputs. One input controls the time the oscillator remains in the '1' state and the other controls the time the oscillator remains in the '0' state. The oscillator frequency may be varied from 500 kHz to above 500 MHz by varying the current supplied to these inputs. The duty cycle of the oscillator may likewise be varied from 1% to 99%[3] by varying the ratio of the currents on these inputs. An externally generated test signal can be gated into the buffer through another input. The oscillator has two buffered outputs. One output monitors the test signal and the other drives the current controlled buffer stage.

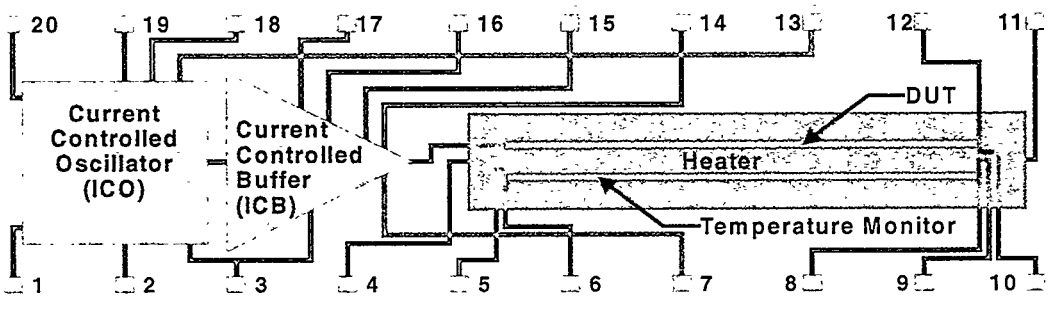

FIGURE 1. Block diagram of electromigration test structure.

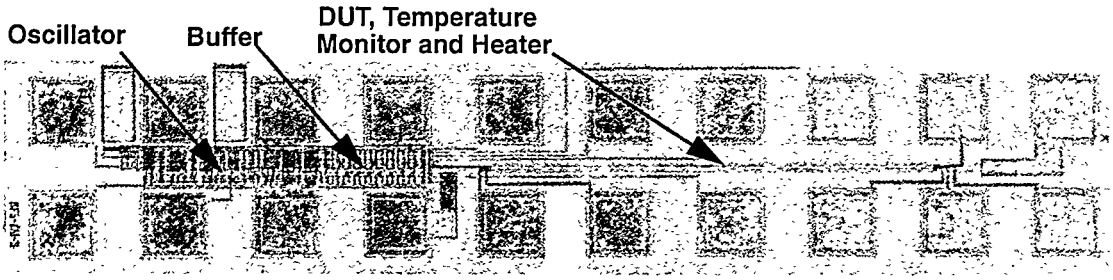

FIGURE 2. Layout drawing of electromigration test structure showing features drawn to scale and the 100 μm by 100 μm pads for electrical connections.

The current controlled buffer stage prevents loading of the oscillator and also controls the peak current applied to the DUT. A DC current input controls the peak current allowed to drive the DUT during both phases (1 or 0) of the oscillator cycle. This stage also has a separate power input (VDDB) to allow larger amplitude signals to drive the DUT. Either a unipolar or a bipolar rectangular signal may be generated and applied to the DUT by varying the ground level (VSS) and the power level voltages on both the oscillator and the buffer stages. The buffer stage also has a selectable input that allows the DUT resistance to be measured.

The DUT and the temperature monitor are parallel 0.5 μm wide metal lines 800 μm in length. The device was originally designed using a two layer metal process and different variations of the device place the DUT and the temperature monitor at either the metal 1 or the metal 2 layer. In one version, the temperature monitor is directly above the DUT, with the DUT being on the metal 1 layer and the temperature monitor being on the metal 2 layer. In this version both devices are centered over the heater. A layout drawing for a metal 1 electromigration structure is shown in Figure 2. A metal 1 electromigration structure was used for all of the experimental work in this paper. Thermal performance of this design can be related to other versions of the device using computer thermal modeling.

The heater is a polysilicon layer capped with a thin layer of platinum silicide to increase its electrical conductivity. The heater is 950 μm long and 15 μm wide. The original Sandia device used a 50 μm wide heater and the narrower heater is expected to cause steeper thermal gradients in the vicinity of the DUT and temperature monitor. The heater is under the DUT and the temperature monitor and accelerates the electromigration effect through heating. The heater has only one connection at each end. However the temperature monitor has four connections to allow accurate four point resistance measurements for thermometry to be made.

Normally the polysilicon/silicide heater is driven between 275 °C and 400 °C to accelerate the electromigration effect in the DUT. It is desirable to maximize acceleration of the electromigration effect through heating to shorten test time. The test temperature depends on the amount of copper added to the aluminum lines. Copper is routinely added to aluminum interconnects to enhance electromigration resistance. If the DUT temperature is too high, copper in the DUT will go into solution in the line changing its properties so

they are not representative of the metal as deposited.[4] The temperature monitor is calibrated before the test so that its resistance can be used to determine the test temperature.

In a typical test, the oscillator is set to a desired frequency and duty cycle. The buffer is set to allow a specific peak current to drive the DUT and the supply voltages to both the oscillator and buffer are adjusted to drive the DUT with either a unipolar or bipolar DC signal. A temperature controller circuit monitors the thermometry line resistance to accurately control the DUT temperature. A load comparable to the DUT is connected from the DUT output to ground and the monitored voltage across that load indicates changes in resistance across the DUT. Tests can be run to a DUT electrically open state, or until the DUT resistance increases by some percentage indicating electromigration failure.

1.5 The Thermal Problem

The high temperatures on the electromigration test structure present several thermal problems. One problem is heating of the buffer and oscillator circuitry by the polysilicon heater. CMOS circuitry often fails at temperatures around 150°C due to thermal generation of carriers.[5] These intrinsic carriers swamp out the extrinsic carriers present in the material and cause leakage across wells in the device. Excessive heating will also decrease electron and hole mobility resulting in slower slew rates for the circuitry. The last buffer stage is about 75 μm from the end of the heater and that temperature will be determined during testing.

Another possible problem is from thermal errors due to thermal gradients along the metal lines over the heater. Thermal gradients along these lines could cause mechanical stress causing them to fail early during testing. It is also desirable that the DUT and the temperature monitor be heated uniformly to the same temperature in order to ensure accurate performance of the device. If the temperature monitor is not uniformly heated, its resistance will represent the average temperature along its length. If the electromigration line is not uniformly heated, the electromigration effect will not be uniform along its length making it difficult to interpret. The thermal gradients along the DUT and temperature monitor are determined.

A second source of heating is a potential problem due to self heating of the DUT from the high peak current density (1E6 A/cm^2 to 10E6 A/cm^2) of its test signal. This causes the DUT to actually be hotter than the temperature monitor. This effect is characterized.

Finally, the transient thermal behavior of the DUT will be investigated. The temperature of the DUT is often assumed to be constant during testing, but the driving signal will cause temperature fluctuations along the DUT at a low enough frequency. The amplitude of these temperature fluctuations at different frequencies are determined.

1.6 Outline of Experimental Procedure

The following experimental procedure was used to characterize the electromigration test structure.

1. A device was cut from a wafer and packaged to simulate the Sandia characterization packaging scheme. Two temperature monitors, one on the structure being characterized and one on a nearby test structure on the same die were thermally calibrated. Infrared microscopy and the temperature monitors in the test die were used to determine steady state temperatures across the device due to the heater being powered to a desired level.
2. External physical device dimensions were determined from layout drawings and optical microscopy. SEM photos of cross sectioned test die were used to determine internal device dimensions including critical device layer thicknesses.
3. A steady state thermal model of the device with the heater powered was constructed and thermally tuned using the results of 1 and 2 above. This model was used to determine the temperature of electronic circuits close to the heater.
4. The steady state thermal model was modified to include average heating effects of the DUT being powered. This model was then used to determine the thermal profile along the DUT length and any temperature differences between the DUT and the temperature monitor.
5. Transient effects due to the frequency of the DUT signal were added to the self heating model generated in 4 above. This model was used to determine the amplitude of temperature excursions on the DUT during testing.

Each of these sections is dealt with in a separate chapter below.

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CHAPTER 2: STEADY STATE MEASUREMENTS

A photograph of a 3.0 x 4.0 mm electromigration test die is shown in Figure 3. The die size was chosen based from previous experience with the Sandia version of the test structure. The size of the test die is important. If the die is made too small, the small die attach area will not allow enough heat conduction to effectively cool the die. A large die requires longer bond wires that can adversely effect high frequency performance. The die was cut to center the HF6-EM-3 electromigration test structure heater to be powered on its surface. The temperature from a nearby test structure (HF6-EM-1) was also monitored in this experiment. Five complete electromigration test structures are visible on this die. This die is cut from a 200 mm wafer and is 0.762 mm (30 mils) thick.

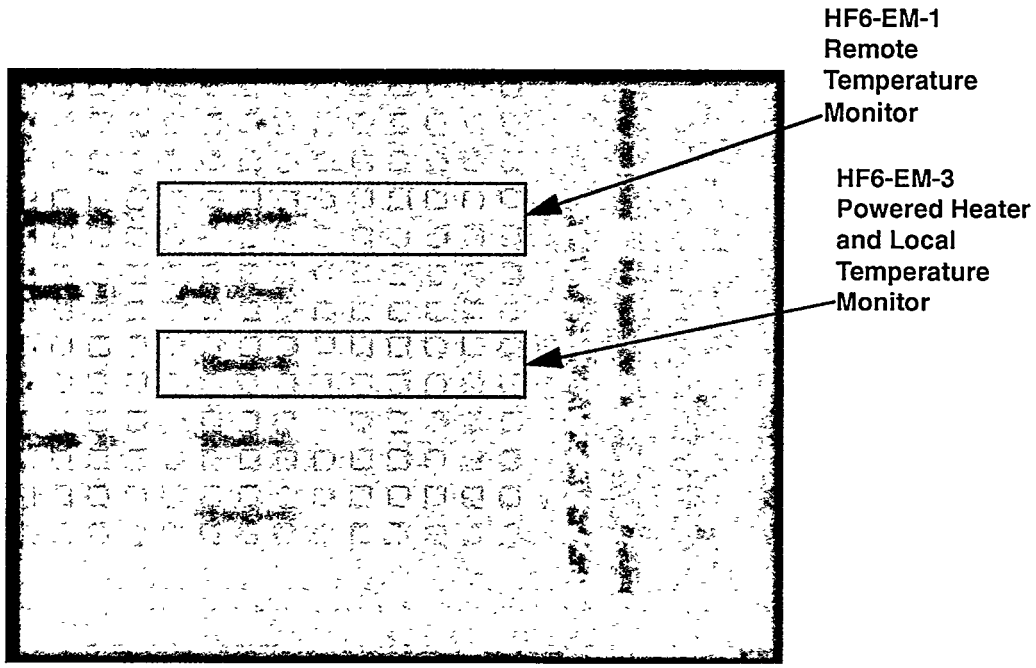

FIGURE 3. Top view of 3 x 4 mm test die showing electromigration test structures to be monitored.

2.1 Device Packaging

Kovar packages were used on earlier generations of electromigration test die. Kovar is an iron-nickel alloy extensively used in microelectronics packages because its thermal coefficient of expansion is close to that of silicon. The test die was die attached to a copper slug instead of a Kovar package to lower the temperature of the electronics near the powered heater on the test die. The thermal conductivity of copper is an order of magnitude greater than that of Kovar (3.9 W/cm-°C vs. 0.15 W/cm-°C at room temperature) so the copper slug presents a lower thermal resistance for heat conduction out of the test die. This lower thermal resistance causes steeper temperature gradients around the powered heater and consequentially lower temperatures away from the heater on the test die.

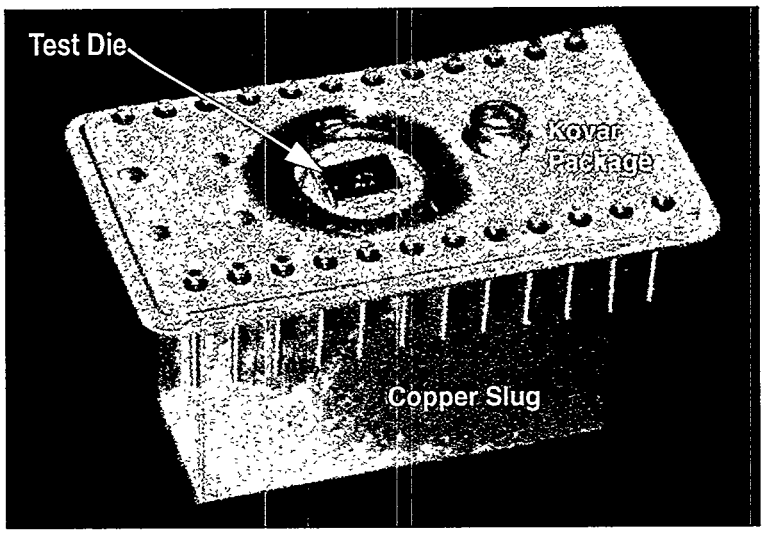

FIGURE 4. Packaging of electromigration test die.

The device package used a slug of copper and a modified Kovar package to connect to the test system. A hole was drilled in the Kovar package to allow the top of the copper slug to be accessed for die attach. The copper slug was screwed and epoxied to the Kovar package and the test die was then directly die attached to the copper slug (Figure 4) using a stress reducing adhesive. This adhesive[6] is designed for use above its 80°C glass transition temperature. This minimizes problems with differing thermal coefficients of expansion (TCE) between the copper slug and the silicon die. All tests for this analysis were conducted with the copper slug and the die at temperatures exceeding 100°C to mimic real life test conditions.

Ten die pads were bonded out to the 24 pin kovar package. The device heater required two bonds, the local temperature monitor required four bonds and the additional remote temperature monitor required four bonds. This additional temperature monitor was used to obtain temperature measurements away from expected large thermal gradients in the vicinity of the powered heater. All of the pads were connected to the Kovar package using a wedge bonder with 1 mil aluminum wire.

2.2 Calibration of Temperature Monitor Lines

Accurate temperature measurements can be obtained from the temperature monitors if they are first calibrated. Temperature calibration is performed on the temperature controlled stage of an infrared microscope* over the range of 25°C to 120°C. This method simplified the calibration procedure. An earlier calibration was performed on parts from the same lot using a convection oven and showed a linear correlation between temperature monitor line resistance and temperature from 25°C to 275°C.

A spring loaded test fixture with a friction socket and a copper block to conduct heat was used to thermally mount the packaged part to the microscope stage. The friction socket

*Infrascope, EDO Barnes Engineering Division, 88 Long Hill Cross Roads, P.O. Box 867, Sheldon CN 06484-0867

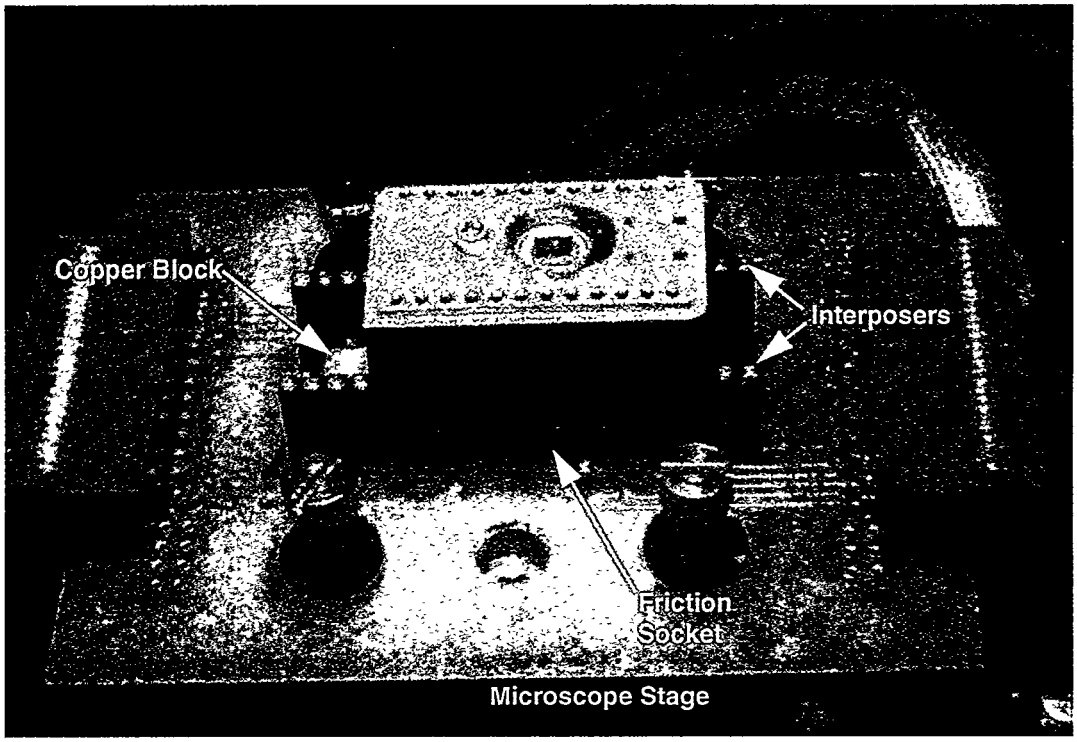

FIGURE 5. Mounting of packaged part to infrared microscope stage.

on the test fixture was equipped with interposers to accommodate the modified device package. The microscope stage was coated with thermal grease* and then the test fixture was screwed to the stage. The copper block provided thermal contact between the temperature controlled stage of the microscope and the bottom of the copper slug of the packaged part. The bottom of the copper slug on the packaged part was also coated with thermal grease and loaded into the top row of interposers (Figure 5).

The two temperature monitors were calibrated prior to initial testing. The local temperature monitor over the powered heater showed an initial decrease in resistance between test runs with the heater powered to 5 W. The local temperature monitor was apparently annealing during testing. This temperature monitor indicated a temperature of 279°C during testing with 5 W of heater power applied. The heater was powered up to 5 W and allowed to run for four hours to anneal the temperature monitor. Figure 6 on page 18 shows the temperature calibration data for both temperature monitors before and after annealing. Linear regression was used to determine the equations of straight lines best representing the data (Figure 6).

The higher temperature of the local temperature monitor caused it to anneal more than the cooler remote temperature monitor. The remote temperature monitor showed almost no change. Measurements of the remote temperature monitor indicate its temperature was 117°C during the 5 W tests. For subsequent testing, the resistances of the two temperature

*Wakefield Engineering 126 Series Thermal Joint Compound

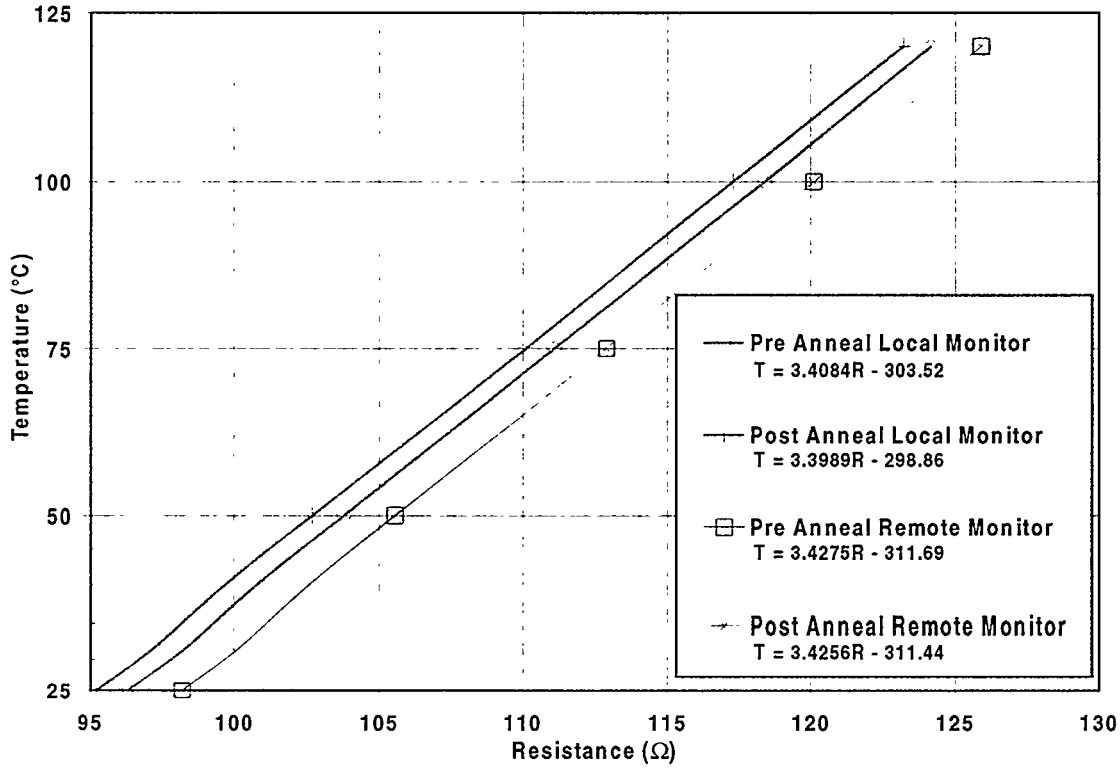

FIGURE 6. Temperature calibration data for temperature monitor lines.

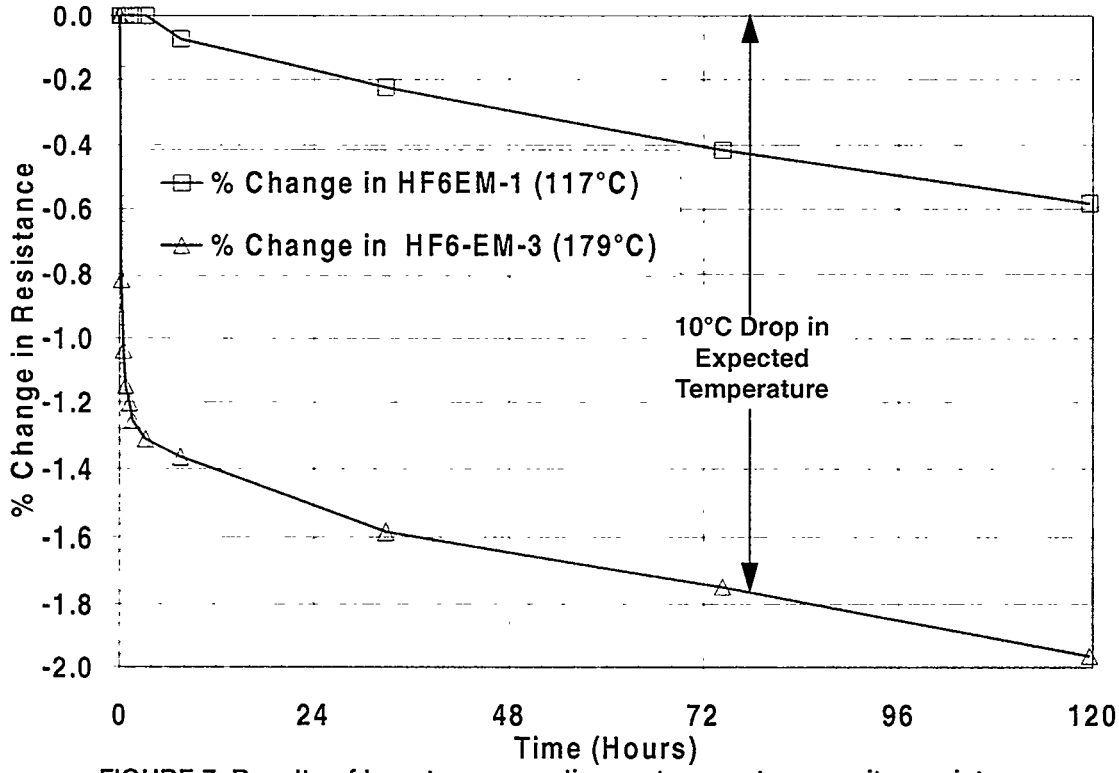

FIGURE 7. Results of long-term annealing on temperature monitor resistances.

monitor lines were recorded after each test at the base microscope stage temperature of 100°C with the device heater unpowered to watch for further annealing. The temperature monitor lines did not appreciably anneal over the remaining tests due to the short time of each test.

A second packaged device was annealed under the same conditions for five days. The results are shown in Figure 7 on page 18. Noise in the remote temperature monitor data caused by the limited resolution of the measurement equipment is apparent during the first four hours of annealing. After 72 hours the error in the temperature measured by the local temperature monitor line is greater than 10°C. The annealing of these lines is a separate problem to be studied and could become a source of error in the electromigration analysis if not addressed in future work.

2.3 Infrared Microscope Test Procedure

A photograph of the infrared microscope is shown in Figure 8 on page 20. Temperature plots were obtained from the infrared microscope by using the following procedure. Before testing, the LN2 dewar on the microscope was filled and allowed to cool the microscope focal plane array for at least 30 minutes. A packaged part was then mounted to the temperature controlled stage of the microscope as previously described. Emissivity is measured over the field of view over a range of 100°C to 110°C. Settling times of five minutes were used at each of these temperatures to allow the test die to come to thermal equilibrium with the temperature controlled stage before data were taken. Appendix A (page 51) contains a detailed discussion of how the infrared microscope measures emissivity and temperature. The temperature controlled stage was then set to the base test temperature of 100°C and 5 W of power are applied to the device heater using a computer controlled power supply.

After allowing the device to come to thermal equilibrium, infrared temperature plots were obtained and resistance readings from the two thermometry lines were recorded along with other pertinent test data. Four different tests were run. The first used a 1X lens to get a thermal image of the entire die surface (Figure 9 on page 20). The second and third tests used a 5X lens to get higher resolution over the entire heater length and also to more accurately determine the temperatures at the corner of the die and on the copper slug. The fourth test used a 10X lens and viewed the end of the heater closest to the buffer circuitry. This test was performed to attempt to resolve peak temperatures near the heater. The remaining three temperature plots and a table showing other collected raw data from the tests is included in Appendix B on page 55.

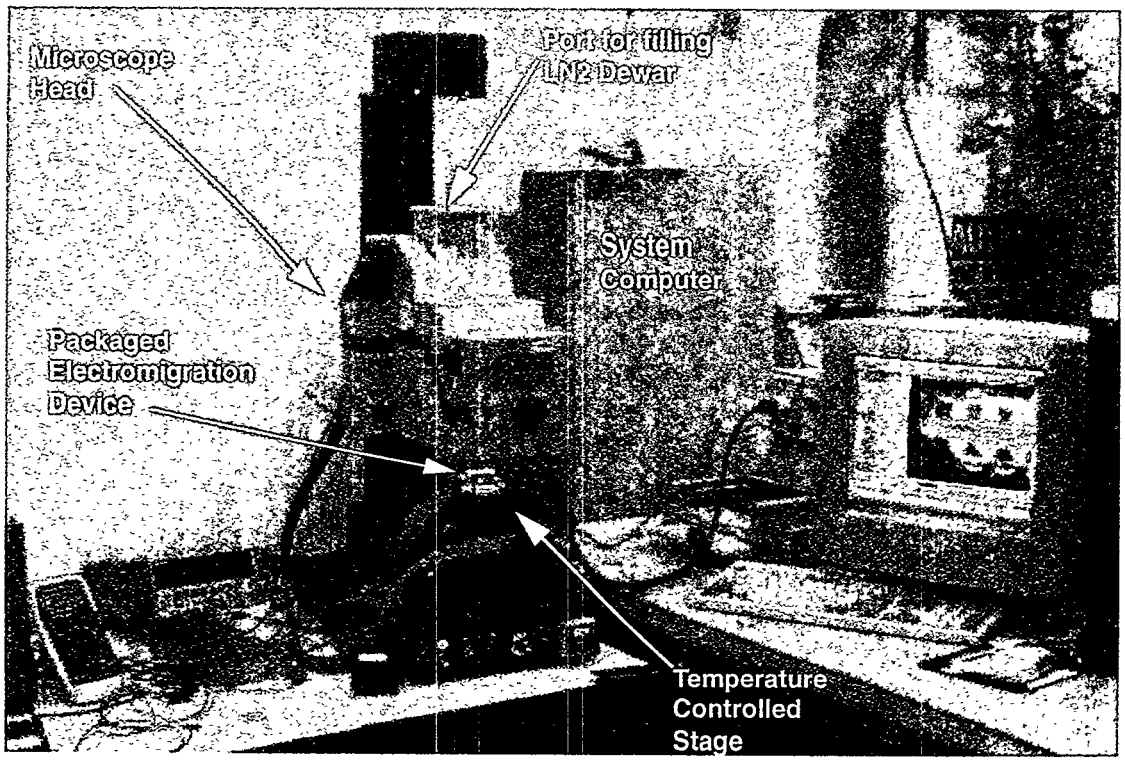

FIGURE 8. Test setup using infrared microscope.

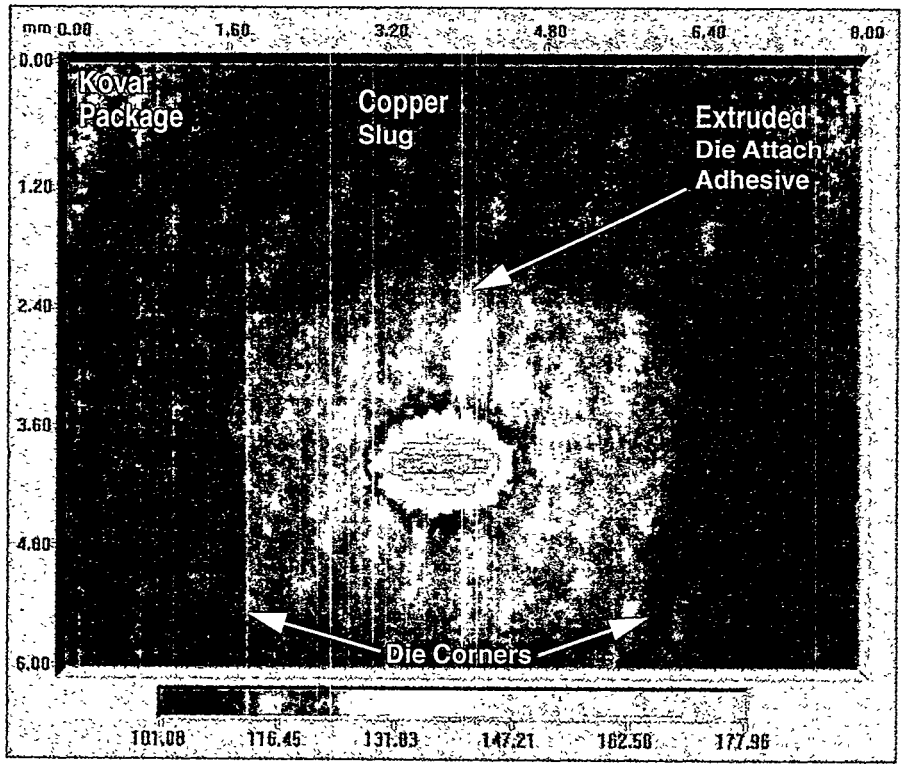

FIGURE 9. Temperature versus test die xy dimension (mm) with 5 W of heater power at 1X magnification.

2.4 Results

A line plot of surface temperatures recorded with the infrared microscope along the center of the length of the heater is shown in Figure 10 on page 22. This graph was produced by compiling both the 1X and the 10X infrared data sets. Both data sets were used to give an accurate depiction of the peak surface temperature measured by the infrared microscope. The 1X data set shows a peak temperature of only 178°C on the die over the heater due to resolution limitations of the infrared microscope. The central symmetry in the peak temperatures over the heater is caused by the mirroring of the 10X data to produce a 10X resolution data set for the full length of the heater. The heater didn't appear to heat uniformly in any of the temperature plots as indicated by the lower center heater temperatures. This effect appears as temperature variations along the heater length, and is probably due to processing defects within the heater element.

The infrared temperature measurement accuracy across the lower temperature areas of the die surface was checked by comparing the infrared results to the results determined by plotting temperatures across the heater width (Figure 11 on page 22). This plot was produced by taking a row of data from the 1X plot across the geometric centerline of the heater length. The peak temperature was lower than shown in Figure 10 due to the lower resolution of the 1X scale (50 μm/pixel). Temperatures across the 15 μm heater were averaged into a 50 μm pixel width at this resolution. The edges of the die are slightly obscured in this chart due to die attach adhesive beading up between the edge of the die and the top surface of the copper slug. This chart shows that the infrared microscope surface temperature over the remote temperature monitor 800 μm from the heater is in agreement within 5 degrees to that indicated by the monitor.

The infrared microscope thermal data in Figure 10 indicate that the peak temperature at the surface over the powered heater is 212°C. This value is questionable because the local temperature monitor indicates an average metal 1 level temperature over the heater of 279°C. The die surface over the heater will be slightly lower than this value as we shall see from the thermal calculations later. The remote temperature monitor was approximately 800μm from the powered heater and indicates a temperature at the metal 1 level of 117°C. This temperature correlates well with the infrared surface data in this region of the device. The surface temperature near a corner of the die was 112°C as recorded by the infrared microscope and the temperature of the copper slug near this die corner was indicated to be 106°C.

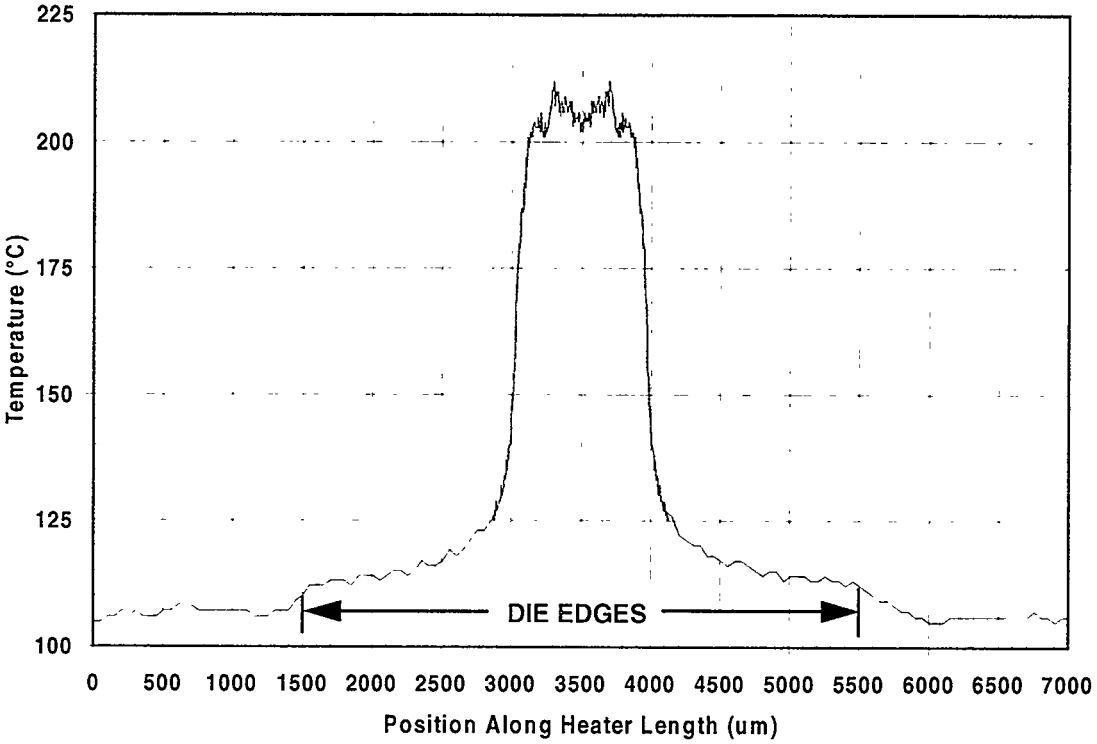

FIGURE 10. Infrared surface temperature data along heater length compiled from 1X and 10X measurements.

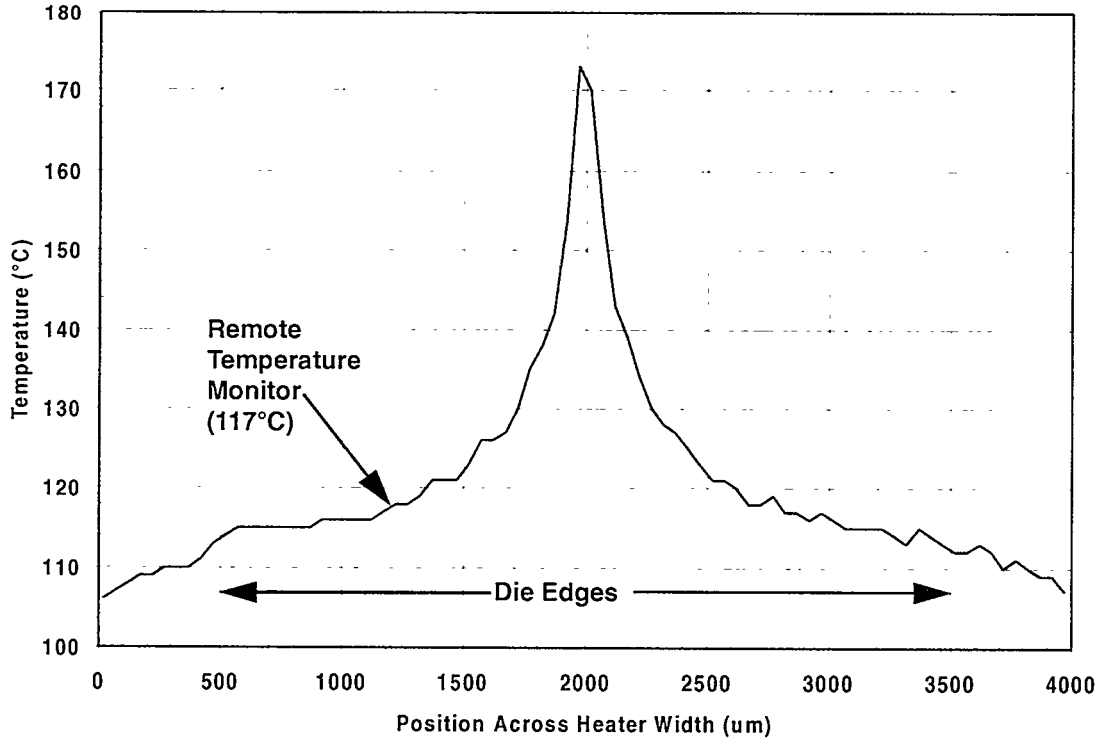

FIGURE 11. Infrared surface data across 15 µm heater width and adjacent die surface

CHAPTER 3: PHYSICAL THERMAL MODEL ELEMENTS

Physical dimensions and properties of all significant thermal elements are required to build an accurate thermal model of the electromigration test device. Information for the thermal grease under the copper slug, the slug, the die attach adhesive, and the die are needed and discussed here.

3.1 Die Dimensions

Feature sizes greater than 20 μm across the surface of the die were determined using optical microscopy. A microscope equipped with a digital measuring device took the photo shown in Figure 12. The digital display was used to determine the heater length, the DUT and temperature monitor lengths, the distance of the remote temperature sensor from the local temperature sensor, and the distance of the buffer circuitry from the end of the heater.

The thicknesses of the layers of die material were determined by cross sectioning device die and then measuring SEM photos taken of the areas of interest. A SEM photograph of a cross sectioned device is shown in Figure 13 on page 24. This device is a metal 1 electromigration test structure cut across the heater width. Several devices from different areas of a wafer were sectioned across the heater element and then photographed in the SEM at different magnifications. The composition of the layers was not specified by the outside vendor, but was assumed to be SiO_2 for all of the interlevel dielectrics. The composition of the die passivation layer was also unknown and is assumed to be either SiN or *p*-glass. This layer was assumed to be similar to SiO_2 in its thermal characteristics for the model.

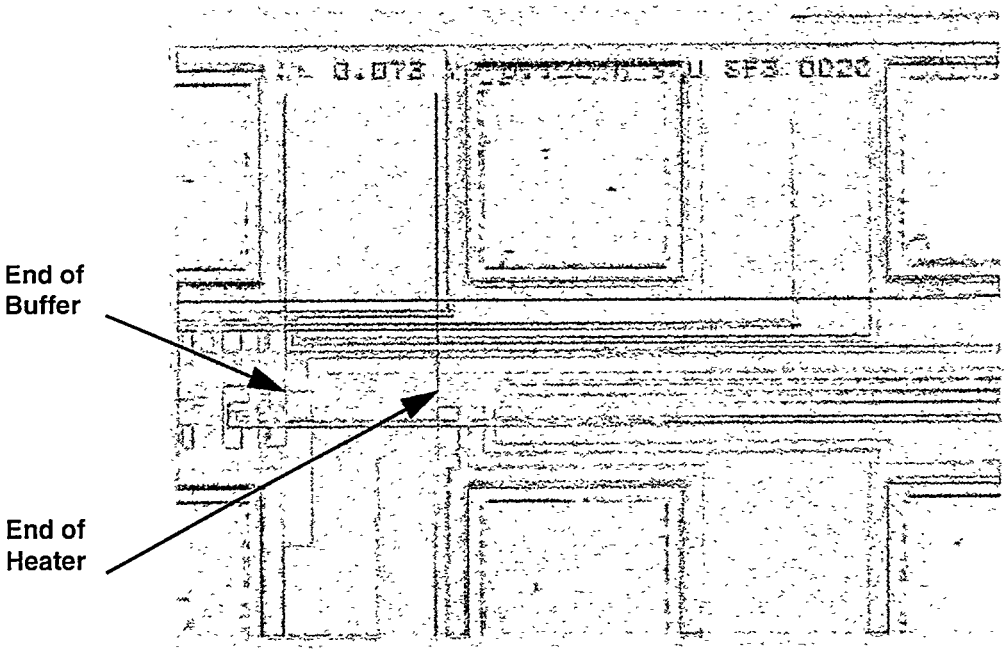

FIGURE 12. Optical photo showing distance from buffer electronics to end of heater.

The heater is polysilicon with a layer of platinum silicide on top of it. A SEM photograph of a cross section of the edge of a device is shown in Figure 14 on page 25. A thin layer is visible above the platinum silicide in this photograph. This layer is probably a spin on glass used to conformally coat the previously deposited layers before another oxide layer was deposited on the wafer. Thin layers in the die such as this one are ignored in the thermal model because they are too thin to cause a significant thermal effect and also because it is likely that their thermal properties are similar to the surrounding SiO_2.

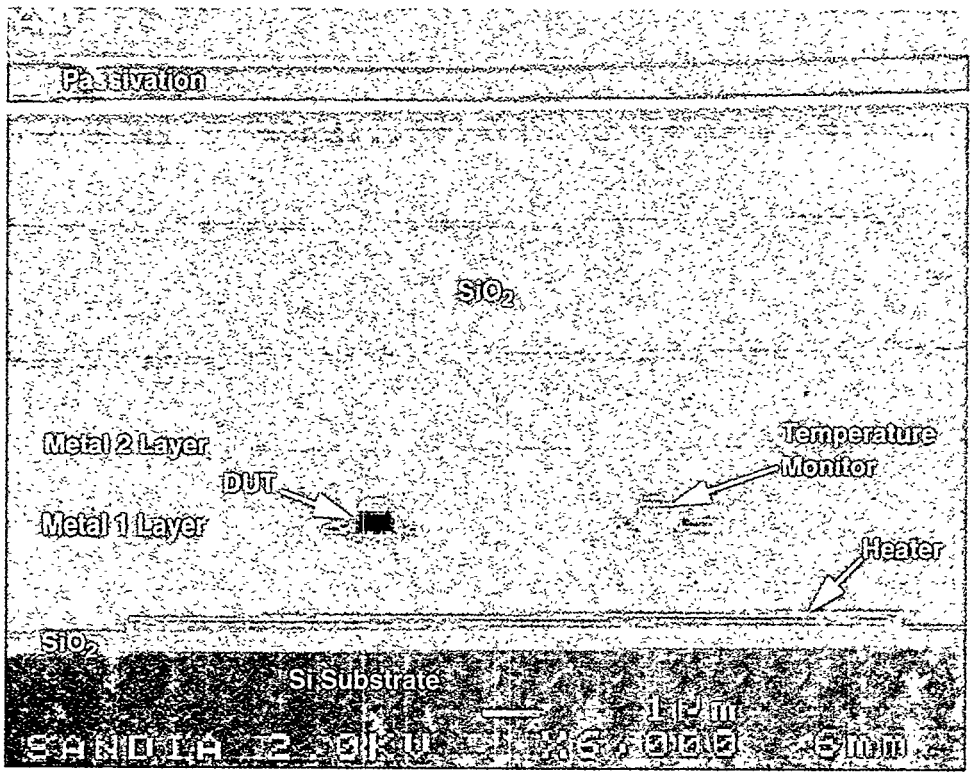

FIGURE 13. SEM photograph of cross section of electromigration structure.

Most of the heater current goes through the platinum silicide layer and since this is quite thin with respect to the surrounding SiO_2 layers, the heater will be modeled as a two dimensional surface heating element.

A diagram of the internal die layers to be modeled is constructed from the photographs. This diagram is shown in Figure 15 on page 25. Elements for only the metal 1 devices are illustrated. The metal 2 devices are similar except that the metal lines are 0.8 μm tall instead of 0.5 μm. For the line over line type of device, the metal 1 DUT and the metal 2 temperature monitor elements are centered over the heater width.

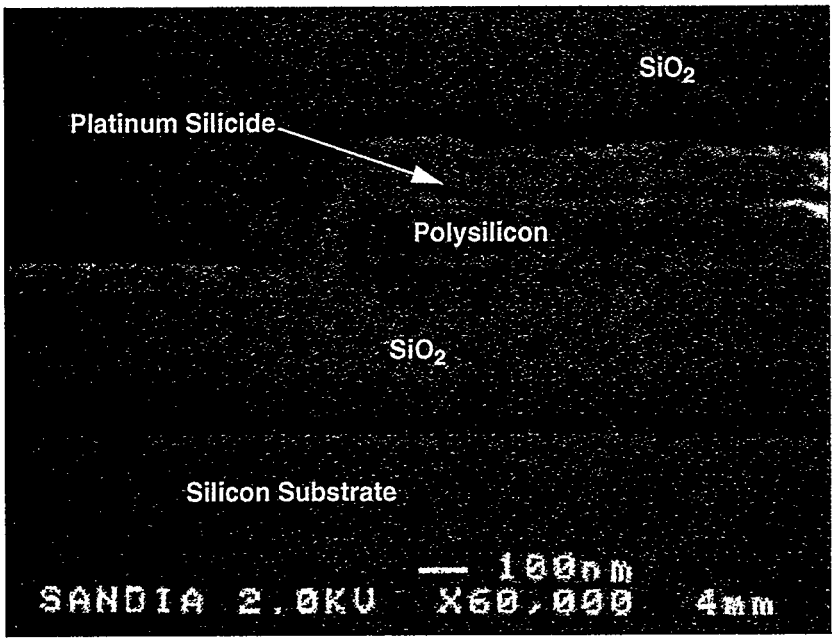

FIGURE 14. SEM photograph of heater cross section.

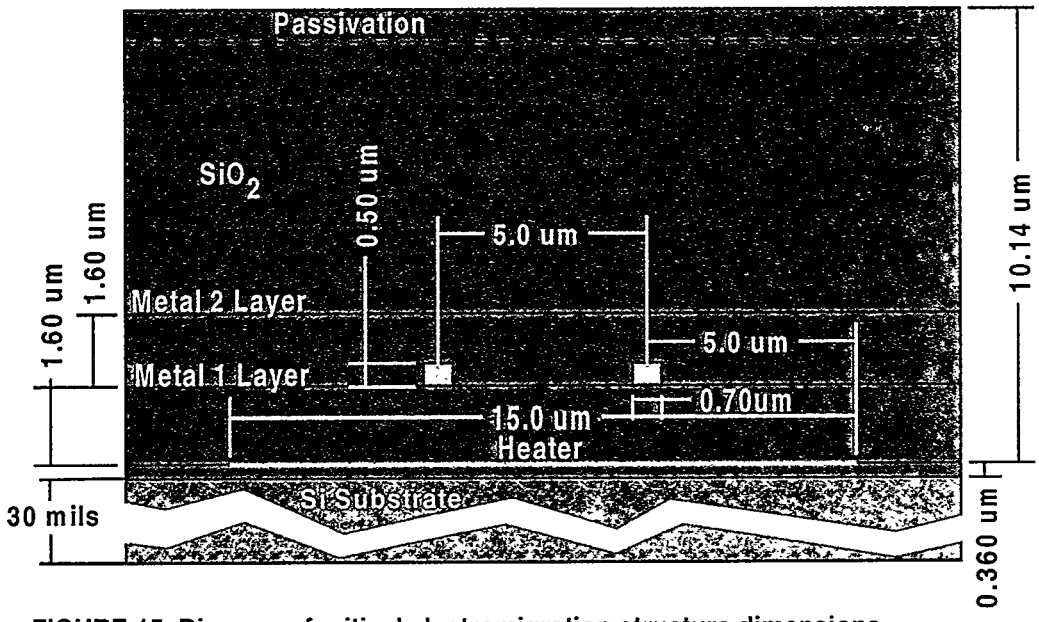

FIGURE 15. Diagram of critical electromigration structure dimensions.

3.2 Other Physical Dimensions

The copper slug was measured using a digital caliper and is 0.95 cm wide by 2.54 cm long by 2.54 cm tall.

The die attach adhesive thickness is approximately 1 mil (0.00254 cm) thick. The die is manually attached to the copper slug and substantial variations in die attach thickness are common. The model is later tuned to agree with the measured thermal resistance of this layer.

A 5 mil thickness is assumed for the thermal grease layer between the copper slug and thermal stage. This thickness and thermal resistance in the model also accounts for any additional resistance through the mounting to the temperature controlled chuck.

CHAPTER 4: STEADY STATE THERMAL MODELING

The infrared microscope provided only limited thermal information about the test die. Surface temperatures near the powered heater have gradients too steep to resolve and internal die temperatures are not measurable through infrared microscopy. This analysis is used to describe temperatures of the DUT and the temperature monitor which are located 8.5 μm below the surface of the die. Of course the infrared system only measures surface temperatures so that internal device temperatures and gradients can be characterized only by producing an accurate thermal model of the device.

4.1 Thermal Analysis Software

I constructed thermal models using a PC based thermal analysis package.* This software supports 3D modeling and allows the use of temperature dependent material properties. Both steady state and transient (time varying) thermal problems may be modeled. This software supports conductive, radiative and convective thermal elements. A complete description of the software package operation and some example problems used to validate the analysis code are given in Appendix C on page 57.

4.2 Material Thermal Conductivities

Steady state models require that the software have either a fixed value or a temperature dependent array of thermal conductivities for each material in the model. The software performs a linear interpolation on array data to determine the thermal conductivity of a material at an intermediate temperature. I used a polynomial curve fit to approximate handbook data, and then performed a nonlinear interpolation every 25°C to improve the accuracy of the model solution.

4.2.1 Silicon

A temperature dependent thermal conductivity array is used for the modeled silicon substrate. I used a temperature dependent thermal conductivity for the silicon elements because the silicon thermal conductivity varies greatly over the range of temperatures found in the die substrate. Values are obtained from a standard reference[7] and interpolated using a polynomial curve fit shown in Figure 16 on page 28. These values were placed in a data array for the analysis software.

*TAS (Thermal Analysis System) from Harvard Thermal Inc., Harvard MA

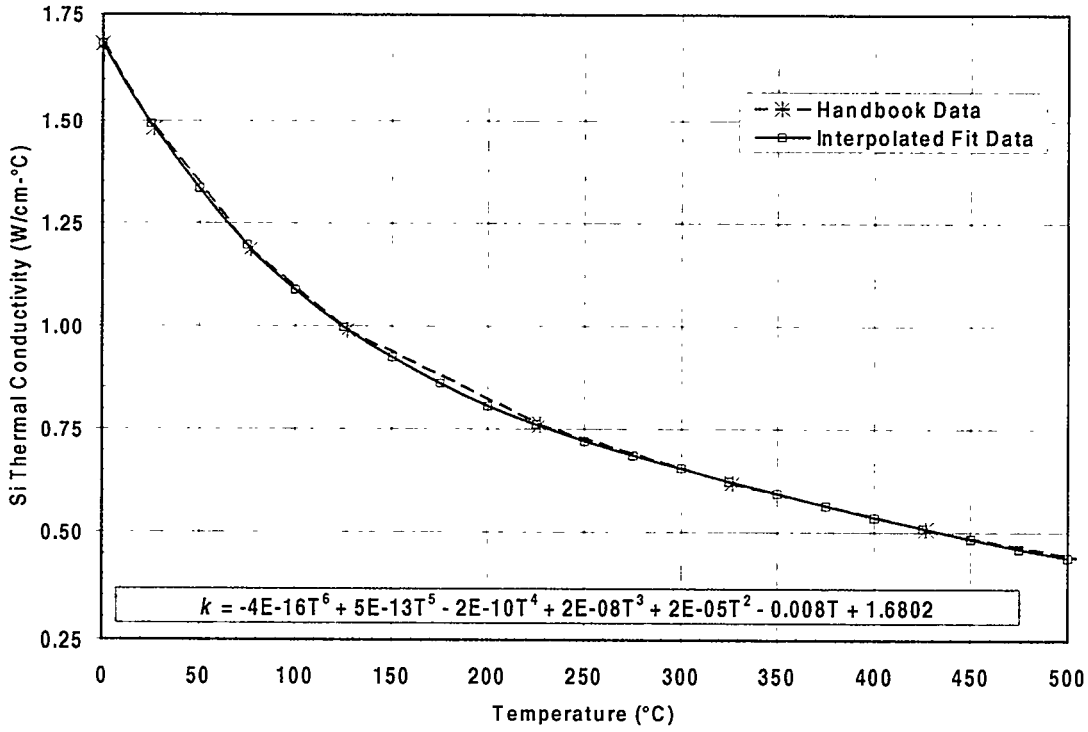

FIGURE 16. Interpolated thermal conductivity of silicon.

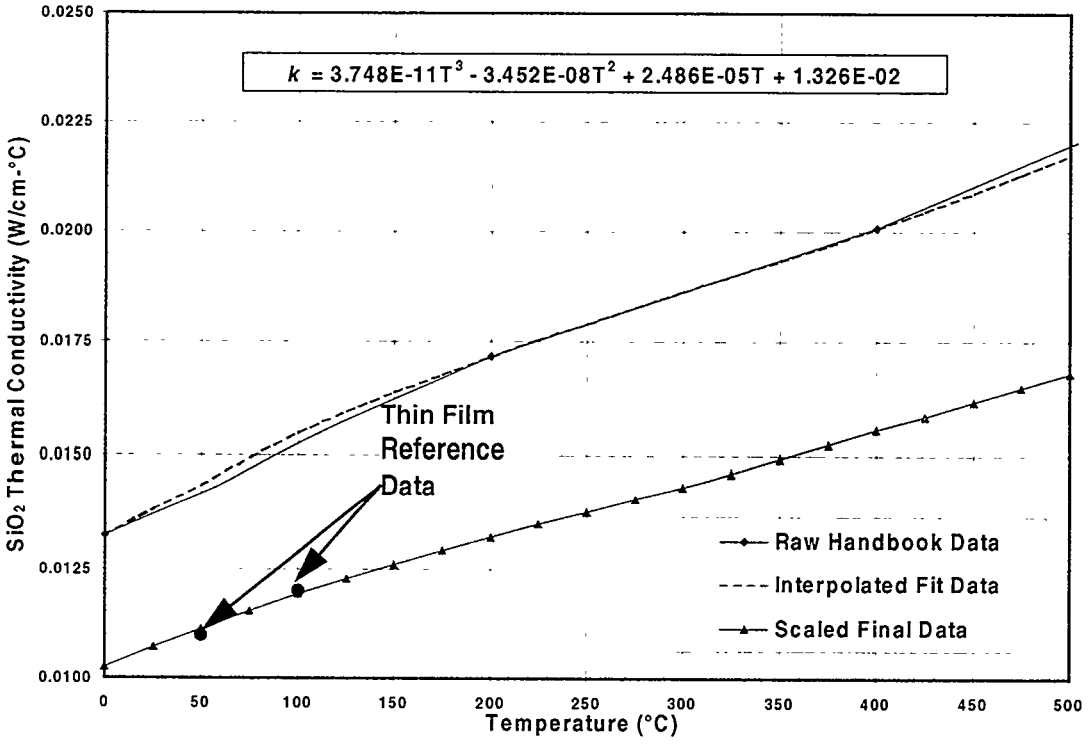

FIGURE 17. Interpolated and scaled SiO_2 thermal conductivity data.

4.2.2 Silicon Dioxide

I also used a temperature dependent thermal conductivity array for the model elements representing SiO_2 layers in the die. Again I choose an array of values for this thermal conductivity because the SiO_2 model temperatures span a wide range. The values used were again obtained from a standard handbook[8] and then fit by a polynomial curve to allowinterpolation in 25 °C increments. A paper on thermal conductivity in thin SiO_2 films[9] gives lower values than the handbook for the thermal conductivity of bulk SiO_2 over the temperature range of interest. I scaled the interpolated data values by 77% to agree with the thin film data in this paper since it is based on SiO_2 as deposited in modern semiconductor fabrication. A plot of the three data sets and several data points from the thin film reference are shown in Figure 17 on page 28.

4.2.3 Thermal Conductivity of Other Materials

Temperature independent thermal conductivities were assumed for the rest of the materials included in the model. I obtained thermal conductivity values for the thermal grease and the die attach adhesive from the manufacturer's data sheets. The manufacturer reports a value of 4 W/m-K or 0.04 W/cm-K for the die attach adhesive. A value of 0.008 W/cm-K was given for the thermal grease. These thermal conductivity values were later tuned to account for thickness variations in these layers. Thermal conductivity values from the TAS software database were used for the copper slug and the aluminum lines. I assumed values for the metal line properties for pure aluminum instead of an aluminum 2% copper alloy. This small amount of copper added to aluminum should only slightly affect the thermal conductivities and has only a weak effect on the model. I used 3.91 W/cm°C for the copper thermal conductivity and 2.37 W/cm°C for the aluminum.

4.3 Quarter Section Thermal Model

The first model I produced was a quarter section model of the device. This model included the die, the die attach adhesive, the copper slug and the layer of thermal grease under the copper slug. I used this model to tune the simulation to match thermal resistance values for the thermal grease and the die attach adhesive, and to determine the operating temperature of the nearby electronic buffer circuitry.

A quarter section model was used to minimize the size of the computer model while allowing the highest possible temperature resolution within the device. Since the entire device as modeled was symmetrical about the center of the die top surface, the temperature profile of any quarter section of the device about the center of the die top surface will give the same results. A pictorial diagram of the quarter section model is shown in Figure 18 on page 30. The heater length runs parallel to the long axis of the copper slug. The copper slug is reduced in height in the model from 1.0" to 0.1" to facilitate timely solutions. Since the temperature gradient across the slug from top to bottom is less than 1°C and most of the heat flux spreads in the top 10 percent of the copper slug, this is a valid approximation. Values for the thermal conductivities of both the die attach and the thermal grease were tuned from the measured infrared data at run time. For example, the infrared data indicated a 6°C temperature rise from the copper block to the die corner with 5 W applied to the

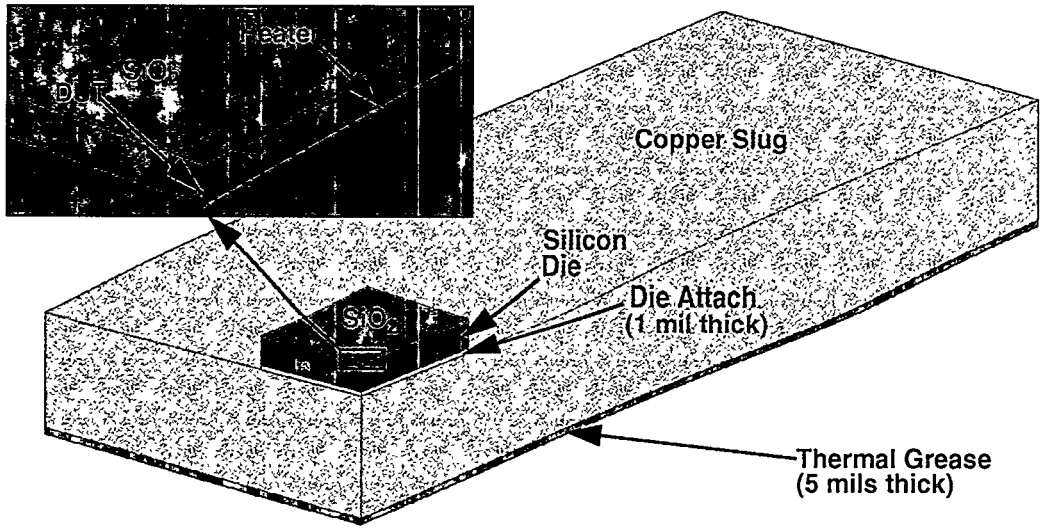

FIGURE 18. Quarter section model pictorial diagram.

heater. If there is an assumed 1 mil (0.00254 cm) layer of thermal grease, the calculated thermal conductivity k is given by Equation 1:

$$k = \frac{q_{Heater} \cdot \Delta X_{DieAttach}}{Area_{Die} \cdot \Delta T} = \frac{5W \cdot 0.00254cm}{(0.3cm \cdot 0.4cm) \cdot 6°C} = 0.0176 \frac{W}{cm \cdot °C} \quad (1)$$

I used this value in the model to match the measured thermal resistance instead of the 0.04 W/cm°C conductivity specified by the vendor. This difference is due to variations in die attach thickness from the assumed 1 mil and to voids existing in the die attach layer. The thermal grease at the bottom of the copper slug was also tuned at run time to take in account all of the thermal resistance from the top of the temperature controlled microscope stage to the bottom of the copper slug. This resistance included two layers of thermal grease and the copper block in the spring loaded test fixture illustrated in Figure 5 on page 17. The temperatures at the bottom of the copper slug increased to about 105°C during testing due to this additional thermal resistance. This was 5°C above the temperature controlled microscope stage set at 100°C. I used a 5 mil layer of thermal grease with a thermal conductivity of 0.005 W/cm°C to account for this 5°C temperature difference.

I meshed the model by trial and error to place the densest mesh where the greatest temperature gradients are found. The model temperatures were calculated many times to observe where the greatest thermal gradients were in the model. The shortest distance between nodes was under the heater in the oxide where six 60 nm (0.000006 cm) thick layers represent the thickness of oxide under the heater. The temperature gradient here was 2.37 million °C/cm! The largest distance between connected adjacent nodes was 0.76525 cm, along the top surface of the copper slug. Here the temperature gradient is only 0.696 °C/cm. These numbers show that the model mesh density varies over five orders of

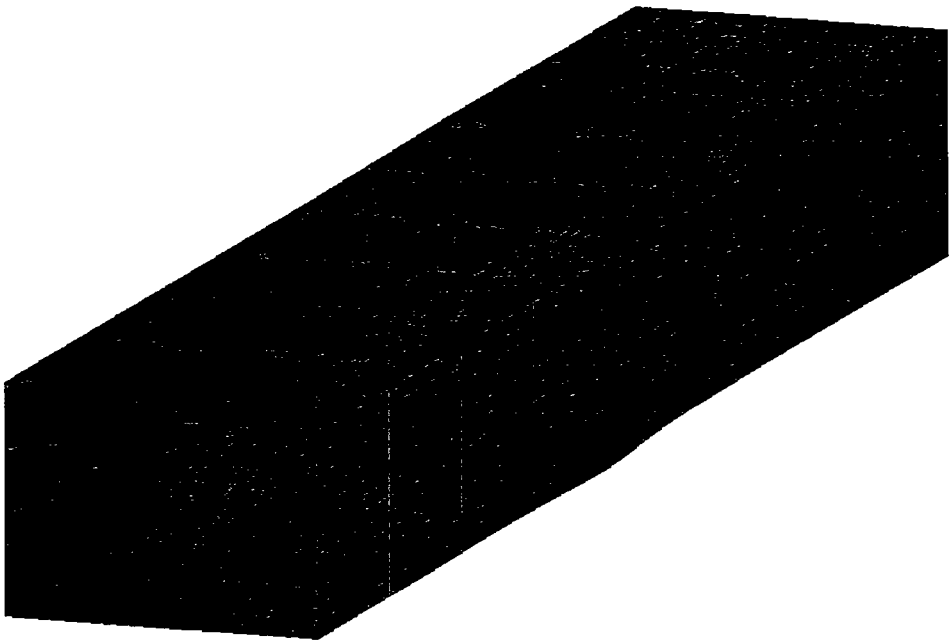

FIGURE 19. Fan style meshing of silicon near heater.

magnitude. The temperature gradients in the model varied over six orders of magnitude. A fan type of meshing is used in the silicon under the heater area to help mesh the model with this extreme variation in node density. The fan style meshing is shown in Figure 19. This allowed a fine mesh under the heater and a coarser mesh in the layers of silicon below. The finished model contains 26,906 nodes representing the corners of 24,360 bricks. Of these bricks, 12,012 represent the oxide on the die since this is where the most dramatic thermal gradients were found. I modeled the heater as an array of surface heating elements in the oxide. This assumes that most of the heater current goes through the platinum silicide layer and rather than the polysilicon part of the heater. The aluminum DUT line was also left out in this first model to further simplify the model meshing.

4.4 Steady State Results

Figure 20 on page 32 compares modeled die surface temperatures along the heater length centered over the heater to measured infrared data. The modeled temperatures agree with the measurements except directly over the heater itself. There are several reasons for this.

1. The infrared microscope is only capable of 5 to 10 μm resolution. Averaging over the modeled curve in 5 μm increments would produce a lower peak temperature.

2. There was some movement of the part during measurement due to expansion during heating. This caused errors in the calculated emissivity of the device.

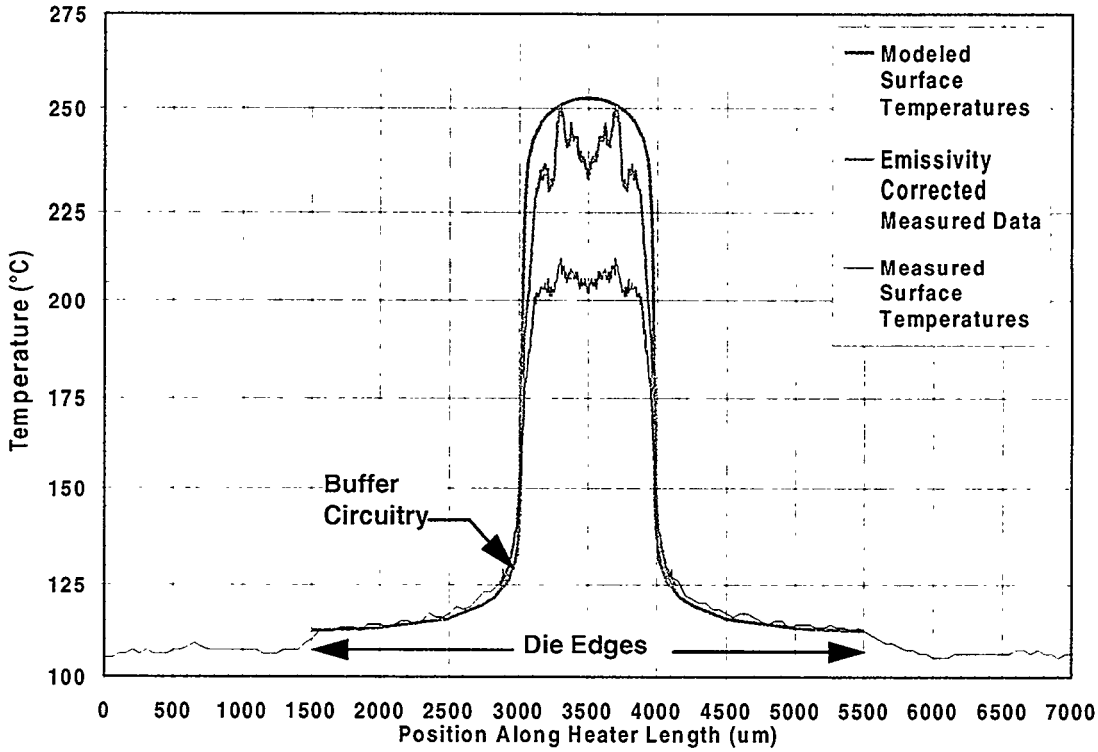

FIGURE 20. Modeled data along heater length.

3. A ±5% change in radiance over the device due to system noise was measured between two 100°C radiance scans.

4. The infrared microscope magnifies emissivity errors at temperatures far from where it was originally calibrated.

5. The emissivity of the SiO_2 decreases with temperature.

This test was performed several times with consistent results. The Emissivity Corrected Measured Data curve in Figure 20 shows the effect of decreasing the device emissivity linearly by 36% over the temperature range from 100°C to 300°C. These data assume an average heater emissivity of 0.47 at 100°C that drops to 0.294 at 300°C.

One goal of this work was to determine the maximum temperature seen by the device electronics. The nearest buffer stage was 75 μm from the end of the heater. Figure 20 shows that the electronics were pulled up by 28.5°C above a 100°C base temperature when the heater was powered at 5 W.

Figure 21 on page 33 shows the surface profile across the center of the width of the heater. This graph again shows as we would expect, that the infrared data do not follow the modeled data at high temperatures. The lower measured peak temperature (<175°C) shows the effect of the limited resolution of the 1X lens on the infrared microscope and the uncertainty in high temperature emissivity. At the lower temperatures of interest, the data agree well. It can be seen that both the modeled data and the infrared data predict that the

temperature at the remote temperature monitor (HF6-EM-1) is 117°C, the same as measured using the resistance of that metal line itself.

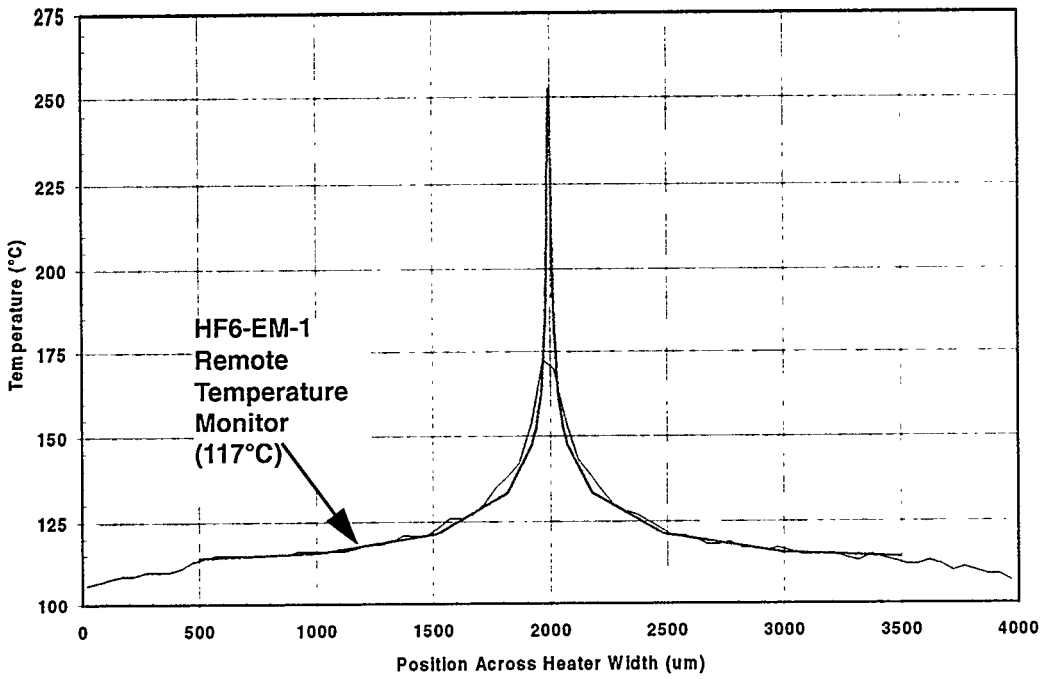

FIGURE 21. Modeled surface temperatures across heater width.

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CHAPTER 5: SELF HEATING OF DUT

The DUT is powered by a current signal from the buffer circuitry. For this model, I assumed a 50 percent duty cycle unipolar signal with a peak current density of between 1 MA/cm^2 and 10 MA/cm^2 powers the DUT. The heater was powered at 5 W, as in the previous section. This part of the modeling was performed to see what thermal effects powering the DUT will have on both its temperature profile and that of the temperature monitor.

5.1 Construction of Half Section Model

A view of the center elements of the half section model is shown in Figure 22.To construct this model I reduced the quarter section model to include only elements above the plane of the heater (all SiO_2) and then converted the previously solved heater layer nodes to boundary temperature nodes. The surface heating elements representing the heater were then deleted allowing the boundary nodes to replace these elements. Next I mirrored these elements about a vertical plane through the center of the heater length to produce a half section model of the die oxide area of interest. I then modified the model mesh by adding bricks to represent aluminum for half of the length of the DUT and the temperature monitor. Volume heating elements were then added to the new aluminum DUT elements to simulate the power dissipated in the DUT.

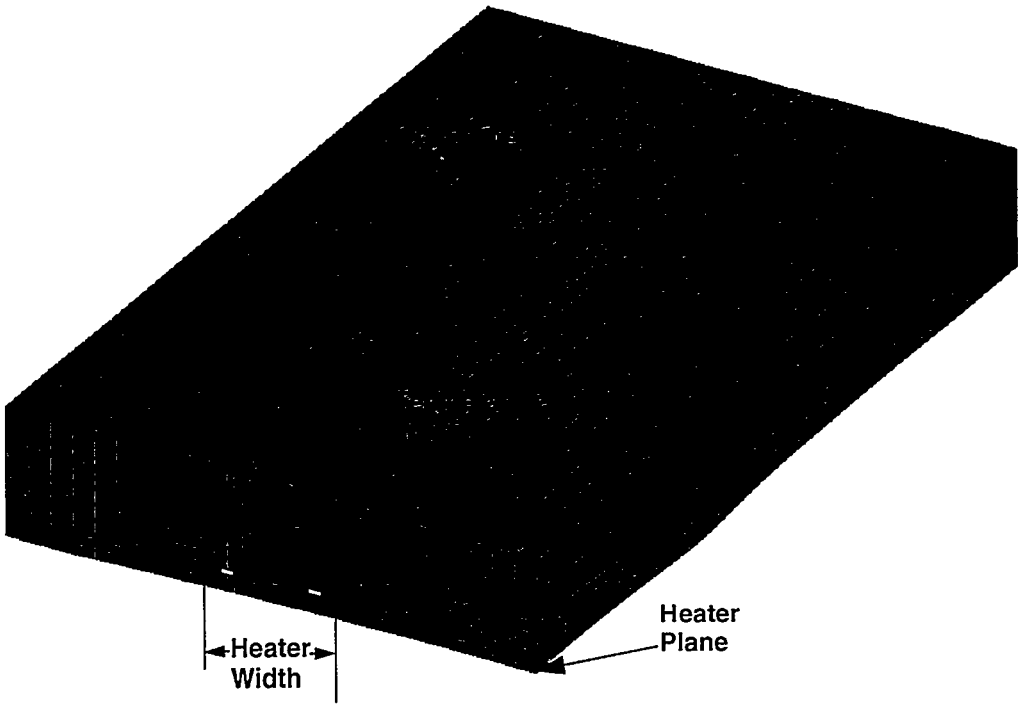

FIGURE 22. Center elements of half section model.

5.2 Calculation of Power Densities in DUT Volume Heating Elements

Since volume heating elements were used to simulate the power dissipated in the DUT, the average power density dissipated in the DUT elements must be determined. I calculated both the peak and average power densities dissipated over the DUT volume by first assuming a 176 Ω resistance for the entire DUT. This value was extrapolated from the measured temperature monitor line data* at 300°C.

The peak current driving the DUT was calculated from the applied peak DUT current density and the cross sectional area of the DUT. Half of the total DUT resistance and the peak current were then used to calculate the peak power dissipated in the modeled half of the DUT. From this the peak volume power density was determined. This calculated power was then halved to give the average power for a 50% duty cycle waveform. The dissipated power was converted to a power density by dividing the power by the volume of the modeled section of the DUT. The half section was created to allow temperature increases on the temperature monitor to be modeled as well as those on the DUT. Table 1 lists the calculated DUT current and power parameters used in this section of the analysis.

Table 1.Current and power parameters for powered DUT.

Peak Signal Current Density (MA/cm^2)	Peak DUT Current (mA)	Peak Power dissipated in ½ DUT (mW)	Peak DUT Power Density (MW/cm^3)	Average Power dissipated in ½ DUT (mW)	Average DUT Power Density (MW/cm^3)
1.0	3.50	2.16	7.708	0.54	3.854
2.5	8.75	13.5	48.18	3.37	24.09
5.0	17.5	54.0	192.7	13.5	96.36
7.5	26.3	121	433.6	30.4	216.8
10	35.0	216	770.8	54.0	385.4

5.3 Effects of DUT Self Heating

A cross section of the center of the model showing an isotherm map of calculated temperatures with an applied current density of 5 MA/cm^2 is shown in Figure 23 on page 37. The center of the DUT is 287°C and the center of the temperature monitor is 280°C. It is apparent that the DUT power results in measurable self heating at this current level.

The 7°C difference in temperature shown in Figure 23 will shift the projected DUT lifetime as shown in Figure 24 on page 37. These curves were produced using Black's Law for a electromigration lifetime (TTF_{50}) model assuming an activation energy for grain boundary diffusion in aluminum/copper lines of $E_A = 0.79$ eV. The TTF_{50} axis refers to the time to failure for 50 percent of the devices using a failure criteria of a five percent increase in DUT resistance. The constant A is related to the metal thickness and width and is derived

*See Figure 6 on page 18. The "Post Anneal Local Monitor" data curve was extrapolated.

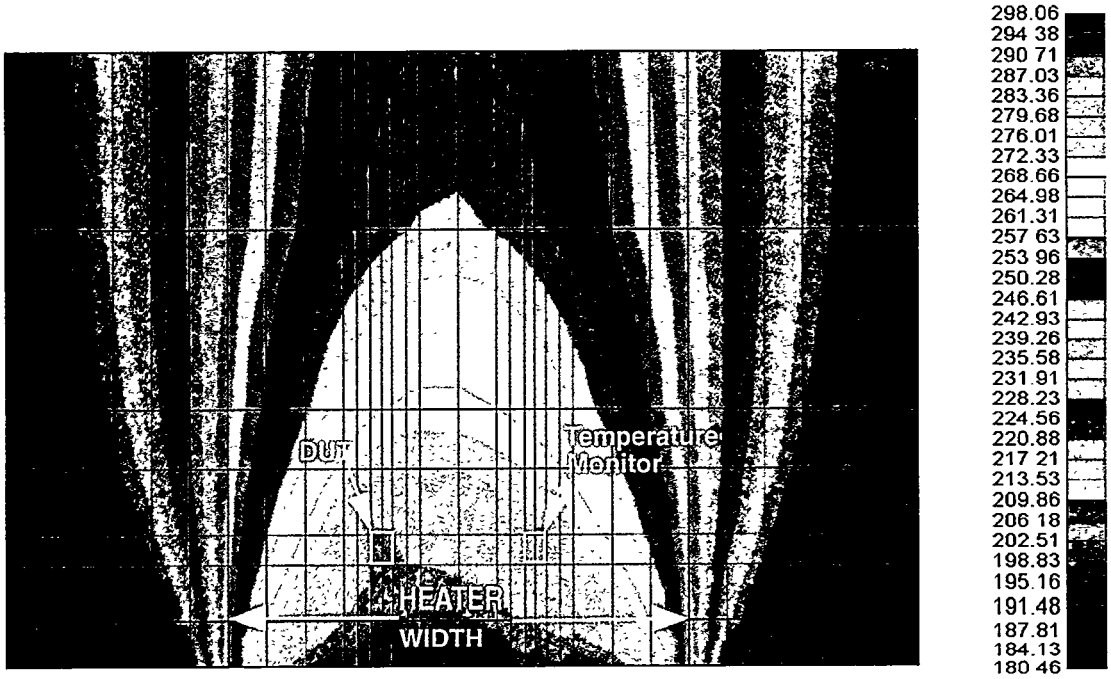

FIGURE 23. Self heating of DUT at 5 MA/cm^2.

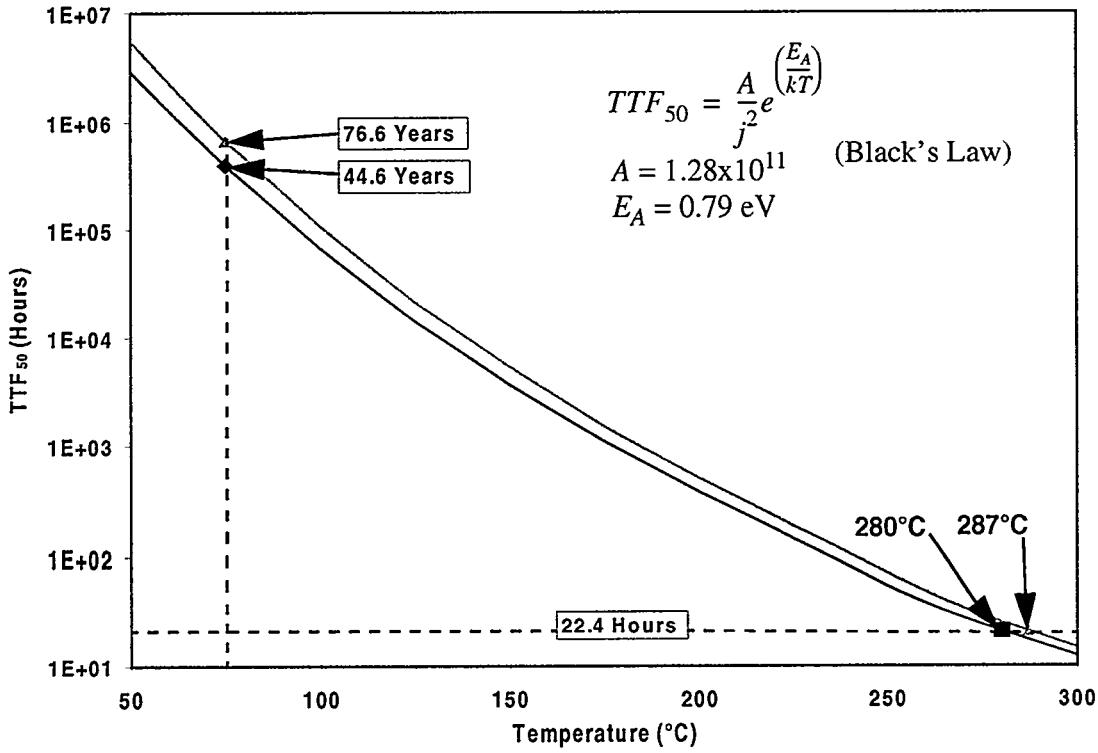

FIGURE 24. Effect of 7°C temperature error on extrapolated electromigration data.

from measured data.[10] The upper curve shows the result for a DUT temperature of 287°C. The lower curve shows the result of assuming the DUT is at the same temperature as the temperature monitor, 280°C. When extrapolated back to 75°C these data show almost a factor of two error in lifetime. A line expected to last for 44 years at 75°C would last for 76 years due to this error in temperature alone. The temperature rise of the DUT due to self heating is significant and may need to be taken into account when performing accelerated electromigration testing.

A plot of the average temperature distribution along the length of the DUT lines at several current densities is shown in Figure 25. This plot also shows the distribution of

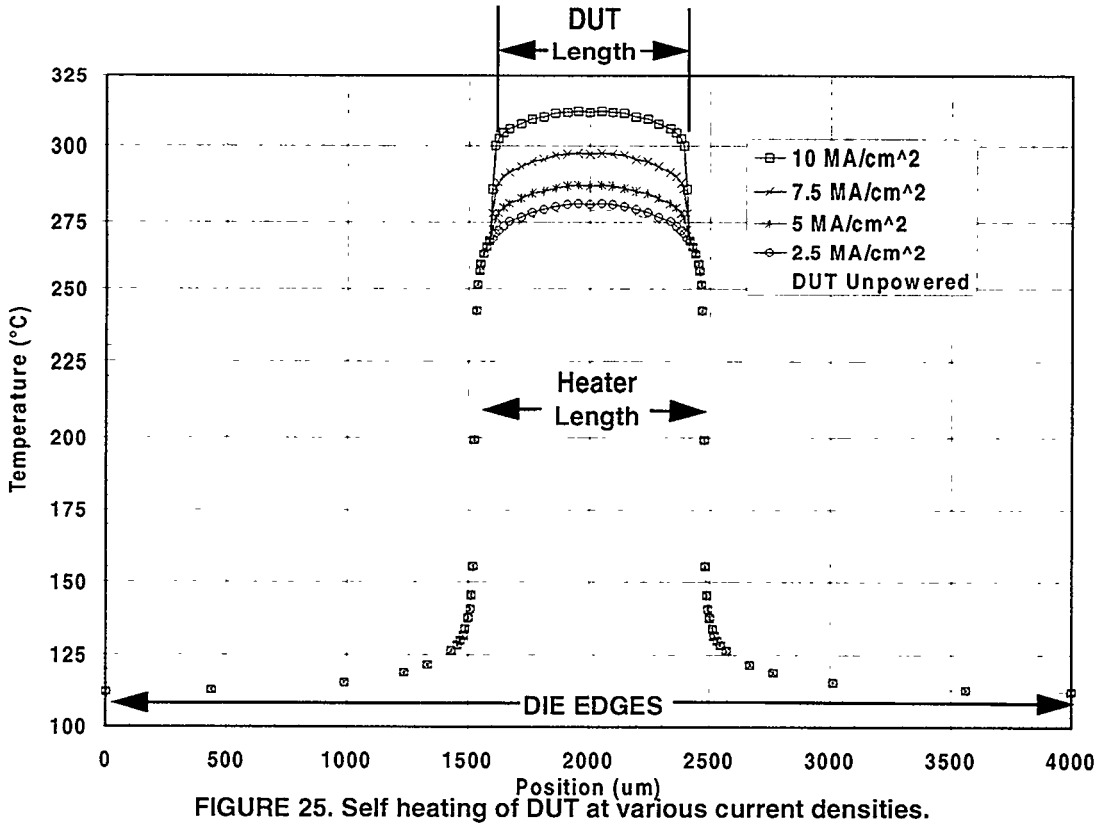

FIGURE 25. Self heating of DUT at various current densities.

temperatures along the DUT length. Average temperature along the DUT profile for various DUT current densities is shown in Table 2. Self heating of the DUT caused the temperature monitor to be pulled up in temperature by more than 1°C only at current densities greater than 5 MA/cm^2. The average DUT temperature was raised by more than 1°C at current densities greater than 1.0 MA/cm^2.

Table 2.Average DUT and Temperature Monitor (TM) temperatures at various current densities.

Current Density (A/cm^2)	0.0E+00		1.0E+06		2.5E+06		5.0E+06		7.5E+06		1.0E+07	
Device Element	DUT	TM	DUT	TM	DUT	TM	DUT	TM	DUT	TM	DUT	TM
Average Temperatures (°C)	276.0	276.0	276.4	276.0	278.1	276.2	284.2	277.0	294.4	278.3	308.5	280.0

The average temperature along the monitor in Table 2 with zero DUT power is 3°C lower than the value measured using resistance thermometry of the temperature monitor in Chapter 2. This is due to the addition of the relatively high thermal conductivity aluminum elements that allow increased heat transfer through the SiO_2 along the length of the metal lines.

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CHAPTER 6: TRANSIENT HEATING OF DUT

The power applied to the DUT is actually time varying instead of the constant average value as assumed in the previous chapter. Time varying temperature variations along the DUT exist and depend on the frequency, duty cycle, and amplitude of the input power waveform. This chapter characterizes the amplitude of DUT temperature variations as a function of the input signal current and frequency.

I used the half section model previously generated to determine the frequency response of the DUT temperature. Instead of applying an average steady state power to the DUT, the volume heating elements that represent DUT self heating are now represented as time varying arrays of power values. To model the transient response of the DUT it was necessary to include both densities and heat capacities for all the materials used in the model.

6.1 Additional Transient Model Thermal Properties

Only aluminum and SiO_2 elements are used in the half section model. Default values from the TAS software database for both the densities and the heat capacities of these materials are used and shown in Table 3. The software used these values to calculate effective thermal capacitances between adjacent nodes.

Table 3.Additional property values for aluminum and SiO_2.

Material	Density (g/cm^3)	Heat Capacity (J/g-°C)
Aluminum	0.0432	0.9003
SiO_2	2.200	7.448

6.2 Results

Figure 26 on page 42 shows the transient temperature of the DUT and temperature monitor at center nodes along their lengths when a 50% duty cycle, 5 MHz waveform with a peak current of $5MA/cm^2$ was applied to the DUT. This graph indicates that both the DUT and the temperature monitor were effected by the self heating of the DUT, but that the transient effects of heating are only seen by the DUT at this frequency.

This graph never reaches a condition where the average DUT and temperature monitor temperatures are constant. The software calculated the temperature at every node in the model for each time step. The size of the calculation time step was determined by the software from the minimum distance between nodes and the material properties. The transient simulations used a time step on the order of $4x10^{-10}$ seconds. This made the transient simulation process quite slow. I chose to write out values to a hard drive during this simulation every 0.02 μs to give ten datum for each power cycle plotted. All node temperatures in the model are written to a disk every 0.02 μs of simulation time generating large data files.

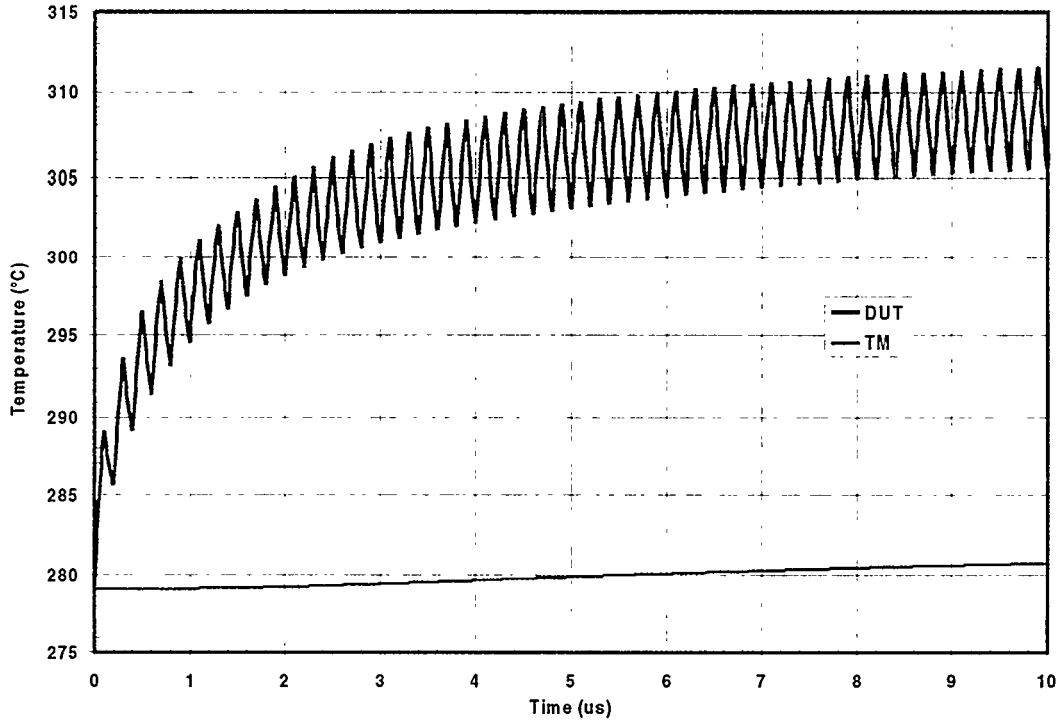

FIGURE 26. Transient response of DUT at 5 MHz.

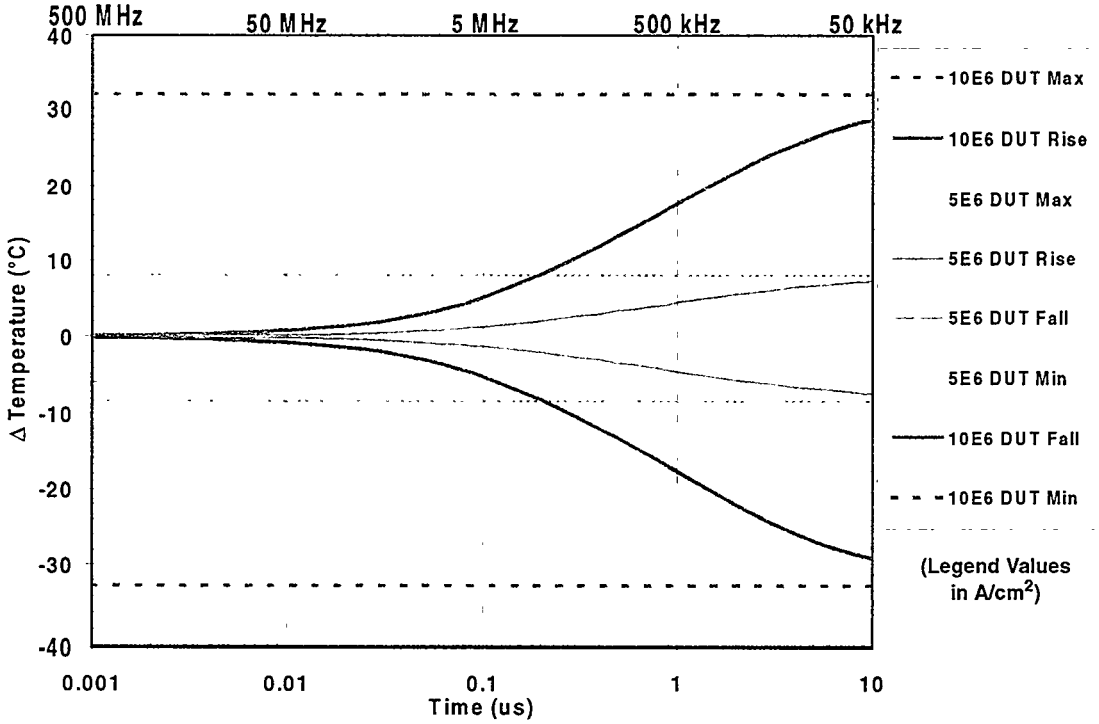

FIGURE 27. Thermal rise and fall characteristics of DUT.

The transient response of the DUT was more efficiently generated by plotting only the rising and falling characteristics of the response at different power levels. Figure 27 on page 42 shows transient responses from steady state conditions including the effect of DUT self heating. Four curves were graphed for each of the two power levels shown in Figure 27. The maximum and minimum power levels were obtained from steady state self heating models with the DUT either fully powered or not powered. The transient characteristics were obtained by first solving a a steady state self heating model to define the average temperatures throughout the model for a given average DUT power level. The DUT power level was doubled to its peak value at time zero to produce the rise time transient responses. The DUT power was set to zero at time zero to generate the fall time characteristics. Ten temperature data sets were collected for every time decade. The average temperature of the DUT was then subtracted from the data to produce a differential temperature graph. The frequencies at the top of this chart assume a 50% duty cycle waveform. For example, a 5 MHz square signal will rise for 0.1 μs and fall for 0.1 μs. A current density of 10 MA/cm^2 showed that the amplitude of the thermal transient on the DUT will be ±5°C about the average DUT temperature. This gave a peak to peak amplitude of about 10°C for the thermal transient.

Rise and fall times were calculated from the data in Figure 27. The 5 MA/cm^2 peak current signal gave a rise time of 10.48 μs and a fall time of 10.58 μs. The larger 10 MA/cm^2 peak current signal showed rise and fall times of 10.22 μs and 10.60 μs respectively. The rise time is faster than the fall time for a given signal power level since the thermal conductivity of SiO_2 increases with temperature.

The data in Figure 27 shows that the transient response of the DUT is fairly symmetrical about the average DUT temperature. At a current density of 5 MA/cm^2, the DUT temperature displayed a peak to peak temperature variation of less than 1°C at frequencies above 50 MHz. For the 10 MA/cm^2 response, the frequency must be doubled to 100 MHz to have the DUT temperature deviate by less than 1°C.

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CHAPTER 7: CONCLUSIONS

There are too many combinations of heater power levels, device base temperatures, and DUT signals to completely characterize this device by directly measuring its temperature response. Rather, simulation tools that allow for further analysis of specific test conditions have been produced and their use demonstrated. This tool development provided an understanding of the device heating and the temperature effects on its operation. This chapter examines some of the issues that could result in enhanced test structure performance.

7.1 Annealing of the Temperature Monitor Element

Since annealing was observed in these elements over the course of a short test, I recommend for long term testing that the power to the DUT and the heater be switched off at regular intervals and a new temperature monitor calibration point at a known temperature be determined. Since only the y-intercept of the calibration data changed and not the slope of the data, this should be sufficient to prevent large temperature drift errors due to annealing.

7.2 Heating of Nearby Electronics

The temperature of the nearby buffer circuitry was determined to be 28.5°C above the 100°C base temperature of the device when the device heater was powered to 5 W. If the device heater is powered to a higher level during actual use to accelerate the rate of DUT electromigration, then this will raise the temperature of the electronics. The most direct way to reduce the temperature of the buffer electronics would be to move them further from the end of the heater or to reduce the heat sink temperature. If the distance between the end of the heater and the buffer electronics were increased from 75 μm to 200 μm, then the electronics would be 21.6°C hotter than the base temperature.

Table 4 on page 46 shows the effect of model variations on the temperatures of the metal 1 layer over the heater center and the end of the buffer electronics. The buffer electronics temperature was taken at the metal 1 level in the die and at that location the heater the vertical temperature drop to the die surface was less than 0.1°C in all cases. The Normalized Average Gradient column shows the average temperature gradient between the two points normalized to the original model conditions. I varied the base temperature of the device, the thickness of the oxide layer under the heater, the thermal conductivity of the die attach, and the power applied to the heater. The rows with higher Normalized Average Gradients show where the greatest temperature difference between the peak metal 1 and the buffer electronics temperatures occurred.

Table 4.Variations in quarter section model temperatures.

Quarter Section Model Variation	Peak Metal 1 Temperature (°C)	Buffer Electronics Temperature (°C)	Normalized Average Gradient
Base Case Calculation	284.7	128.5	1.000
80°C Heat Sink Model Temperature	260.4	107.5	0.979
120°C Heat Sink Model Temperature	309.0	149.5	1.044
2X Die Attach Thermal Conductivity	280.7	125.1	0.996
Thinned Die (20 mil Si Substrate)	285.7	128.6	1.006
300 nm Heater Oxide	272.5	128.5	0.922
600 nm Heater Oxide	331.7	128.5	1.301
2.5 W Heater Power	191.1	114.0	0.494
7.5 W Heater Power	382.0	143.4	1.528
7.5 W Heater Power / 80°C Heat Sink	352.9	120.0	1.491

Decreasing the device base temperature caused the thermal conductivity of the SiO_2 to decrease slightly and allowed less heat flux directly to the substrate instead of out towards the electronics. Unfortunately this also decreased the peak temperature directly. Doubling the thermal conductivity of the die attach actually lowered the temperature gradient for the same reason as above. This shows that the die is large enough to allow heat flow through the die attach with minimal impedance. Thinning the die from 30 mils to 20 mils increased the temperature gradient due to minimization of the heat flux spreading distance in the silicon substrate. Increasing the thickness of the heater oxide to 600 nm from 360 nm insulated the heater from the substrate and allowed it to more effectively heat the area above it while not effecting the buffer electronics temperature. The 2.5 W and the 7.5 W heater power cases show that the temperature gradient is almost linearly related to heater power. The final case of 7.5 W and an 80°C base temperature shows the best way to run the device to keep the electronics cool is to lower the base temperature and boost the heater power.

I recommend that these devices be tested using a temperature controlled stage as a heat sink. This will allow fine tuning of the device thermal profile. If the base temperature is made too low, the thermal gradients along the DUT will increase. If the base temperature is too high, the buffer performance will degrade due to heating.

7.3 Thermal Gradients along the DUT and Temperature Monitor

The temperature gradient along the DUT and temperature monitor lengths was 11.6°C for the 5 W, 100°C base temperature case. The gradients are less than 1°C across the DUT width and height due to the high thermal conductivity of the aluminum and the short distances involved. The model was modified to view the effect of doubling the heater width to 30 μm. With the same heater power the DUT length gradient remained the same but the peak temperature of the DUT dropped by 42°C. The narrow heater design effectively reduces this temperature gradient since applying more power to obtain the same

temperatures with a wider heater will cause the gradient to increase. This analysis does not focus on effects of heater width on tolerances in DUT placement, however for a narrower heater the temperature gradient is much steeper across the width of the DUT and this design will be more sensitive to aberrations along this axis. Changes in DUT location or variations in layer composition or thickness will cause greater variations in temperature between different devices with a narrower heater.

The actual heater surface temperature under the DUT varied by 11.6°C over the length of the DUT. Figure 28 shows the temperatures across the heater surface. The aspect ratio

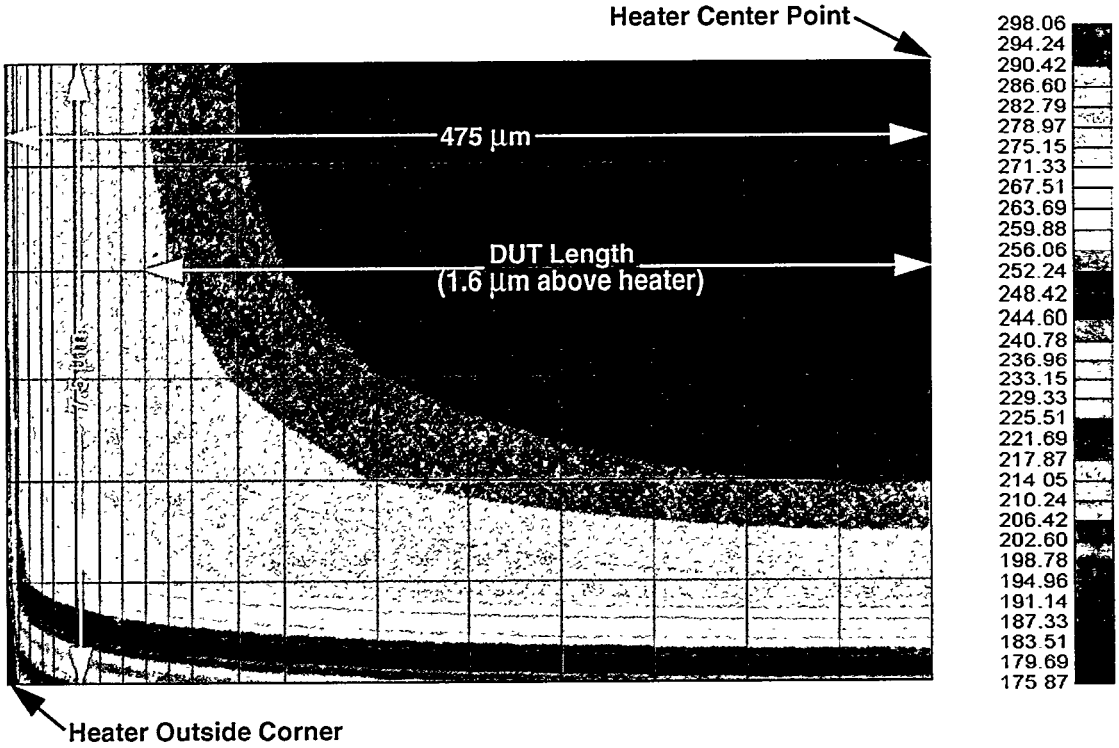

FIGURE 28. Quarter of heater surface temperature profile at 5 W of power.

of this temperature plot was altered to better show the areas of interest. The oxide thickness under the heater was increased to 600 nm from 360 nm and the temperature variation decreased to 11.1°C and the peak heater temperature increased by 52°C. The heater power was then reduced to 4 W which brought the peak heater temperature back to within 3°C of the original value and caused the temperature gradient variation across the heater to decrease to 8.5°C. I modeled the device with no oxide over the heater element to determine its contribution to cooling at the ends of the heater. This had no effect on the magnitude of the gradient across the heater surface although the peak heater temperature increased by 4.4°C. The gradient across the heater surface was due to the thin layer of oxide under the DUT allowing heat flux to diverge below the heater. I recommend that the oxide layer under the heater be kept as thick as possible to reduce the thermal gradient along the DUT. I further suggest redesigning the heater with narrower ends to change its thermal profile as

suggested by Benson[11] for an earlier version of this device. These changes will reduce the magnitude of this thermal gradient.

7.4 Effect of DUT Self Heating

The effect of DUT self heating could cause errors in the DUT lifetime since the DUT temperature increased over that measured by the temperature monitor in the device due to the driving electromigration signal. If average current densities greater than 2.5 MA/cm^2 are used, self heating can significantly contribute to the temperature of the DUT and this temperature difference must be predicted and considered during accelerated electromigration testing. DUT self heating also contributes to thermal gradients along its length. Powering the DUT with a 50% duty cycle pulsed DC waveform of 5 MA/cm^2 peak increased the temperature gradient along it by 3.3°C to 14.9°C. I recommend that thermal modeling be used to characterize the self heating effects and the gradients along the DUT length.

Another method to factor in the DUT self heating effect is to power the temperature monitor at average current densities equal to those through the DUT. If this is done every few minutes and only for a few seconds at a time, the average self heating of the DUT can be determined without causing the temperature monitor to electromigrate. Problems with stress voiding may become an issue and need to be considered if this method is employed.

7.5 Transient Thermal Response of DUT

The transient thermal response of the DUT was characterized at two current densities. Models were produced that allowed for simplified characterization of this response at other current densities. These data can now be used to determine whether an average current model or an on time current model should be used to determine the electromigration driving current. The average current model assumes that the net electromigration effect is equivalent to that produced by the average DC current through the DUT. The on time model assumes that the electromigration effect is equivalent to electromigration produced by the application of the peak current density, but only for the duration of the current pulse width. At low frequencies the on time model was used while at high frequencies where the temperature deviations along the DUT were small, an average current model was used. The DUT has a significant thermal waveform along its length at frequencies below 5 MHz. Thermal modeling seems the easiest way to characterize these transients at high frequencies. Tests can be done to simulate the rising and falling simulations in Chapter 6 by applying the same test signals as used in the simulation although it is doubtful that the high frequency transient response could be accurately captured using external test equipment.

7.6 Limitations of this Analysis

Many simplifications were made in transferring the original device to a model. Thin layers were left out and the effect of heating from the buffer circuitry itself was ignored. Temperature dependent thermal properties were neglected and constants used. The biggest

assumption made in modeling these devices was that all of the elements were perfectly formed during fabrication and that the thermal contact between layers and elements in the die was perfect. The measured data in Chapter 4 indicate significant temperature variations along the heater length suggesting that the heater is less than ideal. The correlation of the measured data in Chapter 2 with the measured data in Chapter 4 indicates that the model is performing well.

A factor only briefly considered in this analysis was the effect of thermal radiation and convection from the exposed device surfaces. Elements representing convection to a 25°C node with a heat transfer coefficient of 2.5 $mW/cm^2 \cdot °C$[12] were added to all of the exterior surfaces of the quarter section model to bound this effect. The result was a 1°C drop in temperatures across the die top surface. This effect is worst case and is probably only half as great in actual use.

Another model looked at the effects of radiation from the exposed model surfaces. Radiative elements were added as above to simulate radiation to a 25°C node. An emissivity of 0.8 was assumed for all exposed device surfaces, and a view factor of 1 was used for this simulation. The view factor is chosen to give a worst case where all of the radiant energy directly impacts the 25°C node. A 0.2°C temperature drop was observed across the die surface. This effect was negligible in light of the effects of varying die attach resistance. The depth of the DUT and the temperature monitor elements below the surface of the die also reduce the magnitude of convection and radiation effects in this analysis.

7.7 Further Work

Only one type of electromigration test structure was analyzed here. Metal 2 and combination metal 1 and metal 2 structures also require analysis. The temperature drops 45.3°C from the heater surface to the top die surface 9.5 μm away over the center of the heater. This means that structures built with elements on the metal 2 level will have different thermal characteristics than these analyzed here. A structure also exists that places the DUT on the metal 1 level and the temperature monitor 1.6 μm above it on the metal 2 level. It is likely that the severe thermal gradient from the heater to the die surface may cause greater degradation of the operation of these devices. A stress analysis of these devices would also be appropriate to determine if the high temperature gradients will significantly contribute to stress voiding. More modeling is required to characterize these devices.

The transient and self heating effects of the DUT need to be accurately measured to provide correlation with the modeled data. Some of the transient work could be done on a temperature monitor at low frequencies and then extrapolated to the higher frequencies. The steady state self heating experiments could also be performed using a temperature monitor element to mimic the DUT behavior.

A determination of the die surface emissivity at high (300°C) temperatures would also be useful in measuring die surface temperatures over a powered heater element with infrared techniques. A special micro-heater stage could be designed to heat the die without heating the microscope head.

7.8 Closing Remarks

The thermal behavior of this device is quite complex. Thorough thermal analysis of the device is required to maximize the effectiveness of this test structure. Tools now exist to perform analyses of future test structures and future work has been laid out to improve the accuracy of these tools. A summary of specific conclusions from this analysis are:

- Annealing of the device temperature monitor may cause errors in the measured temperature of the device. Since the slope of the calibration data is constant with annealing, this effect may be compensated for by determining one new point on the calibration curve. This may be done by switching off the device power and measuring the temperature monitor at a known temperature.
- Moving the buffer electronics at least 200 μm from the end of the heater will get the buffer away from the steep portion of the temperature gradient surrounding the heater. This would greatly enhance cooling of the buffer circuitry.
- Use of a temperature controlled stage when testing these devices will allow the user to achieve the best balance between heating of the buffer electronics and minimization of the temperature gradients along the DUT.
- Thermal gradients along the DUT length are mostly due to the design of the device heater. Increasing the oxide layer thickness under the heater will help reduce this effect. This may not be feasible due to individual manufacturer processing requirements. A sculpted heater with narrower ends to cause greater power dissipation at the ends of the heater would also help alleviate this problem.
- Self heating of the DUT is a significant thermal factor in this design. It may be necessary to take this effect into account during testing.
- The transient thermal response of the device may be determined through thermal modeling. This will allow the proper electromigration current model (on time or average) to be chosen to extrapolate data to at use conditions.
- Thermal modeling should be used to pre-characterize devices manufactured using previously untried vendors fabrication processes. Design changes can then be recommended before a lot with thermal design problems is manufactured.

APPENDIX A: INFRARED MICROSCOPY

A.1 Overview

The InfraScope™ infrared microscope uses a LN2 cooled 160x120 element Indium-Antimonide (InSb) focal plane array (FPA) to measure surface temperatures.[13] The focal plane array is sensitive to IR radiation in the 1.5 to 5.5 μm range. Silicon lenses allow magnifications of 1X, 5X, 10X and 1/5X to 1X (zoom), with the maximum possible resolution being 5 μm per pixel using the 10X magnification range. Temperatures from 30°C to 600°C can be measured with a maximum specified sensitivity of 0.02°C for an 80°C black body target.

The measurement system consists of a microscope head mounted on a motorized stand over a temperature controlled stage (Figure 29). A PC running a Microsoft Windows™ based software package is used to control the microscope. During measurement the device under test (DUT) is thermally and mechanically anchored to the temperature controlled stage.

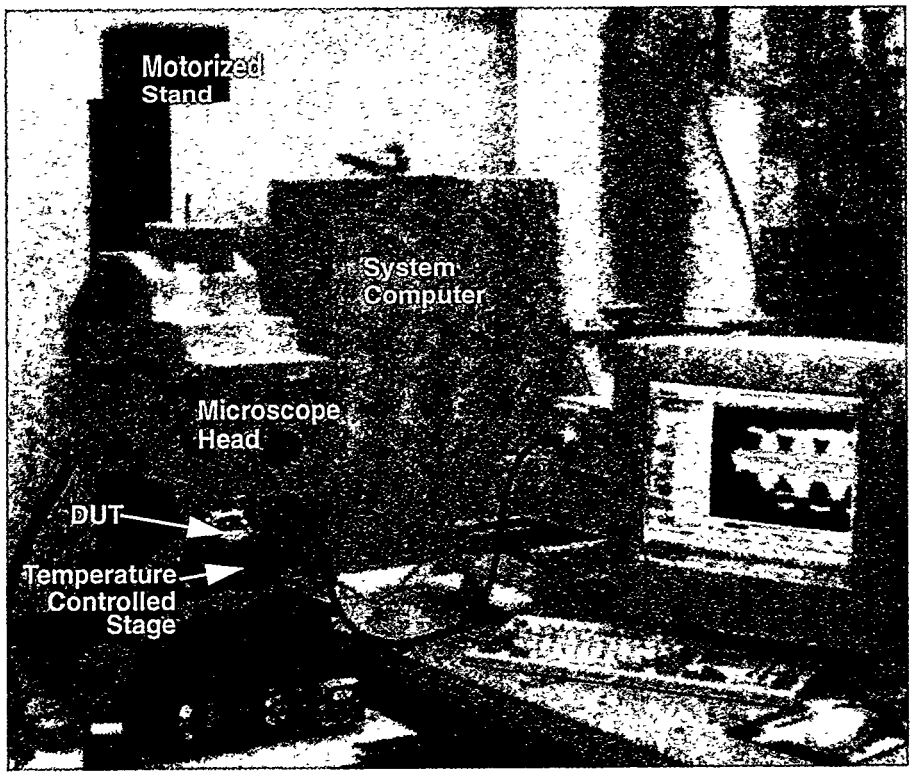

FIGURE 29. InfraScope infrared microscope.

A.2 How the Infrared Microscope Measures Temperature

The microscope relies on radiance measurements of the DUT in order to accurately measure temperatures. The system software has an internal radiance vs. temperature

calibration curve for a black body target. Calibration data are empirically determined by performing a calibration routine on the InSB detector using a black body target.

When a DUT is to be measured using the microscope, three initial radiance scans must be performed. The temperature controlled stage sets the base temperature of the DUT to between 30°C and 120°C during all radiance scans and subsequent measurements. The first two scans are used to determine the surface emissivity of the DUT, and the last one cancels out reflections (Narcissus effect) from outside sources and the cooled focal plane array. This scan is typically performed as close to the operating temperature of the DUT as possible. The system has an auto scan function that allows the user to pick for each of the three radiance scans the temperature, the temperature settling time and the number of frames to be averaged at that temperature. It is important that the DUT not move during data acquisition because the microscope performs calculations on a pixel by pixel basis.

A.2.1 Emissivity Determination

After the Infrascope has acquired the first two radiance scans (Rad1 and Rad2), it can calculate the emissivity of the DUT on a pixel by pixel basis. For each pixel, the emissivity (e) over the temperature range from Rad1 to Rad2 is given by:

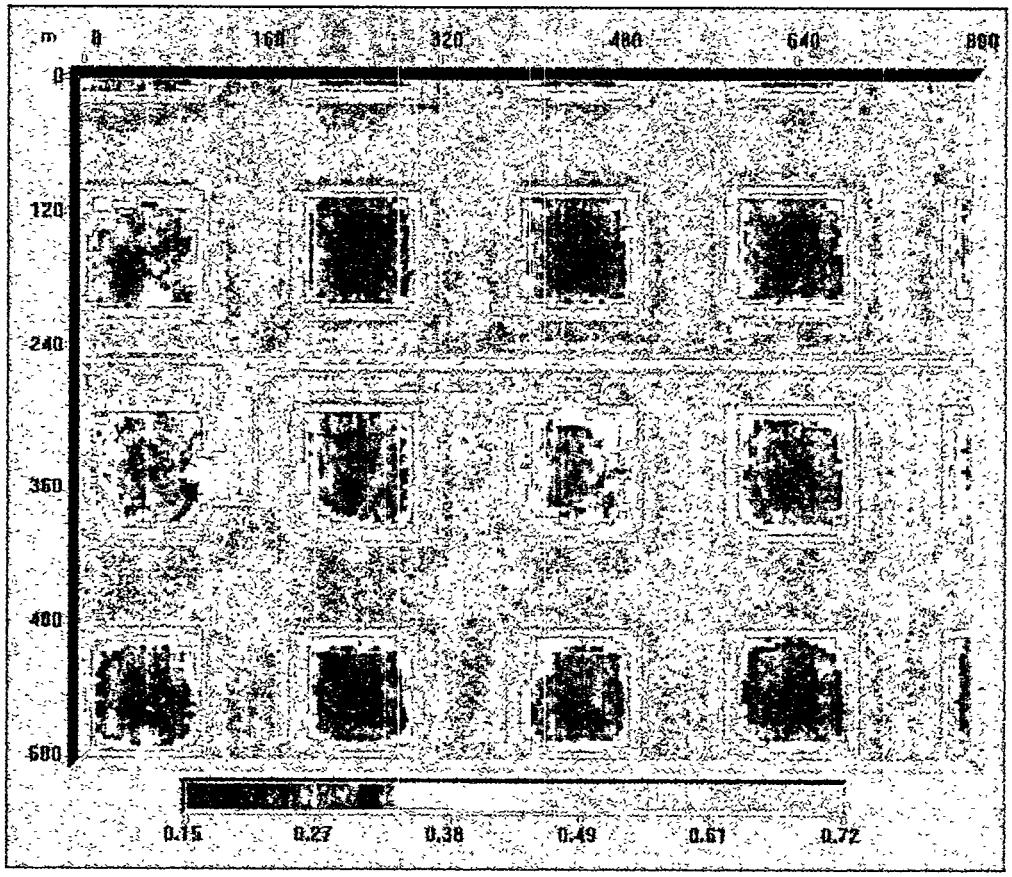

FIGURE 30. Emissivity (e) versus xy die dimensions (μm).

$$e = \frac{Rad2 - Rad1}{BBRad2 - BBRad1} \quad (2)$$

where *Rad2* is the measured pixel radiance at temperature 2, *Rad1* is the measured pixel radiance at temperature 1, *BBRad2* is the black body radiance at temperature 2 and *BBRad1* is the black body radiance at temperature 1. From this information an emissivity plot of the field of view (Figure 30) is calculated.

The emissivity calculations are performed at two temperatures that are chosen to be as close as possible to the operating temperature of the DUT. Emissivity is often temperature dependent and should be determined at as close as possible to the DUT operating temperature. The temperature of the microscope stage can only be controlled between 30°C and 120°C to stay within the temperature range of the detector and to avoid overheating the microscope head.

A.2.2 Cancellation of Narcissus Effect

The Narcissus effect varies with the temperature of the DUT. By using (3),

$$CorrRad = \frac{RadTemp - RadDUT}{e} + BBRad_{DUTBaseTemp} \quad (3)$$

the effect of reflections is cancelled out. In (3) *CorrRad* is the corrected radiance when the DUT is powered, *RadTemp* is the measured radiance when the device is powered, *RadDUT* is the reference unpowered DUT radiance, *e* is the previously calculated emissivity. $BBRad_{DUTBaseTemp}$ is the black body radiance for the unpowered DUT base temperature used during the test from the Infrascope internal calibration. Equation 3 subtracts out the unpowered DUT radiance from the powered DUT radiance, scales the result up to the black body calibration curve and then adds in the radiance effect of the DUT base temperature.

A.2.3 The Infrared Microscope Black Body Calibration Curve

The radiance response of the Infrascope for a given black body temperature is shown in Figure 31 on page 54 along with its response for a body with a 50% emissivity. These data were extracted from the instrument using a built in radiance calculator function. These curves show that the sensitivity of the detector increases with temperature. For example, a change in radiance of 100 mW/cm^2 corresponds to a smaller temperature change at a higher temperature.

A.3 High Temperature Infrared Measurement Errors

A source of error is that surface emissivity is often a temperature dependent property. The effects of a ±20% change in emissivity for a gray body with an emissivity of 50% is seen in Figure 32 on page 54. The ±20% emissivity error will cause up to a 20°C difference in temperature at 275°C. This graph also shows how the detector sensitivity is lower at lower temperatures. Since emissivity is measured at the lower temperatures using this

system, errors in the initial emissivity value determined is likely. At 125°C it only takes about a 1 mW variation in measured radiance to give a 20% emissivity error.

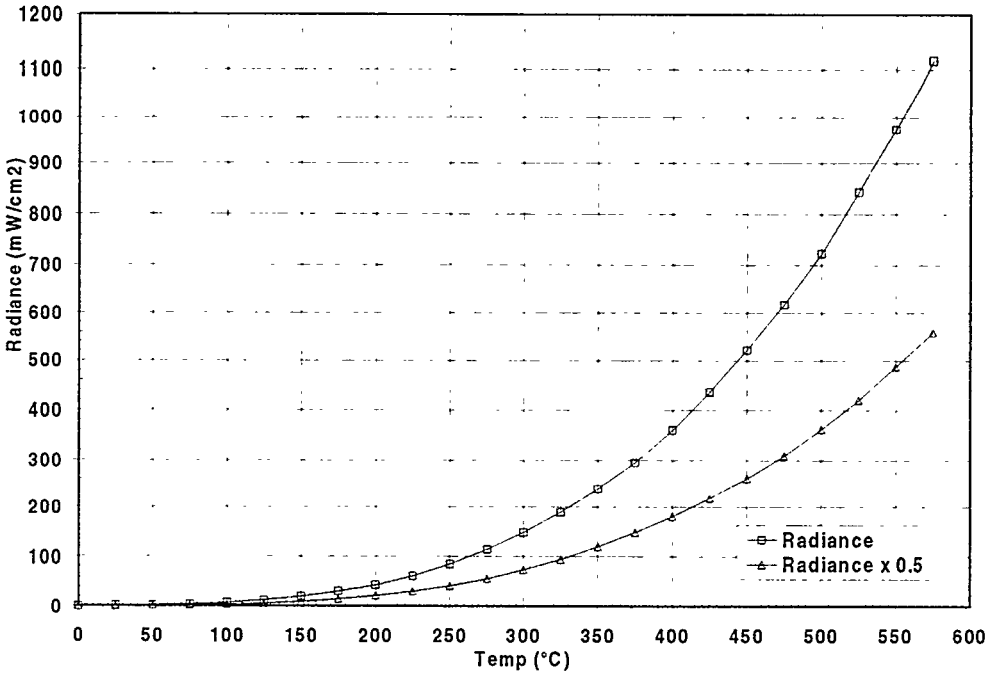

FIGURE 31. Radiance vs. temperature for a black body at 100% and 50% emissivity.

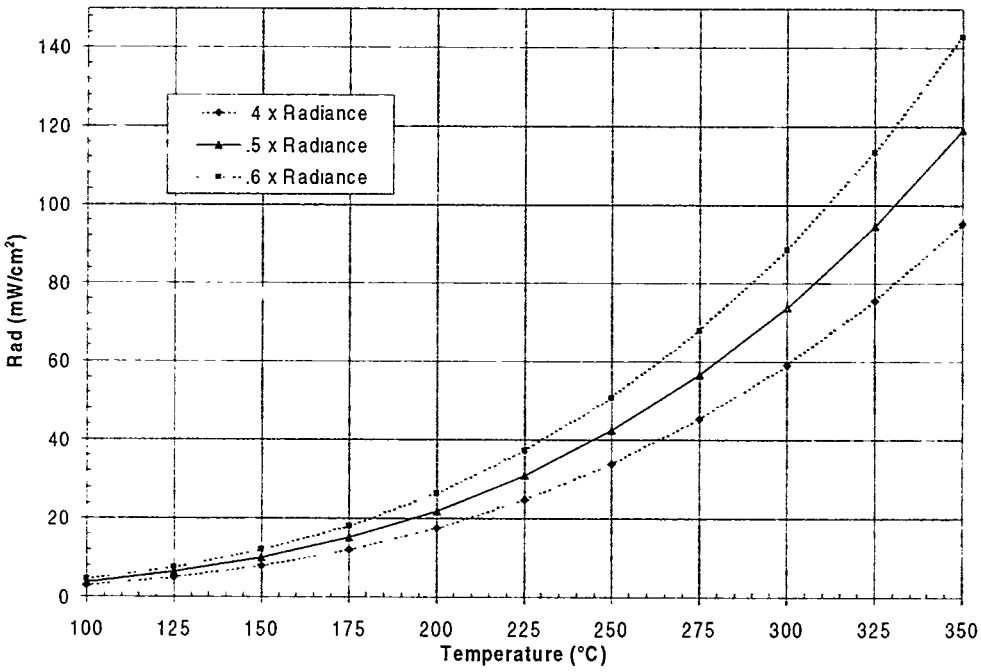

FIGURE 32. Result of ±20% emissivity variation at various temperatures.

APPENDIX B: DATA FROM INFRARED TESTS

B.1 Temperature Plots

Figures 33, 34, and 35 show temperature plots of the packaged test device not included in the main text. All plots were taken with an infrared microscope stage temperature of 100°C and 5 W of power applied to the structure heater.

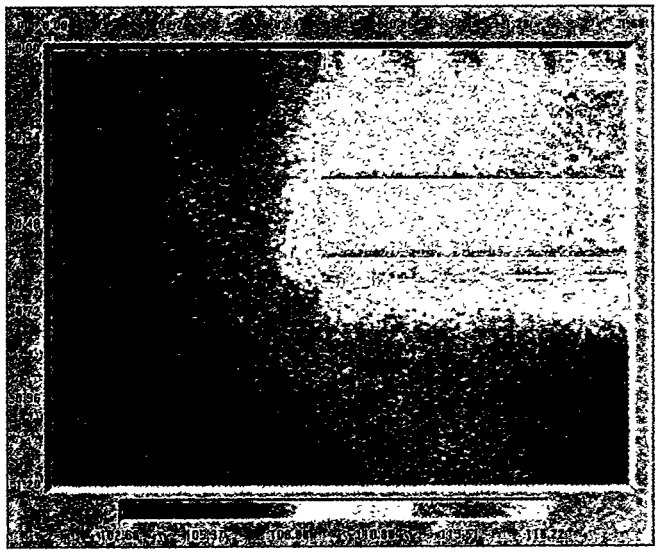

FIGURE 33. Infrared temperature versus die xy dimension (mm) for die corner area using 5X lens.

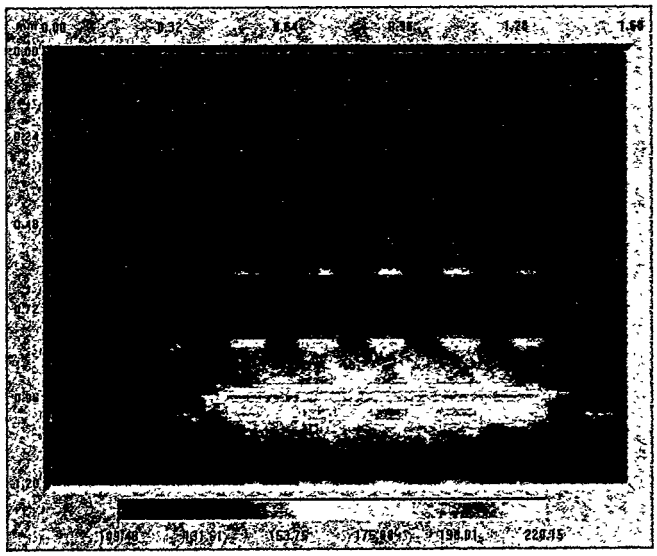

FIGURE 34. Infrared temperature versus die xy dimension (mm) for heater area using 5x lens.

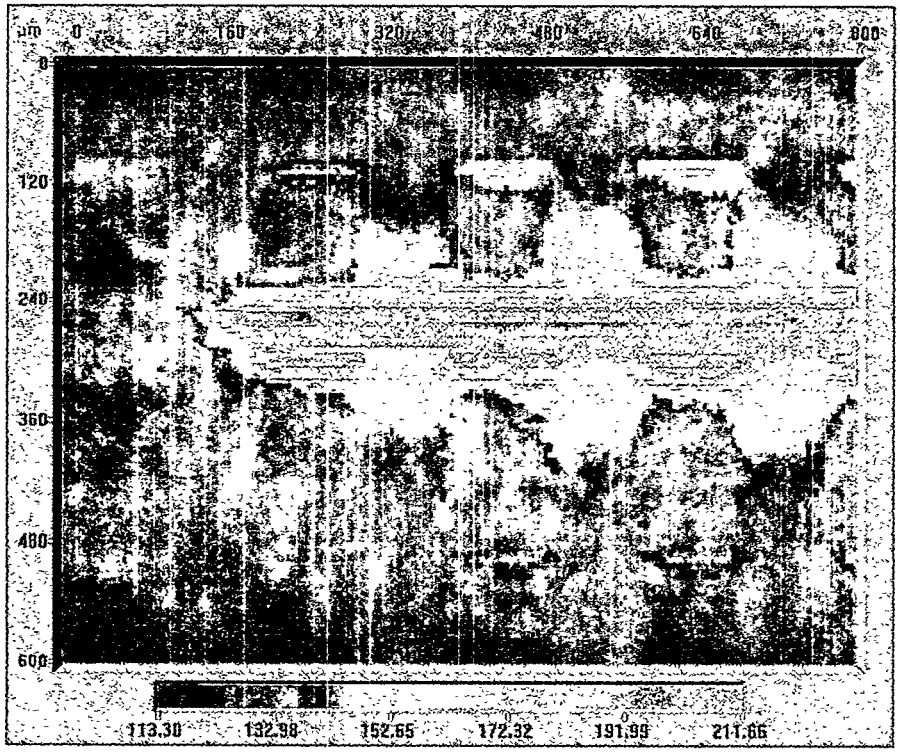

FIGURE 35. 10X temperature versus die xy dimension (µm) for end of powered heater.

B.2 Resistance Line Data

The data in Table 5 were collected during the infrared tests described in this report. All four tests were run on the same packaged part (EM1). The thermometry monitor data show the resistance of the temperature monitor lines during the radiance scans, with the heater powered, and after the heater power was turned off. The calculated temperature is based on the powered measured resistance of the temperature monitor lines.

Table 5.Infrared test data.

		Infrared Microscope Parameters					Local Thermometry Monitor					Remote Thermometry Monitor				
Filename	Device	Lens Mag	Temperature Range (°C)	TRad1 (°C)	TRad2 (°C)	TDUT (°C)	TRad1 (ohms)	TRad2 (ohms)	TPowered (ohms)	Calc. T (°C)	Post Test TRad1 (ohms)	TRad1 (ohms)	TRad2 (ohms)	TPowered (ohms)	Calc. T (°C)	Post Test TRad1 (ohms)
EM1k.job	EM1	1X	30-200	100	110	100	117.3	120.2	170.1	279.29	117.3	120.11	123	125.18	117.38	120.11
EM1l.job	EM1	5X	30-200	100	110	100	117.3	120.2	170.1	279.29	117.3	120.11	123	125.18	117.38	120.11
EM1m.job	EM1	5X	30-200	100	110	100	117.3	120.2	170.1	279.29	117.3	120.11	123	125.18	117.38	120.11
EM1n.job	EM1	10X	30-200	100	110	100	117.3	120.2	170.1	279.29	117.3	120.11	123	125.18	117.38	120.11

APPENDIX C: THERMAL MODELING SOFTWARE CODE VALIDATION

C.1 The Thermal Modeling Software

Thermal modeling is performed using the TAS (Thermal Analysis System) modeling package from Harvard Thermal Inc. This software uses a finite difference method to solve the necessary differential equations. In order to verify the proper use of the modeling software, several example problems were calculated by hand and then compared to modeled results. Originally it was thought that IR photography could verify the models, but thick top layers of SiO_2 in this particular device due to its fabrication in a 5 layer metal process prevent accurate measurements of the actual heater temperature. Several comparisons between analytical and modeled problems are performed here in order to validate the modeling software and model mesh size.

C.2 Finite Difference Calculations

The TAS software calculates all temperatures in a model using the finite difference method. All model elements are converted into effective resistances and capacitances.[14] In an electrical analogy, temperature is analogous to voltage and heat flux to current. The model nodes (corners of bricks and plates) are where the temperatures are calculated and also the connecting points for the calculated resistors and capacitors. Model bricks are 3D material model elements, and model plates are 2D material model elements. The software uses only node resistances when calculating steady state solutions and both resistances and capacitances when calculating transient solutions. For brick elements where all of the internal angles are 90°, 12 RC elements are calculated, along the edges of the brick. For other six sided shapes, 28 RC elements are calculated by using all other possible resistors in the brick as shown in Figure 36. For this reason, when non-rectangular bricks are used in a model, calculation time is lengthened and greater accuracy is obtained with the same mesh size than if rectangular bricks are used in a similar model.

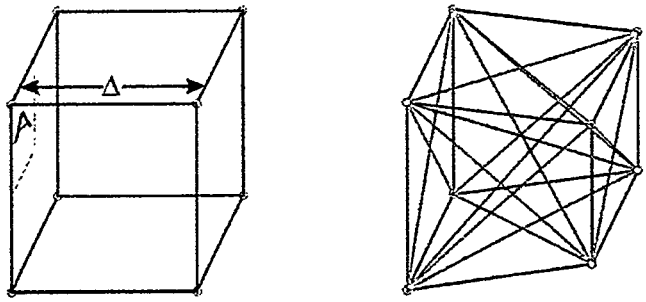

FIGURE 36. Comparison of RC elements for rectangular and non-rectangular bricks.

Each resistance in the model is calculated using:

$$R = \frac{\Delta}{K \cdot A} \tag{4}$$

where Δ is the distance between the nodes, K is the thermal conductivity, and A is the cross sectional area of the path between the nodes. The nodal area A is calculated by taking the product of half the width of the element normal to the heat flow in both directions as shown in Figure 36.

The software uses a steady state analysis routine to calculate the temperature at each node using

$$T_i = T_{iold} \cdot (1 - damp) + damp \cdot \frac{\sum\left(\frac{T_{i-1}}{R_{i-1}}\right) + Q_i}{\sum\left(\frac{1}{R_{(i-1)}}\right)} \quad \textbf{(5)}$$

where T_i is the current temperature at node i, T_{iold} is the temperature at node i during the last iteration, *damp* is a damping factor entered by the user at run time to balance stability of the solution against speed of the model solution, T_{i-1} is the temperature at each adjacent node, R_{i-1} is the thermal resistance to each adjacent node and Q_i is the heat input to node i if any is present. The maximum temperature change at any model node is saved during each complete iteration (a calculation at every node). If it is more than the maximum value specified by the user (typically 0.001 °C or less) then another complete iteration is performed. If not, the percent heat balance is then examined using (6). A maximum percent heat balance is input by the user and used as a second basis for solution completion.

$$Percent\ Balance = \left(\frac{(Q_{model\ input} - Q_{to\ boundary\ nodes})}{Q_{model\ input}}\right) \bullet 100 \quad \textbf{(6)}$$

Nodal heat capacitances are generated as the product of the material density (ρ), the material heat capacity (C_p), and the nodal volume (V). The nodal volume is calculated similar to the area A above with the distance between the nodes multiplied to give a volume. Equation 7 provides transient solutions to the model where Δt is the time step used to solve the model. The time step for each model iteration is calculated as the product of the parallel combination of all resistances attached to a node times the capacitance associated with that node. The smallest time step calculated in the model is used for the time step. A user input allows this value to be scaled by a value less than 1 to provide a converging solution.

$$T_i = \frac{\left(\sum\left(\frac{T_{(i+1)}}{R_{(i+1)}}\right) + Qi\right) \times \Delta t}{\rho C_p V} + T_{old} \quad \textbf{(7)}$$

C.3 Example Problems

C.3.1 Example: A 2D Plate with One Heated Edge

Consider a finite 2 dimensional square plate of SiO_2, with three edges fixed at 0°C and the fourth fixed at 100°C. A Fourier analysis of this plate[12] yields the analytical solution shown in (8) below.

$$T(x,y) = \frac{4T_0}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \frac{\sinh\left(\frac{n\pi y}{L}\right)}{\sinh\left(\frac{n\pi H}{L}\right)} \sin\left(\frac{n\pi x}{L}\right) \quad (8)$$

In (8) T_0 is the 100°C fourth edge temperature on the plate, L and H are the x and y dimension size of the plate respectively, and x and y are a location on the plate with the maximum y value corresponding to the 100°C edge of the plate. A temperature map of this plate carried out to 99 Fourier terms is shown in Figure 37. This map was calculated using a matrix of 33 by 33 equally spaced nodes to represent the plate.

A TAS model of the same structure based on the same node structure is shown in Figure 38 on page 60. Figure 37 shows that even with 99 terms, the Fourier analysis

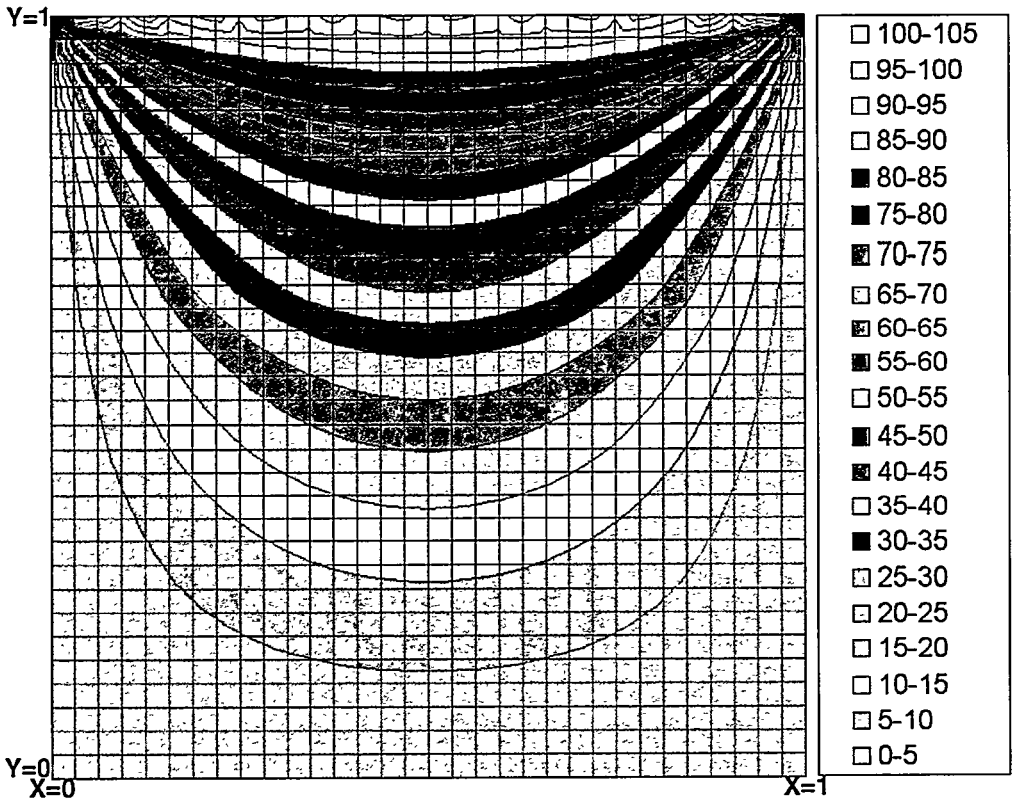

FIGURE 37. 99 term Fourier analysis of plate showing temperatures (°C).

includes the slight effect of uncancelled harmonics at the top heated edge. The finite-difference model does not show these abnormalities. Some specific point temperature values are calculated in Table 6. These values show that as the mesh in the finite difference model is made more dense, the calculated temperatures on the plate converge towards those calculated by the Fourier analysis, and that the error in the model can be reduced to an acceptable level by using a dense enough mesh for the plate.

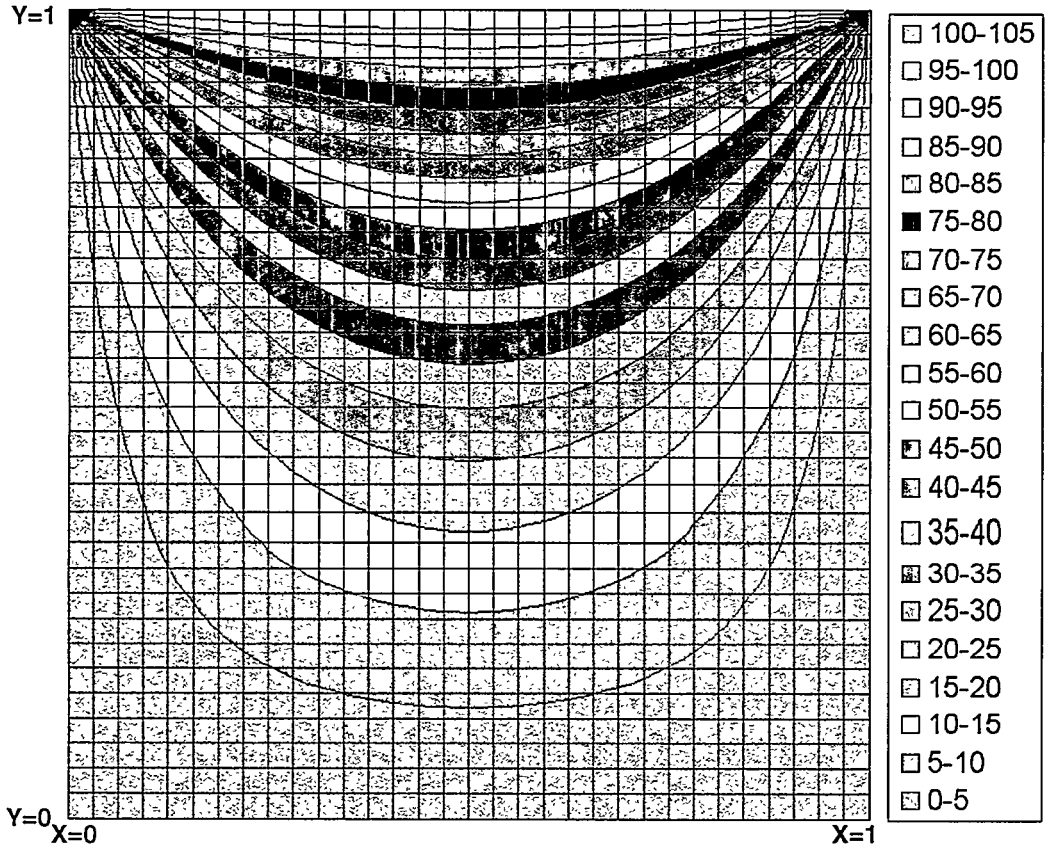

FIGURE 38. TAS model of 2D plate problem temperatures (°C).

Table 6.Specific temperature (°C) values from Example 1.

X,Y Location (X = 1 is Right Edge, Y=1 is Top)	Fourier Analysis (99 terms)	4x4 Model Mesh	8x8 Model Mesh	16x16 Model Mesh	32x32 Model Mesh
1/2, 1	100.3215	100.0000	100.0000	100.0000	100.0000
1/4, 1/4	6.7972	7.1429	6.8947	6.8221	6.8034
1/2, 1/2	25.0000	25.0000	25.0000	25.0000	25.0000
1/2, 3/4	54.0529	52.6786	53.6079	53.9325	54.0222

Table 6.Specific temperature (°C) values from Example 1.

X,Y Location (X = 1 is Right Edge, Y=1 is Top)	Fourier Analysis (99 terms)	4x4 Model Mesh	8x8 Model Mesh	16x16 Model Mesh	32x32 Model Mesh
1/2, 1/4	9.5414	9.8214	9.6273	9.5642	9.5472
1/4, 3/4	43.2028	42.8571	43.1053	43.1779	43.1966
1/4, 1/2	18.2028	18.7500	18.3824	18.2516	18.2152
Max Deviation from Fourier Example	------	4.84%	1.41%	0.36%	0.09%

C.3.2 Example: Transient Heat Flux at the edge of a 3D Solid

Since part of this work involved modeling of transient temperature effects due to self-heating of the device from the built in oscillator, it was necessary to evaluate the accuracy of the TAS software when used in this mode. For this example, a semi-infinite block of SiO_2 was considered. The block was infinite in all directions and had one surface. At t=0 a heat flux was applied to this surface. For simplicity, it was decided the blocks initial temperature would be 0 °C at $t < 0$, and that the applied heat flux to the entire one surface would be 1W/cm^2. An exact analysis of this problem[15] yields (9) for the temperature at the block surface as a function of time.

$$T(t) = \frac{2F_0}{K}\left(\frac{\kappa t}{\pi}\right)^{1/2} \qquad (9)$$

In (9), $T(t)$ is the temperature at the surface of the block, F_0 refers to the heat flux into the block in W/cm^2, K is the thermal conductivity of the block (0.015 W/cm-°C for SiO_2), κ is the thermal diffusivity of the material (0.009155 cm^2/°C), and t is the time in seconds.

The models used to simulate this problem in TAS are shown in Figure 39 on page 62. The first model is simply a 1 cm x 1 cm x 8 cm block with the heat input on the right end. The second and third models have the same geometry and heat load (1W), but each has a greater density mesh where the heat flux is most rapidly changing. Since no radiative or convective elements are contained in this model, the models simulate a 8 cm thick infinite plate in two dimensions. The results from both these different geometries and from the analytical calculations are shown in Figure 40 on page 62. It is apparent that the 8x1x1a model deviates far from the calculated values. The 8x1x1b model and the 8x1x1c model are much closer to the expected values due to the high concentration of nodes where the heat flux is highest. TAS does not use the user's time steps as a basis for it's calculation times. Instead it calculates an RC time based on the node spacing and material. This means that greater accuracy is obtained by using a denser mesh.

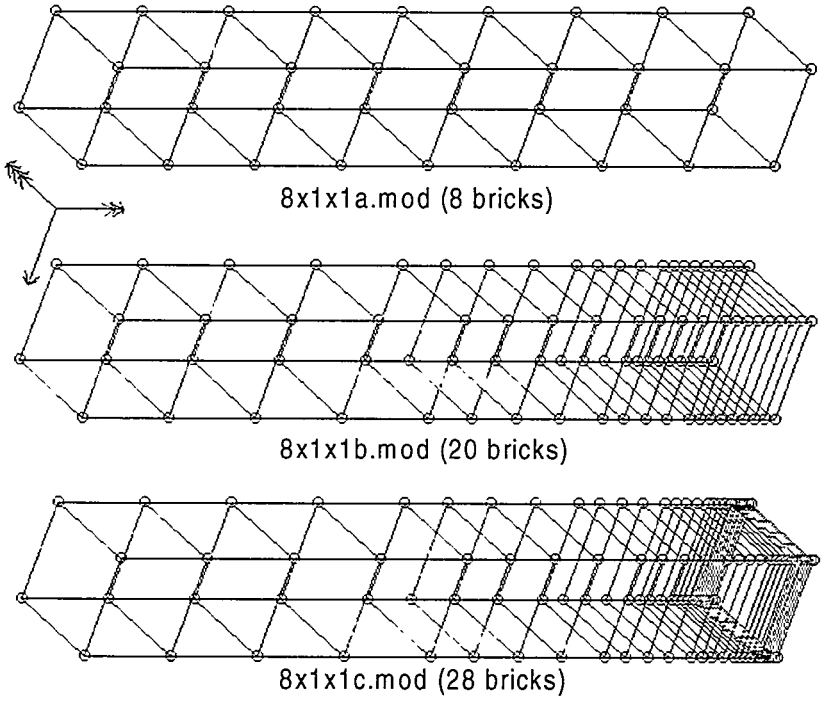

FIGURE 39. TAS models for transient example.

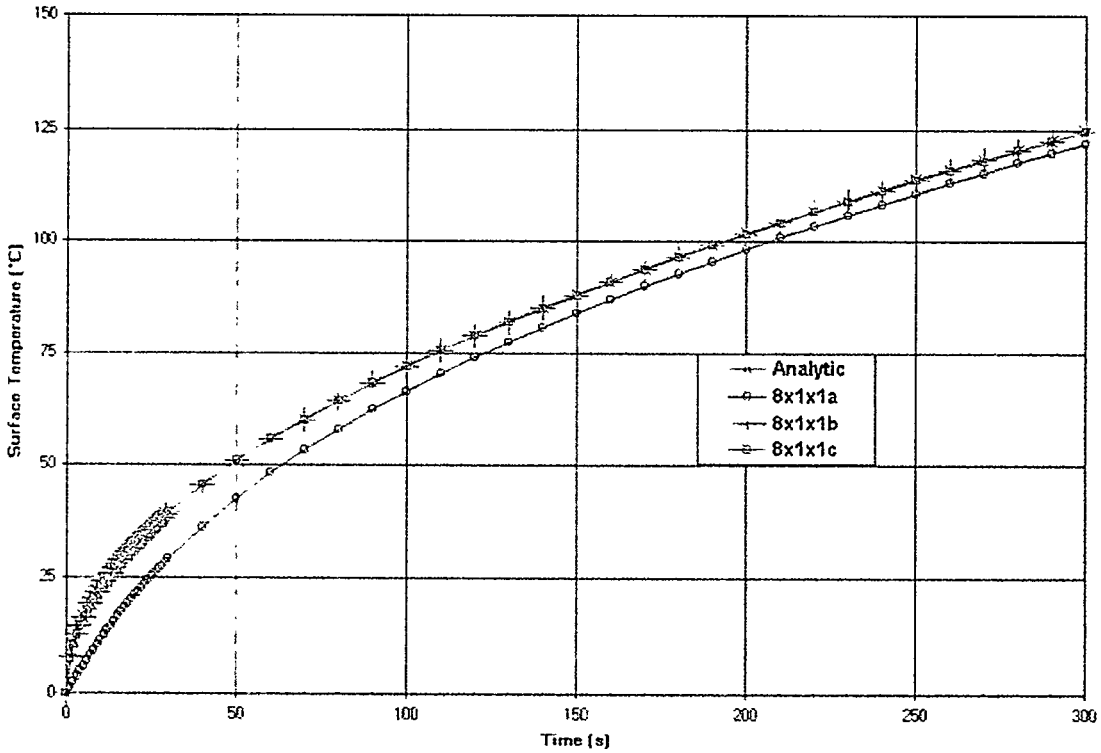

FIGURE 40. Transient heating comparisons.

C.3.3 Example: 1D Fin with Convection

For this example a silicon fin 1 cm long and 0.05 cm thick and wide was used. The base temperature of this fin was set at 100°C and a constant thermal conductivity of 1.15 W/cm-°C was used. The heat transfer coefficient was assumed to be 2.5 mW/cm^2, and the ambient temperature 25°C. The temperature along the length of the fin is governed by (10).[12] In (10), T_x is the temperature along the fin with $x = 0$ at the base of the fin. T_a is the ambient temperature being convected to, and T_b is the temperature at the base of the fin. The length of the fin in the x direction is L, the width and the thickness of the fin are w and t respectively. The thermal conductivity of the fin is given by k and the heat transfer coefficient for the convection is h.

$$T_x = T_a + (T_b - T_a) \cdot \frac{\cosh\left(\frac{L-x}{\sqrt{\frac{kwt}{2h(w+t)}}}\right) + \sqrt{\frac{hwt}{2k(w+t)}} \cdot \sinh\left(\frac{L-x}{\sqrt{\frac{kwt}{2h(w+t)}}}\right)}{\cosh\left(\frac{L}{\sqrt{\frac{kwt}{2h(w+t)}}}\right) + \sqrt{\frac{hwt}{2k(w+t)}} \cdot \sinh\left(\frac{L}{\sqrt{\frac{kwt}{2h(w+t)}}}\right)} \quad (10)$$

A model of the fin was also constructed using the TAS software and is shown in Figure 41.

Temperatures along the center axis of the fin model were plotted and compared to results from (10) in Figure 42 on page 64. The model data deviated less than 0.053% in any instance, from the 16 calculated points along the fin.

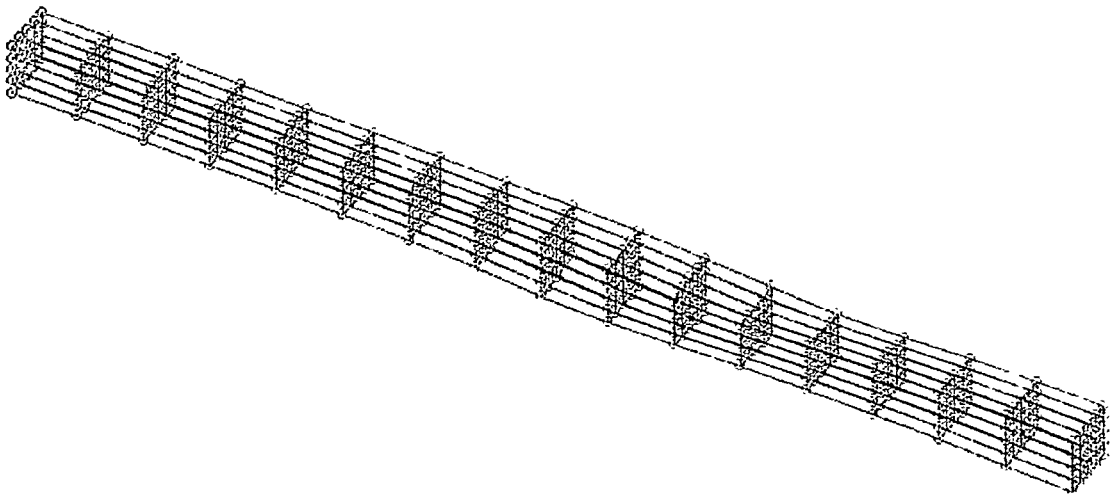

FIGURE 41. TAS model of silicon fin.

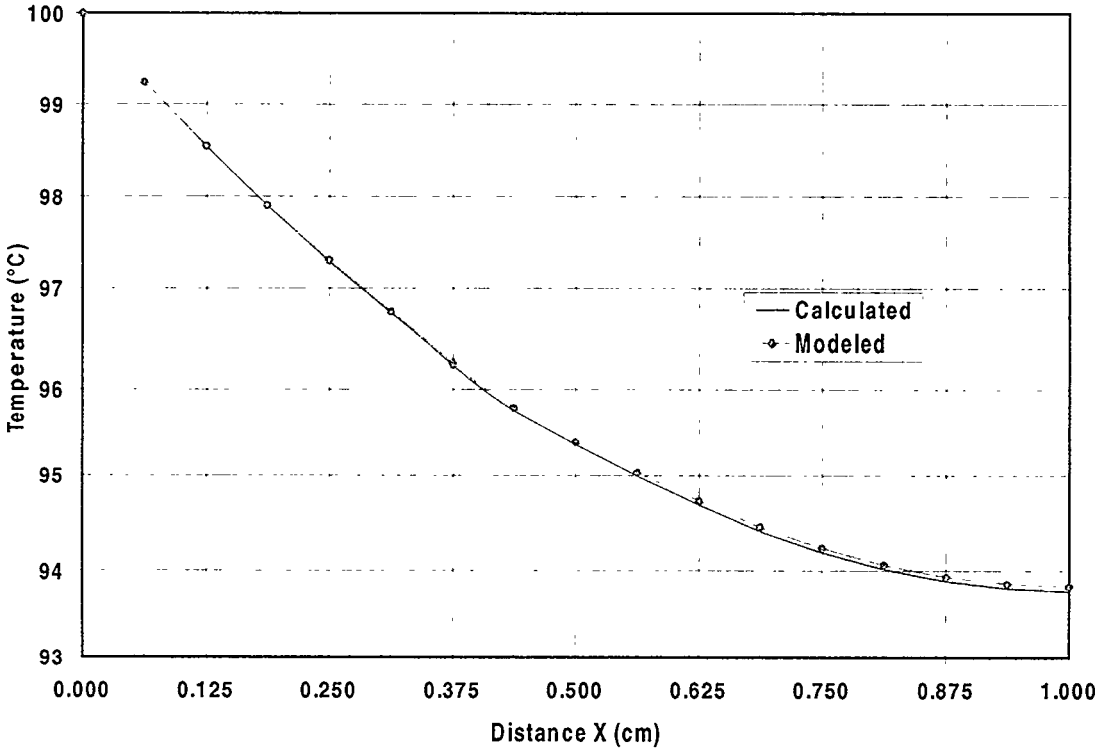

FIGURE 42. Temperature profile along length of Si fin.

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