IDENTIFICATION OF DEFECTS IN SOI WAFERS

SAND--89-2696C
DE90 006020

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Defects and metal contamination in device areas of silicon integrated circuits (IC) can limit yield in IC fabrication. We describe an electrochemical method for identification of structural defects and metal contamination in low-doped n-type silicon (dopant concentration of about $10^{15}/cm^3$). Anodic etching in 5 wt.% hydrofluoric acid produces crystallographic etch pits which correlate with both structural and impurity defects. Etch pit densities also correlate well with reported values of defect densities calculated from gate oxide breakdown (1). We show that the method is particularly suited to defect delineation in thin-film silicon-on-insulator (SOI) wafers. The technique is superior to chemical decoration etches and to transmission electron microscopy for defect delineation in thin-film SOI wafers since it does not etch bulk silicon and it has a detection limit much lower than 10^4-10^5 defects/cm^2. We used the procedure to demonstrate how defect levels are strongly affected by the process parameters used to synthesize Zone Melt Recrystallization (ZMR) and Separation by IMplanted OXygen (SIMOX) wafers.

INTRODUCTION

Defects in device areas of silicon integrated circuits (IC) can limit performance and yield in IC fabrication. Defects in single-crystal silicon are generically classified into two groups: grown-in defects (e.g., interstitials, vacancies, and other point defects), and process-induced defects, (e.g., dislocations and stacking faults). In silicon-on-insulator (SOI) fabrication, defects such as threading dislocations, precipitates, and subboundaries are generated by high fluence, high energy implantation (Separation by IMplanted OXygen-SIMOX) or by crystallization (Zone Melt Recrystallization-ZMR).

Active IC device regions must also be clean, since metal impurities such as iron, copper, and nickel impair SiO_2 integrity (1-4), reduce carrier lifetime (2), and contribute to high device leakage currents (3). For example, nickel and copper precipitate metal silicides at the surface that can nucleate stacking faults or dislocations during heat treatment, thereby damaging oxide integrity (2). Iron diffuses and dissolves in bulk silicon during heat treatment and contributes to a decrease in carrier lifetime (2). Iron is reported to be the most harmful of these three impurities (1,3). Drastic degradation of generation lifetime has been observed for surface iron concentrations ($[Fe]_{surf}$) above $1x10^{12}$ atoms/cm^2, while degradation of surface generation velocity and SiO_2 dielectric breakdown strength have been observed for $[Fe]_{surf}$ above $5x10^{12}$ atoms/cm^2 and $1x10^{13}$ atoms/cm^2, respectively (1).

Detection and identification of defects in thin-film ($\leq$500 nm) SOI wafers can be difficult. Standard chemical decorative etchants (e.g., Wright, Secco, Sirtl) are often unacceptable because they remove bulk silicon at rapid rates (ca. 1000 nm/min). As a result, the chemically-etched silicon films are too thin to develop detectable etch pits (5). Transmission electron microscopy (TEM) is also used; however, sample preparation is time-consuming, the sample can be non-representative of the entire SOI wafer, and the method has a lower limit of detection of 10^4-10^5 defects/cm^2.

We describe here the development of a simple electrochemical method for the decoration and identification of defects and metal contamination in single crystal n-type silicon (6). We also show that the method is particularly suited to the rapid assessment of SOI material quality (7). Further work will include expanding the utility of the technique to thin-film silicon-on-sapphire (SOS) material.

EXPERIMENTAL

The procedure is applicable to (100), n-type silicon with a donor atom concentration of about 10^{15}/cm^3 (3-4 ohm-cm). For silicon substrate wafers, we make ohmic contact to the back of the wafer by pressing a platinum disk against the aluminized back surface of the wafer. In contrast, we make ohmic contact to the top layer of SOI

samples by attaching an indium solder preform to a wafer die following removal of surface silicon dioxide with a buffered oxide etchant. Figure 1 shows the configuration of the die with the preform attached. Front-side contact for SOI samples is used to prevent effects of oxide breakdown on defect delineation that would be expected with back-side contact. Electrochemical etching is performed for 10-30 minutes in 5 wt.% hydrofluoric acid (HF) utilizing a three-electrode configuration with the silicon controlled at +3 volts vs. a Cu/CuF_2 reference electrode. The potential of the Cu/CuF_2 electrode is -0.026 volts vs. a Ag/AgCl reference electrode (when measured in 2 wt.% HF). We typically etch a 40 cm^2 circular area of n-type substrate wafers and an 0.07 cm^2 circular area of SOI samples. Optical microscopy at 50X-1000X magnification is used to observe defects and determine their areal density.

RESULTS

A. Substrate Wafers

Fourier transform infrared spectroscopy (FTIR) measurements of n^- epitaxial silicon on an n^+ substrate before and after electrochemical etching show that this procedure does not remove bulk silicon. It is this property of the electrochemical etch that makes it ideal for thin-film SOI wafers. In Fig. 2, we show that there is no evidence of bulk silicon etching for electrochemical etch times up to 30 minutes. Chemical etchants such as the Wright (8), Secco (9), or Sirtl (10) defect decoration etchants remove bulk silicon at rates as high as 1000 nm/min. This is unacceptable for thin-film SOI since the overlying silicon layer may be as thin as 100 nm.

Electron microscopy of electrochemically-etched silicon showed that crystallographic channels are etched into the silicon. These etch pits, 2-50 μm in size, are formed in discrete regions of high electrochemical activity and are never observed at densities greater than $10^3/cm^2$ on unprocessed Si wafers. In contrast, we have observed localized pit densities as high as $10^7/cm^2$ on contaminated wafers that had been oxidized in steam at 1000^oC. Spreading resistance profiles indicate that dopant atoms are not selectively etched by this procedure.

An optical micrograph of an electrochemically-etched wafer is shown in Figure 3. The wafer was oxidized in O_2 at 1000^oC for 15 minutes prior to electrochemical etching. This resulted in the growth of a 22 nm thick thermal oxide.

The electrochemical etch was followed by a 10 sec Wright etch to enhance the visibility of the etch pits. The Wright etch did not delineate additional etch pits. Crystallographic etch pits are observed at both ends of an oxidation-induced stacking fault, i.e., at locations where partial dislocations intersect the wafer surface. This indicates that structural defects are revealed by the method. Etch pits are also observed in areas where there are no apparent structural defects.

To investigate the applicability of our method for the detection of iron contamination, we introduced low levels of iron doping onto the surfaces of 3-4 ohm-cm n-type silicon by immersion in boiling nitric acid solutions containing various concentrations of $Fe(NO_3)_3$ (1). The wafers were oxidized in O_2 at 1000^oC for 15 minutes prior to electrochemical etching. For all iron-contaminated wafers, we contaminated only one half of the wafer. The other half was protected by a thick thermal oxide. Figure 4 shows a photograph of a wafer contaminated with a 5000 ppm iron solution, oxidized, and then electrochemically etched. The iron-contaminated half has electrochemical etch pit densities as high as $10^7/cm^2$, causing the reflectance of the surface to be much lower than the uncontaminated half (densities about $10^3/cm^2$).

Figure 5 shows the relationship between etch pit density and the level of iron contamination. The relationship between surface iron concentration on silicon wafers and the iron concentration in the nitric acid solution used to contaminate the wafers was previously determined by atomic absorption spectroscopy (1), and has been incorporated into Figure 5. Also shown is the data of Takizawa et al. (1) on the correlation between SiO_2 defect density and $[Fe]_{surf}$. They calculated SiO_2 defect density from the dependence of the yield (breakdown field > 8 MV/cm) on the gate area (0.25 and 0.09 cm^2). As evident in Figure 5, both etch pit density and SiO_2 defect density increase rapidly with increasing surface iron concentration. This correlation suggests that defect densities determined by the electrochemical etch can be related to oxide electrical quality. We are currently expanding the scope of this part of the work to include copper and nickel as contaminants and to further examine the correlation between defect density and oxide integrity.

B. SOI Wafers

We have used this method to delineate defects in SIMOX and ZMR wafers. For singly-implanted, high dose, high energy SIMOX wafers, electrochemical etch pit densities can reach levels as high as $10^8/cm^2$. Using new techniques such as multiple implant/multiple anneal and substrate heating, etch pit densities can be as low as 10^2-$10^3/cm^2$, similar to densities found in virgin n^- substrates.

The optical micrograph in Fig. 6 shows electrochemically decorated defects in a SIMOX wafer produced by multiple implantation at 200 kV, with a total dose of $1.8x10^{18}$ O^+/cm^2, and at a substrate temperature of 610^oC. Following each implantation step, the sample was annealed at high temperature in a nitrogen/oxygen atmosphere. In this sample, etch pit densities ranged from 10^3-$10^5/cm^2$. In ZMR samples (produced by the graphite strip heater method and consisting of a 400 nm silicon layer over a 1200 nm silicon dioxide layer), electrochemical etching delineated subboundaries along the (100) orientation, while crystallographic etch pits associated with the sub-boundaries were parallel with the (110) direction.

We also used the electrochemical etch procedure to demonstrate how defect levels are strongly affected by the process parameters used to synthesize SIMOX wafers. For example, a SIMOX wafer produced by implantation of $1.8x10^{18}$ O^+/cm^2 at 150 kV, with a substrate temperature of 550^oC, had etch pit densities ranging from 10^3-$10^5/cm^2$. In comparison, a SIMOX wafer produced by implantation of $1.8x10^{18}$ O^+/cm^2 at 200 kV, with a substrate temperature of 700^oC, had etch pit densities of only 10^2-$10^3/cm^2$. In both cases, the samples were annealed at 1300^oC for 6 hours, and the resulting SOI structure consisted of a 220 nm silicon device layer over a 380 nm silicon dioxide insulating layer.

CONCLUSIONS

The electrochemical etch technique is superior to chemical etchants and to TEM for defect delineation in thin-film SOI wafers because it does not etch bulk silicon and it has a detection limit much lower than 10^4-$10^5/cm^2$. The method has the additional advantages of being rapid,

relatively simple, and inexpensive, requiring only basic electrochemical cells and instrumentation.

ACKNOWLEDGMENTS

The authors thank B. Cordts of Ibis Corp., Danvers, MA, for supplying some of the SIMOX wafers used in this study, M. J. Carr and N. A. Creager for electron microscopy, and K. S. Schubert and J. H. Perry for performing the oxidations. Spreading resistance profilimetry was performed at Solecon Laboratories, San Jose, CA. This work was performed at Sandia National Laboratories supported by the U.S. Department of Energy under contract number DE-AC04-76DP00789.

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DISCLAIMER

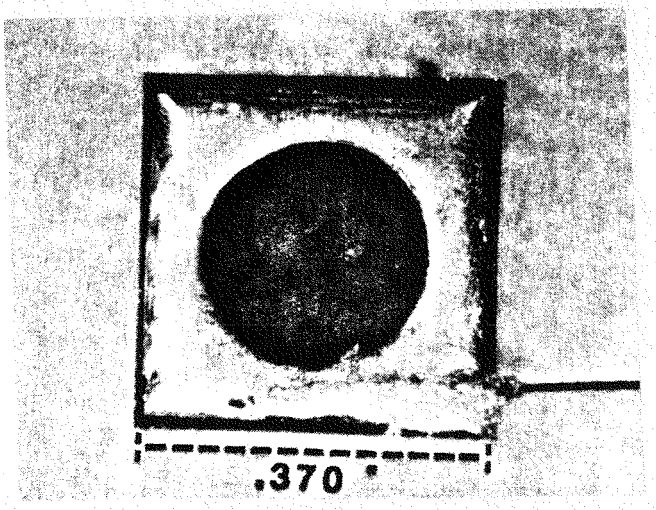

Figure 1. Ohmic contact to silicon device layer of SOI sample made with an indium solder preform. Platinum wire attached to the solder is used for electrical connection to the potentiostat.

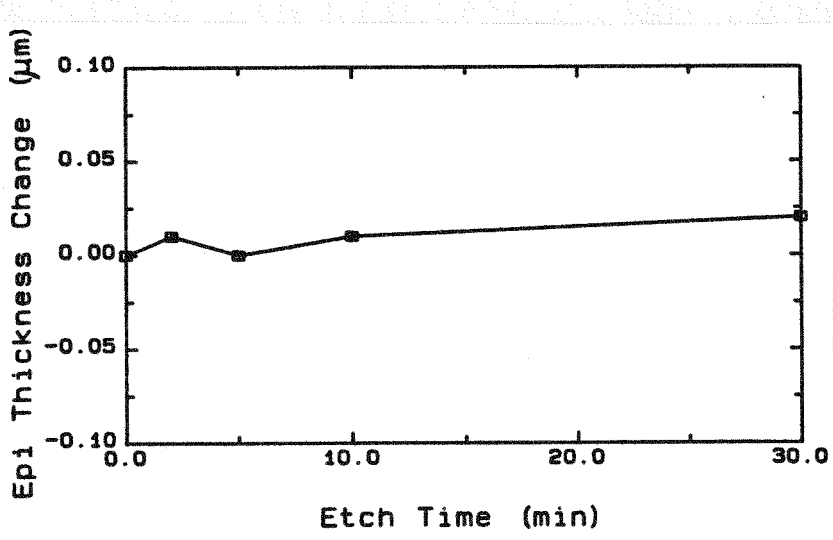

Figure 2. Change in thickness of n^-/n^+ epitaxial layer (as determined by FTIR) as a function of electrochemical etch time. 3 volts vs. Cu/CuF_2 reference electrode, 5 wt.% HF.

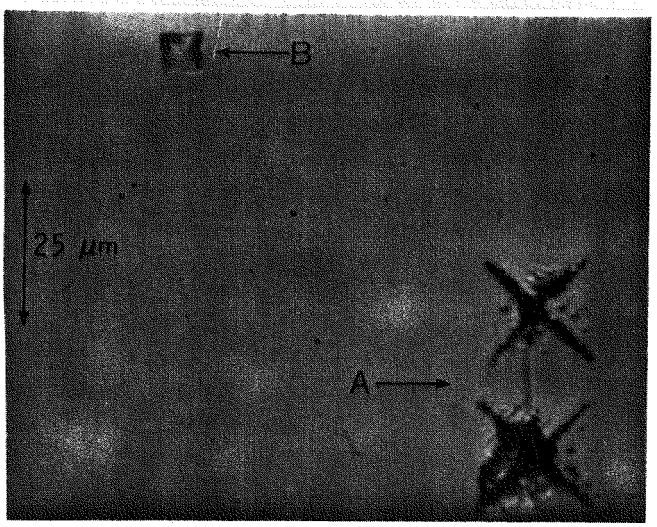

Figure 3. Optical micrograph of electrochemically etched/Wright etched silicon substrate wafer. Wafer had been oxidized in O_2 at $1000^{O}C$ for 15 min prior to etching. (A) etch pits decorating an oxidation-induced stacking fault, (B) example of an etch pit not apparently associated with a structural defect.

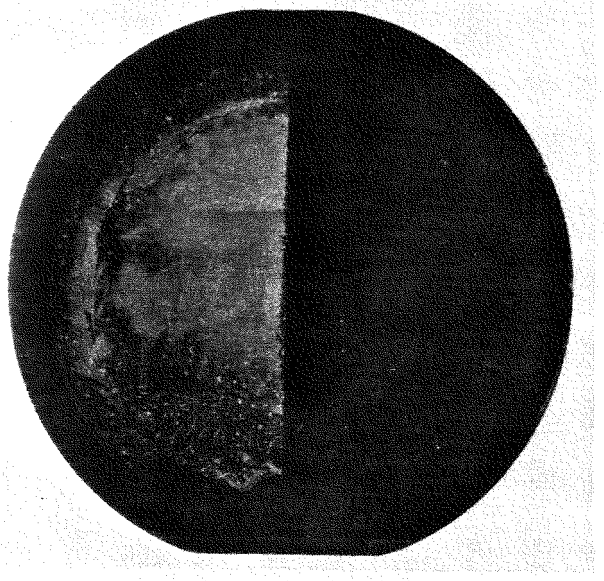

Figure 4. Optical photograph of electrochemically etched 100 mm diameter silicon substrate wafer. Wafer had been oxidized in O_2 at $1000^{O}C$ for 15 min prior to etching. Left half of wafer was previously exposed to iron contamination, right half was not contaminated.

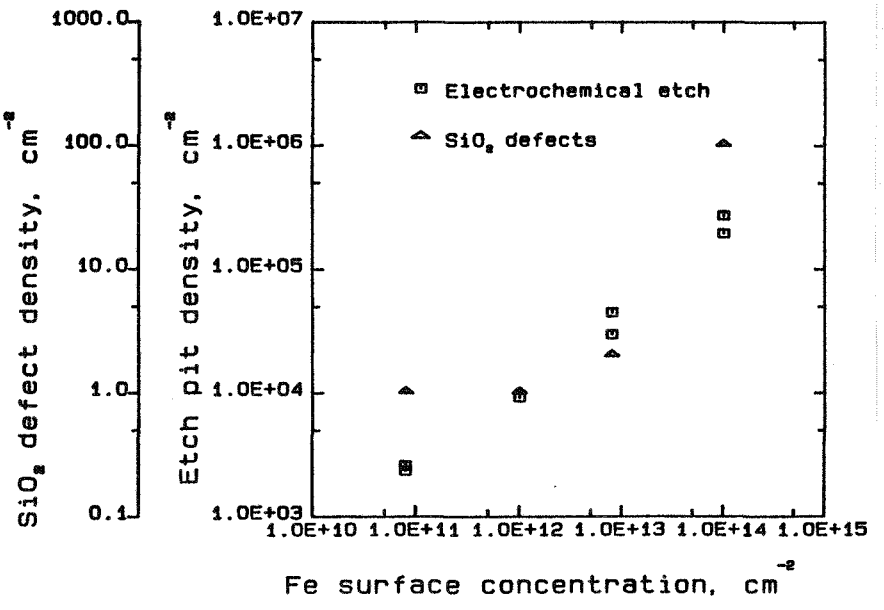

Figure 5. Electrochemical etch pit density (squares, from this work) and SiO_2 defect density (triangles, from Ref. 1) as a function of $[Fe]_{surf}$.

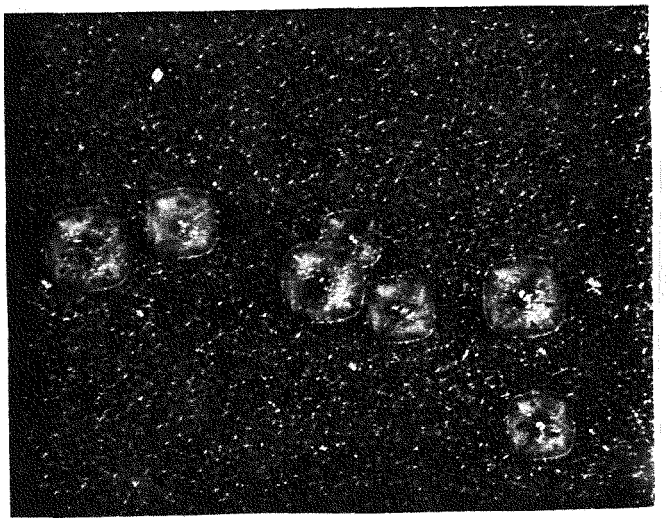

Figure 6. Electrochemically-etched SIMOX wafer (1.8×10^{18} O^+/cm^2, 200 kV, 610^0C, multiple implant/high temperature anneal). Etch pit density 10^3-$10^5/cm^2$. Etch pit size is 40 μm.