CMOS IC I_{DDQ} Testing for the 1990s

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ABSTRACT

Significant improvements in CMOS IC quality, reliability, and fabrication yield can be readily achieved in the 1990s by appropriate implementation of tests for quiescent power supply current (I_{DDQ}). As part of an overall quality management program, I_{DDQ} testing incorporated with design for testability and modified conventional logic response testing enables 100% stuck-at fault coverage, quality improvement goals of defective levels less than 100 PPM, and reliability greater than 0.999 for 30 years.

INTRODUCTION

Competitiveness in mainstream CMOS IC manufacturing in the 1990s requires significant, continuous improvement in quality, reliability, and fabrication yields. Companies with long range goals for success are implementing comprehensive quality management programs that assure the development of quality processes for all work, from product conception through design, fabrication, testing, delivery, and customer usage [1]. Considerable impact can be made towards achieving zero defects by incorporating I_{DDQ} testing with structured design for testability and conventional logic response testing.

IC manufacturers must develop technologies that can be produced in a stable, baselined process with sufficient statistical control of all critical quality and reliability factors. Specific information is therefore required on the nature and extent of defects and reliability-limiting mechanisms for these technologies. I_{DDQ} testing provides the means for identifying defects and failure mechanisms so that root causes can be defined for corrective action. I_{DDQ} testing also provides the quality metric needed to properly measure true physical defect levels of outgoing product, as opposed to conventional testing based solely on the unrealistic assumption that all IC abnormalities immediately produce internal stuck-at faults or incorrect logic outputs.

This paper provides an overview of I_{DDQ} testing and how it can be implemented to achieve significant improvements in CMOS IC quality, reliability, and fabrication yields.

I_{DDQ} TESTING

The CMOS IC I_{DDQ} test method measures the quiescent power supply current for each test vector (logic state) and is a clear indicator of most defects, failure mechanisms, and many types of design errors. This method intuitively results from the nature of CMOS technology; i.e., properly designed and fabricated CMOS circuits have nanowatt logic [2], so deviations from this produce elevated quiescent current in one or more logic states. For example, Sandia's high reliability 16 bit microprocessor (65,000 transistors; functionally equivalent to the National 32C016) and 64K SRAM (417,000 transistors; functionally equivalent to commercial 64K x 1 SRAMs) have I_{DDQ} less than 40 nA (V_{DD} = 5.5 V). Sandia Labs and Philips have used I_{DDQ} testing for the production of high reliability ICs since the 1970s. These companies and others have found a direct relationship between I_{DDQ} test acceptance rates and yields, quality, and reliability. In a 1975 article, a strong correlation was shown between increased I_{DDQ} magnitude and excessive propagation delay time, which was a prime suspect for failures in the field [3]. Other papers early in the 1980s emphasized the sensitivity of the I_{DDQ} technique for various CMOS defects, such as bridging shorts and open circuits [4], and discussed the relationship between elevated I_{DDQ} and stuck-at faults [5]. Subsequent papers in the 1980s addressed these and other aspects of I_{DDQ} testing [6].

I_{DDQ} Testing and Stuck-At Fault Detection

Fig. 1 (a,b) illustrates the ability of I_{DDQ} to detect stuck-at faults (SAFs) [7]. It shows a 2-NAND gate in which the output node C is (a) stuck-at one (SA1) and (b) stuck-at zero (SA0). The output node C-SA1 in Fig. 1(a) can be detected by I_{DDQ} if node C is logically driven to the zero state by AB =

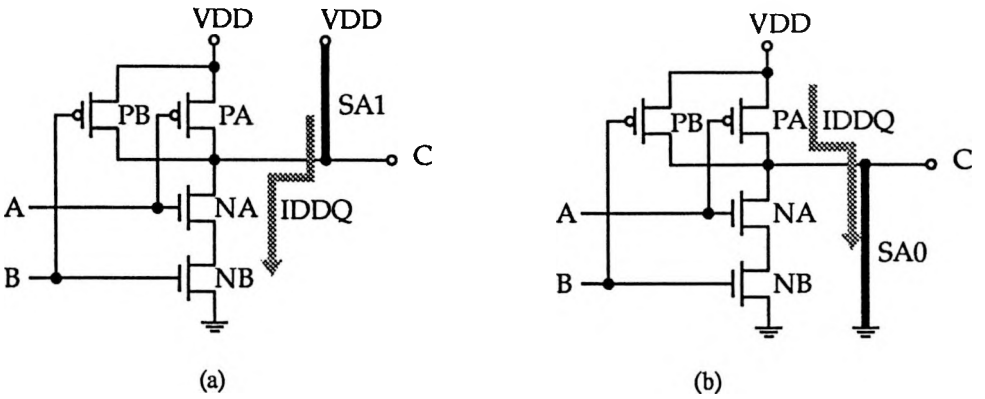

Fig. 1. (a) 2-NAND gate with a SA1 fault on node C.
(b) 2-NAND gate with a SA0 fault on node C.

11. A contention then occurs as the pull down transistors try to produce a zero state and the SA1 fault holds the one state, causing significant elevation of I_{DDQ} (I_{SSQ}), as measured in the V_{DD} (V_{SS}) path. A similar I_{DDQ} increase is observed for node C-SA0 in Fig. 1(b) when AB = 00, 01, or 10. The six SAFs associated with the 2-NAND gate can be detected with just two vectors (AB = 00, 11) if the I_{DDQ} test method were used. This compares to the normal minimum three vectors (AB = 11, 10, 01) when SAFs are evaluated using conventional logic response testing. In a similar manner, it can be shown that, with proper control, I_{DDQ} testing detects all multiple SAFs and redundant SAFs. The condition of assuring that all potential SAF sites are controlled to both logic states (0 and 1) is referred to as 100% node-state coverage. Since observation with I_{DDQ} testing is not via the logic response at the IC's primary output pins, all computational complexity for output path sensitization becomes unnecessary.

I_{DDQ} Testing and Defect Detection

The utility of I_{DDQ} testing lies in detecting a very high percentage of the dominant physical defects in CMOS ICs without additional circuitry [8]. Common defects such as gate oxide shorts and interconnection shorts (bridges) are detected in the same manner as SAFs; i.e., the gate or transistor level nodes are controlled in the appropriate manner for the defects to be detected and observation occurs via the I_{DDQ} magnitude. Some physical defects and failure mechanisms in CMOS ICs can cause "catastrophic" logic failure for any and all operating conditions. However, most defects and mechanisms in viable, baselined fabrication situations usually produce more subtle degradation of the IC's performance. ICs with defects such as gate oxide shorts can have unstable logic performance which may be highly dependent upon operational parameters such as clock frequency, V_{DD} magnitude, temperature, and radiation. Because of this, traditional functional or stuck-at test methods will not detect a high percentage of ICs with these prevalent physical defects. Table 1 provides an approximate grading of different test methods for various common types of CMOS IC defects [8]. Maximizing yield, quality, and reliability improvements requires knowledge of the dominant physical defects and their circuit effects for the particular design, technology, and manufacturing situation to structure a mixed mode strategy of I_{DDQ} and logic stimulus/response testing.

Table 1. Test method effectiveness versus CMOS IC defect type.

	Test Method			
Defect type	Functional	Stuck-at	Stuck-open	I_{DDQ}
Gate oxide short	poor	poor	poor	good
Bridge short	fair	fair-good	good-fair	good
Punch-through	fair	fair	fair	good
Parasitics, pn junc.	poor	poor	poor	good
Open drain	poor	fair	good	fair
Open gate	fair	good	good	fair
Open transm. gate	fair	fair	fair	good

In addition, I_{DDQ} has proven to be extremely useful for failure analysis by providing defect/mechanism identification and spatial localization. Immediate determination of many categories of defects and mechanisms is possible using I_{DDQ}/V_{DD} signatures. And fault isolation can be achieved with submicron precision using nondestructive techniques such as photon emission correlated with I_{DDQ} magnitude.

TEST GENERATION AND GRADING

I_{DDQ} testing beneficially changes the requirements for test generation and fault simulation algorithms/tools. Automatic

test pattern generation (ATPG) for SAFs can be much more efficient when the algorithms are redirected to generate test vectors that produce high node-state coverage for I_{DDQ} testing rather than generating conventional vectors for logic response testing. The improvements achieved by doing this include reduced vector set sizes, increased and more accurate SAF coverage, coverage of logically redundant SAFs and multiple SAFs, increased coverage of CMOS non-SAF defects, and significantly reduced cpu cost for ATPG and fault simulation [7].

For example, a Sandia IC had a functional test set in excess of 100,000 vectors and an estimated 65% single SAF coverage. A simple modification to the ATPG tool for conventional SAF test generation produced an I_{DDQ} test vector set which achieved 99.97% SAF coverage with only 259 vectors [7]. For 22 of the ISCAS'89 sequential benchmark circuits [9], the SAF coverage improvement was not as dramatic but indicated a trend towards increased fault coverage for increasing circuit size even though no design changes were made to these circuits, such as resets on flip-flops or scan path insertion. This shows the potential of I_{DDQ} testing to achieve high SAF coverage for circuits which were not designed to have "reasonable" testability. Additional improvement in the detection of SAFs and other types of defects can be achieved when ICs are designed with testability features, such as scan design, which increase the IC's controllability. Fig. 2 shows the test vector count reduction achieved with I_{DDQ} testing for the sequential benchmark circuits. An extrapolation of these data to a circuit size of 50,000 nodes gives a reduction in vector count of two orders of magnitude for I_{DDQ}-modified ATPG. Also, for these sequential benchmark circuits, ATPG for I_{DDQ} testing required less cpu time by factors ranging from 2 to 162.

CONCLUSIONS

Significant improvements in CMOS IC yields, quality, and reliability can be readily achieved with a quality management program which uses I_{DDQ} testing with design for testability and modified conventional logic response testing. Additional benefits include reduced test vector set sizes, reduced cpu cost for ATPG and fault simulation, and a more realistic measurement of stuck-at fault coverage and physical defect detection. I_{DDQ} testing offers opportunities for academia, industry manufacturers and users, and the government to develop and implement new techniques and processes for CMOS ICs.

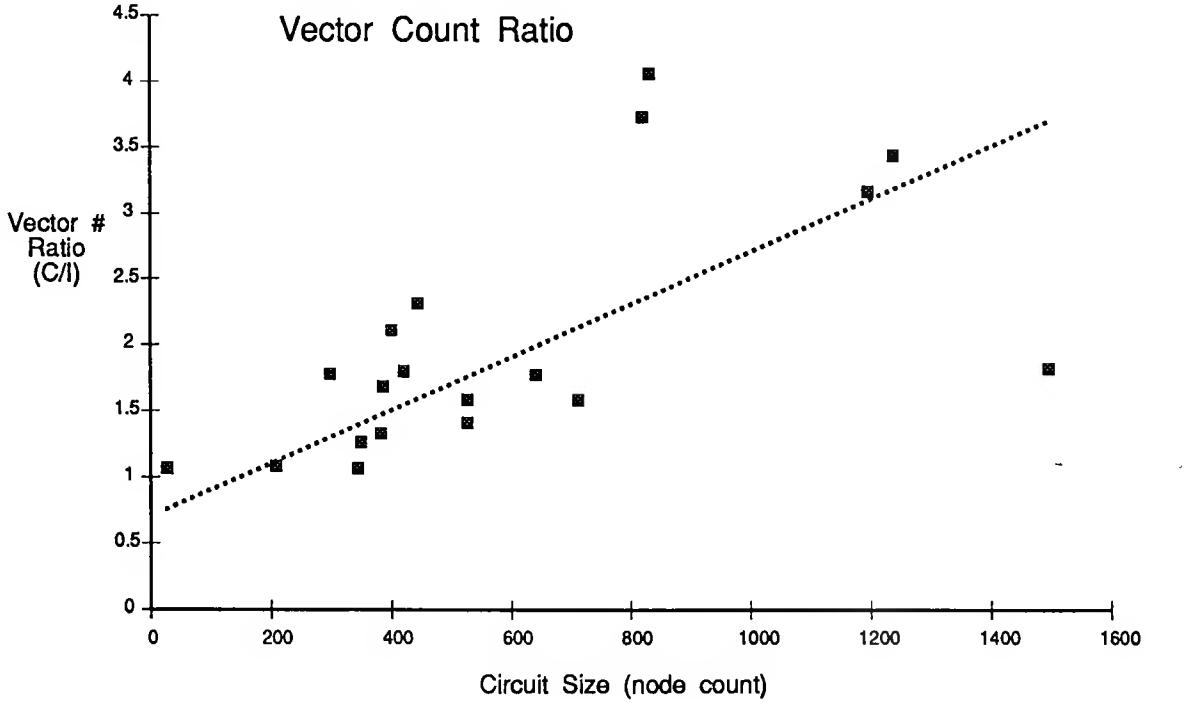

Fig. 2. Ratio of vector set sizes for conventional ATPG and modified ATPG.

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