.9095 @

# SANDIA REPORT

SAND87—1734 • UC—906
Unlimited Release
Printed November 1989

# SANDUS Checkout Procedure

David K. Werling

**Prepared by**
**Sandia National Laboratories**
**Albuquerque, New Mexico 87185 and Livermore, California 94550**
**for the United States Department of Energy**
**under Contract DE-AC04-76DP00789**

DO NOT MICROFILM
COVER

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

## DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

---

## DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

Issued by Sandia National Laboratories, operated for the United States Department of Energy by Sandia Corporation.

**NOTICE:** This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government, any agency thereof or any of their contractors or subcontractors. The views and opinions expressed herein do not necessarily state or reflect those of the United States Government, any agency thereof or any of their contractors.

Printed in the United States of America. This report has been reproduced directly from the best available copy.

Available to DOE and DOE contractors from
Office of Scientific and Technical Information
PO Box 62
Oak Ridge, TN 37831

Prices available from (615) 576-8401, FTS 626-8401

Available to the public from
National Technical Information Service
US Department of Commerce
5285 Port Royal Rd
Springfield, VA 22161

NTIS price codes
Printed copy: A03
Microfiche copy: A01

SAND--87-1734

DE90 007902

# SANDUS CHECKOUT PROCEDURE

NOVEMBER 27, 1989

SAND 87-1734

DAVID K. WERLING

**DISCLAIMER**

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

MASTER

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

# SANDUS CHECKOUT PROCEDURE

SAND87-1734

November 27, 1989

David K. Werling

NTS Instrumentation Development Division 9321
Sandia National Laboratories
Albuquerque, New Mexico 87185

## ABSTRACT

This set of procedures is designed to guide an operator through the complete SANDUS (Sandia Digital Underground System - MA164 Digital Data Acquisition System) system checkout. Each piece of Common Equipment is operationally checked by following this procedure. These steps should be performed in their entirety prior to each Nevada Test Site (NTS) event. It is assumed the operator has the experience with the SANDUS and the program DHTEST to run these procedures.

TABLE OF CONTENTS

INTRODUCTION . . . . . 1
INITIAL CHECKS . . . . . 3
TA485A CONTROLLER . . . . . 5
TA484A MULTIPLEXER . . . . . 8
TA486A PROGRAMMER TIMER . . . . . 11
TA488B TRIGGER GENERATOR . . . . . 16
TA489A CALIBRATOR . . . . . 23
TA566A POWER CONTROLLER/ENCODER . . . . . 26
TA493A SIGNAL CONDITIONER CRATES . . . . . 33
TA493B DATA MODULE CRATES . . . . . 33
TA591 & TA592 DATA MODULE . . . . . 36
TA595 ISOLATION JUNCTION BOX . . . . . 38
TA510 TRANSLATOR COUPLER . . . . . 40
SUMMARY . . . . . 43

# INTRODUCTION

The SANdia Digital Underground System (SANDUS) is a digital data acquisition system capable of collecting data from up to 128 unique analog channels and up to 88 eight bit digital channels. This system is capable of simultaneously conditioning, amplifying, digitizing, and internally storing the data from all channels. The channels record analog signals with amplitudes in the range of 1 mV to 10 V at frequencies from dc to 100 KHz, with accuracy to 99.976%, and/or signals with amplitudes in the range of 8 mV to 4 V at frequencies from dc to 10 MHz, with accuracy to 99.61%. The digitized data is continually output to a remote location for processing. The entire system may be controlled locally, remotely, or automatically in adverse electrical and environmental locations. For more specific information, see SAND86-1397, SANDUS MA164 Digital Data Acquisition System Specifications and SAND86-1398 SANDUS Command System Message and Data Format both by J. M. Opalka and D. K. Werling.

This set of procedures is designed to guide an experienced operator through a SANDUS system checkout. When all procedures have been successfully run, the system is ready to be fielded on an NTS event. Fielding should then consist of first, defining triggers, range time signals, all interconnects for non-standard experiments; second, connecting to experiments, triggers, timing signals, data streams, monitor streams, etc.; third, the check out of all triggers, timing signals, data streams, monitor streams; and fourth working with experimenters until the correct data is being recorded to the experimenter's satisfaction. During all of this, system tests should be routinely run so the operator knows at all times the exact condition of each channel and all common equipment. After the system is configured and set up for the event, an adequate set of auto tests should be run by using the test routine "Test as Set Up" for the Data Modules and Signal Conditioners. A redundancy check should be run on both the TA488B Trigger Generator and the TA566A Power Controller/Encoder after the system is down hole, but before the Mandatory Full Participation (MFP) dry run. The TA489A Calibrator should pass a weekly "Test Memory" check throughout the fielding effort. The TA488B Trigger Generator should pass a "Hardware Check" to each crate weekly throughout the fielding effort. The auto power down feature, plus the power down 1 and power down 2 setups in the TA566A Power Controller/Encoder should be checked weekly throughout the fielding effort. Memory retention of each module should be verified every weekend throughout the fielding effort. For more information on any of these tests, see the appropriate section within this manual.

Some conditions should have been met before starting these procedures.

1. All equipment should have been thoroughly bench checked before being placed in the system for the first time. Generally, no piece of Common Equipment can be 100% checked

out on the bench, however each Data Module and Signal Conditioner should have passed a full set of system diagnostics by being run through an ACE system or SANDUS. Each Operator's Manual (as they are released) will contain a detailed or step by step description of the necessary steps to check out that piece of equipment. When these steps have been faithfully followed for each piece of equipment, then the equipment may be assembled into a system.

2. These tests should be run by an experienced operator. "Experienced" means an operator who is familiar enough with the SANDUS as a System to be able to troubleshoot problems at least down to a chassis level, and who is familiar with the operation of the program DHTEST.

The data is the only reason for the SANDUS system and the prime responsibility of the SANDUS Operator is not just to collect data, but to collect the best quality data possible. This is the reason for the seemingly exhaustive testing in some cases. We have tried to leave absolutely nothing to chance, but that is truly impossible.

## INITIAL CHECKS

These initial steps are a preliminary crate and module check to get the system into a known state so the rest of the procedures may be run.

1. Load the TA493A Signal Conditioner and TA493B Data Module Crates 0 through 17 with 128 TA590-1 100 KHz Signal Conditioners and TA591 100 KHz Data Modules.

2. Initialize these 128 modules with known set up parameters, as follows:

   A. From the main menu of DHTEST, select "ED". Edit the file for channel 0. Select the following setup:

   | | |
   |---|---|
   | Signal Cond = TA590-1 | Data Module = TA591 |
   | Offset = 0 | Gain = 1 |
   | Filter = 100 KHz | Trigger Mode = Ext A |
   | Memory Size = 16K | Conversion = 8 Bit Lin |
   | Sample Interval = 2 usec | Trigger Inhibit = Disabled |
   | Calibration Mode = Data | |

   B. From the main menu of DHTEST, select "DM", Channel 0, "LS" (Load Status). This will write the above setup parameters to channel 0. Exit the Data Module Routine.

   C. From the main menu of DHTEST, select "COPY". Copy from channel 0 to all other channels ("0,1,177"). This will copy the setup from channel 0 to channels 1 through 177 in the core file.

   D. From the main menu of DHTEST, select "488".

      (1) From the TA488B Trigger Generator menu, select "CA" to program the Trigger Generator for Crate Arms. Select "0-17" to program all crates. Enter "1" for each crate to program the Trigger Generator to arm all crates with Arm 1.

      (2) From the TA488B Trigger Generator menu, select "TA" to program the Trigger Generator for Trigger A. Select "0-17" to program all crates. Enter "1" for each crate to program the Trigger Generator to Trigger 1 for each crate.

      (3) From the TA488B Trigger Generator menu, select "TB" to program the Trigger Generator for Trigger B. Select "0-17" to program all crates. Enter "3" for each crate to program the Trigger Generator to Trigger 2 for each crate.

E. From the main menu of DHTEST, select "INIT". Initialize the Data Modules with the new setup information.

3. Push the Arm button on the front panel of the TA488B Trigger Generator. Make sure each module has armed by observing each channel through the TA666A Data Selector.

4. Push the Trigger 1 button on the front panel of the TA488B Trigger Generator. Make sure each module has triggered by observing each channel through the TA666A Data Selector.

5. Push the Arm button on the front panel of the TA488B Trigger Generator. While looking at each module through the TA666A Data Selector push the +/- Test Switch on the respective Signal Conditioner to make sure + Test drives the amplifier output signal positive and - Test drives the amplifier output signal negative.

6. From the main menu of DHTEST, select "SP" (Special Data Module Tests). Select "LC" (Linearity Check On/Off). Select "1" to turn Lin Check ON. Put all 128 modules into Linearity Check by selecting "0,177", then Arm (push Arm on the Trigger Generator) and Trigger (push Trigger 1 on the Trigger Generator). Make sure there are 16 equal increment steps in the memory of each data module by observing them through the TA666A Data Selector.

7. If any of the above tests fail, a "Test All" Data Module Test may be run to help isolate and define the error condition.

## TA485A CONTROLLER

These procedures test the Command Link to each element (Common Equipment and channels) in the SANDUS System. Also checked is the Power On Reset (POR) signal to each element.

1. Initialize the Data Modules with the setups in Initial Checks section Step 2, to load their status registers with valid data, unless already done.

2. From the main menu of DHTEST, run "TM" (Test Module).

3. From the Module Test menu, run "SR" (Status Register). Run this test on channels 0 through 177 ("0T177,E"). All channels should pass. This verifies that there is a module in the slot and it is powered, there is an operational Command Link between the computer and the module, and the module's status registers can be written and read via the Command Link.

4. Power down the TA488B Trigger Generator - the backup oscillator lights on the Decode 2 board in all sixteen TA493B Crates should be lit. Power the TA488B back up, the lights should remain lit. Push the TA485A Controller Power On Reset (POR) Button - this should momentarily light the TA488B reset lamp plus reset all the Decode 2s to primary oscillator and turn OFF the backup oscillator light. This checks POR to each crate and to the TA488B and preliminarily checks the 50 MHz master oscillator signal from the TA488B into the Decode 2 board in the TA493B Crate.

5. From the main menu of DHTEST, select "488". TA488B initial conditions:

   A. Install 1D-J45 (schematic sheet 17) and 1D-J54 (sheet 18) diode SIP headers with the common pin as pin 8.

   B. Install 1D-J63 (sheet 17) and 1D-J72 (sheet 18) diode SIP headers with the common pin as pin 8.

   C. Install 1D-J81 (sheet 17) and 1D-J90 (sheet 18) diode SIP headers with the common pin as pin 1.

   D. Install 1B-J75 (sheet 2), 1B-J84 (sheet 3) and 1B-J93 (sheet 4) SIP headers with the common pin as pin 8.

6. From the TA488B Trigger Generator menu, run "TH" (Test Hardware). Select one module from one crate to test (such as channel 10, crate 1), with one pass per trigger test. This test should pass with no errors. This checks the Command Link to the TA488B as it writes and reads its status registers and memory.

7. From the main menu of DHTEST, select "489".

8. From the TA489A Calibrator menu, run "TM" (Test Memory). This checks the TA489A memory plus the Command Link to the TA489A as it writes and reads every memory location.

9. Put the TA484A Multiplexer in single-channel mode from the front panel - the Status - Single light should be lit. Send a TA485A Controller Power On Reset (push the POR button on the front panel); the Single Light should go out and the Run Light should be lit. This checks the TA485A POR to the TA484A.

10. From the main menu of DHTEST, select "GN" (general test routine).

11. To check the Command Link to the TA484A Multiplexer: from the general test routine menu, select "NE" (new message), 4 messages, 9 bytes:

| | Message 1 | Message 2 | Message 3 | Message 4 |
|---|---|---|---|---|
| Byte 3 | 200 | 200 | 200 | 200 |
| Com Equip | Yes | Yes | Yes | Yes |
| Byte 4 | 120 | 140 | 120 | 140 |
| Byte 5 | 12 | 12 | 205 | 205 |
| Byte 6 | 252 | 252 | 125 | 125 |
| Byte 7 | 20 | 20 | 120 | 120 |
| Byte 8 | 0 | 0 | 0 | 0 |

List the message ("LS") and compare bytes 4 through 8 to the above list. Next enter "MK" (Mask on return data), and select "N" (turn the mask OFF). Then enter the command "GO" and enter 10 passes. If no errors are reported, the Command Link to the TA484A should be operational.

12. On the front panel terminal of the TA486A Programmer Timer, enter "L" to list its program on the internal printer. If there is no Start Entry, program several events into its internal memory by referring to the TA486A Programmer Timer Programming Instruction Manual. After listing the program, the TA486A should remain in a Not Ready State.

13. Send a TA485A Controller POR (push the POR button on the front panel) - the TA486A Programmer Timer Not Ready Light should extinguish, but the Run Light should remain ON. The Run Light indicates the microprocessor within the TA486A is running. This has checked the POR to the TA486A.

14. From the Main Menu of DHTEST, select "FILES".

15. From the FILES menu, select "PW" (Put the Core File into a Working File). Select any work file (1-4). Enter ",E" for the channel numbers to select no channels. Enter "Y" to update common equipment files. This stores the TA486A Programmer Timer memory (plus TA484A Multiplexer, TA488B Trigger Generator and TA489A Calibrator) into the selected Working File.

16. From the FILES menu, select "GW" (Get a copy of a Working File into Core). Select the same work file number as used in Step 15 above. This puts the new TA486A Programmer Timer file into the Core File.

17. From the TA486A Programmer Timer front panel terminal, displaying "What shall I do?", press E <ENTER> to Erase. This erases the entire TA486A event entry programming. The Not Ready Light should remain ON after this test.

18. From the main menu of DHTEST, select "INIT" (Initialize), and include the TA486A Programmer Timer initialization. The TA486A Not Ready Light should extinguish at the end of this initialization.

19. From the TA486A Programmer Timer front panel terminal, list the program ("L"). This listing should be identical to that obtained in Step 12 above. This has checked the Command Link to the TA486A along with some of the cabling and parts of the TA486A Extension Panel.

## TA484A MULTIPLEXER

If just the TA484A Multiplexer is to be checked, run the following steps, plus Steps 9, 10 and 11 of the TA485A Controller checkout and Steps 18 through 21 of the TA488B Trigger Generator checkout.

This test will check portions of the TA485A Controller and Command Link cabling, all of the data streams through the TA484A and the Multiplexer cabling, a complete Data Module status register check, and a partial Data Module check.

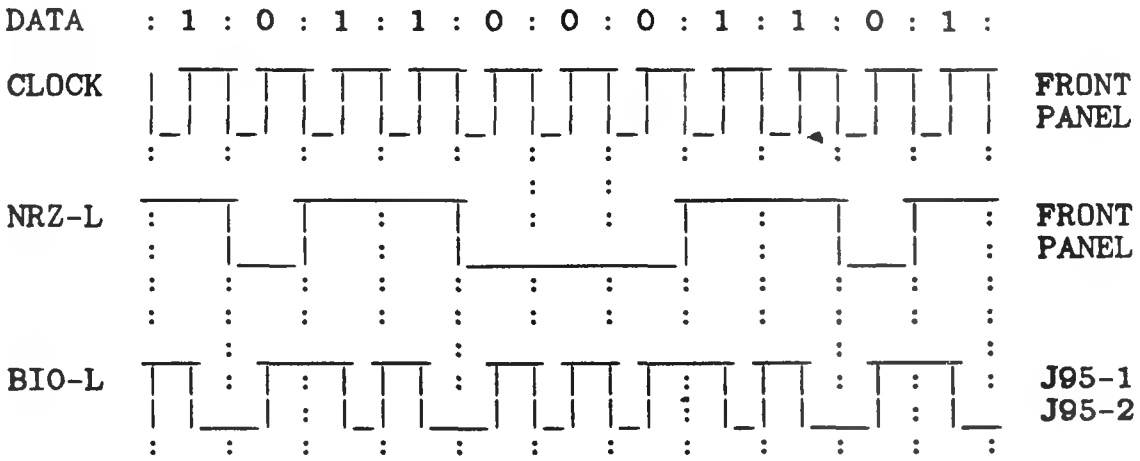
1. From the main menu of DHTEST, select "INIT". Initialize the Data Modules following Step 2 of the Initial Checks section of this manual, to load their status registers with valid data.

2. From the main menu of DHTEST, select "TM" (Test Module).

3. From the Module Test menu, run "DS" (Data Stream). This verifies that the status output (status registers) in the data stream contains the same pattern as the data module status registers as read via the Command Link.

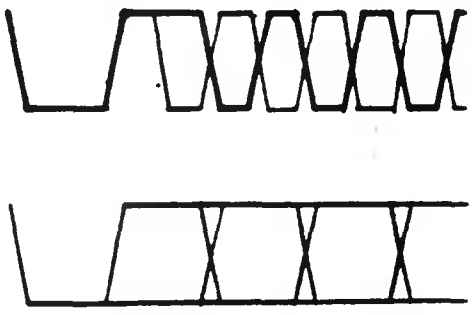
4. Check channels 0 through 177 ("0T177,E").

5. Monitor the BIO-L signals (terminated at the oscilloscope in 50 ohms) for quality of signal. Check at all bit rates by changing the bit rate through the Command Link (TA485A Controller). Trigger the scope (negative) on NRZ-L (front panel monitor) and monitor the BIO-L signal from the rear panel (both J95-1 and J95-2). The first displayed waveform should have no ghosts (data) on the positive edge. Retrigger the scope (positive) on NRZ-L, now the first displayed signal should have no ghosts on the negative edge. The following two drawings demonstrate this display. The bottom trace is the NRZ-L data, the top trace BIO-L data; the first drawing indicates it is triggered on the negative edge, the second on the positive edge. To further define NRZ-L and BIO-L Waveforms for troubleshooting purposes, see the following timing diagram:

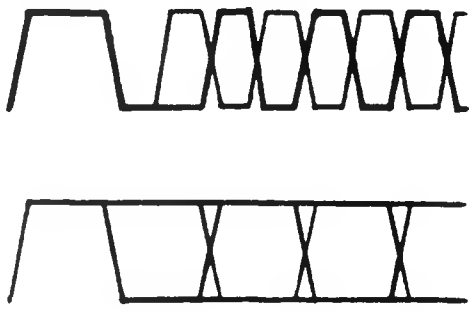



NRZ-L is defined as nonreturn-to-zero-level. A "true" is represented as one level and a "false" is represented as the other level.

Bi-Phase-Level (or Split Phase, Manchester II + 180 degrees). A "true" is represented as a transition at mid bit time from a "true" to a "false". A "false" is represented as a transition at mid bit time from a "false" to a "true".




NRZ-L TO BI0-L CONVERSION




NRZ-L TO BI0-L CONVERSION

6. Using the TA666A Data Selector, select the following channels and observe the data display for the proper output code:

    Channel 200 - 888
    Channel 201 - 888
    Channel 202 - 888
    Channel 205 - 888

7. Observe channel 203. Changing the format of the TA484A Multiplexer should give the following results on the TA666A data display:

    Format 1 - 246
    Format 2 - 251
    Format 3 - 263
    Format 4 - 272

8. Initialize the TA489A Calibrator with valid calibration information. Observe channel 214 through the TA666A and push the Start Cal button on the TA489A. The TA666A data display should indicate the following:

    040 - System in Cal, Block 0, Calibrator running
    140 - System in Cal, Block 0, Calibrator in Wait State
    041 - System in Cal, Block 1, Calibrator running
    141 - System in Cal, Block 1, Calibrator in Wait State
    042 - System in Cal, Block 2, Calibrator running
    142 - System in Cal, Block 2, Calibrator in Wait State
    043 - System in Cal, Block 3, Calibrator running
    143 - System in Cal, Block 3, Calibrator in Wait State
    000 - Calibration cycle complete

## TA486A PROGRAMMER TIMER

If just the TA486A Programmer Timer is to be checked, run the following steps plus Steps 12 through 19 of the TA485A Controller checkout. The following steps will thoroughly check the TA486A functions plus the TA486A Extension Panel and cable wiring to the rest of the system.

1. Using the TA486A Tester, bypassing the TA486A Extension Panel, turn ON each input signal, one at a time, until all 28 are ON. Each should show up on its front panel indicator (1 through 28).

2. Using the TA486A Tester, send the four pulses to the TA486A. NOTE: The TA486A Tester receives its power from the TA486A's J RNG TIME IN connector and its return through the TA486A's E1 (or, a return path will be provided if an RG58 cable is connected between the tester's J PULSE OUT and the TA486A's J IN). The tester should be set up for positive pulses, DC coupled. Each pulse should show up on the TA486A front panel indicator (29 - 32).

3. Using the TA486A front panel terminal (or the system terminal, if selected through the Terminal Select Panel (select TA486A) and on the TA486A front panel (EXT TERM)), turn ON each output (Simulate Output), one at a time until all 32 are ON. By bypassing the TA486A Extension Panel with the TA486A Tester, both the TTL output signals and the Relay Outputs should be indicated.

4. Recable the TA486A back into the system. Perform the following steps to check out the TA486A interface to other elements:

   A. Turn ON the TA486A Output 1 (Simulate Output) (488 Lockout). The TA488B Trigger Generator should not be able to send any arms. Turn OFF the TA486A Output 1. The TA488B should still not be able to send any arms. Send a TA485A Controller POR. The TA488B should now be able to arm a module.

   B. Turn ON Output 2 (488 Arm 1). This should turn ON the Arm 1 Light on the TA488B Trigger Generator front panel.

   C. Turn ON Output 3 (488 Arm 2). This should turn ON the Arm 2 Light on the TA488B Trigger Generator front panel.

   D. Turn ON Output 4 (488 Trigger Inhibit ON). This should turn ON the Trigger Inhibit Light on the TA488B Trigger Generator front panel. Turn OFF Output 4. The Trigger Inhibit Light should remain on.

   E. Turn ON Output 5 (488 Trigger Inhibit OFF). This should turn OFF the Trigger Inhibit Light on the TA488B Trigger

Generator front panel. Turn OFF Output 5. The Trigger Inhibit Light should remain off.

F. Turn ON Output 6 (Programmer Reset). This should turn ON the Reset Light on the TA488B Trigger Generator front panel. Push the TA486A Reset to turn output 6 off.

G. Turn ON Output 9 (Hold). This should turn ON Status Bit 6 of Word 5 on the TA566A Power Controller/Encoder (indicated on the TA566A front panel). Push the TA486A Reset to turn output 9 off and reset the status bit.

H. Turn ON Output 12 (Lockout). This should turn ON Status Bit 7 of Word 5 on the TA566A Power Controller/Encoder (indicated on the TA566A front panel). Push the TA486A Reset to turn output 12 off and reset the status bit.

I. Turn ON Output 17 (Start Cal). This should start a TA489A Calibration Cycle. Observe the TA486A inputs 13, 14 and 15 during the cal cycle:

   (1) Input 15 turns ON and stays ON throughout calibration.

   (2) Inputs 13 and 14 are both OFF during Block 0.

   (3) Input 13 is ON and 14 is OFF during Block 1.

   (4) Input 13 is OFF and 14 is ON during Block 2.

   (5) Inputs 13 and 14 are both ON during Block 3.

   (6) Input 15 turns OFF when the TA489A finishes its calibration sequence.

J. Push the TA486A front panel Reset button.

K. Turn ON Output 17 (Start Cal). While the system is in calibration, turn OFF Output 17, and turn ON Output 18. This should abort the TA489A Calibration Cycle. Push the TA486A Reset.

L. Turn ON Output 19 (489 Lockout). The 28V indicator on the front panel of the TA489A Calibrator should turn OFF and remain off for about 25 seconds. Push the TA486A Reset, then the TA485A Controller POR.

5. Switch the Terminal Select Panel to TA486A and select External Terminal on the TA486A front panel. From the System Terminal, program the TA486A memory with the following event file:

| EVENT # | INPUT SIGNAL | ON TIME | DEFINITION |
|---|---|---|---|
| 3 | 1 | -6:00.00 | START TIME |
| 4 | 2 | -5:00.00 | CHECK TIME |
| 5 | 3 | -4:45.00 | CHECK TIME |
| 6 | 4 | -1:00.00 | CHECK TIME |
| 7 | 5 | -0:30.00 | CHECK TIME |
| 8 | 6 | -0:02.00 | CHECK TIME |
| 9 | 7 | -0:01.00 | CHECK TIME |
| 2 | 8 | --- | HOLD |
| 1 | 9 | --- | RESET |
| | 10 | --- | POWER DOWN #1 |
| | 11 | --- | POWER DOWN #2 |
| | 12 | --- | |
| | 13 | --- | 489 BLOCK ID 0 |
| | 14 | --- | 489 BLOCK ID 1 |
| | 15 | --- | 489 SYSTEM IN CAL |
| | 16 | --- | 489 OUTBOARD CAL |
| | 17 | --- | |
| | \| | | |
| | 28 | --- | |
| 10 | 29 | +0:00.00 OUTPUT 14 ON | PLUS TIME START |
| | 30 | --- | |
| | 31 | --- | |
| | 32 | --- | |

| EVENT # | OUTPUT FUNCTION | ON TIME | OFF TIME | DEFINITION |
|---|---|---|---|---|
| 11,12 | 1 | -00:01.80 | +00:01.00 | 488 LOCKOUT |
| 13,14 | 2 | -00:02.00 | +00:01.00 | 488 ARM 1 |
| 15,16 | 3 | -00:30.00 | -00:29.00 | 488 ARM 2 |
| 17,18 | 4 | -00:10.00 | -00:09.90 | 488 TRIG INH ON |
| 19,20 | 5 | +00:01.00 | +00:01.10 | 488 TRIG INH OFF |
| | 6 | --- | --- | |
| | 7 | --- | --- | |
| | 8 | --- | --- | |
| | 9 | --- | --- | |
| 21,22 | 10 | -06:00.00 | +03:00.00 | 566 POWER DOWN #2 |
| 23,24 | 11 | -06:00.00 | +03:00.00 | 566 POWER DOWN #1 |
| 25,26 | 12 | -00:02.00 | +00:10.00 | 566 LOCKOUT |
| 27,28 | 13 | -00:02.00 | +00:01.00 | 484 LOCKOUT |
| 29 | 14 | -06:00.00 | --- | 484 PROGRAMMER RUNNING |
| | 15 | --- | --- | PWR DN 2 INTERLOCK |
| | 16 | --- | --- | PWR DN 1 INTERLOCK |
| 30,31 | 17 | -04:30.00 INPUT 5,6, 7 OFF OUTPUT 24 OFF | -04:29.90 OUTPUT 17 ON | 489 AUTO CAL |
| 32,33 | 17 | -04:29.80 INPUT 5,6, | -04:29.70 OUTPUT 17 | 489 AUTO CAL |

| | | | | |
|---|---|---|---|---|
| | | 7 OFF<br>OUTPUT 24<br>OFF | ON | |
| 34,35 | 17 | -04:29.60<br>INPUT 5,6,<br>7 OFF<br>OUTPUT 24<br>OFF | -04:29.50<br>OUTPUT 17<br>ON | 489 AUTO CAL |
| 36,37 | 18 | -00:31.00 | -00:30.90 | 489 STOP CAL |
| 38,39 | 19 | -00:02.00 | +00:01.00 | 489 LOCKOUT |
| | 20 | --- | --- | |
| 40,41 | 21 | -00:02.00 | +00:01.00 | 485 LOCKOUT |
| | 22 | --- | --- | |
| | 23 | --- | --- | |
| 42 | 24 | -00:30.00 | --- | INTERNAL CAL INHIBIT |
| | 25 | --- | --- | |
| | \| | | |
| | 32 | --- | --- | |

6. Start a dry run (Simulate, Input, 1); make sure the following happens when indicated (this may take several runs to observe all the following events):

   A. Each input puts the TA486A into the proper state (e.g., -06:00.00 (input 1), -05:00.00 (input 2), -04:45.00 (input 3), -01:00.00 (input 4), -00:30.00 (input 5), -00:02.00 (input 6), -00:01.00 (input 7), HOLD (input 8), RESET (input 9), Plus Time Start (input 29)).

   B. The TA489A Calibrator starts a calibration cycle at -4:30.00:
      (1) Input 15 turns ON and stays ON throughout the calibration sequence.
      (2) Inputs 13 and 14 are both OFF during Block 0.
      (3) Input 13 is ON and 14 is OFF during Block 1.
      (4) Input 13 is OFF and 14 is ON during Block 2.
      (5) Inputs 13 and 14 are both ON during Block 3.
      (6) Input 15 turns OFF when the TA489A finishes its calibration sequence.

   C. The TA488B Trigger Generator sends Arm 2 at -30 seconds (you must push the TA488B Reset button after -01:00.00 to see the indication on the front panel of the TA488B).

   D. The TA485A Controller Final Lockout Indicator lights at -0:02.00.

   E. The TA488B Trigger Generator sends Arm 1 at -00:02.00 (push the TA488B Reset button after -00:30.00).

   F. The TA486A waits at +0:00.00 for input 29 to be simulated, then continues (push Trigger 1 on the TA488B Trigger Generator front panel to generate input 29).

   G. Observe a triggered channel after zero time through the

TA666A Data Selector. The TA488B Trigger Generator should not be able to Arm that channel after zero time (checks Lockout).

H. The TA488B Trigger Generator Trigger Inhibit Light turns ON from -10 sec to +1 sec.

I. The TA566A Power Controller/Encoder Status, Word 3, Bit 7 (Programmer Running) turns ON at -6:00.00 and OFF when a Programmer Reset is activated.

J. The TA566A Power Controller/Encoder Status, Word 5, Bit 7 (Lockout) turns ON at -00:02.00 and OFF at +00:10.00.

7. From the main menu of DHTEST, select "486", then "SR" (Set Sim Input Register). Select input 1, then enter "0" and see that input 1 turned ON as indicated by the LED on the front panel of the TA486A.

8. Repeat Step 7 for inputs 2 through 32. The display for inputs 29, 30, 31 and 32 will stay ON for only about 1 second.

## TA488B TRIGGER GENERATOR

If just the TA488B Trigger Generator is to be checked, perform steps 4A, 4B, 4C, 4D, and 4E of the TA486A Programmer Timer Checkout, then the following steps.

The TA488B Hardware Test runs a very thorough checkout of the Trigger Generator. When used with the redundancy check, the confidence level in the checkout of the TA488B should be very high.

1. Initial TA488B conditions:

   A. Install 1D-J45 (schematic CK-T94748, sheet 17) and 1D-J54 (sheet 18) diode SIP headers with the common pin as pin 8.

   B. Install 1D-J63 (sheet 17) and 1D-J72 (sheet 18) diode SIP headers with the common pin as pin 8.

   C. Install 1D-J81 (sheet 17) and 1D-J90 (sheet 18) diode SIP headers with the common pin as pin 1.

   D. Install 1B-J75 (sheet 2), 1B-J84 (sheet 3) and 1B-J93 (sheet 4) SIP headers with the common pin as pin 8.

2. In DHTEST, run the TA488B Hardware Check ("TH") for one module in Crate 0 (e.g., Channel 0, Crate 0) with front panel Arm check. This test should pass with no errors.

   A description of the error messages follows:

DEFINITIONS

| | | |
|---|---|---|
| ITM=1 TRIG 1 | ITM=2 TRIG 1 DELAY | ITM=0 TRIG 4 |
| ITM=3 TRIG 2 | ITM=4 TRIG 2 DELAY | ITM=7 TRIG 5 |
| ITM=5 TRIG 3 | ITM=6 TRIG 3 DELAY | |
| ITT=0 TRIG 1 | ITT=1 TRIG 2 | ITT=2 TRIG 3 |
| ITT=4 TRIG 4 | ITT=5 TRIG 5 | |
| EXT1=TRIG A | EXT2=TRIG B | |

Error Message example 1:
DID NOT TRIGGER AND SHOULD HAVE ITM=2 ITT=0 EXT1
The Trigger Generator was programmed for Trigger 1 Delay (ITM=2) to go out as Trigger A (EXT1), and should have been sent with Trigger 1 (ITT=0). The module did not trigger.

Error Message example 2:
TRIGGERED AND SHOULD NOT HAVE ITM=4 ITT=2 EXT2
The Trigger Generator was programmed for Trigger 2 Delay (ITM=4) to go out as Trigger B (EXT2), but it should not have

been sent with Trigger 3 (ITT=2). The module triggered.

3. Run the TA488B Hardware Check ("TH") for one module in Crate 1 (e.g., Channel 10, Crate 1) with front panel Arm check. This test should pass with no errors.

4. Run the TA488B Hardware Check ("TH") for one module in Crate 2 (e.g., Channel 20, Crate 2) with front panel Arm check. This test should pass with no errors.

5. Run the TA488B Hardware Check ("TH") for one module in Crate 3 (e.g., Channel 30, Crate 3) with front panel Arm check. This test should pass with no errors.

6. Run the TA488B Hardware Check ("TH") for one module in Crate 4 (e.g., Channel 40, Crate 4) with front panel Arm check. This test should pass with no errors.

7. Run the TA488B Hardware Check ("TH") for one module in Crate 5 (e.g., Channel 50, Crate 5) with front panel Arm check. This test should pass with no errors.

8. Run the TA488B Hardware Check ("TH") for one module in Crate 6 (e.g., Channel 60, Crate 6) with front panel Arm check. This test should pass with no errors.

9. Run the TA488B Hardware Check ("TH") for one module in Crate 7 (e.g., Channel 70, Crate 7) with front panel Arm check. This test should pass with no errors.

10. Run the TA488B Hardware Check ("TH") for one module in Crate 10 (e.g., Channel 100, Crate 10) with front panel Arm check. This test should pass with no errors.

11. Run the TA488B Hardware Check ("TH") for one module in Crate 11 (e.g., Channel 110, Crate 11) with front panel Arm check. This test should pass with no errors.

12. Run the TA488B Hardware Check ("TH") for one module in Crate 12 (e.g., Channel 120, Crate 12) with front panel Arm check. This test should pass with no errors.

13. Run the TA488B Hardware Check ("TH") for one module in Crate 13 (e.g., Channel 130, Crate 13) with front panel Arm check. This test should pass with no errors.

14. Run the TA488B Hardware Check ("TH") for one module in Crate 14 (e.g., Channel 140, Crate 14) with front panel Arm check. This test should pass with no errors.

15. Run the TA488B Hardware Check ("TH") for one module in Crate 15 (e.g., Channel 150, Crate 15) with front panel Arm check. This test should pass with no errors.

16. Run the TA488B Hardware Check ("TH") for one module in Crate 16 (e.g., Channel 160, Crate 16) with front panel Arm check. This test should pass with no errors.

17. Run the TA488B Hardware Check ("TH") for one module in Crate 17 (e.g., Channel 170, Crate 17) with front panel Arm check. This test should pass with no errors.

18. From the TA488B menu, select "SD" (Set Delays). Select T1,T2,T3. Set the three delays to any convenient times, other than zero (zero actually selects the longest delay).

19. From the TA484A Multiplexer menu, select "RT" (reset time). Select 10.7 sec.

20. From the front panel of the TA488B, send an Arm 1, then at about 1 second intervals, send a Trigger 1, then Trigger 2, then Trigger 3 (sequence must be completed within 10.7 seconds of Arm 1).

21. From the 488 routine within DHTEST, set the TA488B delay times to T1=0.040 MSEC, T2=010.0 USEC and T3=01.00 MSEC. From the main menu of DHTEST, select TIM (TA484A Multiplexer Counter Times). The terminal should display something equivalent to the following:

| TRIGGER | TIME REF TO ARM | TIME REF TO FIDU | ACTUAL COUNTER REG |
|---|---|---|---|
| TRIG 1 | 1148436.780 USEC | 0.000 USEC | 17 60 154 3 |
| TRIG 2 | 1148476.480 USEC | 39.700 USEC | 320 67 154 3 |
| TRIG 3 | 2198505.660 USEC | 1050068.880 USEC | 243 123 215 6 |
| TRIG 4 | 2198515.660 USEC | 1050078.880 USEC | 227 125 215 6 |
| TRIG 5 | 3234452.220 USEC | 2086015.440 USEC | 363 260 243 11 |
| TRIG 6 | 3235446.140 USEC | 2087009.360 USEC | 23 163 244 11 |

This list shows that Trigger 2 arrived at the TA484A 39.7 usec after Trigger 1 (Trigger 1 Delay); Trigger 4 arrived 10.0 usec after Trigger 3 (Trigger 2 Delay) (1050078.880 - 1050068.880); Trigger 6 arrived 993.92 usec after Trigger 5 (Trigger 3 Delay) (2087009.360 - 2086015.440). Trigger 1 Delay should be accurate to within 1 usec, Trigger 2 Delay to within 100 nsec, and Trigger 3 Delay to within 10 usec of the programmed delay time. This test shows that the Delays are working correctly within the TA488B and that the TA484A trigger counters are accurate.

22. From the main menu of DHTEST, select "TM" (Test Module). Run "TF" (Trigger Functions) test, on channels 0 through 177 ("0T177,E"). These tests should pass with no errors.

23. Run the TA488B Redundancy Check. While running this check, power down the TA488B whenever pulling or installing integrated circuits. Always put an integrated circuit back into the same location from which it was removed, even if two of the removed ICs are the same type of integrated circuit. This test should also be run after the system is down hole,

about one week before the MFP (Mandatory Full Participation) dry run.

A. Install 1D-J45 (schematic sheet 17) and 1D-J54 (sheet 18) diode SIP headers with the common pin as pin 8.

B. Install 1D-J63 (sheet 17) and 1D-J72 (sheet 18) diode SIP headers with the common pin as pin 8.

C. Install 1D-J81 (sheet 17) and 1D-J90 (sheet 18) diode SIP headers with the common pin as pin 1.

D. Install 1B-J75 (sheet 2), 1B-J84 (sheet 3) and 1B-J93 (sheet 4) SIP headers with the common pin as pin 8.

E. Run a single pass of the TA488B hardware check (under DHTEST main menu, select "488", then select "TH") to any crate (e.g., Channel 10, Crate 1). This test should pass with no errors.

F. Pull ICs at locations 1D-G46, 1D-G62, 1E-A46, & 1E-A62 (sheets 17 & 18).

G. Run a single pass of the TA488B hardware check ("TH") to any crate. This test should pass with no errors.

H. Replace ICs removed in Step F. Pull 1D-G54, 1D-G70, 1E-A54, & 1E-A70 ICs (sheets 17 & 18).

I. Run a single pass of the TA488B hardware check ("TH") to any crate. This test should pass with no errors.

J. Replace ICs removed in Step H. Pull 1F-G23, 1F-G34, 1F-G45, 1F-G56, 1F-E45, & 1F-E56 ICs (sheets 24, 25, 26 & 27).

K. Run a single pass of the TA488B hardware check ("TH") to any crate. This test should pass with no errors.

L. Replace ICs removed in Step J. Pull 1D-E10, 1D-E21, 1D-G19, 1E-A19, 1E-G19 & 1F-A19 ICs (sheets 24, 25, 26, & 27).

M. Run a single pass of the TA488B hardware check ("TH") to any crate. This test should pass with no errors.

N. Replace ICs removed in Step L. Pull IC 1A-A1 (sheet 7).

O. Push the TA485A Controller front panel POR. TA493B Crate (all) will sync on the TA488B Master Oscillator (indicator on Decode 2 Board should extinguish).

P. Replace IC 1A-A1. Pull IC 1A-A9 (sheet 7).

Q. Push the TA485A Controller front panel POR. TA493B Crate (all) will sync on the TA488B Master Oscillator (indicator on Decode 2 Board should extinguish).

R. Replace IC 1A-A9. Pull IC 1A-E19 (sheet 8).

S. Run a single pass of the TA488B hardware check to any crate. This test should pass with no errors.

T. Replace IC 1A-E19. Pull IC 1A-E27 (sheet 8).

U. Run a single pass of the TA488B hardware check to any crate. This test should pass with no errors.

V. Replace IC 1A-E27. Pull IC 1C-A10 (sheet 28).

W. Push the TA485A Controller front panel POR. TA493B Crate (all) will sync on the TA488B Master Oscillator (indicator on Decode 2 Board should extinguish).

X. Replace IC 1C-A10. Pull IC 1C-C10 (sheet 28).

Y. Push the TA485A Controller front panel POR. TA493B Crate (all) will sync on the TA488B Master Oscillator (indicator on Decode 2 Board should extinguish).

Z. Replace IC 1C-C10. Enable Trigger Inhibit in a Data Module Status Register through the Command Link. Make sure the selected module will arm and trigger from the TA488B front panel switches.

AA. Enable the TA488B Trigger Inhibit through the front panel. The selected module will arm but will not trigger.

AB. Pull IC 2B-A12 (sheet 29). Push the Reset Switch on the front panel of the TA488B. The selected module should arm and trigger from the TA488B front panel switches.

AC. Push the Trigger Inhibit Switch on the front panel of the TA488B. The selected module will arm but will not trigger.

AD. Replace IC 2B-A12. Pull IC 2B-C12 (sheet 29). Reset the TA488B. The selected module should arm and trigger from the TA488B.

AE. Enable the TA488B Trigger Inhibit. The selected module will arm but will not trigger.

AF. Replace IC 2B-C12. Pull ICs 1C-E10 & 1C-E26 (sheet 30). Monitor 1C-G10 (referenced pin number) for a 10 usec negative going pulse when the indicated front panel switch is activated:

| 1C-G10 Pin | Front Panel Trigger | Actual Trigger Checked |
|---|---|---|
| 2 | Trigger 1 | Trigger 1 |
| 5 | Trigger 2 | Trigger 2 |
| 6 | Trigger 1 | Trigger 1 Delayed |
| 9 | Trigger 3 | Trigger 3 |
| 12 | Trigger 2 | Trigger 2 Delayed |
| 15 | Trigger 3 | Trigger 3 Delayed |
| 16 | Arm 1 | Arm 1 |
| 19 | Arm 2 | Arm 2 |

AG. Replace ICs 1C-E10 & 1C-E26. Pull ICs 1C-E18 & 1C-E34 (sheet 30). Monitor IC 1C-G10 (referenced pin number) for a 10 usec negative-going pulse when the indicated front panel switch is activated:

| 1C-G10 Pin | Front Panel Trigger | Actual Trigger Checked |
|---|---|---|
| 2 | Trigger 1 | Trigger 1 |
| 5 | Trigger 2 | Trigger 2 |
| 6 | Trigger 1 | Trigger 1 Delayed |
| 9 | Trigger 3 | Trigger 3 |
| 12 | Trigger 2 | Trigger 2 Delayed |
| 15 | Trigger 3 | Trigger 3 Delayed |
| 16 | Arm 1 | Arm 1 |
| 19 | Arm 2 | Arm 2 |

AH. Replace ICs 1C-E18 & 1C-E34. Reset the TA488B. Make sure the TA488B will Arm and Trigger a module. Carefully touch a grounded clip lead to IC 2B-E12, pin 4 momentarily (sheet 32). The TA488B will not output arms and the front panel will not indicate an arm (Lockout check).

AI. Pull IC 2B-E32 (sheet 32). Reset the TA488B. Make sure the TA488B will Arm and Trigger a module. Carefully touch a grounded clip lead to IC 2B-E12, pin 4 momentarily (sheet 32). The TA488B will not output arms and the front panel will not indicate an arm (Lockout check).

AJ. Replace IC 2B-E32. Pull IC 2B-G32 (sheet 32). Reset the TA488B. Make sure the TA488B will Arm and Trigger a module. Carefully touch a grounded clip lead to IC 2B-E12, pin 4 momentarily (sheet 32). The TA488B will not output arms and the front panel will not indicate an arm (Lockout check).

AK. Leave power on and unplug one power cord to the TA488B. One of the 5V power indicators on the front panel should extinguish (this takes about 10 seconds). Measure VCC on the Augat Board for a value between +5.0 and +5.10 volts.

AL. Run a single pass of the TA488B Hardware Check to any crate as in step 23.E. above. This test should pass with no errors.

AM. Reverse the power cords to the TA488B. The second 5V power indicator on the front panel should extinguish and the first should now be illuminated (this takes about 10 seconds). Measure VCC on the Augat Board for a value between +5.0 and +5.10 volts.

AN. Run a single pass of the TA488B Hardware Check to any crate. This test should pass with no errors.

AO. Plug both TA488B power cords back into the rack outlet strip. Both 5V power indicators should again be illuminated. Measure VCC on the Augat Board for a value between +5.0 and +5.10 volts.

AP. This completes the TA488B redundancy check.

24. From the main menu of DHTEST, select "SP" (Special Data Module Tests). Select "LC" (Linearity Check On/Off). Select "1" to turn Lin Check ON. Put all 128 modules into Linearity Check by selecting "0,177", then Arm (push Arm on the TA488B front panel) and Trigger (push Trigger 1 on the TA488B front panel). Select "LC", then "0", then "0,177" to turn Lin Check off on all channels. Check that all memories contain the sixteen equal increment steps of Lin Check by observing each through the TA666A.

25. Cycle power on the TA488B at least six times. With power up, observe each channel through the TA666A for sync word and that it is still in Lin Check. This is to make sure the Trigger Generator doesn't send Arms while powering down or up.

## TA489A CALIBRATOR

The following steps will thoroughly check the TA489A Calibrator. If just the TA489A is to be checked, no other procedures need to be run.

1. From the main menu of DHTEST, select "489".

2. From the TA489A menu, run "TM" (Test Memory). This writes and reads each bit in the Calibrator memory. This test should pass with no errors.

3. From the main menu of DHTEST, select "ED". Edit the file for channel 0. Select the following setup:

   Signal Cond = TA590-1 Data Module = TA591

   Offset = 0 Gain = 1
   Filter = 100 KHz Trigger Mode = Ext A
   Memory Size = 16K Conversion = 8 Bit Lin
   Sample Interval = 2 usec Trigger Inhibit = Disabled
   Calibration Mode = Data

   Calibration Setup Information:

   | | | | |
   |---|---|---|---|
   | Block 0 | Voltage Cal | Voltage Source | -3.750 Volts |
   | Block 1 | Voltage Cal | Voltage Source | 0.000 Volts |
   | Block 2 | Voltage Cal | Voltage Source | +2.500 Volts |
   | Block 3 | Voltage Cal | Voltage Source | +3.750 Volts |

   If any 10 MHz modules (TA590-10/TA592) are to be used in this test, their respective files should be set up as follows:

   Signal Cond = TA590-10 Data Module = TA592

   Offset = 0 Gain = 1
   Filter = 10 MHz Trigger Mode = Ext A
   Memory Size = 16K Conversion = 8 Bit Lin
   Sample Interval = 20 nsec Trigger Inhibit = Disabled
   Calibration Mode = Data

   Calibration Setup Information

   | | | | |
   |---|---|---|---|
   | Block 0 | Voltage Cal | Voltage Source | -1.500 Volts |
   | Block 1 | Voltage Cal | Voltage Source | 0.000 Volts |
   | Block 2 | Voltage Cal | Voltage Source | +1.000 Volts |
   | Block 3 | Voltage Cal | Voltage Source | +1.500 Volts |

4. From the main menu of DHTEST, select "DM", Channel 0, "LS" (Load Status). This will write the above setup parameters to channel 0. Exit the Data Module routine.

5. From the main menu of DHTEST, select "COPY". Copy from channel 0. Enter "0,1,177". This will copy the setup from

channel 0 to channels 1 through 177 in the core file. If any 10 MHz modules (TA590-10/TA592) are to be used in this test, they should be selectively copied as described within the COPY routine within DHTEST. This will not save the information in a working file or in the master file. If a work file is desired, follow the procedure outlined in Steps 14 and 15 of the TA485A Controller Checkout.

6. From the main menu of DHTEST, select "INIT". Initialize the Data Modules and the TA489A Calibrator with the new setup information contained in the core file.

7. From the main menu of DHTEST, select "TM" (Test Module).

8. From the menu of Test Module, run "CF" (Calibration Function Check). Run the test for modules 0 through 177 ("0T177,E"). This will check the calibration control lines and has run a partial check of the Signal Conditioner.

9. On the front panel of the TA489A Calibrator, select Auto Cal Block Select. Set up for Block 0, and press Start. This will calibrate all channels for block 0 information only. If a 100 KHz channel is selected, the voltage source will output -3.75 volts (-3/4 full scale). If a 10 MHz channel is selected, the voltage source will output -1.50 volts (also -3/4 full scale). The channel offset is 0, and the channel gain is 1, so the TA666A Data Selector should indicate a 40 (+/- a couple of counts) for each channel (for either a 100 KHz or 10 MHz channel). All channels should be checked.

10. On the front panel of the TA489A Calibrator, select Auto Cal Block Select. Set up for Block 1, and press Start. This will calibrate all channels for block 1 information only. If a 100 KHz channel or a 10 MHz channel is selected, the voltage source will output 0.000 volts. The channel offset is 0, and the channel gain is 1, so the TA666A Data Selector should indicate a 200 (+/- a couple of counts) for each channel. All channels should be checked.

11. On the front panel of the TA489A Calibrator, select Auto Cal Block Select. Set up for Block 2, and press Start. This will calibrate all channels for block 2 information only. If a 100 KHz channel is selected, the voltage source will output +2.50 volts (+1/2 full scale). If a 10 MHz channel is selected, the voltage source will output +1.00 volts (also +1/2 full scale). The channel offset is 0, and the channel gain is 1, so the TA666A Data Selector should indicate a 300 (+/- a couple of counts) for each channel. All channels should be checked.

12. On the front panel of the TA489A Calibrator, select Auto Cal Block Select. Set up for Block 3, and press Start. This will calibrate all channels for block 3 information only. If a 100 KHz channel is selected, the voltage source will output +3.75 volts (+3/4 full scale). If a 10 MHz channel is

selected, the voltage source will output +1.50 volts (also +3/4 full scale). The channel offset is 0, and the channel gain is 1, so the TA666A Data Selector should indicate a 340 (+/- a couple of counts) for each channel. All channels should be checked.

13. From the main menu of DHTEST, select "TM" (Test Module).

14. From the Test Module menu, run "SI" (Filter and Sample Interval Checks). Run this test on channel 0. This will check the TA489A Command Link Step Response Function.

## TA566A POWER CONTROLLER/ENCODER

If just the TA566A Power Controller/Encoder is to be checked, run the following steps. These steps alone will thoroughly check out the TA566A. A redundancy check is included even though the chassis redundancy is in the process of being enhanced. Until it is, the following steps are valid.

1. Run the TA566A Redundancy Check. While running this check, power down the TA566A whenever pulling or installing integrated circuits. Always put an integrated circuit back into the same location from where it came, even if there are others of the same type integrated circuits available. This redundancy check must also be run after the SANDUS arrives down hole, about one week before the MFP (Mandatory Full Participation) dry run.

   A. Pull the integrated circuits in locations 2D-A19 (schematic sheet 16), 2D-A35 (sheet 16), 2D-C1 (sheet 16), 2D-C17 (sheet 17), 2D-C33 (sheet 17), 2E-E1 (sheet 17), 2E-E17 (sheet 18), 2E-E33 (sheet 18), 2E-G1 (sheet 18), 2E-G17 (sheet 19), & 2E-G33 (sheet 19). Make sure all elements (TA484A Multiplexer, TA486A Programmer Timer (if enabled), TA488B Trigger Generator, TA489A Calibrator, and all 16 TA493A Crates and TA493B Crates) will still power up and down from the TA566A.

   B. Replace all integrated circuits pulled in Step 1.A. above.

   C. Pull ICs 2D-A27 (sheet 16), 2D-A43 (sheet 16), 2D-C9 (sheet 16), 2D-C25 (sheet 17), 2D-C41 (sheet 17), 2E-E9 (sheet 17), 2E-E25 (sheet 18), 2E-E41 (sheet 18), 2E-G9 (sheet 18), 2E-G25 (sheet 19), & 2E-G41 (sheet 19). Make sure all elements will still power up and down from the TA566A.

   D. Replace all integrated circuits pulled in Step 1.C. above.

   E. Pull Phase A power cord, make sure all elements will still power up and down from the TA566A. Measure VCC on the Augat Board for a value between +5.0 and +5.10 volts. Plug the Phase A power cord back in.

   F. Pull Phase B power cord, make sure all elements will still power up and down from the TA566A. Measure VCC on the Augat Board for a value between +5.0 and +5.10 volts. Plug the Phase B power cord back in. Measure VCC on the Augat Board for a value between +5.0 and +5.10 volts.

   G. This completes the TA566A redundancy check.

2. Power down the TA486A Programmer Timer. The system should not power down from any glitches on the Power Down control lines from the TA486A.

3. Power up the TA486A Programmer Timer. The system should not power down from any glitches on the Power Down control lines from the TA486A.

4. Repeat steps 2 and 3 at least six times.

5. Power down the TA566A. The system should power down. Turn the MA164 Power Control Switch OFF on the front panel of the TA566A. Power up the TA566A. The system should not power up.

6. Power down the TA566A. Turn ON the MA164 Power Control Switch located on the front panel of the TA566A. Power up the TA566A. The system should go through its normal three-step power-up sequence, which is to first power up the Common Equipment (TA484A Multiplexer, TA486A Programmer Timer, TA488B Trigger Generator, and TA489A Calibrator), second (about 500 msec later) to power up Crates (TA493A and TA493B Crates) 0 through 7, and last to power up Crates 10 through 17.

7. The TA486A Programmer Timer should be programmed as defined in the TA486A checkout procedure, Step 5. Add to the TA486A program as follows:

   A. Turn Outputs 10 and 11 OFF at -5:55.00.

   B. Turn Output 16 (power down #1) ON at -5:45.00.

   C. Turn Output 16 OFF at -5:44.80 (ON for 200 msec).

   D. Turn Output 15 (power down #2) ON at -5:30.00

   E. Turn Output 15 OFF at -5:29.80 (ON for 200 msec).

   Plug the TA486A Programmer Timer directly into the rear power strip (bypassing the extension panel) so the TA566A will not power it down. The following list shows the changes to the TA486A event file entered in Step 5 of the TA486A Programmer Timer Checkout.

| OUTPUT | ON TIME | OFF TIME | DEFINITION |
|---|---|---|---|
| 10 | -6:00.00 | -5:55.00 | POWER DOWN NUMBER 2 |
| 11 | -6:00.00 | -5:55.00 | POWER DOWN NUMBER 1 |
| 15 | -5:30.00 | -5:29.80 | PWR DN 2 INTERLOCK |
| 16 | -5:45.00 | -5:44.80 | PWR DN 1 INTERLOCK |

8. Set the switches within the TA566A as follows:

| | | |
|---|---|---|
| 2E-A1 to 2E-A2 | ON | TA488B Power Down 1 |
| 2E-A6 to 2E-A7 | ON | TA489A Power Down 1 |
| 2E-A11 to 2E-A12 | ON | TA484A Power Down 1 |

| | | |
|---|---|---|
| 2E-A26 to 2E-A27 | ON | Crate 0 Power Down 1 |
| 2E-A31 to 2E-A32 | ON | Crate 1 Power Down 1 |
| 2E-A36 to 2E-A37 | ON | Crate 2 Power Down 1 |
| 2E-A41 to 2E-A42 | ON | Crate 3 Power Down 1 |
| 2E-A46 to 2E-A47 | ON | Crate 4 Power Down 1 |
| 2E-B1 to 2E-B2 | ON | Crate 5 Power Down 1 |
| 2E-B6 to 2E-B7 | ON | Crate 6 Power Down 1 |
| 2E-B11 to 2E-B12 | ON | Crate 7 Power Down 1 |
| 2E-B18 to 2E-B17 | OFF | Crate 10 Power Down 2 |
| 2E-B23 to 2E-B22 | OFF | Crate 11 Power Down 2 |
| 2E-B28 to 2E-B27 | OFF | Crate 12 Power Down 2 |
| 2E-B33 to 2E-B32 | OFF | Crate 13 Power Down 2 |
| 2E-B38 to 2E-B37 | OFF | Crate 14 Power Down 2 |
| 2E-B43 to 2E-B42 | OFF | Crate 15 Power Down 2 |
| 2E-B48 to 2E-B47 | OFF | Crate 16 Power Down 2 |
| 2E-C3 to 2E-C2 | OFF | Crate 17 Power Down 2 |

9. Start the TA486A Programmer Timer running at -6:00.00 (Simulate Input 1). When it passes -5:30, the system should still be powered up since the power down signal is less than the 520 msec time out built into the TA566A.

10. Delete the TA486A Programmer Timer program entries for Plus Time Start (input 29) and those to turn Outputs 15 and 16 OFF. These event numbers are shown on the TA486A program listing.

11. Start the TA486A Programmer Timer running at -6:00.00 (Simulate Input 1). When it passes -5:45, the TA484A Multiplexer, TA488B Trigger Generator, TA489A Calibrator, and Crates 0 through 7 should power down. When it passes -5:30, Crates 10 through 17 should power down.

12. Set the switches within the TA566A as follows:

| | | |
|---|---|---|
| 2E-A3 to 2E-A2 | OFF | TA488B Power Down 2 |
| 2E-A8 to 2E-A7 | OFF | TA489A Power Down 2 |
| 2E-A13 to 2E-A12 | OFF | TA484A Power Down 2 |
| 2E-A28 to 2E-A27 | OFF | Crate 0 Power Down 2 |
| 2E-A33 to 2E-A32 | OFF | Crate 1 Power Down 2 |
| 2E-A38 to 2E-A37 | OFF | Crate 2 Power Down 2 |
| 2E-A43 to 2E-A42 | OFF | Crate 3 Power Down 2 |
| 2E-A48 to 2E-A47 | OFF | Crate 4 Power Down 2 |
| 2E-B3 to 2E-B2 | OFF | Crate 5 Power Down 2 |
| 2E-B8 to 2E-B7 | OFF | Crate 6 Power Down 2 |
| 2E-B13 to 2E-B12 | OFF | Crate 7 Power Down 2 |
| 2E-B16 to 2E-B17 | ON | Crate 10 Power Down 1 |
| 2E-B21 to 2E-B22 | ON | Crate 11 Power Down 1 |
| 2E-B26 to 2E-B27 | ON | Crate 12 Power Down 1 |
| 2E-B31 to 2E-B32 | ON | Crate 13 Power Down 1 |
| 2E-B36 to 2E-B37 | ON | Crate 14 Power Down 1 |
| 2E-B41 to 2E-B42 | ON | Crate 15 Power Down 1 |
| 2E-B46 to 2E-B47 | ON | Crate 16 Power Down 1 |
| 2E-C1 to 2E-C2 | ON | Crate 17 Power Down 1 |

13. Power the system back up.

14. Start the TA486A Programmer Timer running at -6:00.00 (Simulate Input 1). When it passes -5:45, Crates 10 through 17 should power down. When it passes -5:30, the TA484A Multiplexer, TA488B Trigger Generator, TA489A Calibrator, and Crates 0 through 7 should power down.

15. Reconfigure all Power Down Select Jumpers in the TA566A for Power Down Number 1 (all switches ON), or put in shot configuration.

16. If the All Power Good light is illuminated on the front panel of the TA566A, enable the Auto Power Down switch. If the All Power Good light is not lit, some piece of equipment (common equipment or crate) is not sending its status bit. Rectify this situation by turning the piece of equipment on, or repairing the equipment. The TA566A Front Panel "Bad Comm Equip" or "Bad Crate" Display should indicate which piece of equipment is at fault, or, alternately observe the front panel Encoder 1 Display, Words 1, 2 and 3 as indicated in Step 16, below. Select "TM" (test module) under the main menu of DHTEST, then run "TA" (test all) for any channel. At the end of this test the system should still be powered up. Turn OFF the Auto Power Down switch.

17. Monitor the TA566A Front Panel Encoder 1 Display. Bit 0 is the LSB (situated to the right), Bit 7 is the MSB. Check that the following bits (lights) turn OFF for the indicated condition (with noted exceptions):

Word 1

| | |
|---|---|
| Bit 0 | Crate 0 Power (Alternately turn OFF each crate) (either the A or the B Crate OFF should indicate) |
| Bit 1 | Crate 1 Power (Alternately turn OFF each crate) |
| Bit 2 | Crate 2 Power (Alternately turn OFF each crate) |
| Bit 3 | Crate 3 Power (Alternately turn OFF each crate) |
| Bit 4 | Crate 4 Power (Alternately turn OFF each crate) |
| Bit 5 | Crate 5 Power (Alternately turn OFF each crate) |
| Bit 6 | Crate 6 Power (Alternately turn OFF each crate) |
| Bit 7 | Crate 7 Power (Alternately turn OFF each crate) |

Word 2

| | |
|---|---|
| Bit 0 | Crate 10 Power (Alternately turn OFF each crate) |
| Bit 1 | Crate 11 Power (Alternately turn OFF each crate) |
| Bit 2 | Crate 12 Power (Alternately turn OFF each crate) |
| Bit 3 | Crate 13 Power (Alternately turn OFF each crate) |
| Bit 4 | Crate 14 Power (Alternately turn OFF each crate) |
| Bit 5 | Crate 15 Power (Alternately turn OFF each crate) |
| Bit 6 | Crate 16 Power (Alternately turn OFF each crate) |
| Bit 7 | Crate 17 Power (Alternately turn OFF each crate) |

Word 3

| | |
|---|---|
| Bit 0 | TA484A & TA618 Power (Turn OFF each unit) (either unit should indicate) |
| Bit 1 | TA485A Power (Turn OFF the TA485A) |
| Bit 2 | TA486A Power (Turn OFF the TA486A) |
| Bit 3 | TA488B Arms Enabled (OFF when TA486A output 1 ON) |
| Bit 4 | TA488B Power (Turn OFF the TA488B) |
| Bit 5 | TA489A Power (Turn OFF TA489A Power) |
| Bit 6 | TA566A Power (pull one power cord at a time) (either power supply should indicate) |
| Bit 7 | TA486A Programmer Running (ON when countdown starts) |

Word 4

| | |
|---|---|
| Bit 0 | Not Used |
| Bit 1 | TA486A Status OK (Send TA485A POR to turn bit OFF) |
| Bit 2 | TA488B Status OK (Send TA485A POR to turn bit OFF) |
| Bit 3 | System in Cal (ON when Start Cal) |
| Bit 4 | Not Used |
| Bit 5 | Not Used |
| Bit 6 | Phase B AC Volts OK (Unplug TA566A B power cord) |
| Bit 7 | Phase C AC Volts OK (Unplug TA566A C power cord) |

Word 5

| | |
|---|---|
| Bit 0 | Phase A Frequency OK (Unplug TA566A A power cord) |
| Bit 1 | Fidu (ON when push TA488B Trigger 1) |
| Bit 2 | Compton (ON when push TA488B Trigger 2) |
| Bit 3 | Spare (ON when push TA488B Trigger 3) |
| Bit 4 | Arm 1 (Momentarily ON when push TA488B Arm 1) |
| Bit 5 | Arm 2 (Momentarily ON when push TA488B Arm 2) |
| Bit 6 | Hold (ON when turn TA486A output 9 ON) |
| Bit 7 | Lockout (ON when turn TA486A output 12 ON) |

Word 6

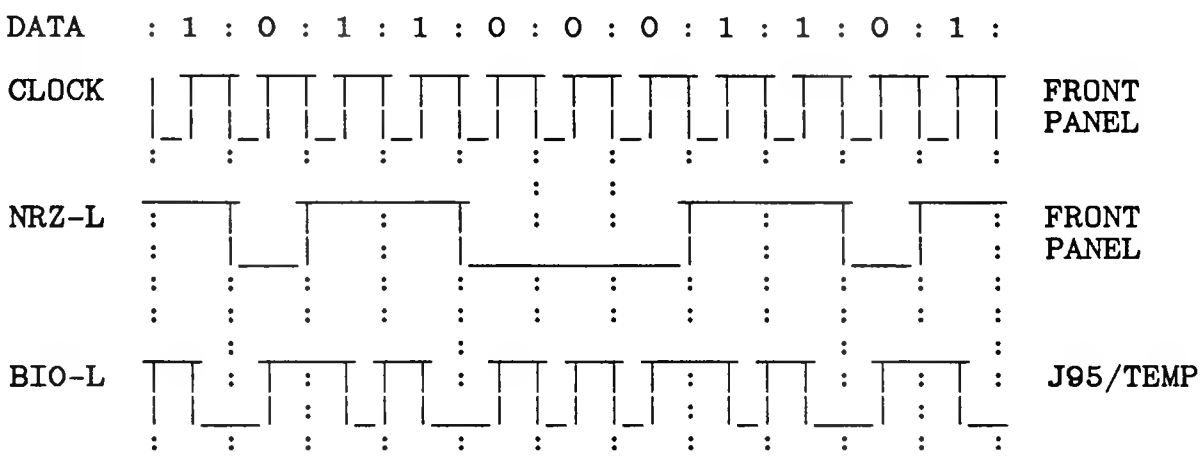
| | | |
|---|---|---|
| Bit 0 | 1 | Phase A Voltage |
| Bit 1 | 2 | Read the bits and add up their |
| Bit 2 | 4 | binary weights, e.g., |
| Bit 3 | 8 | 01111110 = 126 Volts shown on |
| Bit 4 | 16 | the Front Panel Display |
| Bit 5 | 32 | |
| Bit 6 | 64 | |
| Bit 7 | 128 | |

Word 7

| | | |
|---|---|---|
| Bit 0 | 1 | Temperature |
| Bit 1 | 2 | Read the bits and add up their |
| Bit 2 | 4 | binary weights, e.g., |
| Bit 3 | 8 | 01001011 = 75 Degrees shown on |
| Bit 4 | 16 | the Front Panel Display |
| Bit 5 | 32 | |
| Bit 6 | 64 | |
| Bit 7 | 128 | |

18. Monitor the BIO-L signals (terminated at the scope in 50 ohms) for quality of signal. Trigger the scope (positive) on Encoder 1's NRZ-L data (front panel NRZ monitor with switch

selected for Encoder 1) and monitor the BIO-L signal from the rear panel (J95/TEMP, pin 7). The first displayed waveform should have no ghosts (data) on the negative edge. Retrigger the scope (negative) on NRZ-L, now the first displayed signal should have no ghosts on the positive edge. Repeat this step with the front panel switch selected for Encoder 2 and monitoring J95/TEMP, pin 8. The two drawings in the TA484A Multiplexer section demonstrate this display. The bottom trace is the NRZ-L data, the top trace BIO-L data; the first drawing indicates it is triggered on the negative edge, the second on the positive edge. To further define NRZ-L and BIO-L Waveforms for troubleshooting purposes, see the following timing diagram.




NRZ-L is defined as nonreturn to zero level. A "true" is represented as one level and a "false" is represented as the other level.

Bi-Phase-Level (or Split Phase, Manchester II + 180 degrees). A "true" is represented as a transition at mid-bit time from a "true" to a "false". A "false" is represented as a transition at mid-bit time from a "false" to a "true".

19. If the All Power Good light is illuminated on the front panel of the TA566A, enable the Auto Power Down switch. If the light is not lit, see Step 15 above. This switch-enabled function automatically powers the system down if the internal temperature exceeds 100 degrees F, if Phase A AC frequency is not between 54 Hz and 66 Hz, if Phase A, Phase B or Phase C AC voltage is not between 105 and 125 volts, or if any crate or piece of common equipment loses power.

    A. Located between racks 4 and 5, in the lower rear portion of the rack is the temperature monitor probe. Heat this probe with a heat gun until the front panel monitor exceeds 100 degrees F. Be careful not to overheat nearby cables or other components. The system should power down. Disable Auto Power Down and power the system back

up. Enable the Auto Power Down function when the temperature is again below 100 degrees F.

B. Unplug the phase A power cord from the TA566A. The system should power down. Plug the power cord back into the power strip, disable the Auto Power Down feature (the TA566A will not power up with the Auto Power Down feature enabled as it shows the TA566A in a fault condition while powering up) and power the system back up. Enable the Auto Power Down function.

C. Unplug the phase B power cord from the TA566A. The system should power down. Plug the power cord back into the power strip, disable the Auto Power Down feature and power the system back up. Enable the Auto Power Down function.

D. Unplug the phase C power cord from the TA566A. The system should power down. Plug the power cord back into the power strip, disable the Auto Power Down feature and power the system back up. Enable the Auto Power Down function.

E. Turn OFF crate 0 (either the TA493A or TA493B crate). The system should power down. Turn the crate back ON, disable the Auto Power Down feature and power the system back up. Enable the Auto Power Down function.

F. Turn OFF crate 10 (either the TA493A or TA493B crate). The system should power down. Turn the crate back ON, disable the Auto Power Down feature and power the system back up. Enable the Auto Power Down function.

G. Turn OFF the TA484A Multiplexer. The system should power down. Turn the chassis back ON, disable the Auto Power Down feature and power the system back up. Enable the Auto Power Down function.

H. Repeat Step 18.G with the following pieces of Common Equipment:
   (1) TA485A Controller
   (2) TA486A Programmer Timer
   (3) TA488B Trigger Generator
   (4) TA489A Calibrator

## TA493A SIGNAL CONDITIONER CRATES AND TA493B DATA MODULE CRATES

Prerequisite is that the crate has been bench checked before it is placed in the system. The power is checked and adjusted, the battery charger is adjusted to 4.65 to 4.70 volts, etc. For a complete description of the bench check procedures, see the TA493A and TA493B Crate Checkout Procedures. If all preceding procedures have been followed, the crates are partially verified: Calibration Functions, Trigger Generator Functions, Power Control, Status, Data output, and Commands. The remaining tests reverify some of these functions as well as checking out address selection, data input lines and Data Module memory retention.

If just a set of crates is to be checked, run the following procedures plus Steps 1, 2 & 3 of the TA485A Controller Checkout, Steps 2, 3 & 4 of the TA484A Multiplexer Checkout, Steps 1 through 17 (whichever steps are applicable for that set of crates) of the TA488B Trigger Generator Checkout, and Steps 1, 2 & 3 of the TA489A Calibrator Checkout. These procedures will very thoroughly check all crate functions plus give a complete checkout of the Signal Conditioners and Data Modules.

1. Check the cabling to crates 0 and 1 for the TA484A Multiplexer and TA485A Command Link and their respective terminators. The TA484A Multiplexer, J0-3 cable should connect to the TA493B Crate 0, J84-I. The TA493B Crate 0, J84-0 should connect to the TA493B Crate 1, J84-I. The TA493B Crate 1, J84-0 should have a terminator installed. The TA485A Controller, J0-3 cable should connect to the TA493B Crate 0, J85-I. The TA493B Crate 0, J85-0 should connect to TA493B Crate 1, J85-I. The TA493B Crate 1, J85-0 should have a terminator installed. Install TA590-1 Signal Conditioners and TA591 100 KHz Data Modules in all slots.

2. From the main menu of DHTEST, select "TM" (Test Module).

3. From the Test Module menu, run "TA" (Test All). Data Module ("DM") and Signal Gain ("SG") checks could be run, but the time savings are minimal. Run the test for modules 0 through 17 ("0T17,E").

4. Change the Multiplexer and Command Link cabling to make Crate 0 = 1, and Crate 1 = 0, as follows. The TA484A Multiplexer, J0-3 should connect to TA493B Crate 1, J84-I. TA493B Crate 1, J84-0 should connect to TA493B Crate 0, J84-I. The TA493B Crate 0, J84-0 should have a terminator installed. The TA485A Controller, J0-3 should connect to TA493B Crate 1, J85-I. The TA493B Crate 1, J85-0 should connect to TA493B Crate 0, J85-I. The TA493B Crate 0, J85-0 should have a terminator installed.

5. From the Test Module menu, run "DS" (Data Stream) for modules 0 and 10 ("0,10,E").

6. Repeat Steps 3 through 5 for each set of crates (2-3, 4-5, 6-7, 10-11, 12-13, 14-15, and 16-17).

7. Recable the TA484A Multiplexer and TA485A Controller to all crates as outlined in Step 1 above.

8. From the Test Module menu, run "TI" (Trigger Inhibit). Run this test for modules 0 through 177 ("0T177,E"). The program requests:

```
****  SET MANUAL TRIGGER INHIBIT ON THE TA488  ****
          THEN ENTER A CARRIAGE RETURN
```

   Push the Trigger Inhibit button on the front panel of the TA488B Trigger Generator (the LED should be illuminated), then hit a carriage return.

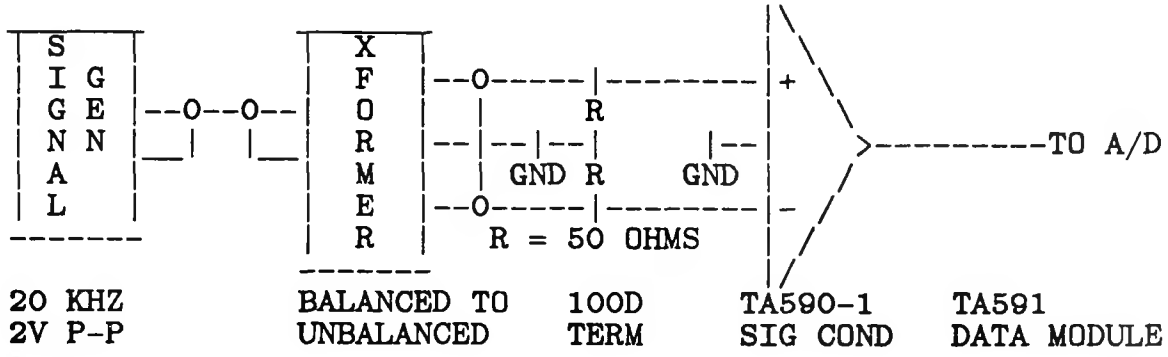
9. Install sixteen TA591R (Real Time) Data Module Memory Boards (keep the TA590-1 Signal Conditioners) in all memory board slots of a crate pair. The crate pairs are as follows: 0-1, 2-3, 4-5, 6-7, 10-11, 12-13, 14-15, or 16-17.

10. From the Test Module menu, run Data Module Tests ("DM") for all modules within that crate pair. This will check that the module will go into a memory mode during Calibration, that 8 bit and 12 bit modes operate correctly, plus operational data module tests.

11. Install TA591R modules in all slots of the next crate pair.

12. Repeat Steps 9, 10 and 11 until all slots have been tested for Real Time operation.

13. Run a 20KHz 2V p-p Sine Wave (set up loaded with 50 ohms) into a balanced to unbalanced 1:1 50 ohm transformer (to furnish a differential output), then into the TA493A Crate with a standard 100D termination. The center tap of the balanced side of the transformer must be tied to the signal input shield. This is meant to check both + and - data lines through the crate.




If a 2 volt peak-to-peak signal is seen through the TA666A Data Selector, the crate wiring is good. If a 1 volt signal

is seen, one of the two data inputs (+ or -) is either open or shorted. If a 4 volt peak to peak signal is seen at the output, one of the signal lines to the terminator is open.

14. Perform Step 13 for channels 0 through 177, with the channel gain set to 1, the sample interval set to 2 usec and the filter set to 100 KHz. Use the same procedure shown in Steps 6 and 7 of the TA489A Calibrator to set up the system.

15. Install TA590-10 and TA592 Modules in all slots of a crate pair.

16. From the Test Module menu, run "DS" (Data Stream) for all modules in that crate pair.

17. Repeat steps 15 and 16 until all crate slots are checked with a 10 MHz module.

18. When in shot configuration, "TA" (test all) should be run on all channels in the system.

19. From the main menu of DHTEST, select "SP" (Special Data Module Tests). Select "LC" (Linearity Check On/Off). Select "1" to turn Lin Check ON. Put all 128 modules into Linearity Check by selecting "0,177", then Arm (push Arm on the TA488B front panel) and Trigger (push Trigger 1 on the TA488B front panel). Select "LC", then "0", then "0,177" to turn Lin Check off on all channels. Check that all memories contain memory sync and the sixteen equal increment steps of Lin Check by observing each through the TA666A.

20. Power down the system for a minimum of 48 hours.

21. Power the system back up and observe each channel through the TA666A for sync word and that it is still in Lin Check. This is to check the memory retention of each channel.

## TA591 & TA592 DATA MODULE

The data modules have been quite thoroughly checked at this point, but are lacking in the memory checkout. The "SI" test has only done a cursory check of the memory. Each memory board (TA591 only) should be cycled through this Memory Tester to make sure there are no bad bits. The memory test boards have been designed to thoroughly test the TA591 Memory Boards under program control. Due to the difference in configuration of the TA592 Memory Boards, they may not be tested in this manner. A TA592 Memory Board Tester is forthcoming, but until it is complete (both hardware and software), to test a TA592 Memory Board, follow Steps 3, 4 and 5 below.

1. From the main menu of DHTEST, run the "MT" (Memory Test) option.

2. Select any channel, install the memory tester boards (special A/D and Control Boards), run the routine for at least two cycles of each TA591 memory board installed in the system.

3. While observing each 10 MHz Channel through the TA666A Data Selector, Arm the module through the TA488B Trigger Generator and adjust the Signal Conditioner zero to a count (on the TA666A Data Selector) of 176 or 177. This is to eliminate the noise of zero crossings from the Flash A/D Converters. Program the channel's offset to Minus Full Scale, and the memory size to 16K. Arm and Trigger the module by pushing the Arm and Trigger 1 buttons on the front panel of the TA488B Trigger Generator. There should be no extraneous pulses (other than sync word) on the scope trace.

4. Repeat Step 3 for offsets of minus 3/4 Full Scale, minus 1/2 Full Scale, minus 1/4 full scale, zero (center band), plus 1/4 full scale, plus 1/2 full scale, and plus 3/4 full scale. There should be no extraneous pulses (other than sync word) on the scope trace.

5. Steps 3 and 4 have not yet checked for two bits being shorted together. Put the TA592 module into Linearity Check (through the TA485A Controller) and change the Sample Interval to 40 nsec. Arm and Trigger the module with the TA488B Trigger Generator and observe the data through the TA666A Data Selector. There should be sixteen discrete steps with no extraneous pulses on the scope trace. What appears to be memory noise may show up at major bit transitions (-1/2 full scale, zero crossing, and + 1/2 full scale), but it is caused by the Flash A/D Converter.

- NOTE -

If the procedure is being entered at this point, and whenever a new module is installed in the system, perform the following steps:

1. From the main menu of DHTEST, select "TM" (Test Module).

2. From the Test Module menu, run Test All ("TA") for modules 0 through 177 ("0T177,E"), or for the newly installed module.

3. Run Steps 1 through 5 shown previously in this procedure.

## TA595 ISOLATION JUNCTION BOX

To thoroughly check a system before it goes downhole, all signals should be run into the system from outside the window. As soon as the Isolation Junction Box (IJB) is available, the following tests should be run (before the IJB is available, the following tests should be run from the TA595 end of the cable to at least check the cable wiring):

1. Pulse each of the six trigger lines, taking into account the in-line attenuation and transformer polarity - make sure the proper trigger reaches the TA488B Trigger Generator as indicated on the TA488B front panel indicator:

| TA595 | TA488B |
|---|---|
| Fidu 1 | Trigger 1A |
| Fidu 2 | Trigger 1B |
| Compton 1 | Trigger 2A |
| Compton 2 | Trigger 2B |
| Spare 1 | Trigger 3A |
| Spare 2 | Trigger 3B |

2. Observe the monitor signal at the output of the TA595 (terminated in 50 ohms). It should appear as a clean BIO-L signal as described in Step 18 of the TA566A Power Controller/Encoder Checkout. The TA566A front panel monitor point (also terminated in 50 ohms) is the NRZ-L equivalent. Trigger the scope on the front panel NRZ-L data and display the NRZ-L and BIO-L signals. The BIO-L should follow the NRZ-L in that a "one" is represented by a low to high transition and a "zero" is represented by a high to low transition.

3. Provide 28 volts to the following pins on the TA595 Range Time Panel (Range Time In) and observe the front panel of the TA486A Programmer Timer (Ref. A=28V, B=RTN, watch the polarity carefully):

| TA595 Range Time In | TA486A |
|---|---|
| A-B | Input 1 |
| C-D | Input 2 |
| E-F | Input 3 |
| G-H | Input 4 |
| J-K | Input 5 |
| L-M | Input 6 |
| N-P | Input 7 |
| R-S | Input 8 |
| T-U | Input 9 |
| V-W | Input 10 |
| X-Y | Input 11 |
| Z-a | Input 12 |

4. Turn ON the following outputs on the TA486A Programmer Timer one at a time and observe the TA595 Range Time Panel output (Prog Time Out) with an ohmmeter, both before and after:

| TA486A Output | TA595 Prog Time Out |
|---|---|
| 25 | A-B shorted |
| 26 | C-D shorted |
| 27 | E-F shorted |
| 28 | G-H shorted |
| 29 | J-K shorted |
| 30 | L-M shorted |
| 31 | N-P shorted |
| 32 | R-S shorted |

TA510
TRANSLATOR COUPLER

Prior to receiving the Translator Couplers, each data cable should be checked in a manner such as the one illustrated below.

1. Install TA590-1 Signal Conditioners and TA591 Data Modules in all slots. If TA590-10/592 Modules are used, appropriate changes should be made in the following setup information (see Steps 3 & 5 of the TA489A Calibrator checkout).

2. From the main menu of DHTEST, select ED. Edit the file for channel 0. Select the following setup:

   Offset = 0 — Gain = 1
   Filter = 100 KHz — Trigger Mode = Ext A
   Memory Size = 16K — Conversion = 8 Bit Lin
   Sample Interval = 2 usec — Trigger Inhibit = Disabled
   Calibration Mode = Data

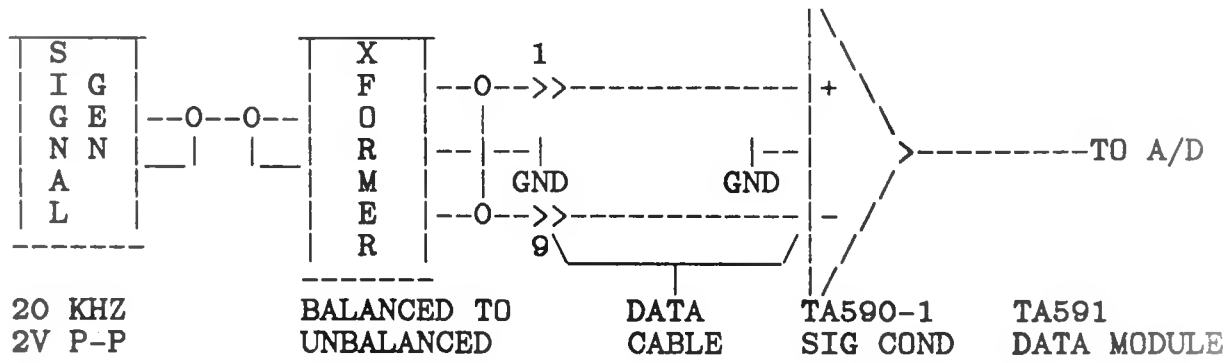
   Calibration Setup Information:
   Block 0 Special K1 (SPK1) (pulls in K1 in the Source Coupler)
   Block 1 Special K2 (SPK2) (pulls in K2 in the Source Coupler)
   Block 2 Special K3 (SPK3) (pulls in K3 in the Source Coupler)
   Block 3 Gage

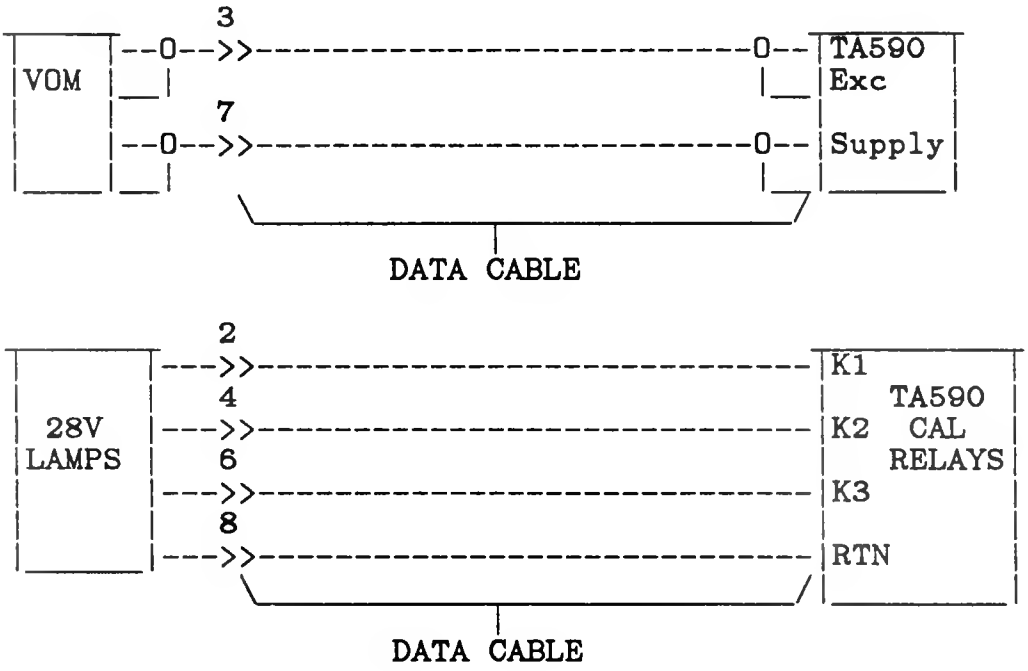
3. From the main menu of DHTEST, select "DM", Channel 0, "LS" (Load Status). This will write the above setup parameters to channel 0. Exit the Data Module Routine.

4. From the main menu of DHTEST, select "COPY". Copy from channel 0. Enter 0,1,177. This will copy the setup from channel 0 to channels 1 through 177 in the core file.

5. From the main menu of DHTEST, select "INIT". Initialize the data modules and TA489A Calibrator with the new setup information.

6. A test box is required that connects directly to the Data Cable, and brings out +/- Excitation Lines, indicators for the three calibration relay voltages, and a single ended input for the data lines, similar to that drawn below.






Data Cable Defined:

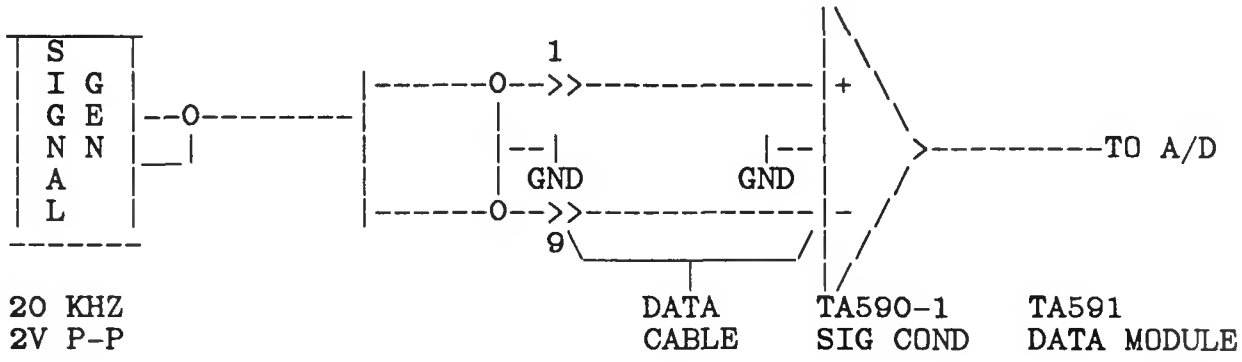
| | |
|---|---|
| Pin 1 | +Data |
| Pin 2 | K1 Cal relay voltage |
| Pin 3 | +Excitation |
| Pin 4 | K2 Cal relay voltage |
| Pin 5 | NC |
| Pin 6 | K3 Cal relay voltage |
| Pin 7 | -Excitation |
| Pin 8 | Cal relay return |
| Pin 9 | -Data |

7. Run a 20KHz, 2V p-p Sine Wave (set up loaded with 50 ohms) into the test box input (into a balanced to unbalanced 1:1 50 ohm transformer). This furnishes a differential input to the amplifier. The center tap of the balanced side of the transformer must be tied to the signal input shield. If a 2 volt peak to peak signal is seen through the TA666A Data Selector, the data lines are good. If a 1 volt signal is observed, one of the two data lines (+ or -) is either open or shorted.

8. The excitation lines should be observed for correct voltage, and measured for shorts to ground. The shields of the excitation lines should both be common to the shields of the data lines.

9. When the channel is calibrated for Block 0, K1 indicator should illuminate, Block 1 should illuminate K2, and Block 2 should illuminate K3. Block 3 should leave all relays OFF and should show the 20KHz sine wave in memory.

10. To perform a simple common mode test, "TEE" the signal generator output into both the plus data and minus data lines of the signal conditioner. There should be no data output from the amplifier.




11. To thoroughly check a system before it goes downhole, all data signals should be run into the system from outside the window. As soon as the Translator Couplers are available, every input signal should be simulated outside the window and recorded in the Data Module memory. All excitation lines should be checked for opens and shorts, and the three calibration relay lines checked with the available test box.

## SUMMARY

These procedures have been written and thoroughly checked with a SANDUS. Each element will be verified if the procedure is faithfully followed. This was not intended to limit an operator's ingenuity at troubleshooting, nor to downplay that importance, but to establish set procedures for a complete system checkout, so the fielding effort may be accomplished with less effort.

Use these procedures to fully verify a SANDUS or to reverify an element when it is reintroduced to the system after repair or modification, or simply when it has been removed from the system for some reason (to reverify the cable connections, etc.). The full set of procedures should be repeated after any move and when the system is fully configured for a test.

Through the use of routine testing the operator knows at all times the exact condition of each channel and all common equipment. After the system is configured and set up for the event, a weekly set of auto tests should be run by using the test routine "Test as Set Up" for the Data Modules and Signal Conditioners. A redundancy check should be run on both the TA488B Trigger Generator and the TA566A Power Controller/Encoder after the system is down hole, about one week before the Mandatory Full Participation (MFP) dry run. The TA489A Calibrator should pass a weekly "Test Memory" check throughout the fielding effort. The TA488B Trigger Generator should pass a Hardware Check to each crate weekly throughout the fielding effort. The auto power down features, plus the power down 1 and power down 2 functions (applicable to shot configuration) in the TA566A Power Controller/Encoder should be checked weekly throughout the fielding effort. Data Module memory retention for all channels should be checked over each weekend of the fielding effort as detailed in steps 18, 19 and 20 of TA493A Signal Conditioner Crate and TA493B Data Module Crate system checkout contained in this document.

DISTRIBUTION:

EG&G Energy Measurement Group (3)
Attn: E. Rivera
R. Salas
M. Ward
Kirtland AFB
Albuquerque, NM 87115

2345 B. C. Walker
3141 S. A. Landenberger (5)
3151 W. L. Garner (3)
3154-1 C. H. Dalin (8) for DOE/OSTI
8524 P. W. Dean
9300 J. E. Powell
9320 M. J. Navratil
9321 W. B. Boyer
9321 R. D. Aden
9321 E. D. Baker
9321 R. E. French
9321 P. J. Green
9321 P. C. Kaestner
9321 L. N. Koenig
9321 J. W. Lee
9321 R. R. Olsberg
9321 J. M. Opalka
9321 W. G. Perkins
9321 D. K. Werling (5)
9321 A. T. Wilkey
9322 C. W. Cook
9322 R. Davis
9322 G. J. Hansen
9322 E. S. Herrera
9322 W. C. Jernigan
9322 R. G. Oliveira
9322 J. L. Romine
9322 P. L. Wehrman
9323 G. L. Ogle
9323 J. W. Allen
9323 B. C. Bedeaux
9323 T. D. Burford
9323 L. A. Dubes
9323 T. F. Hendrickson
9323 G. R. Herreid
9323 L. J. Keck

9324 P. L. Nelson
9324 M. L. Bakos
9324 D. J. Belding
9324 A. L. Brazda
9324 M. E. Burke
9324 R. B. Caudell
9324 J. A. Chael
9324 D. A. Geene
9324 J. G. Jones
9324 W. J. Kluesner
9324 G. O. Miller
9324 R. L. Wilson
9325 R. L. Rutter
9325 D. C. Browne
9325 J. A. Johnson
9325 R. L. Kinchen
9325 C. D. Lucas

DO NOT MICROFILM
THIS PAGE