ANL-HEP-CP--90-33

DE90 011107

RAD-HARD ELECTRONICS DEVELOPMENT PROGRAM FOR SSC LIQUID-ARGON CALORIMETERS

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ABSTRACT

The development program for radiation-hard low-noise low-power front-end electronics for SSC calorimetry is described. Radiation doses of up to 20 MRad and neutron fluences of 10^{14} neutrons/cm^2 are expected over ten years of operation. These effects are simulated by exposing JFETs to neutrons and ionizing radiation and measuring the resulting bias, leakage current and noise variations. In the case of liquid-argon calorimeters, a large part of the front-end circuitry may be located directly within the low-temperature environment (90 K), placing additional constraints on the choice of components and on the design. This approach minimizes the noise and the response time. The radiation damage test facilities at Argonne will also be described. These include sources of neutrons, electrons, and gamma radiation.

INTRODUCTION

The high energy and luminosity at SSC will generate a severe radiation environment for the detector materials. Estimates indicate that the radiation caused by the normal beam/beam interactions and subsequent particle/detector-material interactions will be equivalent to an accidental beam loss into the detector every six days. The expected radiation environment of a generic detector has been well described in [1]. The size and complexity of the proposed detectors as well as the high event rate for the collider dictate that the instrumentation be placed near or inside the detectors. This places a particularly harsh constraint on the electronics, which must remain operational for the projected ten-year lifetime of the detector.

A block diagram of a possible SSC detector is shown in Fig. 1 [2]. In this figure, the predicted radiation doses for neutrons and ionizing radiation are shown for several positions inside the calorimeter. It should be noted that these numbers are only rough estimates, as more accurate calculations of the radiation will depend largely on the actual geometry and materials used in construction. As shown in Fig. 1, the calorimeter is split into barrel and forward sections, with the most severe doses being close to the beamline in the forward section.

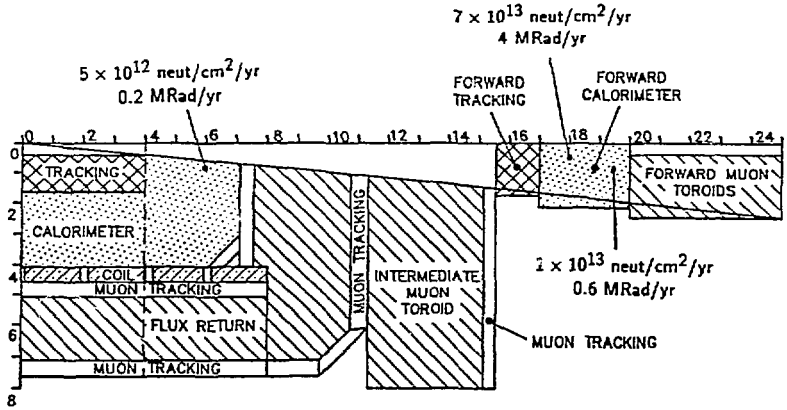


Figure 1: A possible detector implementation for SSC. The total radiation dose is shown for several locations within the calorimeter [2].

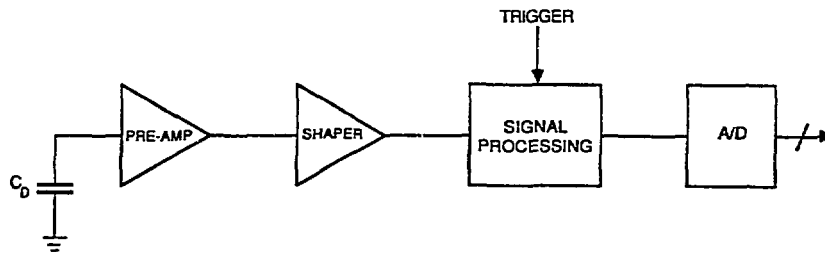


Figure 2: Detector front-end electronics.

A liquid-argon ionization chamber is one type of calorimeter which has been proposed for use in SSC detectors. It consists of plates of a heavy absorber material (typically iron, lead, or uranium) which sit in a cryostat filled with liquid argon. The designed segmentation of the detector will determine the number of plates and therefore the number of readout channels; quantities upward of 200,000 channels have been estimated for SSC. This places several constraints on the electronics associated with the calorimeter:

- They must be reliable over a large temperature range (90 K to room temperature).
- They must be low power, both due to the large number of channels, and due to thermal dissipation constraints inside the liquid-argon cryostat.
- They must be fast due to the high event rate (60 MHz).
- They must be low noise in order to maximize the energy resolution of the calorimeter.
- They must be radiation resistant to the levels described above.

A schematic of the detector front-end electronics is shown in Fig. 2. In this configuration, a charge pre-amplifier is connected directly to the detector plates in order to measure the charge generated by particles traveling through the calorimeter. A shaping amplifier is used to maximize the signal-to-noise ratio with optimal or near-optimal filtering. An analog signal processor follows the shaper and contains the waveform sampler, analog pipeline, trigger amplifiers, and event storage. Finally, an analog-to-digital converter is necessary to store the information in a computer.

The requirements and location of each section will determine the semiconductor technology to be used. In the case of the pre-amplifier, the low noise, temperature, and radiation-susceptibility requirements make JFETs the technology of choice. This is due to:

- Inherent radiation hardness due to the fact that the JFET is a majority carrier device and does not rely on oxides for charge control.
- Excellent noise performance of JFETs due to extremely low leakage currents and $1/f$ noise.
- The JFET noise performance is optimum at low temperatures, typically near 120 K.

The radiation hardness of JFETs will be discussed in this paper. We will give a qualitative account of the damage mechanisms due to radiation as well as test results on device performance at fluences up to 10^{15} neutrons/cm^2. Previous pre-amp designs have used commercially available JFETs with excellent results [3]. For example, at the HELIOS experiment at CERN, JFET pre-amps are used inside the liquid-argon cryostat and have shown 99.8% reliability. Although these pre-amps were not specifically designed for radiation immunity, we have also tested their radiation behavior with neutrons and gamma radiation. The balance of the electronics (shaper, signal processing, A/D) is currently under development. We are evaluating several rad-hard full-custom processes for this purpose, including CMOS, BiCMOS, SOS, and monolithic JFET.

Radiation damage testing will be necessary for all potential materials used in SSC detectors. Thus, the accessibility and availability of radiation sources will be key for any successful rad-hard design. Argonne National Laboratory has complete facilities for irradiation of materials with neutrons and ionizing radiation. These facilities are available to outside users and are currently used for evaluation of semiconductors and scintillators.

RADIATION DAMAGE MECHANISM IN JFETS

Radiation damage in JFETs has been well characterized with respect to DC and small-signal parameters [4,5,6]. However, to our knowledge, no comprehensive study has been made on the behavior of the device noise with respect to radiation. A JFET is pictured in Fig. 3 and consists of a conducting channel between source and drain whose dimensions are modulated by a variable width depletion region. The depletion width is controlled by varying the voltage on the gate terminal with respect to the source. Sources of noise in the JFET are as follows:

- Leakage current between the gate and source due to generation in the depletion region.
- $1/f$ noise due to generation-recombination centers in the depletion region [7].
- Thermal noise due to the finite resistance of the conducting channel between source and drain.

Upon exposure to neutrons, the JFET will experience damage to the crystal lattice due to collisions between the neutrons and the silicon atoms (Fig. 4). The resulting kinematic displacements, or vacancies, will have a finite mobility and will tend to accumulate around donor atoms. In addition, within a short range of a given collision, a cascade of silicon recoils will cause larger defect "clusters." Displacements and clusters will cause intermediate energy states, or traps, to exist in the bandgap. These mid-band states will make it easier for a carrier to jump to the conduction band. This translates into an increased leakage current ΔI_G in the device, which will be proportional to the density of the traps,

$$\Delta I_G = \alpha \phi V \qquad (1)$$

where V is the volume of the depletion region, ϕ is the neutron fluence, and α is a leakage current damage constant which relates the neutron fluence to the displacement density and

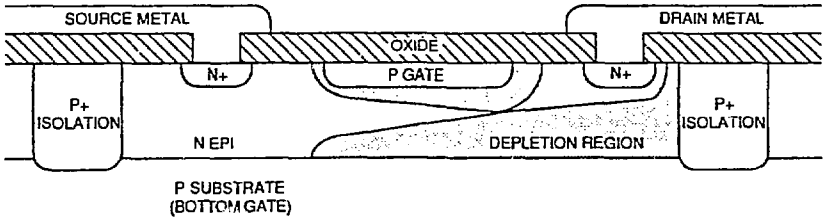


Figure 3: Cross-section of junction field-effect transistor.

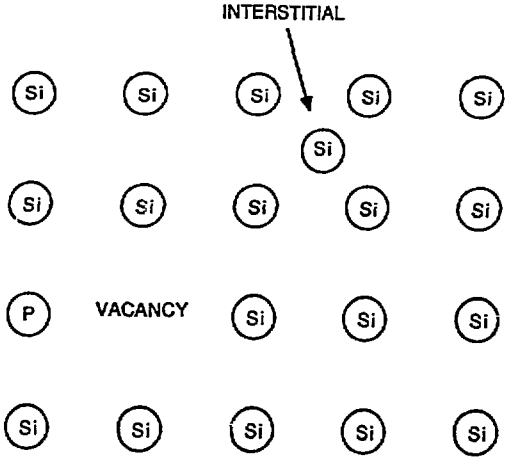


Figure 4: Neutron damage mechanism in silicon. Fast neutrons will damage the crystal and cause vacancies in the lattice, which will increase leakage currents [5].

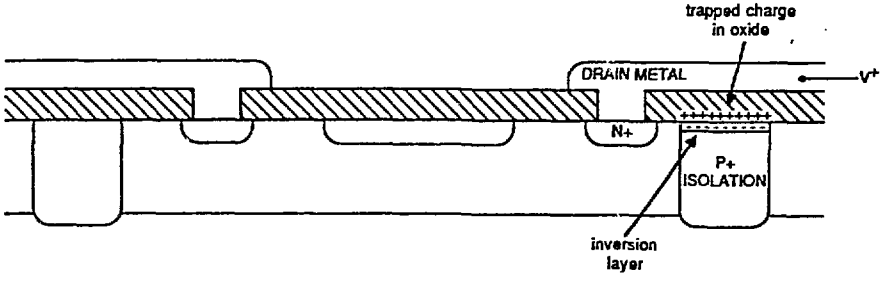


Figure 5: Ionizing radiation damage mechanism in the JFET. Charge build-up in the oxide can cause inversion in the p-type isolation region [3].

will depend on processing, temperature, and neutron energy [8]. Thus, the leakage current is strictly a volume effect in the silicon, and may be minimized by using smaller devices.

Ionizing radiation will cause carrier generation in all of the transistor materials, including the metal, silicon crystal, and silicon dioxide. As shown in Fig. 3, the oxide is used to insulate the metallization from the top of the die. In the case of the metal and silicon, the excess generated charge will be conducted away with little effect. However, in the case of the oxide, the charge will become trapped, causing a net charge to build up in the oxide. Enough of this built-up charge, together with a positive voltage on the metal, can cause a surface inversion in the p-type isolation region (Fig. 5). The mechanism is similar to that of an MOS transistor, where the threshold voltage V_t is given by

$$V_t = \Phi_{ms} + 2\Phi_f + \frac{Q_b}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} \tag{2}$$

where Φ_{ms} is the metal-silicon work potential, Φ_f is the Fermi potential, Q_b is the channel charge, C_{ox} is the oxide capacitance, and Q_{ss} is the trapped charge in the oxide. The net result of the inversion is an increased leakage current due to the increased area of the p-n junction [4]. This effect can be minimized by heavily doping the p-type isolation (increasing Q_b), which will increase the threshold voltage and make it harder to cause inversion.

Ambient temperature will have an effect on the radiation damage, both with respect to neutrons and ionizing radiation [4,6]. Annealing effects occur because at higher temperatures (e.g. room temperature), the displacements and trapped charges caused by the radiation will tend to dissipate due to thermal motion. The result will be a decrease in the radiation damage. At SSC, annealing will generally not occur because the devices will always be held at liquid-argon temperature. However, annealing is an issue in the damage testing environment where the devices may be tested at room temperature. Thus, care must be taken when comparing tests done at low temperature (where noise is lower but there is no annealing), and at room temperature (where noise is higher but may be lessened due to annealing).

NEUTRON DAMAGE TESTING

Neutron damage testing was conducted at the IPNS facility at Argonne with the neutron spectrum shown in Fig. 6. The JFETs were irradiated at room temperature while under typical bias conditions. Measurements were performed approximately one week after the actual irradiation, which allowed the neutron activation of the devices to subside. All annealing effects should stabilize during such time. Fig. 7 shows measurements of I-V curves and gate leakage current before and after the irradiation. In the case of the I-V curves, ~5% variations were observed after exposure to 10^{14} neut/cm^2 (typical 10-year dose at SSC). Measurements of transconductance showed <2% variation. Thus, these JFETs could be used successfully at SSC with little or no loss in gain or bandwidth.

The gate leakage current (Fig. 7b) increased by one order of magnitude after the irradiation at room temperature. However, between room temperature and liquid-argon temperature, the leakage can be expected to drop by about six orders of magnitude. By extrapolating from the post-irradiated room-temperature measurement, the leakage current at 90° K will be on the order of 0.1 fA, which will not adversely affect the noise of the pre-amplifier.

Fig. 8 shows the room-temperature series noise for neutron fluences ranging from 10^{13} to 10^{15} neut/cm^2. The main effect of the neutrons is to increase the $1/f$ noise due to the displacement damage. Due to the limitations of our test equipment, we have not been able to directly measure the noise at the high frequencies which are of most interest. However, we can get an estimate of the high-frequency behavior by linearly extrapolating the $1/f$ noise and assuming the thermal noise to be constant (dashed lines in Fig. 8). This assumption should be valid because the thermal noise is proportional to the transconductance, which,

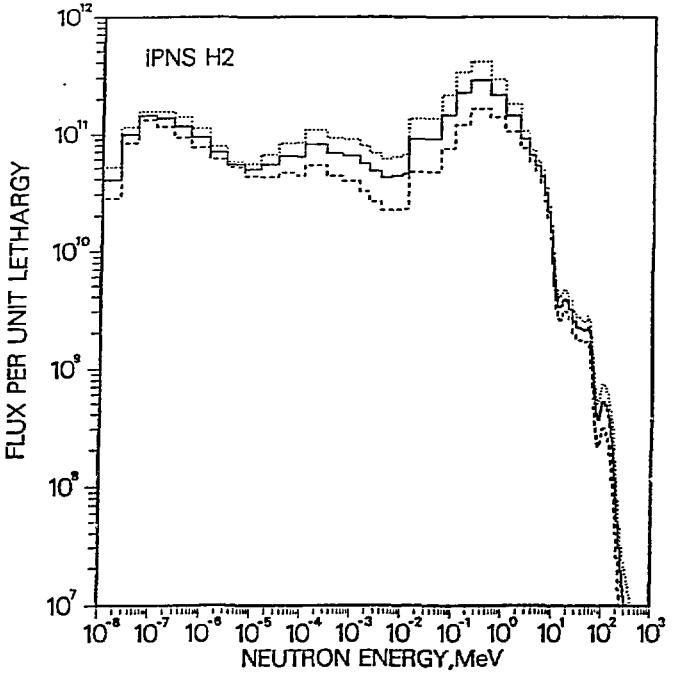


Figure 6: Neutron spectrum at Intense Pulsed Neutron Source.

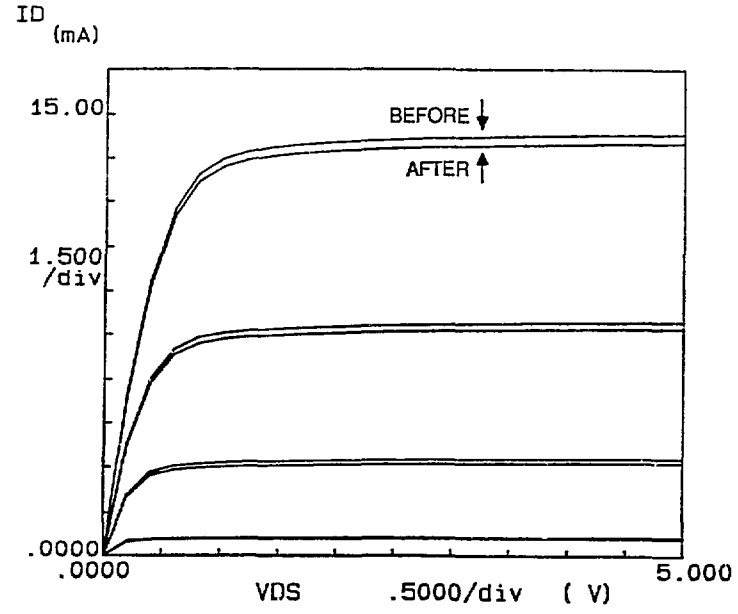
as mentioned above, remains essentially unchanged by the neutrons. Assuming a bipolar shaping function of 100 ns peaking time, the noise will be bandlimited to the high-frequency region shown in the figure. After 10^{14} neut/cm^2, the noise increase, though measurable, is far less dramatic than the increase of the equivalent noise voltage at lower frequencies. This was confirmed by using one of the irradiated JFETs as the input transistor to an un-irradiated HELIOS pre-amp. An increase of 25% in the equivalent noise charge (ENC) was measured with 100 ns bipolar shaping at room temperature. This increase will be smaller at true operating conditions, i.e. at liquid-argon temperature and at faster shaping times.

IONIZING RADIATION DAMAGE TESTING

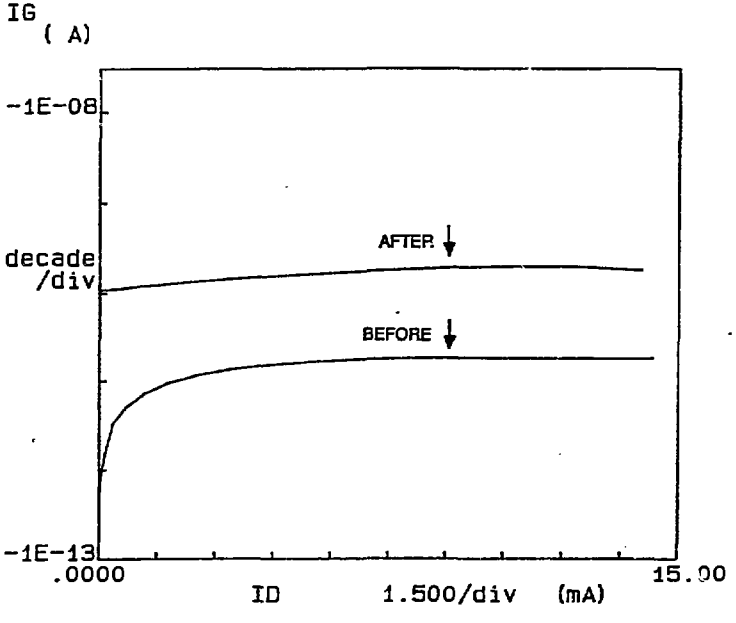
Several of the HELIOS JFET pre-amplifiers were subjected to 12 MRad(Si) of Cobalt-60 gamma radiation at Brookhaven at the rate of 5 kRad(Si)/hr. The devices were irradiated with power applied while kept at their normal operating temperature of ~120 K, and were kept cold for the duration of testing. The resulting change in the amplifier noise is shown in the noise spectrum of Fig. 9, which shows the ENC with respect to the shaping time constant for unipolar shaping. The ENC worsens, especially at longer shaping time constants. This corresponds to an increase of leakage current as the positive charges in the oxide drift to the oxide/silicon interface and cause inversion in the silicon. However, long shaping times are not of interest for SSC applications, therefore making this behavior unimportant. At the shorter shaping times (<100 ns), the noise increase is less than 20%.

RADIATION TEST FACILITIES

Because Argonne National Laboratory was for a number of years the site of one of the world's major high energy physics accelerators (ZGS), experienced groups were developed to supervise radiation safety, dosimetry, etc. After the ZGS was closed, these facilities continued to serve the needs of the various accelerators which continued to operate at Argonne. The



(a)



(b)

Figure 7: DC characteristics for SNJ132L JFET, before and after exposure to 10^{14} neutrons/cm^2. (a) I-V curves. (b) Gate leakage current.

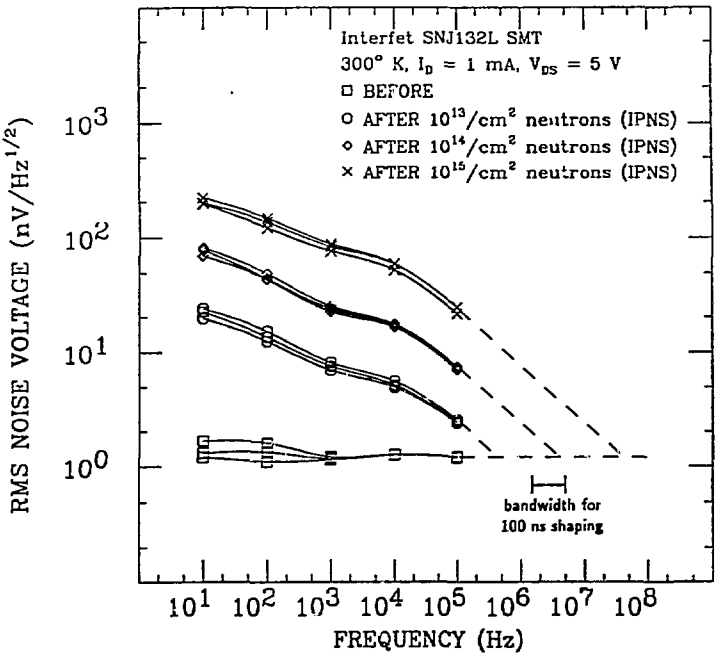


Figure 8: Input series noise for SNJ132L JFET, before and after exposure to neutrons.

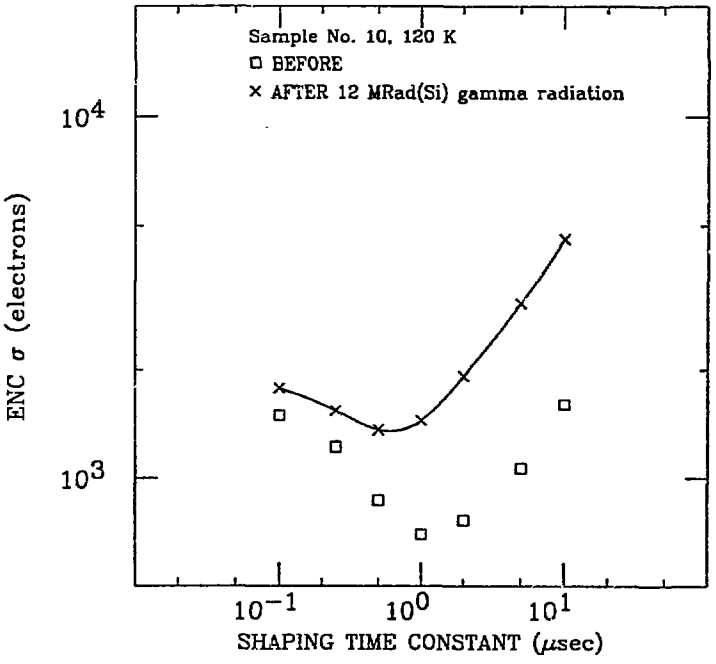


Figure 9: Equivalent noise charge spectrum for HELIOS pre-amplifier, before and after exposure to 12 MRad (Si) gamma radiation.

availability of these services makes the performance of radiation damage studies at Argonne particularly straightforward and efficient from the experimenter's point of view.

Intense Pulsed Neutron Source (IPNS):

The Intense Pulsed Neutron Source at Argonne is used routinely in an on-going program of material science research. It is a large well-staffed facility which runs a well defined schedule on average of two weeks per month throughout the year. This device is unique in that it can give in minutes or hours neutron fluences characteristic of several years of operation in the SSC environment at very forward pseudorapidities. Additionally, the IPNS offers the advantage over a reactor in that there is virtually no gamma contamination of the neutron flux. This is particularly valuable in semiconductor radiation damage testing because it allows the effects of displacement damage to be distinguished from the effects of ionization damage.

The IPNS uses a 50 MeV Linac and 500 MeV Rapid Cycling Synchrotron to produce a 500 MeV proton beam which is transported to a spallation target in a large experimental hall. The shielding in this facility has a number of ports which are used for material science experiments, and two test ports which are used parasitically for such things as radiation damage studies. One port is approximately 1 cm (3/8") diameter and the other is approximately 5 cm (2") in diameter. The neutron flux at either port is approximately 10^{12} neut/cm^2/sec, and the neutron energy is shown in the spectrum of Fig. 6. Fortunately, the neutron spectrum is roughly similar to the spectrum of the albedo neutrons in an SSC detector, peaking at approximately 1 MeV.

We have done a large number of neutron damage exposures using the test ports at fluences ranging from 10^{12} to 10^{17} neut/cm^2. These exposures have involved MOS, JFET, and bipolar semiconductors, and plastic scintillator.

Cobalt-60 Source:

Within the Biology Division, Argonne has a large Co-60 source which is used routinely in life science research. This source is capable of producing up to 2 MRad(Si)/hr. The source is periodically calibrated with an ion chamber which is calibrated by NIST, and subsequently only half-life corrections are made in dose calculations. This source has been used in tests of radiation damage in CMOS devices at room and cryogenic temperatures.

22-MeV Electron Linac:

The Chemistry Division at Argonne has a 22-MeV electron linac which is available for radiation damage research. The nominal beam current of the linac is 50 microamps, however this number may be reduced by as much as three orders of magnitude at the user's discretion. Typically, the beam is focused to a spot 0.6 cm (1/4") in diameter, however the user can de-focus the beam so that it fills the beampipe. Accordingly, the flux of 22 MeV electrons can be varied to fit the users requirements over a very large magnitude. This is particularly useful in semiconductor radiation damage research.

Fast Neutron Generator:

The Fast Neutron Generator in the Engineering Physics Division at Argonne is is capable of producing neutrons for radiation damage research through the Be(d,n) reaction, and is used currently for neutron physics. It consists of a dynamitron, which is similar to a large Cockroft-Walton accelerator, and can accelerate 7 MeV deuterons onto a thick beryllium target to yield 2.5 MeV neutrons and produce a flux of up to 10^{10} neut/cm^2/sec. The spatial constraints at the dynamitron are much more relaxed than at IPNS, allowing much easier installation of a cryostat for neutron damage research at cryogenic temperatures.

ACKNOWLEDGMENTS

The authors would like to thank T. Scott and G. Schulke of IPNS for help with the neutron irradiations.

Work supported by the U.S. Department of Energy, Division of High Energy Physics, under contract W-31-109-ENG-38.

REFERENCES

[1] D.E. Groom, ed., "Radiation Levels in the SSC Interaction Regions," *SSC-SR-1033*, June 10, 1988.

[2] J.W. Dawson, L.J. Nodulman, "Development of Radhard VLSI Electronics for SSC Calorimeters," in *Supercollider 1*, M. McAshan, ed., Plenum Press, New York, 1989, pp. 203-216.

[3] HELIOS Collaboration, unpublished report.

[4] D.J. Allen, et al., "Gamma-Induced Leakage in Junction Field-Effect Transistors," *IEEE Trans. on Nucl. Sci.*, Vol. NS-31, No. 6, Dec. 1984, pp. 1487-1491.

[5] S.S. Naik, W.G. Oldham, "Neutron Radiation Effects in Junction Field-Effect Transistors," *IEEE Trans. on Nucl. Sci.*, Vol. NS-18, No. 5, Oct. 1971, pp. 9-17.

[6] G.C. Messenger, M.S. Ash, *The Effects of Radiation on Electronics Systems*, Van Nostrand Reinhold Co., New York, 1986.

[7] M.B. Das, J.M. Moore, "Measurements and Interpretation of Low-Frequency Noise in FET's," *IEEE Trans. on Electron Devices*, Vol. ED-21, No. 4, April 1974, pp. 247-257.

[8] H.W. Kraner, Z. Li, K.U. Posnecker, "Fast Neutron Damage in Silicon Detectors," *Nucl. Instr. and Meth.*, A279 (1989), pp. 266-271.