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High-Efficiency Silicon Solar Cells for a 22-Sun Line-Focus Module

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HIGH-EFFICIENCY SILICON SOLAR CELLS FOR A 22-SUN LINE-FOCUS MODULE

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Sandia Contract 05-2557

ABSTRACT

The purpose of this program was for Solarex, a commercial silicon solar cell supplier, to demonstrate the capability of fabricating high efficiency 38.4 cm^2 concentrator cells in a production environment. These cells were designed for use in 22-sun line-focus concentrator module that could generate 20kW for the PVUSA EMT-1 project. The cells were fabricated using p-type, .8 ohm-cm silicon, randomly textured fronts, dual-layer anti-reflective coatings, passivated emitters, restricted emitter/metallization contact areas, and silver gridlines with large cross-sectional areas. Prismatic covers were used to eliminate losses from gridline shadowing. Cell efficiencies as high as 20.34% were demonstrated on covered cells at 20 suns air mass 1.5 illumination. The process sequence includes a single diffusion step, a thin thermal oxide growth, and two mechanically registered photolithography steps.

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1 INTRODUCTION

For this contract, Solarex developed a 38.4 cm^2 silicon solar cell to be used with a prismatic cover in a 20kW 22-sun linear-focus concentrator module produced by the Entech Corporation for the PVUSA EMT-1 project. The program goal was to fabricate 20 cells of this type having an average active area efficiency of at least 21.5% at 20 suns illumination. This was intended to insure an illuminated area efficiency of over 20.4% after application of prismatic covers and interconnects. Evaluation of final device performance based on active area measurement, however, was not straight-forward. As a result, prismatic covers and copper interconnects were attached to the cells to permit a more accurate final cell efficiency measurement.

The highest illuminated area efficiency on a cell fabricated during this program was 20.34% measured at Sandia National Laboratories on a cell after attachment of cover and interconnects. To our knowledge, this is the highest efficiency concentrator cell of this size produced anywhere as of this writing. This also represents a significant improvement over our efficiency baseline established using a similar, but less optimized solar cell supplied to Entech for the 300-kW Austin project for which the average covered cell efficiency was 18.9%.

The cells for this program were fabricated using p-type .8 ohm-cm silicon, randomly textured fronts, dual-layer anti-reflective coatings, passivated emitters, restricted emitter/metallization contact areas, and silver gridlines with large cross-sectional areas. Prismatic covers diverted light that would have otherwise hit the gridlines onto the active current-collecting area of the cell. The fabrication sequence included two photolithography steps and one diffusion step.

Section 2 of this report describes the baseline design established prior to this program, our strategy for improving its performance, the improved cell structure, and its fabrication sequence. Results at concentration are discussed in Section 3. In Section 4, several options for further development are presented.

2 CELL DESCRIPTION

2.1 BASELINE (ENTECH/AUSTIN)

Our approach for this program was to improve the performance of the solar cells produced for the 300-kW linear focus concentrator system being installed in Austin by Entech. The average covered cell efficiency for the 25,300 cells supplied for that program was 18.9%. Those cells had identical physical dimensions as the cells developed for this program but were fabricated using a simpler and less optimized process sequence.

Figure 1 shows a pair of these cells oriented on a 5-inch round silicon wafer from which they are fabricated. The cells have two parallel 0.12 inch wide busbars along the cell edges. 190 Gridlines on 0.020-inch centers cover close to 20% of the illuminated area of the cell. The corner of each cell is truncated, reflecting a compromise between efficient utilization of the available "real estate" of the silicon wafer and optimal solar cell packing density in the receiver.

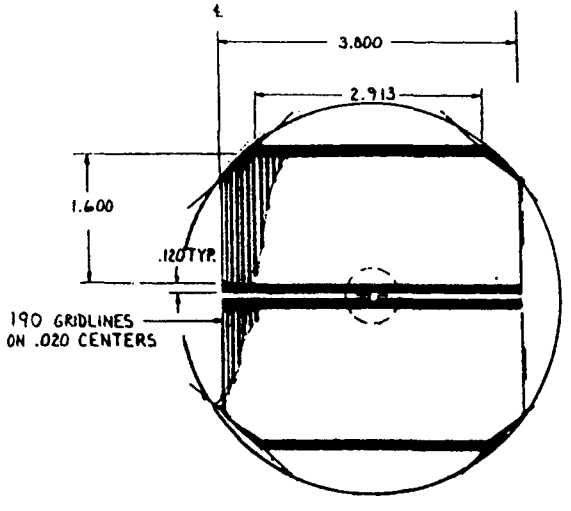


Figure 1

2 Cells on 5-Inch Silicon Wafer

The Austin cells had a random pyramidal textured surface, which resulted in an increase of approximately 4% in short-circuit current and brought the cell efficiency from the 18.25% to the 19% efficiency range.

2.2 DESIGN PARAMETERS

We identified the following key modifications to improve the performance of the baseline cells to the program target:

o Emitter passivation. A thin oxide layer, thermally grown across the entire diffused layer, was added to the Austin structure. This required a modification to the baseline diffused layer so that the desired sheet resistivity would be obtained after the oxide growth. Oxidation parameters had to be controlled to avoid increasing the reflectance or absorptance of the anti-reflective coating.

o Contact area reduction. The same thin oxide used to passivate the emitter was also used to limit the contact area between the grid metallization and the emitter. The busbar metallization was completely isolated from the diffused layer underneath by this oxide. Separate photolithography steps were used to form openings in the thin oxide for contacting and to form the metallization pattern. An alignment technique based on mechanical registration rather than the use of a mask aligner was developed.

o Grid metallization cross-section. This cross-section was increased to minimize possible contributions to series resistance from conduction losses in the gridlines or from contact resistance.

To verify that the procedures we used to form the passivating oxide layer were effective, we prepared several cell samples for external quantum efficiency measurement. These results are shown in Figures 2-5, which are quantum efficiency vs. wavelength curves

for cells produced under the following conditions:

Fig. 2: Baseline structure (Austin cell) with no emitter passivation.

Fig. 3: Thin oxide grown at 870°C.

Fig. 4: Thin oxide grown at 980°C.

Fig. 5: Thin oxide grown at 980°C and then removed.

Each of the samples had untextured surfaces, dual layer anti-reflective coatings, and approximately 20% gridline coverage.

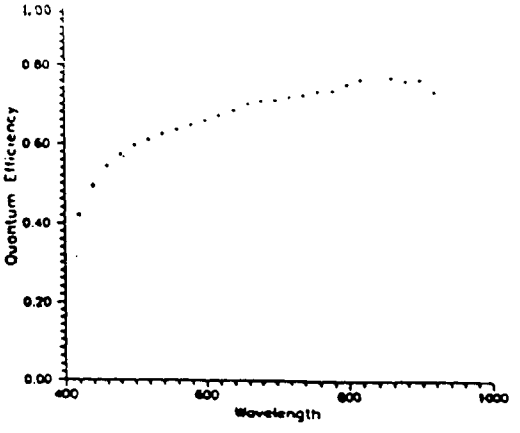


Figure 2
External Quantum Efficiency vs. Wavelength
- No Thin Oxide Grown

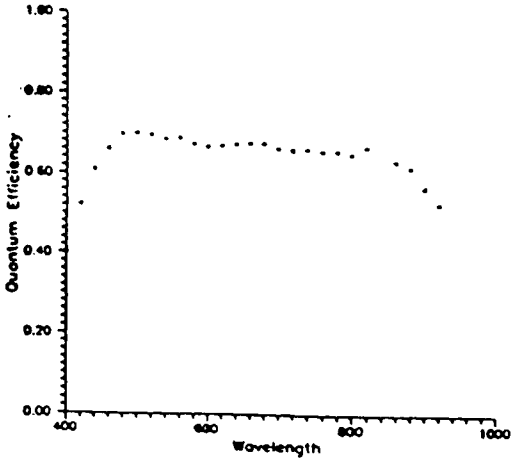


Figure 3
External Quantum Efficiency vs. Wavelength
- Thin Oxide Grown at 870°C

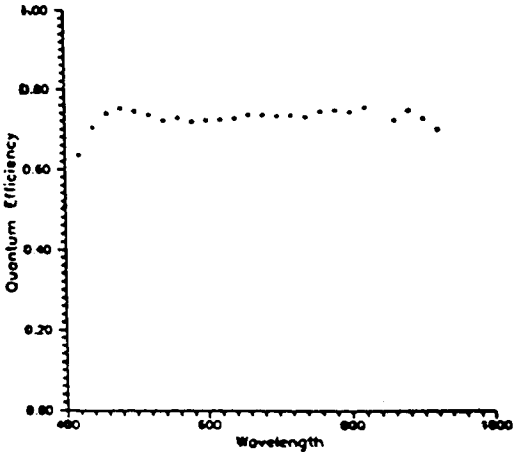


Figure 4
External Quantum Efficiency vs. Wavelength
- Thin Oxide Grown at 980°C

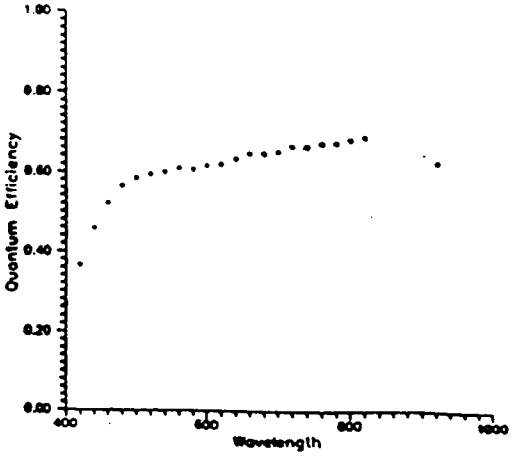


Figure 5
External Quantum Efficiency vs. Wavelength
- Thin Oxide Grown at 980°C
And Then Removed

Figure 2 shows a decrease in quantum efficiency for the unpassivated sample at short wavelengths. This is improved by the thermal oxide present on the front surface of the sample shown in Figure 3 and further improved by the higher temperature thermal oxide present on the sample shown in Figure 4. To determine whether the surface improvements were the result of the actual presence of the passivating oxide or some other related effect such as modification of the diffused layer by the heat treatment, the oxide layer was grown and then removed from the sample of Figure 5. The quantum

efficiency curve for this sample indicates a return to the poorer blue response of the unpassivated sample of Figure 2.

Based on this result, emitter passivation as applied to these test samples was included in the cell design. Although slightly better blue response was achieved using the higher temperature oxidation (980°C), we selected the lower temperature (870°C) to avoid lowering the surface concentration of the diffused layer to the point that contact resistance could become a problem.

The improvement in performance expected by passivating the emitter was estimated using the computer model PC-1D, (developed by D. T. Rover, P. A. Basore and G. M. Thorson). Although actual values of front surface recombination velocity are not precisely known, assuming an improvement from a composite value (for both active area and metallized area) of 1×10^6 to 1×10^4 cm, a gain in short-circuit current density of 5.3% and a gain in open circuit voltage of 3.5% could be expected.

We used PC-1D to optimize the cell design in terms of thickness and bulk resistivity. Figures 6-9 show PC-1D simulations of active area short circuit current density, open-circuit voltage, fill factor, and active area efficiency at 22 suns as a function of bulk resistivity for different thicknesses. The model's default relationship between bulk minority carrier lifetime and impurity concentration was used.

We conducted an experiment to evaluate the relationships modelled in Figures 6-9 and found that, despite an offset of about 1.5% (possibly based on imprecision in reflection estimates entered into the model) the dependence of short-circuit current on thickness was reasonably close to that predicted by PC-1D. The comparison between PC-1D predictions and actual measurements are shown in Figure 18. The experimental results for fill factor and open-circuit voltage were apparently dominated by processing differences and did not show the behavior predicted by the model over the limited thickness range evaluated.

The model predicts the highest efficiency for lower bulk resistivity silicon. As bulk resistivities approach 2.0 ohm-cm, better overall performance is expected for thicker

FIGURE 6

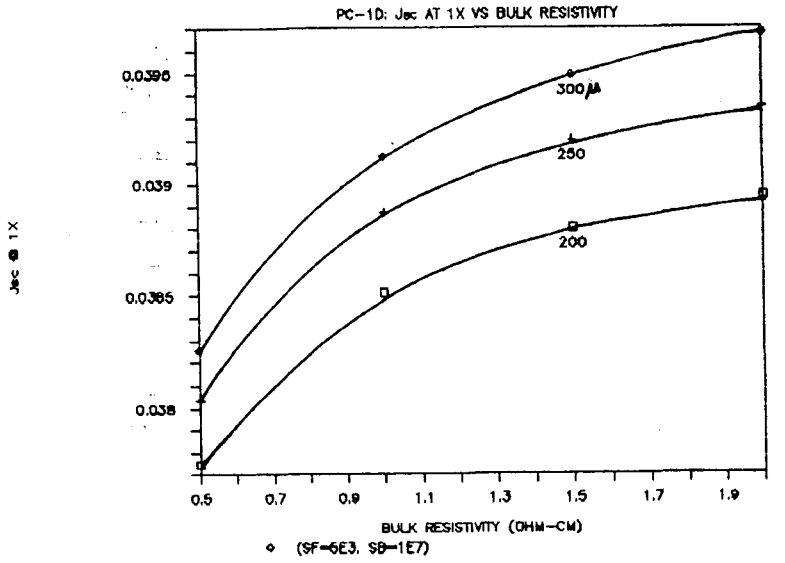


FIGURE 7

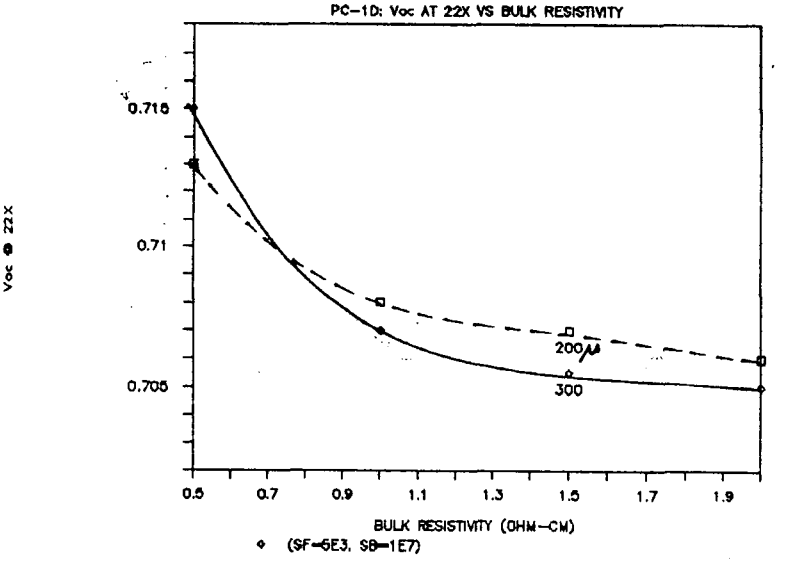


FIGURE 8

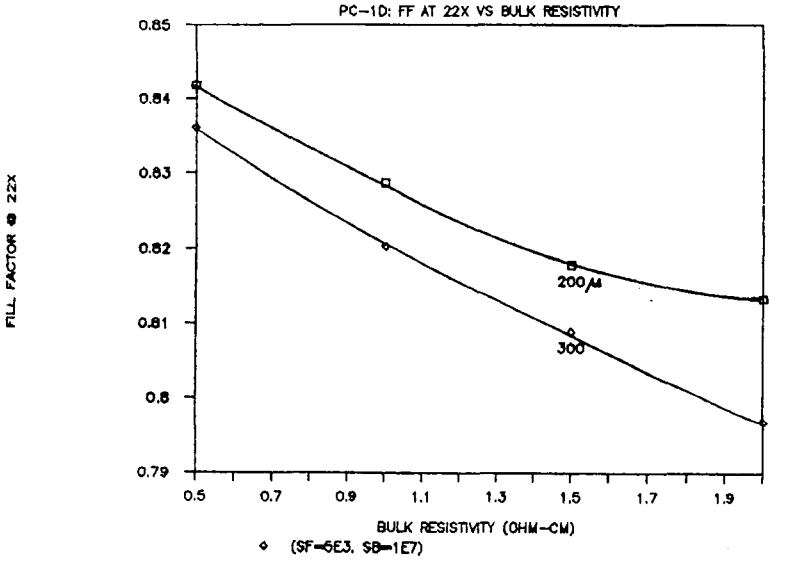


FIGURE 9

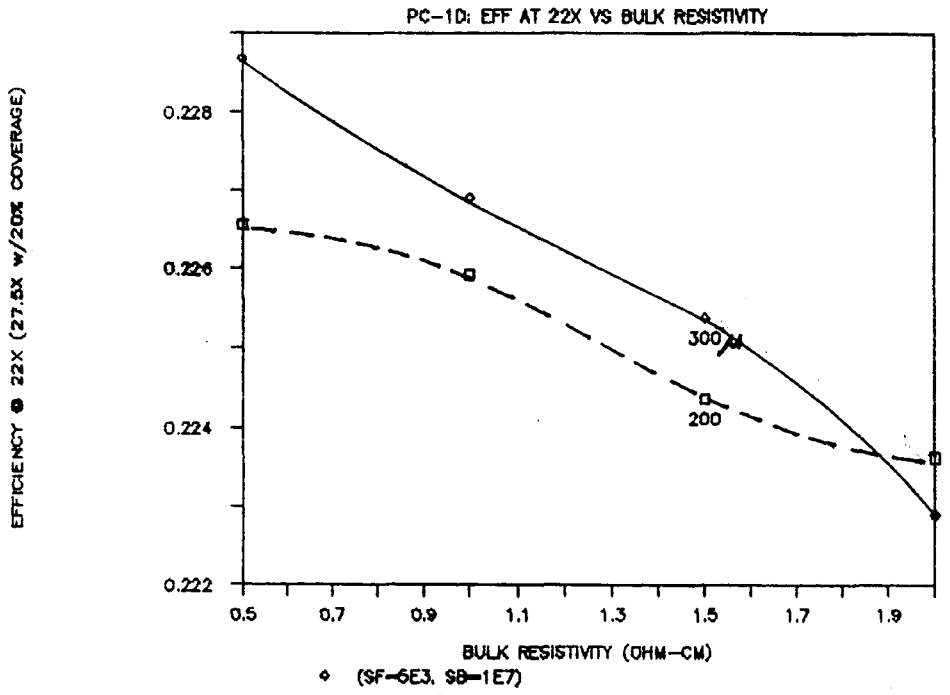
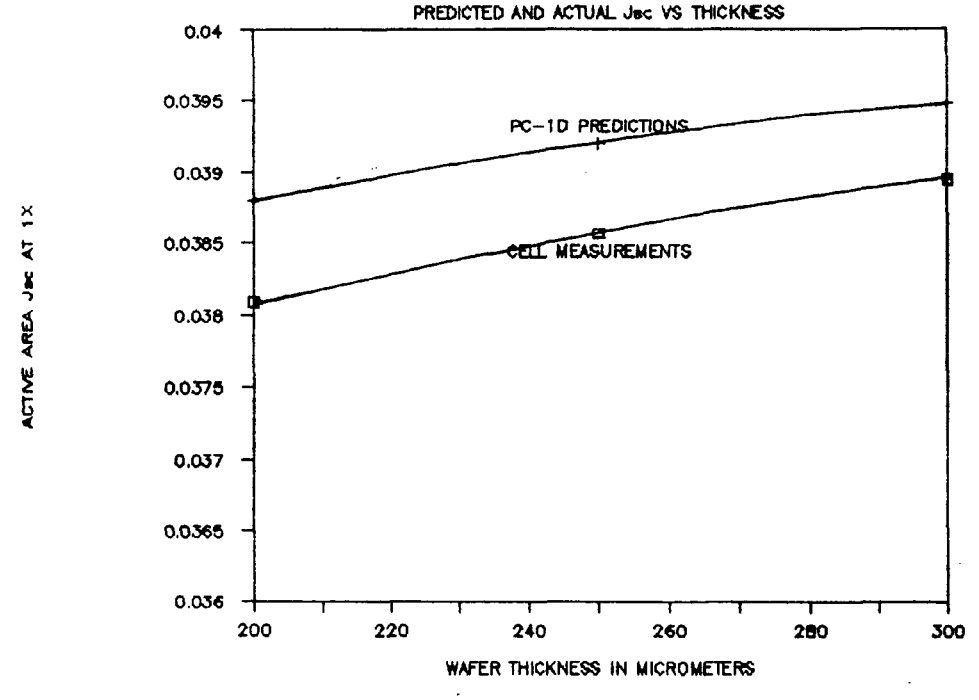


FIGURE 10



substrates. Above that resistivity range, losses from resistance in the bulk, overpower the gain in short-circuit current predicted for thicker substrates.

We chose 300 micrometer substrates, which with the added metallization thickness that resulted after plating, were about as thick a wafer as we felt could be reasonably handled in production. We used .8 ohm-cm silicon because we were able to obtain a sufficient quantity of 5-inch diameter silicon to work with within the limited time frame of the program. We used both silicon grown by the standard Czochralski technique (CZ) and a batch of silicon grown using an experimental magnetic stabilization technique (MCZ).

Based on the expected improvement predicted for the lower resistivity substrates, we also evaluated more heavily doped, .18 ohm-cm, float zone 4-inch diameter silicon. These, along with other 4-inch diameter 1 ohm-cm float zone silicon samples, resulted in cells that were shorter than the cell size required for this program, but provided additional information.

2.3 CELL STRUCTURE

Figure 10 shows a cross-sectional view of the cell developed for this program. As in the Austin cells, the front surface has a random pyramidal texture covered by a dual-layer anti-reflective coating. However, underneath the anti-reflective coating is a passivating oxide that restricts the area of contact to a fraction of the total metallized area, as shown in Figure 11.

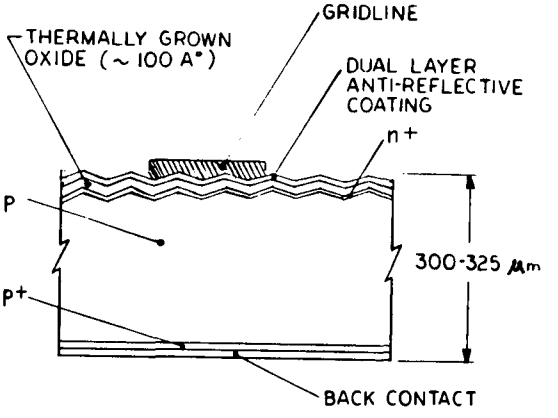


Figure 11
Solar Cell Cross Section

A single diffused layer covers the entire front surface, including the area under the cell busbars. Contact is made to the diffused region by a series of rectangular openings in the thin oxide at regular intervals along the length of the gridline.

A back surface field, formed by alloying aluminum paste, covers the entire back of the cell. Contacts are made by evaporating layers of titanium and palladium and then electroplating 13 micrometers of silver to both front and back.

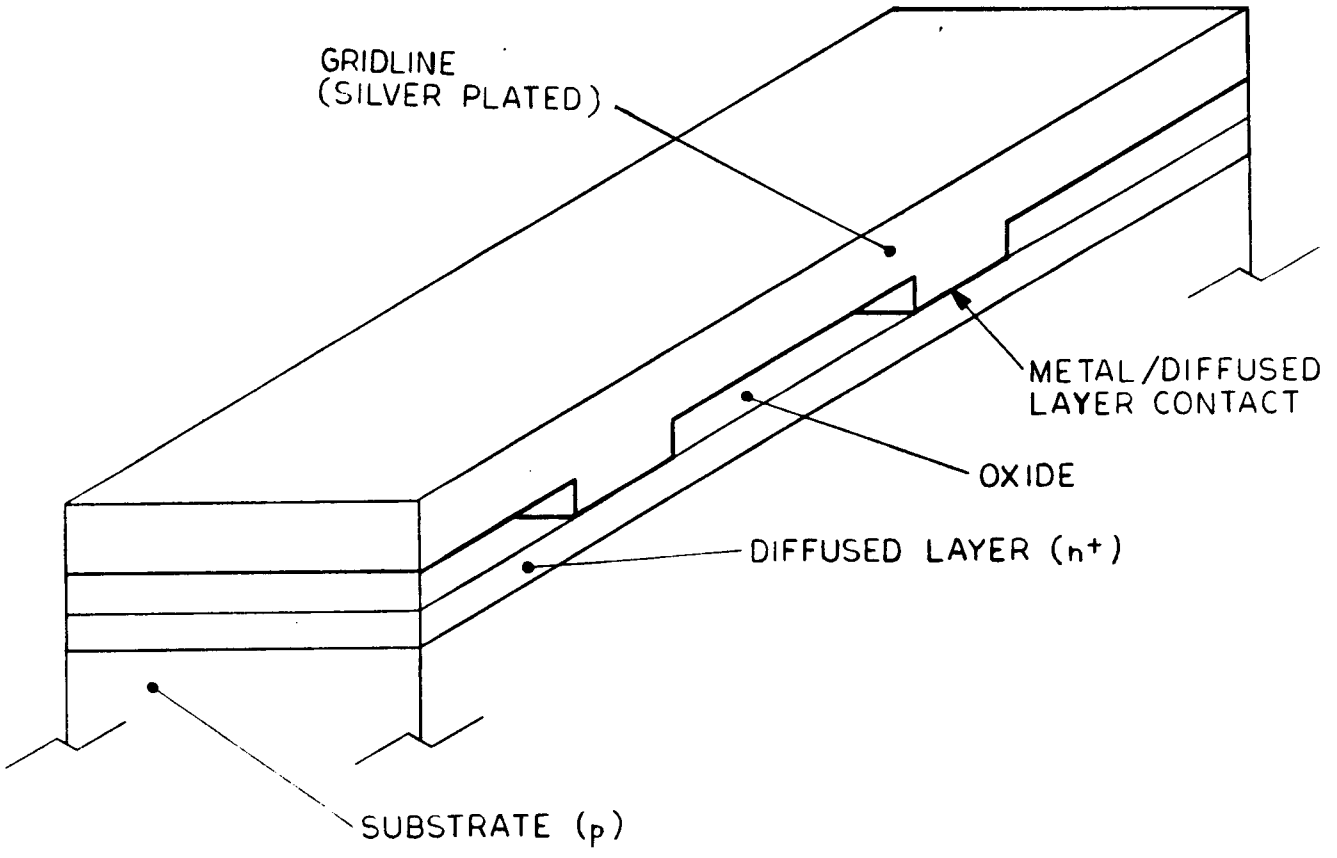


Figure 12
Detail of Contact Between Gridline and Diffused Layer

2.4 PROCESS SEQUENCE

Table I outlines the steps used to fabricate the cells developed for this program. The diffusion temperature was reduced from the temperature used for the Austin program, resulting in an increase in sheet resistivity from 75 ohm per square to 100 ohm per square. Following the growth of the thin oxide at 870°C, the sheet resistivity decreased to 75 ohm per square providing adequate diffused layer conductivity without excessively compromising short wavelength response.

Two photolithography steps were used: one to pattern the thin passivating oxide, the other to form a mechanically aligned metallization pattern. Preliminary trials were run to attempt to include possible further optimization of the cell design, such as deep diffusion under the gridlines or elimination of diffused layers under the bus bars. However, we settled on the sequence of Table I, which we thought would have the best chance of meeting the program goals within the allotted time period.

TABLE I

PROCESS SEQUENCE FOR 22X CONCENTRATOR CELLS

STEP	COMMENT
NaOH ETCH	300-325 MICROMETERS
KOH ETCH	4% SOLUTION WITH IPA, 100° C, 12 MIN, RANDOM PYRAMIDS 10 MICROMETERS HIGH.
ROUNDING ETCH	HNO_3:HF, 20:1, 90 SEC
RCA CLEAN	
DIFFUSION	PHOSPHINE SOURCE, 100 OHM/SQ (BEFORE OXIDE GROWTH)
HF DIP	
RCA CLEAN	
GROW THIN OXIDE	870° C, O_2 FLOW FOR 45 SECONDS
ALLOY/HCL ETCH	ALUMINUM PASTE
PHOTO 1	THIN OXIDE PATTERN
HF/RESIST REMOVAL	
PHOTO 2	FRONT METAL CONTACT PATTERN ALIGN BY MECHANICAL REGISTRATION
FRONT TiPd EVAP	
LIFTOFF	
BACK TiPd/Ag EVAP	
AG PLATE	13 MICRONS HIGH
AR	1/4 WAVELENGTH: TiO_x, Al_2O_3
SINTER	
CUT	DICING SAW
SINTER	EDGE PASSIVATION
TEST	AM1.5 DIRECT

3 RESULTS

After several preliminary runs to optimize process parameters, we ran an experiment using several different types of silicon based on the cell structure and process sequence described above.

As originally planned, we sent cells to Sandia for measurement at concentration without attachment of covers or interconnects. However, this interim measurement of active area efficiency did not turn out to be a reliable predictor of final results because of large series resistance losses. This is most likely because the probe spacing did not sufficiently simulate the interconnects designed for this concentration level. To circumvent this problem, we selected several cells from each group and sent them to Entech Corporation where copper interconnects were attached to the cells.

Prismatic covers were also attached to the cells. The presence of the covers eliminated uncertainties inherent in estimating active areas on uncovered cells often leading to overly optimistic predictions of covered cell performance. The cells were then sent to Sandia for measurement at concentration.

Results for the best 20 cells measured in this manner are shown in Table II. The best cell had an efficiency of 20.34% with three-quarters of the group having an average efficiency exceeding 20% at 20 suns. The average for the 20 cells was 19.8% using a small spectral mismatch factor calculated at Sandia to account for differences between the test cells and the calibration cell. These same cells were also measured at Entech Corporation where a somewhat higher, 20.3% average efficiency was measured for the group. The efficiencies are based on the illuminated area which excludes the wide bus bars on the edges of the cells.

The cells peak in efficiency roughly between 20 and 30 suns as shown in Figure 13. The difference between the best and worst cells of Table II can be attributed to a large extent to differences in fill factor, although the specific cause of that difference has not been determined. On each wafer processed were two cell patterns. The metal/diffused

layer contact area for one was 3.1% and for the other 6.2%. No significant difference between the two were detected in the data taken at concentration.

FIGURE 13

EFFICIENCY VS CONCENTRATION

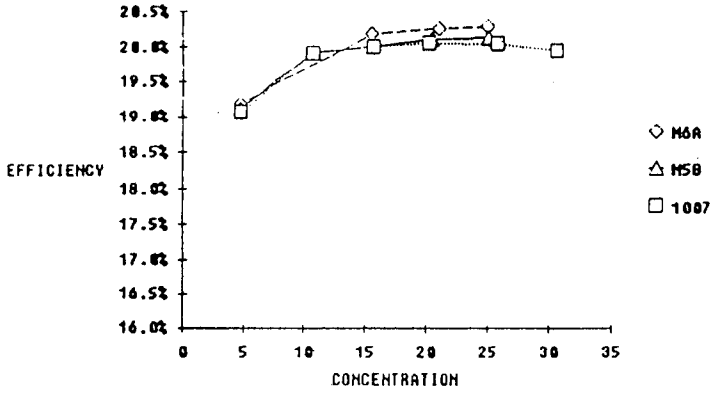


TABLE II

CELL EFFICIENCIES AT 20 SUNS AM1.5 DIRECT
WITH COVERS AND INTERCONNECTS ATTACHED

CELL I.D.	EFF @20X	CUMULATIVE EFF
M6A	20.34%	20.34%
M5B	20.29%	20.32%
C37A	20.25%	20.30%
M4A	20.25%	20.28%
C39B	20.18%	20.26%
1007	20.18%	20.25%
C19A	20.13%	20.23%
M2A	20.02%	20.21%
M9B	19.97%	20.18%
M4B	19.92%	20.15%
C39A	19.88%	20.13%
M3B	19.71%	20.09%
M7B	19.68%	20.06%
M6B	19.61%	20.03%
M1A	19.59%	20.00%
M12A	19.43%	19.96%
M5A	19.41%	19.93%
M7A	19.34%	19.90%
M12B	19.32%	19.87%
C17A	19.19%	19.83%

Table III shows results from each of the four groups of silicon used to process these cells. The .2 ohm-cm float zone silicon resulted in lower short-circuit current densities, which were not compensated for by the small improvements in open-circuit voltage and fill factor. The standard Czockralski (CZ) and the magnetically purified (MCZ) .8 ohm-cm silicon produced cells with no detectable difference in short-circuit current density. The 1 ohm-cm float zone silicon suprisingly had lower short-circuit current densities than either of the Czockralski groups with nearly the same doping level.

TABLE III

SUMMARY OF COVERED CELL RESULTS AT 20 SUNS

SILICON		Jsc @1X	Voc @20X	FF @20X	EFF @20X	SAMPLE SIZE
1 OHM-CM CZ	MEAN:	0.0364	0.683	0.794	19.8%	6
	MAX:	0.0367	0.686	0.810	20.25%	
	MIN:	0.0359	0.681	0.776	19.1%	
	S.D.:	0.0002	0.002	0.012	0.5%	
1 OHM-CM MCZ	MEAN:	0.0364	0.681	0.797	19.8%	14
	MAX:	0.0368	0.686	0.816	20.34%	
	MIN:	0.0358	0.677	0.781	19.3%	
	S.D.:	0.0003	0.003	0.010	0.3%	
1 OHM-CM FZ	MEAN:	0.0357	0.681	0.810	19.7%	5
	MAX:	0.0363	0.686	0.817	20.18%	
	MIN:	0.0349	0.679	0.806	19.3%	
	S.D.:	0.0005	0.003	0.004	0.3%	
.2 OHM-CM FZ	MEAN:	0.0347	0.685	0.817	19.4%	4
	MAX:	0.0350	0.686	0.822	19.55%	
	MIN:	0.0343	0.683	0.813	19.3%	
	S.D.:	0.0003	0.001	0.003	0.1%	

4 POTENTIAL FOR FURTHER OPTIMIZATION

The following approaches were considered during the course of this work but fell outside the scope of the program:

1) Eliminate one photolithography step by etching the thin oxide mask immediately before metal deposition. This would passivate the emitter only, however, and would place the entire metallized area in contact with the diffused layer.

2) Use a very deep diffused layer across the entire front surface to reduce recombination. This could be used in conjunction with the first approach to eliminate a photolithography step.

3) In contrast, addition of a photolithography step, mask alignment, and a diffusion step would permit further potential performance improvements of the device by allowing separate optimization of the diffused layers for the emitter and the contact areas.

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