Conf-921005--12

LBL-32278
UC-000

Lawrence Berkeley Laboratory
UNIVERSITY OF CALIFORNIA

Engineering Division

Received by OSTI

DEC 21 1992

Presented at the IEEE 1992 Nuclear Science Symposium, Orlando, FL, October 25–31, 1992, and to be published in the Proceedings

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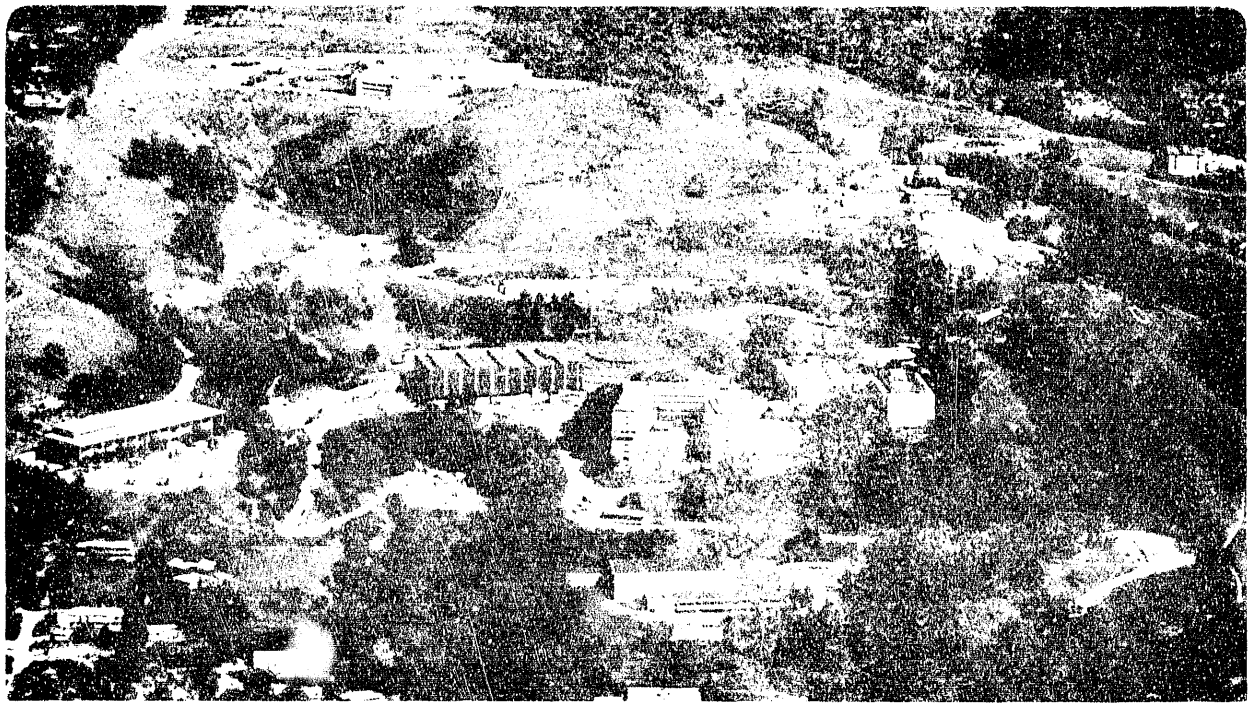

Prepared for the U.S. Department of Energy under Contract Number DE-AC03-76SF00098

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A LOW POWER 12-BIT ADC FOR NUCLEAR INSTRUMENTATION

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MASTER

A LOW POWER 12-BIT ADC FOR NUCLEAR INSTRUMENTATION

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ABSTRACT

A low power, successive approximation, analog-to-digital converter (ADC) for low rate, low cost, battery powered applications is described. The ADC is based on a commercial 50 mW successive approximation CMOS device (CS5102). An on-chip self-calibration circuit reduces the inherent differential non-linearity to 7%. A further reduction of the differential nonlinearity to 0.5% is attained with a four bit Gatti function. The Gatti function is distributed to minimize battery power consumption. All analog functions reside with the ADC while the noisy digital functions reside in the personal computer based histogramming memory. Fiber optic cables carry all digital information between the ADC and the personal computer based histogramming memory.

I. INTRODUCTION

Our initial application of a low power, low noise ADC was with a gamma-ray spectrometer planned for NASA's comet rendezvous mission, CRAF. This ADC and a companion low power gated integrator were an integral part of the planned pulse processing electronics [1].

Many experiments are often located in electrically noisy environments. Some of the common sources of noise include ground loops and high frequency noise pickup in cables. Today, laboratory instrumentation commonly include personal computers (PC's), whose video monitors and switching power supplies are often a major source of noise. Presented here are techniques to minimize or eliminate some of these noise sources without sacrificing unclear instrumentation quality. It is desirable to convert analog signals to digital signals as close to the analog signal source as possible. Therefore, all sensitive analog circuitry and the ADC reside in the same battery powered NIM bin. Communication between the ADC and the PC is best done over fiber optic cables, since fiber optic cables are ideally suited to the transmission of digital information without creating conduits for electrical noise. Our present application, instrumentation of micro-calorimeters [4], is an extreme example of low noise requirements. Noise levels on the order of a few tens of eV, or less, are not uncommon.

II. CIRCUIT DESCRIPTION

Refer to the block diagram in Fig. 1. The serial ADC is in NIM bin 1, which is battery powered. The serial to parallel converter is in NIM bin 2, whose only connections to bin 1 are two fiber optic cables. Bin 2 is electrically cabled to a modified PC based pulse height analyzer(PHA). It is a commercial Nucleus PHA with modifications to accept an external 13-bit parallel digital word instead of the normal ADC output. Bin 2 and the PHA process only digital data, where line power and switching power supplies are not detrimental to data.

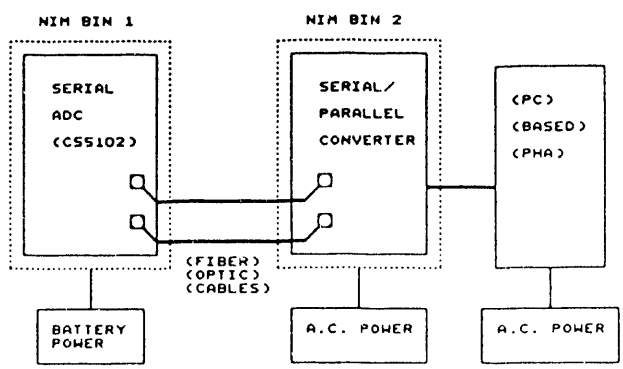

Fig. 1. Block Diagram

Refer to Fig. 2A. This particular serial ADC is appropriate to our application in several ways. Serial ADC's are inherently lower power than parallel ADC's due to their single bit architecture and offer options to place some of the external circuitry in other places. There is an internal self-calibrating feature. An internal track and hold circuit minimizes external support circuitry even more.

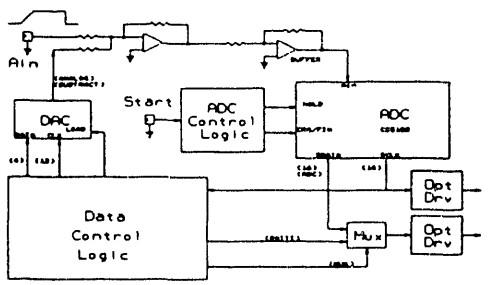

Fig. 2A Analog to Digital Converter

A flat topped analog signal, either from a peak detector stretcher or a gated integrator, drives the ADC module at input, Ain. The internal track and hold circuit has a capacitance at this node. The value of this capacitance is sufficiently high to require a buffer with a low output impedance for accuracy and moderate slew rate.

A digital "START" signal initiates a conversion cycle. Some ADC logic is required to sequence the ADC through this conversion cycle. Acquiring the analog input is an internal process requiring two modes of operation. The first mode is the coarse mode, where a high slew rate amplifier is enabled to acquire the input level as quickly as possible, but only coarsely. The second mode is the fine mode, where a high gain amplifier accurately acquires the analog input, albeit slowly. This acquisition technique provides the highest throughput with the most accuracy. After the coarse and fine sequence, the ADC logic generates a "HOLD" signal, which sets the ADC in a hold mode and begins conversion.

There are two inexpensive, commercially available fiber optic cables, light emitting diodes (LED's), optical receivers, and connecting hardware. No special tools are required for assembling the system but some care should be put into polishing the ends of the fibers to maximize light coupling between the LED and receiver. As the only means of communication between the two bins, the fiber optic cables electrically isolate the battery powered bin from the data acquisition part of the system. A 16-bit serial data format is used for communication. The first twelve data bits are ADC data and the last four data bits are Gatti data. There are sixteen serial clocks. The data control logic detects twelve data bits and then multiplexes the four Gatti bits to fill the sixteen bit format.

A digital to analog converter (DAC) is part of the analog subtraction circuit. The data control logic loads a four bit digital number into the DAC and an equivalent analog value, in the range of zero to sixteen least significant bits (LSB's), is subtracted from Ain. Later, this analog subtraction is complemented with a digital addition of the same value.

Refer to Fig. 2B. This module converts serial data to parallel data. Two optical receivers convert optical signals to electrical signals. Sixteen serial data bits are shifted into a sixteen bit shift register by sixteen serial clocks. The sixteen bit data format consists of twelve bits of data and four bits of Gatti data. These Gatti bits are binarily added to the ADC data bits in the 12-bit adder to complement the analog subtraction, which took place before the analog to digital conversion. Addition requires a fixed time. The control logic circuit then checks for overflow. If it detects no overflow, the data is unchanged. If it detects overflow, the data is changed to all zeroes. Currently, all overflow data is placed in channel zero. However, a more meaningful solution is to place it in the highest channel number. In either case, a data ready FF is set and data ready(DRDY) is sent to the PHA. The PHA reads the data and returns a data acknowledge(DACK) to complete the handshake.

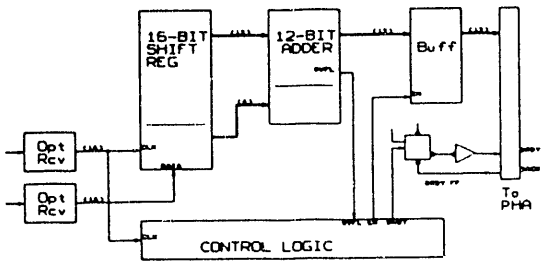

Fig. 2B. Serial to Parallel Converter

III. FUTURE ACCOMMODATIONS

Increasing the dynamic range of any analog signal processor is generally desirable. The analog input to this ADC is limited to +5 volts. On the other hand, the distributed architecture as presented here can readily accommodate a one bit increase from 12 to 13 bits of digital data. A novel idea conceived but not implemented in the design of a gated integrator [2] can exploit this one additional bit. The general idea is to stack one 12-bit range on top of another 12-bit range. The 13th bit value defines which of the two ranges. If the signal is in the high range, the bit is a one. If the signal is in the low range the bit is a zero. In either case the ADC converts a 0 volt to +5 volt analog signal just as before but now receives the 13th bit as a separate digital signal. The ADC concatenates the 13th bit to the 12-bits of converted data forming a 13-bit data for the PHA.

IV. TEST RESULTS

Differential Non-Linearity test. The ADC was tested with an analog ramp generator. A modified PC-based PHA was used to histogram data from the ADC.

Conversion time...80 us
DNL.....0.5% pk-pk
INL.....5% (upper 95%)
Input Range.....0 to 5.0v

V. ACKNOWLEDGMENTS

This work was supported by NASA through the U.S. Department of Energy under Contract No. DE-AC03-76SF00098.

Reference to a company of product name does not imply approval nor recommendation of a product by the University of California or the U.S. Department of Energy to the exclusion of others that may be suitable.

VI. REFERENCES

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