JFET Monolithic Preamplifier with Outstanding Noise Behaviour and Radiation Hardness Characteristics

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Abstract

A second series of monolithic preamplifiers based on epitaxial channel JFETs and intended for calorimetry at hadron colliders has been realized. The employed buried layer process has been upgraded, resulting in a lower pinch-off voltage and a reduced power dissipation. Results will be presented on noise, dynamic behaviour and radiation damage. New versions of the preamplifier have been designed for both large capacitance detectors and for low capacitance pre-shower detectors.

I - INTRODUCTION

The motivations that led to the design of a monolithic preamplifier based upon epitaxial-channel, diffused-gate N-JFETs have been discussed in previous papers [1, 2, 3]. The circuit diagram of the charge-sensitive preamplifier, realised by means of a junction-insulated monolithic process based upon a buried layer technology, is shown in fig. 1 [2, 3].

In the version implemented so far the feedback elements R_F, C_F and the load resistors R_1, R_2 are off-the-chip components. In the circuit of fig. 1 J_1 and J_2 constitute a cascode structure. The JFETs J_3, J_4, J_7 realise a bootstrapped load to present a high impedance on the drain of J_2. The JFET J_7 serves also the purpose of buffering this high impedance point. The JFET J_8 is the output stage. The cascoded current generator (J_5, J_6) maintains the gain of the buffer J_7 as close as possible to unity, to avoid any spoiling in its bootstrapping action which results in a decreased open-loop gain of the preamplifier. The standing current in the input branch is determined by the current source J_3, while the one in the second branch is determined by the current source J_5. In the closed-loop connection the gate-to-source voltage of J_1 is fixed by the reference current of J_3. It determines through the resistors R_2 and R_1 the current in J_8 and the voltage on its source, and consequently the voltage of the high impedance point on the drain of J_2. The JFETs J_1, J_2, J_7, J_8 define the signal path inside the preamplifier and therefore are realised as shorter channel devices with 5 μm gate length (SC). The LC JFETs J_3, J_4, J_5, J_6, that implement current references and active loads are devices with a longer channel (7 μm).

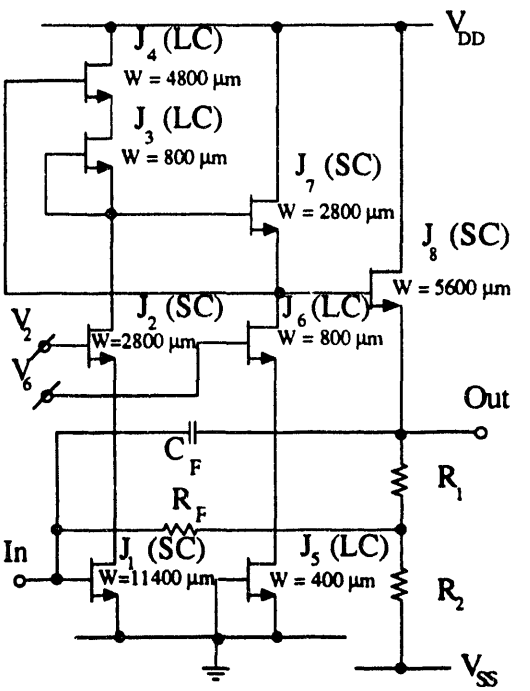

Fig. 1 - Charge-sensitive preamplifier employing epitaxial-channel, diffused-gate N-JFETs.

A microphotograph of the preamplifier chip is shown in fig. 2. The very first realisation of the N-JFET preamplifier suffered from a low yield due to a poor control of the pinch-off voltage. This resulted in devices that, though functional, showed standing currents and power dissipation levels exceeding the design values. The analysis of their noise and small signal behaviour, however, proved to be very useful in setting up a comparison with the characteristics of the specimens coming out from a second batch. This one showed a much better control of the pinch-off voltage, with current and power levels very close to the expected values.

A new version which is now being implemented has been designed with the aim of making the circuit behaviour largely independent of the process parameters. The results obtained with the first batches of the monolithic N-JFET preamplifier are discussed in this paper along with the criteria employed

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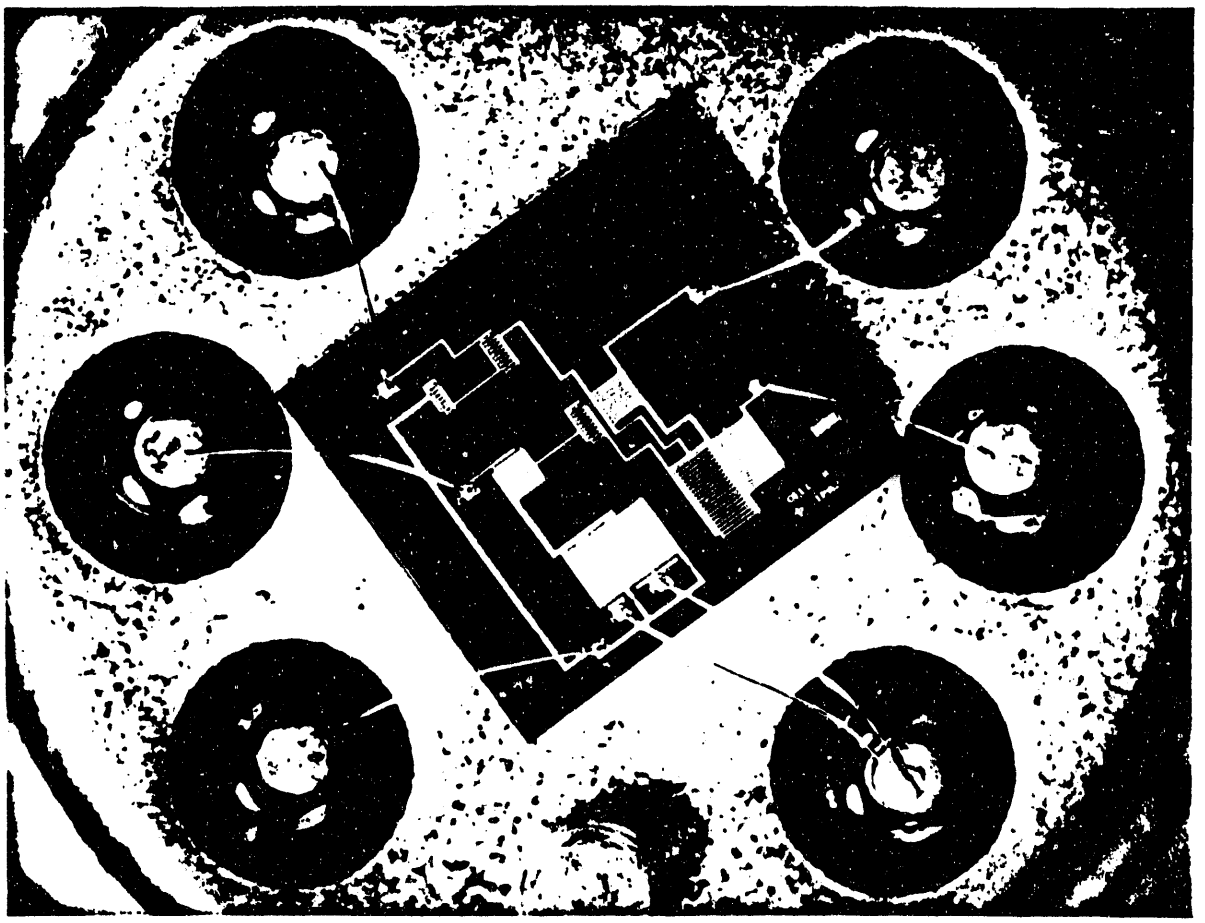


Fig. 2 - Microphotograph of the preamplifier chip.

in the design of the new circuit.

II - ANALYSIS OF THE RESULTS OBTAINED WITH THE N-JFET PREAMPLIFIERS

In this section the results obtained with monolithic preamplifiers coming out from the first production batches will be discussed. A summary of results on the behaviour of some preamplifiers featuring different values of the standing current I_D in the input JFET is provided in Table I. The layout and the package of some of the preamplifiers belonging to these two batches, those in the dual-in-line package, were designed so as to provide access to some internal nodes. This was done to allow parameter measurements on the individual devices by means of test pads added in the layout and bonded to pins of the chip carrier. These connections, however, results in an increase of the stray capacitances, particularly in the high impedance point on the drain of J_2. In the TO-78 metal package preamplifiers the additional bonding pads have no longer been introduced, so that their frequency response is not limited by unduly added strays.

The preamplifier labelled 1 in the table belongs to the first batch which, as pointed out in the introduction, has a pinch-off voltage larger than the design value. It features a standing current I_D of 9.2 mA in the input branch of fig. 1. The input device J_1 at this current has a measured g_m of 48.3 mA/V. The essential characteristics of this preamplifier labelled 1 in Table I are described by the plots (a) through (c) in fig. 3.

From the frequency dependence of the magnitude of the open-loop gain, plotted in fig. 3a, it can be inferred that the product of the frequency corresponding to the dominant pole and the dc gain is 200 MHz. At large values of the open-loop gain however the secondary pole, which occur at a frequency slightly below 30 MHz, becomes a limitation. The outstanding noise behaviour of this preamplifier is apparent in fig. 3b. The noise spectrum referred to the input of the preamplifier consists of a Lorentzian term with a characteristic frequency around 300 Hz added to a white noise component of less than 0.6 $nV/\sqrt{Hz}$. The fifth and sixth columns of Table I compare the measured values of the white noise and those calculated from the measured or extimated transconductance of J_1, on the basis of the theoretical relationship for the thermal noise in the channel, that is $dv^2/df = 4kT \cdot 0.7/g_m$. For instance, in the case of the specimen 1 in Table I, the gate spreading resistance in J_1 and the white noise contributions from devices other than the input JFET do not add more than

16 % to the theoretically expected thermal noise in J_1. Plot 3c describes the dependence vs C_D of the Equivalent Noise Charge (ENC) where C_D is the capacitance added to the preamplifier input to simulate the detector. The shaping filter used for these measurements is unipolar semigaussian of peaking time t_p. According to the results plotted in fig. 3c the $dENC/dC_D$ sensitivity at 1 μs peaking time is 2.87e/pF. The preamplifiers labelled 2 through 6 in Table I belong to the second batch featuring pinch-off voltages much closer to the design values. The standing currents in the input devices range from 2 to 5 mA. These values and the relevant g_m were obtained by indirect methods.

The plots of fig. 4 describe the basic features of the metal TO-78 package circuit, which is labelled 6 in Table I. As a first remark from Table I and fig. 4a, in spite of its lower g_m, the preamplifier 6 has a product of the dominant pole frequency by the dc gain (200 MHz). This is related to the lower strays shunting the drain of J_2 in the metal case version.

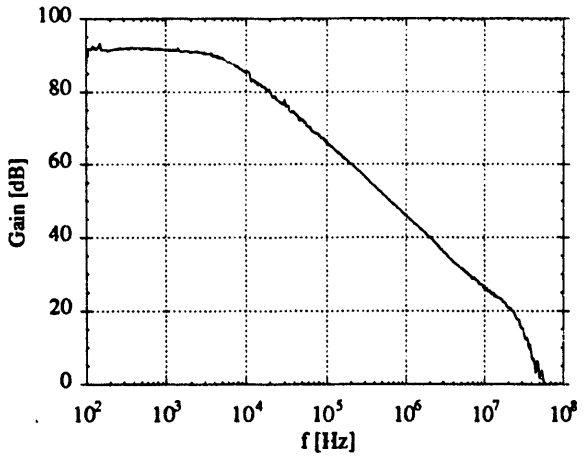
The noise behaviour of the preamplifier 6 is shown in fig. 4b. The experimental white noise is about 0.68 $nV/\sqrt{Hz}$ and the theoretical one is 0.61 $nV/\sqrt{Hz}$, that is the white noise contributions coming from devices other than the input JFET do not add more than 11% to the theoretically expected thermal noise in J_1.

The plot 4c describes the dependence of the ENC on the capacitance added at the preamplifier input. According to the results plotted in fig. 4c the $dENC/dC_D$ at 1 μs peaking time is 3.85 e/pF, which is very close to the theoretically expected value (3.52 e/pF).

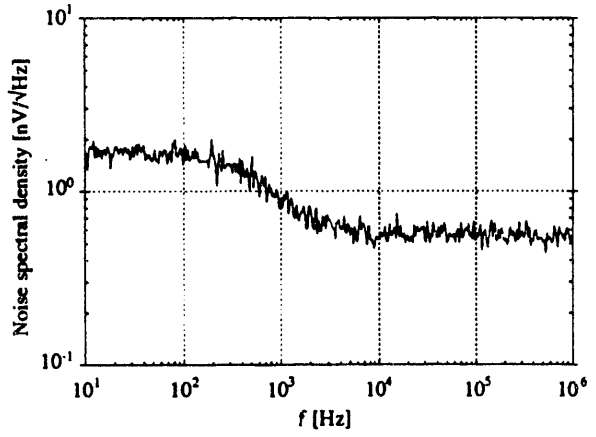
Table I

Main Features of the Monolithic Preamplifiers

P	FEATURES	I_d[mA]	$g_m\left[\frac{mA}{V}\right]$	$SW_e\left[\frac{nV}{\sqrt{Hz}}\right]$	$SW_t\left[\frac{nV}{\sqrt{Hz}}\right]$	$\frac{SW_e}{SW_t}$	GBW [MHz]
1	TEST PADS ADDED (ceramic carrier)	9.2	48.3	0.57	0.49	1.16	200
2	TEST PADS ADDED (ceramic carrier)	1.9	22	0.76	0.72	1.05	112
3	TEST PADS ADDED (ceramic carrier)	2	23	0.75	0.70	1.07	127
4	NO TEST PADS (TO-78)	3	26	0.73	0.68	1.07	194
5	TEST PADS ADDED (ceramic carrier)	4	32	0.66	0.60	1.10	136
6	NO TEST PADS (TO-78)	5	31	0.68	0.61	1.11	200



(a)



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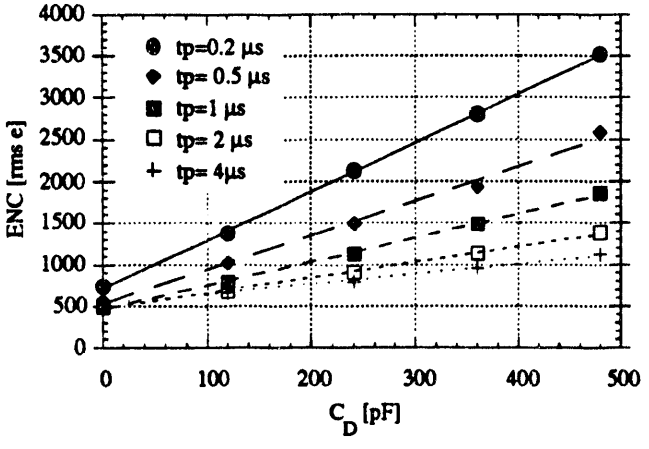


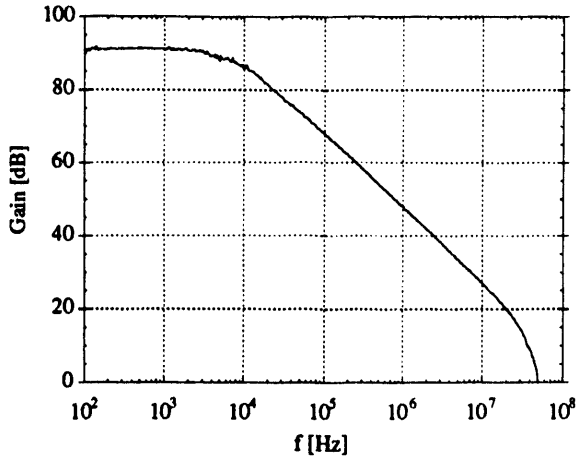
(c)

Fig. 3 - Characteristics of the preamplifier labelled 1 in Table I.

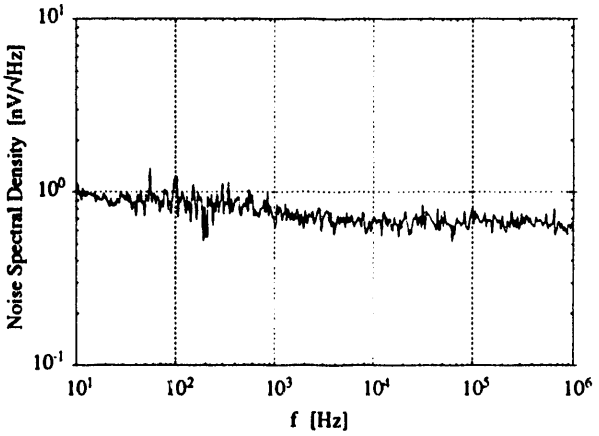
(a) Open-loop gain versus frequency dependence.

(b) Spectral density of the noise voltage referred to the preamplifier input as a function of frequency.

(c) ENC as a function of the capacitance C_D added at the input. The peaking time t_p of the weighting function is the parameter in the family of curves.



(a)



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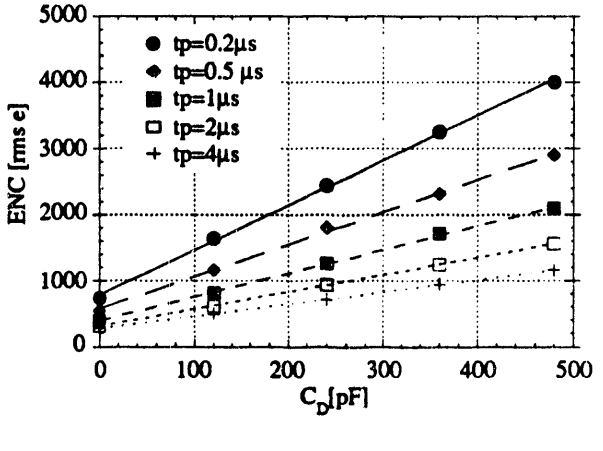


(c)

Fig. 4 - Characteristics of the preamplifier labelled 6 in Table I.

(a) Open-loop gain-frequency dependence.

(b) Spectral density of the noise voltage referred to the preamplifier input as a function of frequency.

(c) ENC as a function of the capacitance C_D added at the input. The peaking time t_p of the employed weighting function is the parameter in the family of curves.

III - RADIATION HARDNESS CHARACTERISTICS

The discussion about the radiation hardness characteristics of the buried layer N-JFET preamplifier is not one of the main subjects in this paper, for the relevant information has been provided elsewhere [4, 5, 6]. Very concisely, the preamplifiers belonging to the first production batch have been exposed to subsequent irradiation steps of ^{60}Co γ-rays up to a 40 Mrad integrated dose. The circuits were functional with unnoticeable degradation in their signal behaviour up to the highest value of the absorbed dose. A noise degradation was observed, as illustrated in fig. 5.

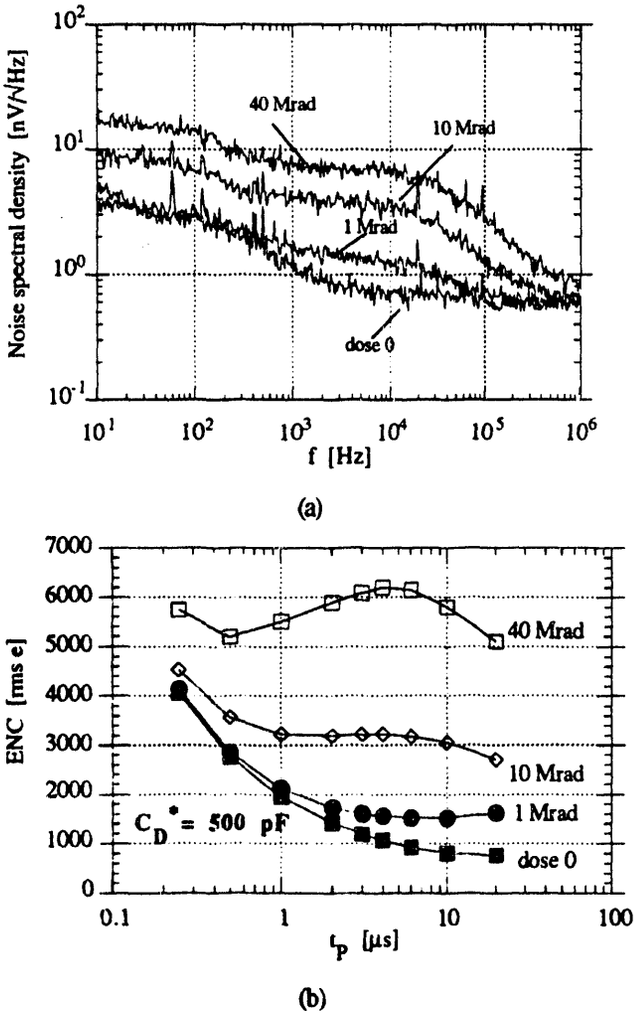


Fig. 5 - Noise degradation in a preamplifier exposed to increasing doses of ^{60} Co γ-rays.
(a) Noise voltage spectrum.
(b) Equivalent Noise Charge.

Analysis of the plots of fig. 5a points out that the irradiation seems to be responsible for a modification in the low frequency portion of the spectrum with the appearance of a Lorentzian term with the characteristic frequency of a few tens of kHz. The white noise portion of the spectrum is virtually unaffected. Consequently, the plots of the ENC as a function of the peaking time of the filter (fig. 5b), show that the effect of irradiation becomes smaller as t_p is reduced. If the plots of fig. 5b are extrapolated to the region of t_p, that is of interest for the applications at the future Hadron colliders, it may be inferred that the tested circuits seem to have an adequately low radiation sensitivity in their noise behaviour.

Besides, the monolithic preamplifier can be considered as radiation hard as a discrete circuit made of single devices of the same characteristics.

The monolithic circuit turns out to be, for instance, less sensitive to γ-radiations than GaAs discrete preamplifier [7].

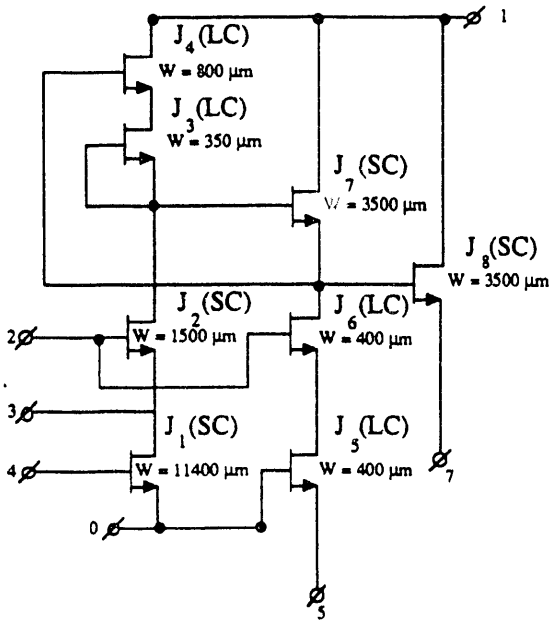
IV - PREAMPLIFIER WITH REDUCED DEPENDENCE ON THE PROCESS PARAMETERS

The realisation of a new version of the monolithic N-JFET preamplifier is now under way. The new design has been improved in two aspects. First, measures were taken to reduce as much as possible the dependence of the circuit behaviour on the process parameters. In particular, the possibility has been provided to externally adjust the standing current in J_1, so as to keep its transconductance and therefore the white noise of the preamplifier as well as its power dissipation largely predictable.

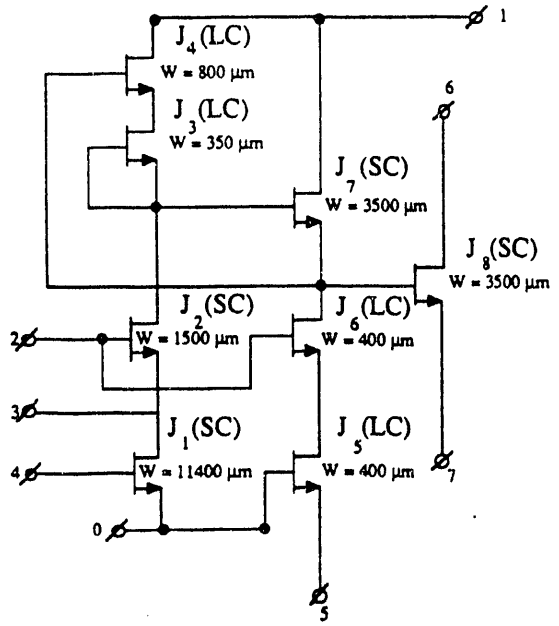
Secondly, the circuit has been modified in order to suit two different connections: the ordinary charge-sensitive one and the so called current feed-by configuration [8,9].

The new monolithic structures are shown in fig. 6a and b. They differ simply for the fact that the drain of J_8 is connected to the positive bias metal bus in the case of fig. 6a while it is terminated to an external pin in the case of fig. 6b. The structure (a) is used to implement the ordinary charge-sensitive connection, while (b) is employed in the combined charge-sensitive and current feed-by connection as shown in fig. 7. The configuration of fig. 7 is designed around the monolithic structure of fig. 6b. The open drain configuration of J_8 makes a current-sensitive output available. The voltage V_o taken on the source of J_8 implements the charge-sensitive function. If B were an ideal buffer with an extremely large input impedance and the monolithic structure were ideally free from bandwidth limitations, the current i_o available at the drain output of J_8 would be a faithful reproduction of the detector signal. In the actual case a broadening of the detector current may result from the finite gain-bandwidth product of the monolithic preamplifier and a gain factor larger than unity may arise from the unavoidable strays loading the source of J_8. An obvious design goal for the current feed-by function is to keep the gain-bandwidth product in the monolithic structure as large as possible and the capacitive load on the source of J_8 as small as possible. If these conditions are adequately well met the current feed-by configuration can be used to transmit the detector current signal at the output. Here it can be combined with the signals coming from similar units and all the signals can be injected into a summing virtual ground. Both structures of fig. 6 are intended to be, as previously stated much less

process-dependent than that of fig. 1.



(a)



(b)

Fig. 6 - New monolithic structures based on N-JFET buried layer technology.
(a) Configuration suitable for charge-sensitive connections.
(b) Configuration suitable for current feed-by connections.

The way in which this reduced dependence is achieved can be understood with reference to fig. 6. Here JFET J_3, which constitutes the current reference for the input branch, is a device of a smaller size than the corresponding one of fig. 1 which has an 800 µm-channel width. Throughout the expected range of pinch-off voltages (- 1.2 V to - 1.8 V) the current in J_1 will never drop below 2 mA and will never exceed 4 mA.

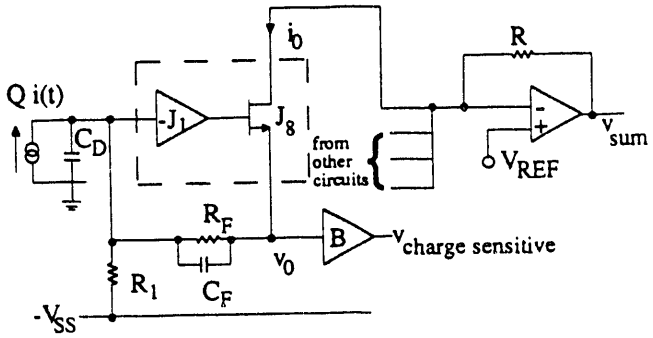


Fig. 7 - Combined charge-sensitive and current feed-by functions.

The desired value of the standing current in J_1 is 4 mA, as this ensures a suitably large value of the transconductance, about 35 mA/V, and an accordingly suitably low spectral density of white noise, less than 0.57 $nV/\sqrt{Hz}$. To reach this current value in J_1, an external resistor R_{EXT} connected between pin 3 and the positive supply provides the additional current required for J_1 in the case of pinch-off voltages close to the lower limits.

The simulation of the circuit behaviour has been carried out with reference to the charge-sensitive connection.

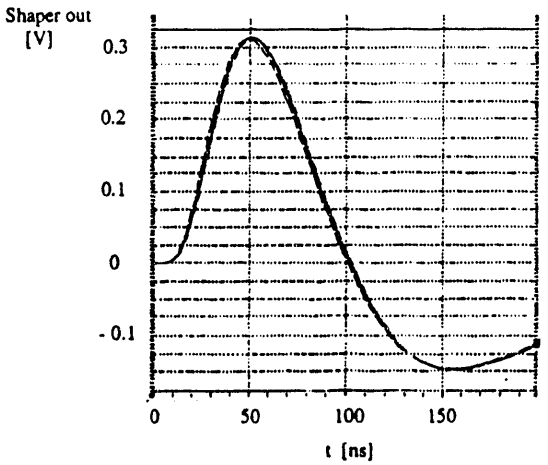


Fig. 8 - Preamplifier output signals shaped by a bipolar filter. The signals correspond to three different values (-1.2, -1.4V and -1.8V) of the pinch-off voltage in the preamplifier devices.

The analysis of the linearity characteristics with the preamplifier loaded by a hundred-ohms resistor and followed by an ideal bipolar shaper of about 40 ns peaking time, has shown that up to a 2V signal at the preamplifier output the resulting integral nonlinearity error is within ±0.2%. The dependence of the shaped pulse on the process parameters of the preamplifier is described in fig. 8. The bipolar signals of fig. 8 refer to three different values of the process pinch-off voltage, - 1.2 V and - 1.8 V corresponding to the lower and

upper limits of the expected pinch-off range and - 1.4 V.

As shown in fig. 8 the variations in shape and the fluctuations of the peaking time remain sufficiently small as the process pinch-off voltage is varied throughout its expected range.

V - CONCLUSIONS

The results obtained from the first two batches of the monolithic N-JFET preamplifier have demonstrated that the circuit has reached very satisfactory performances in terms of noise, dynamic behaviour and radiation hardness. The new version which is now being implemented employs design criteria that are oriented to the reduction of the dependence on the process parameters, especially the pinch-off voltage.

VI - ACKNOWLEDGEMENTS

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The effort produced by M. Hoye and L. Rehn of Interfet Co. to improve the buried layer JFET process is also acknowledged.

VII - REFERENCES

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